Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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FINAL

Am7201

High Density First-In First-Out (FIFO) 512 x 9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **512 x 9 organization**
- **Cycle times of 35/45/65 ns for standard products**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption**
- **Status flags—full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for XI—CMOS threshold**
- **Pin compatible with industry standard devices**

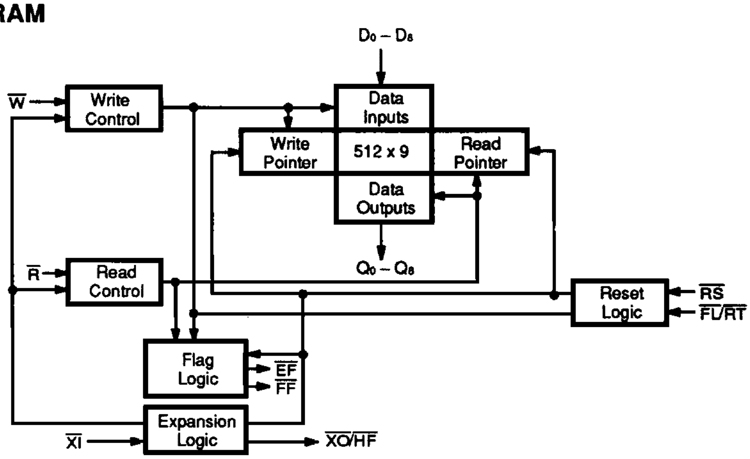
GENERAL DESCRIPTION

The Am7201 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can input and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz for Standard Products. Status flags are provided to signify empty, full and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7201 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7201 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



10175G-1

Figure 1.

PRODUCT SELECTOR GUIDE

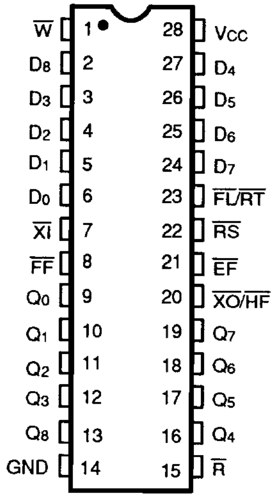
Part Number	Am7201-25	Am7201-35	Am7201-50
Access Time	25 ns	35 ns	50 ns
Maximum Power Supply Current	70 mA	60 mA	60 mA
Operating Frequency	28.5 MHz	22.2 MHz	15.3 MHz
Operating Range	Com'l	Com'l	Com'l

Publication# 10175 Rev. G Amendment /0
Issue Date: September 1992

CONNECTION DIAGRAMS

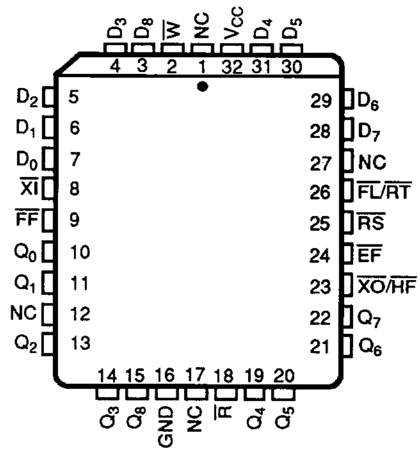
Top View

DIPs



10175G-2

PLCC

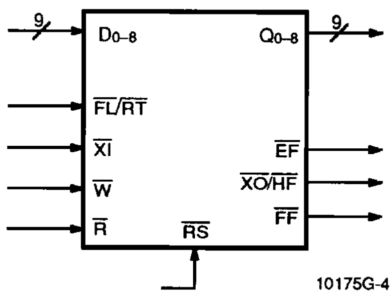


10175G-3

Note:

Pin 1 is marked for orientation for plastic packages.

LOGIC SYMBOL



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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM7201 -25 P C

OPTIONAL PROCESSING
Blank = Standard processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)

PACKAGE TYPE
P = Plastic DIP (600 mil) (PD 028)
J = Plastic Leaded Chip Carrier (PL 032)
R = Plastic DIP (300 mil) (PDW028)

SPEED OPTION
-25 = 25 ns t_A
-35 = 35 ns t_A
-50 = 50 ns t_A

DEVICE NUMBER/DESCRIPTION
Am7201
High Density First-In First-Out (FIFO) 512 x 9-Bit
CMOS Memory

Valid Combinations	
AM7201-25	PC, RC, JC
AM7201-35	
AM7201-50	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

PIN DESCRIPTION

D_{0-8}

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

$\overline{EF}$

Empty Flag (Output; Active LOW)

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO contains data to be read. The $\overline{EF}$ goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. $\overline{EF}$ LOW inhibits further Read operations.

The $\overline{EF}$ goes HIGH after the rising edge of Write ($\overline{W}$) during the first write cycle for an empty FIFO (See Figure 4). The $\overline{EF}$ goes LOW after the falling edge of Read ($\overline{R}$) during the read cycle which creates the empty condition.

During a Reset cycle, the $\overline{EF}$ is driven LOW (active).

$\overline{FF}$

Full Flag (Output; Active LOW)

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The $\overline{FF}$ goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. $\overline{FF}$ LOW inhibits further Write operations.

The $\overline{FF}$ goes HIGH after the rising edge of Read ($\overline{R}$) during the first read cycle following a full condition (See Figure 6). The $\overline{FF}$ goes LOW after the falling edge of Write ($\overline{W}$) during the write cycle which creates the full condition.

During a Reset cycle, the $\overline{FF}$ is driven HIGH (inactive).

$\overline{FL}/\overline{RT}$

First Load/Retransmit (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD ($\overline{FL}$) pin when in the Depth-Expansion Mode. The device receiving data first will have the $\overline{FL}$ input tied LOW, while the remaining devices will have the $\overline{FL}$ pin tied HIGH. The states of the $\overline{FL}$ and Expansion In ($\overline{XI}$) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit ($\overline{RT}$) input during Single Device Mode. The device can be instructed to retransmit the previously written data when $\overline{RT}$ is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q_{0-8}

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read ($\overline{R}$) is HIGH.

$\overline{R}$

Read (Input; Active LOW)

The falling edge of Read ($\overline{R}$) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag ($\overline{EF}$) being LOW. Valid data appears on the outputs (Q_{0-8}) after the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the Data Outputs (Q_{0-8}) will return to a high impedance condition.

$\overline{RS}$

Reset (Input; Active LOW)

The falling edge of Reset ($\overline{RS}$) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag ($\overline{EF}$) is driven LOW (active), and both the Half-Full Flag ($\overline{HF}$) and Full Flag ($\overline{FF}$) are driven HIGH (inactive).

V_{CC}

Power Supply

This pin is the +5 V power supply for the FIFO.

$\overline{W}$

Write (Input; Active LOW)

The falling edge of Write ($\overline{W}$) initiates a write cycle, except when the device is full, as indicated by the Full Flag ($\overline{FF}$) being LOW. Data is latched into the FIFO on the rising edge of $\overline{W}$.

$\overline{XI}$

Expansion In (Input; Active LOW)

Expansion In ($\overline{XI}$) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the $\overline{XI}$ pin is connected to the Expansion Out ($\overline{XO}$) pin of the previous device, except for the $\overline{XI}$ pin of the first device which is connected to the $\overline{XO}$ pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

$\overline{XO}/\overline{HF}$

Expansion Out/Half-Full Flag (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out ($\overline{XO}$) signal during Depth Expansion Mode. In this mode, the $\overline{XO}$ pin is connected to the Expansion Input ($\overline{XI}$) pin of the following device, except for the $\overline{XO}$ pin of the last device which is connected to the $\overline{XI}$ pin of the first device.

When in Single Device Mode (Expansion In ($\overline{XI}$) pin grounded) this output operates as a Half-Full Flag ($\overline{HF}$). After half the FIFO has been filled, the $\overline{HF}$ will be set LOW at the falling edge of the next Write ($\overline{W}$) operation. The $\overline{HF}$ will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the FIFO. The $\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$ during the read operation which eliminates the half-full condition (See Figure 5).

During a Reset cycle, the $\overline{HF}$ is driven HIGH (inactive).

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

FUNCTIONAL DESCRIPTION

The Am7201 CMOS FIFO is designed around a 512 x 9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 511. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

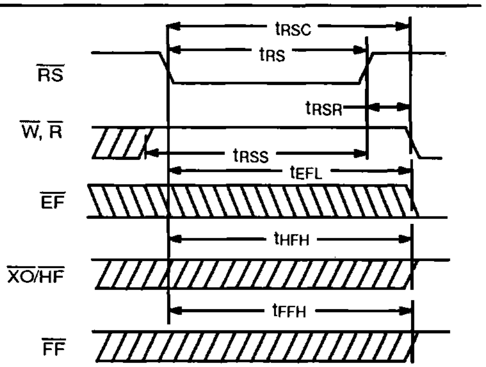
Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7201. The write, read, data-in and data-out lines of the Am7201 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting the FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.



10175G-5

Figure 2. Reset Timing

Writing Data to the FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D_0–D_8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 256 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 512 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO t_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data from the FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q_0–Q_8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q_0–Q_8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 255 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until t_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

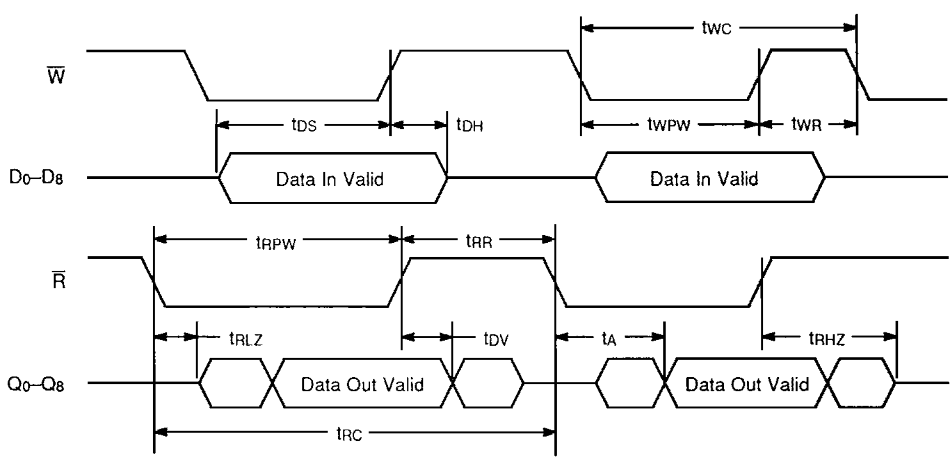
1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.



10175G-6

Figure 3. Asynchronous Write and Read Timing

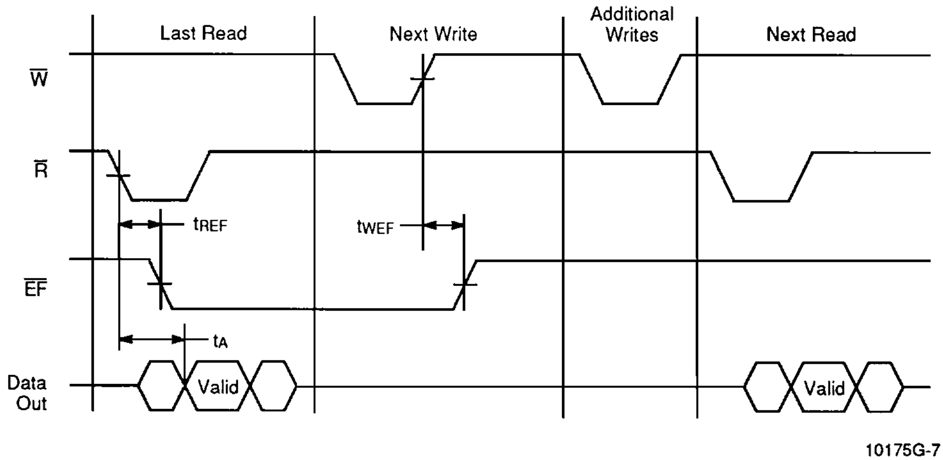
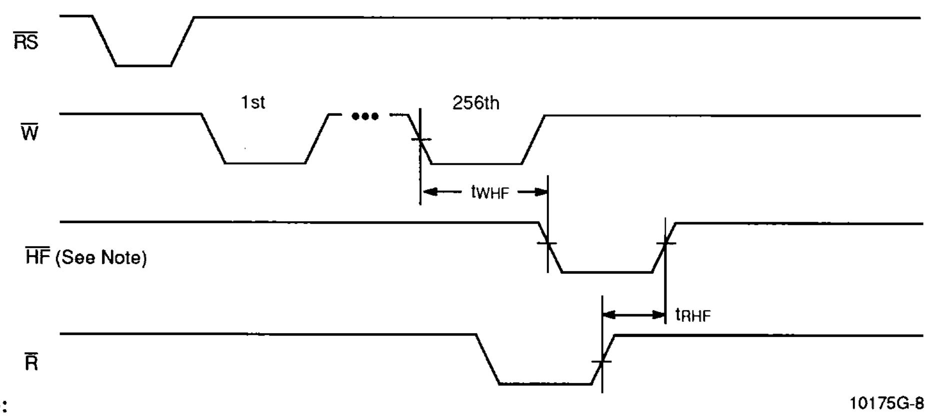


Figure 4. Empty Flag Timing



Note:

Depending on the precise phase of W̄ and R̄, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when W̄ and R̄ are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

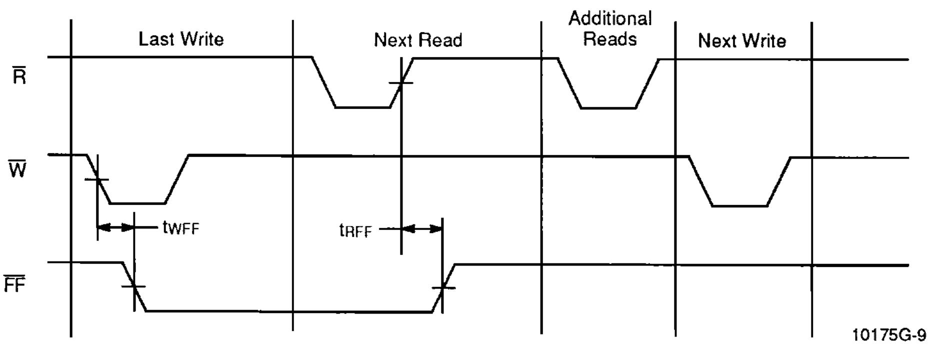


Figure 6. Full Flag Timing

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 256 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 256 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 512 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 512 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1.)

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 12 and 13, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7201 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 13.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

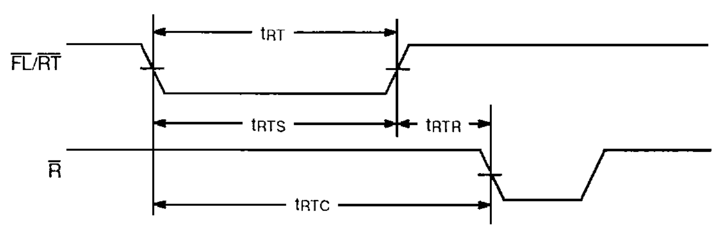
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 14 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 511, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the Am7201 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 15.)

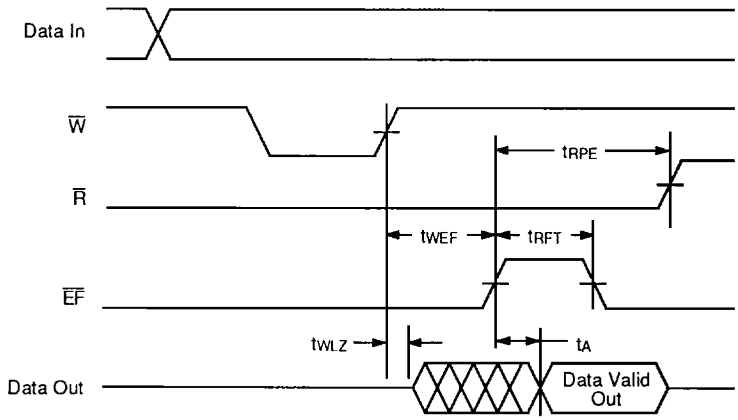


Note:

$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

10175G-10

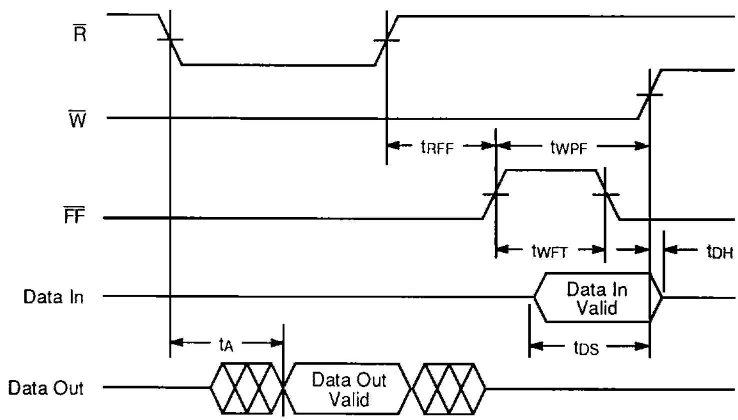
Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

10175G-11

Figure 8. Read Data Flow-Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

10175G-12

Figure 9. Write Data Flow-Through Mode

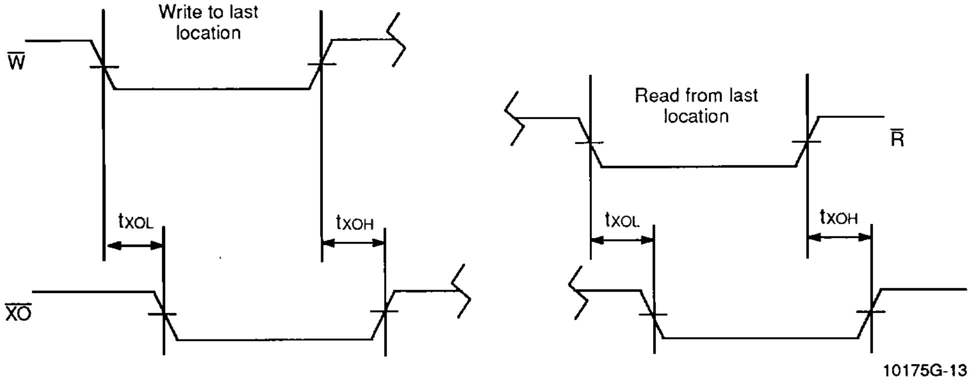


Figure 10. $\overline{XO}$ Delay from Clock

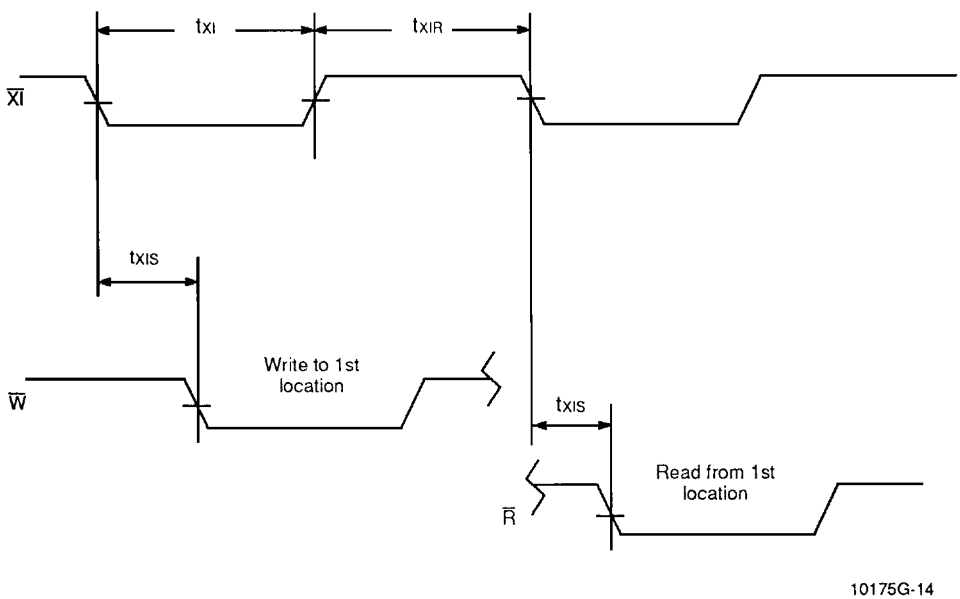
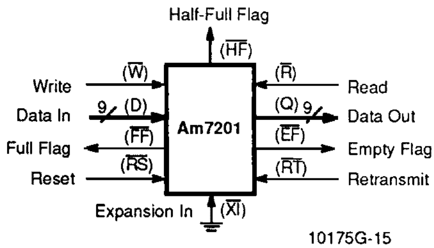
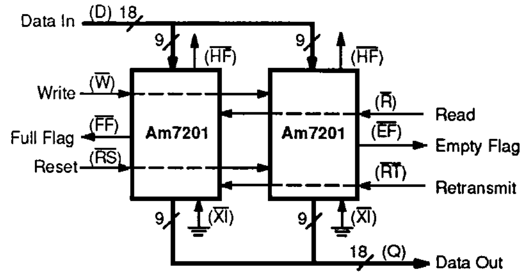


Figure 11. 1st Clock Pulse Delay from $\overline{XI}$



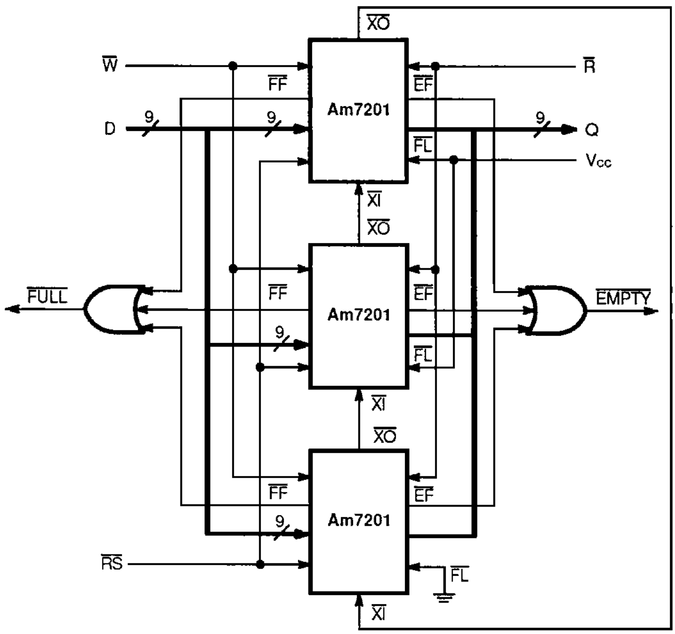
10175G-15

Figure 12. Single FIFO Configuration



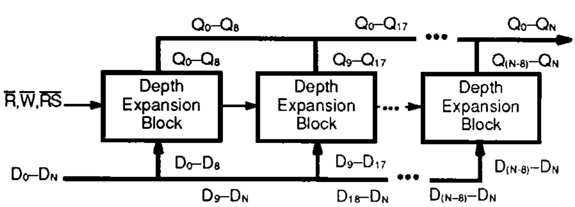
10175G-16

Figure 13. Width-Expansion to Form a 512 x 18 FIFO



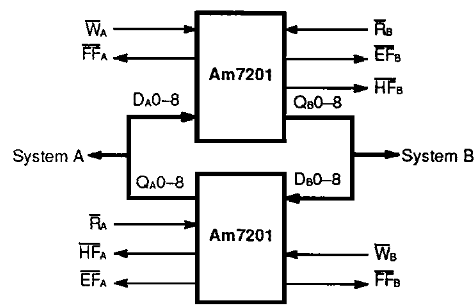
10175G-17

Figure 14. Depth-Expansion to Form 768 x 9 FIFO



10175G-18

Figure 15. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques



10175G-19

Figure 16. Bidirectional FIFO Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... –0.5 V to +7.0 V

Input Voltage .... –0.5 V to V_{CC} +0.5 V

Ambient Temperature with
Power Applied .... –55°C to +125°C

Storage Temperature .... –55°C to +150°C

Power Dissipation .... 1.0 W

DC Output Current .... 50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) .... 0°C to 70°C
Supply Voltage, (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7201-25 t_A = 25 ns		Am7201-35 t_A = 35 ns		Am7201-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	–1	1	–1	1	–1	1	μA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	–10	10	–10	10	–10	10	μA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0		2.0		2.0		V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)		0.8		0.8		0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5		3.5		3.5		V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)		1.5		1.5		1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = –2 mA	2.4		2.4		2.4		V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA		0.4		0.4		0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)		70		60		60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)		20		20		20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} – 0.2 V) (Note 4)		5		5		5	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$. V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Figures	Am7201-25 Min.	Am7201-25 Max.	Am7201-35 Min.	Am7201-35 Max.	Am7201-50 Min.	Am7201-50 Max.	Unit
Write and Flag Timing									
t_{WC}	Write Cycle Time	3	35		45		65		ns
t_{WPW}	Write Pulse Width	3	25		35		50		ns
t_{WR}	Write Recovery Time	3	10		10		15		ns
t_{DS}	Data Setup Time	3,9	15		18		30		ns
t_{DH}	Data Hold Time	3,9	0		0		5		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		25		30		45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		35		45		65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		25		30		45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5		10		10		ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	9	25		35		50		ns
Read and Flag Timing									
t_{RC}	Read Cycle Time	3	35		45		65		ns
t_A	Access Time	3,4,8,9		25		35		50	ns
t_{RR}	Read Recovery Time	3	10		10		15		ns
t_{RPW}	Read Pulse Width	3	25		35		50		ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5		5		5		ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5		5		5		ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3		18		20		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		25		30		45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5		35		45		65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		25		30		45	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	8	25		35		50		ns
Reset Timing									
t_{RSC}	Reset Cycle Time	2	35		45		65		ns
t_{RS}	Reset Pulse Width	2	25		35		50		ns
t_{RSS}	Reset Setup Time	2	25		35		50		ns
t_{RSR}	Reset Recovery Time	2	10		10		15		ns
t_{EFL}	Reset to Empty Flag LOW	2		35		45		65	ns
t_{HFH}	Reset to Half-Full Flag High	2		35		45		65	ns
t_{FFH}	Reset to Full Flag HIGH	2		35		45		65	ns
Retransmit Timing									
t_{RTC}	Retransmit Cycle Time	7	35		45		65		ns
t_{RT}	Retransmit Pulse Width	7	25		35		50		ns
t_{RTS}	Retransmit Setup Time (Note 2)	7	25		35		50		ns
t_{RTR}	Retransmit Recovery Time	7	10		10		15		ns

Notes:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
2. Values are guaranteed by design and are not currently tested.

SWITCHING CHARACTERISTICS (continued)

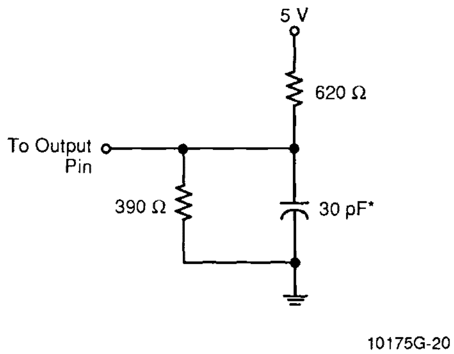
Parameter Symbol	Parameter Description	Figures	Am7201-25		Am7201-35		Am7201-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Expansion Timing									
t_{XOL}	Read/Write to $\overline{XO}$ LOW	10		25		35		50	ns
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	10		25		35		50	ns
t_{XI}	$\overline{XI}$ Pulse Width (Note 2)	11	25		35		50		ns
t_{XIR}	$\overline{XI}$ Recovery Time (Note 2)	11	10		10		10		ns
t_{XIS}	$\overline{XI}$ Setup Time	11	10		10		10		ns

Notes:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
2. Values are guaranteed by design and are not currently tested.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output timing reference levels	1.5 V
Output load	See Figure 17



* Includes jig and scope capacitances.

Figure 17. AC Test Load

CAPACITANCE (V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Description (Note 1)	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.