Rochester Electronics®

Datasheet

AM79C970A

PCnet™-PCI II Single-Chip Full-Duplex Ethernet Controller for PCI Local Bus Product

Single-chip Ethernet controller for the Peripheral Component Interconnect (PCI) local bus. Supports ISO 8802-3 (IEEE/ANSI 802.3) and Ethernet standards. Direct interface to the PCI local bus (Revision 2.0 compliant). High-performance 32-bit Bus Master architecture with integrated DMA buffer management unit for low CPU and bus utilization. Software-compatible with AMD PCnet family, LANCE/C-LANCE, and Am79C900 ILACC register and descriptor architecture. Compatible with PCnet family driver software Full-duplex operation for increased network bandwidth.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

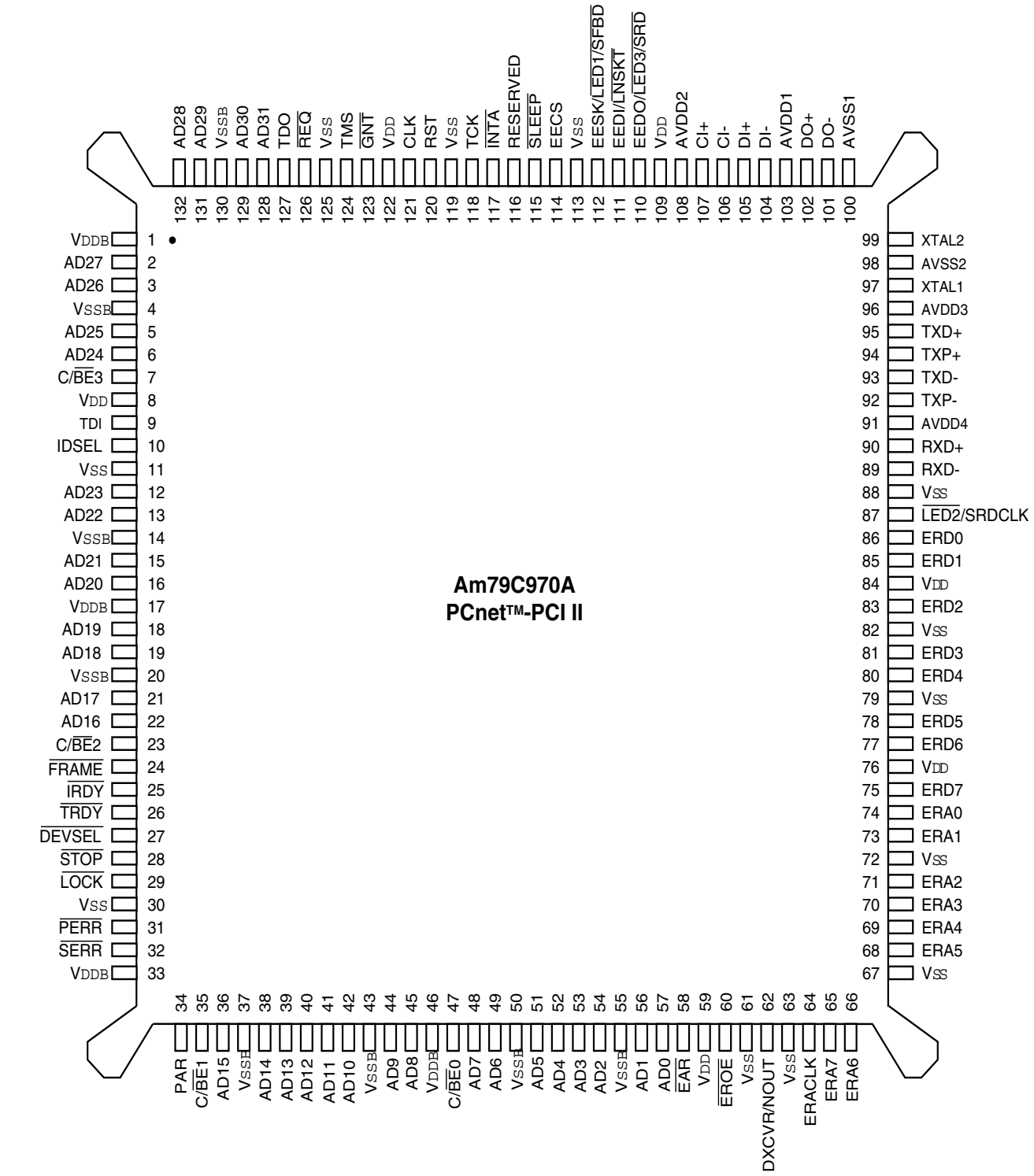
- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

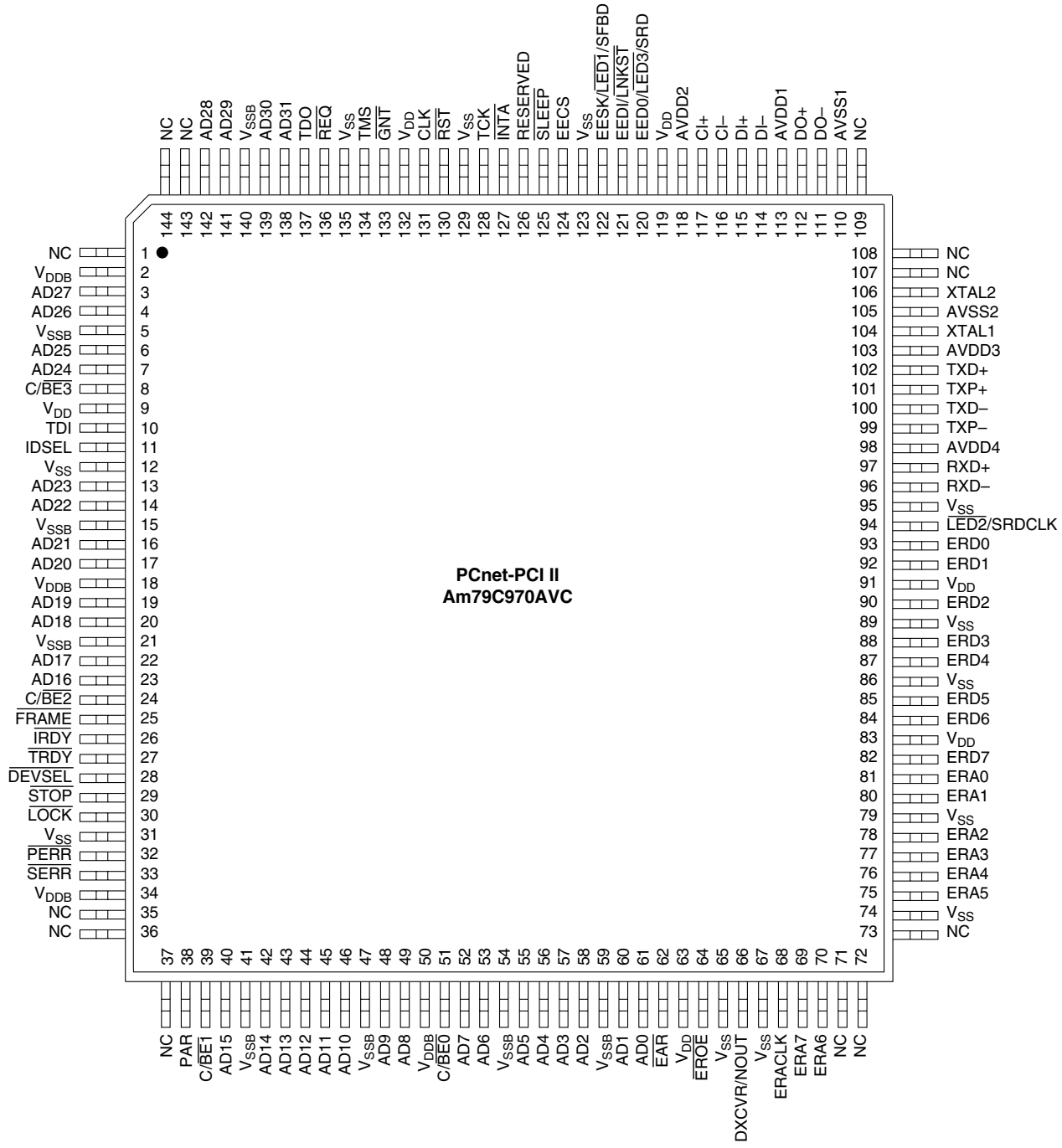
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

CONNECTION DIAGRAM



CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature Under Bias . . –65°C to +125°C

Supply Voltage to AV_{SS} or V_{SSB}
(AV_{DD}, V_{DD}, V_{DDB}) . . . . . 0.3 V to +6.0V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to + 70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to + 85°C

Supply Voltages

(AV_{DD}, V_{DD}) . . . . . +5V ± 5%
(V_{DDB} for 5 V Signaling) . . . . . +5V ± 5%
(V_{DDB} for 3.3 V Signaling). . . . . + 3.3 V ± 10%

All inputs within the range: . . . AV_{SS} – 0.5 V ≤ V_{IN} ≤ . . . . . AV_{DD} + 0.5 V, or . . . . . V_{SS} – 0.5 V ≤ V_{IN} ≤ V_{DD} + 0.5 V, or . . . . . V_{SSB} – 0.5 < V_{IN} < V_{DDB} + 0.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Digital Input Voltage for 5 V Signaling					
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
Digital Output Voltage for 5 V Signaling					
V_{OL}	Output LOW Voltage	I_{OL1} = 3 mA I_{OL2} = 6 mA I_{OL3} = 12 mA (Note 1)		0.45	V
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = –2 mA (Note 3)	2.4		V
Digital Input Leakage Current for 5 V Signaling					
I_{IX}	Input Low Leakage Current (Note 4)	V_{IN} = 0 V, V_{DD} = V_{DDB} = 5 V	–10	10	µA
Digital Output Leakage Current for 5 V Signaling					
I_{OZL}	Output Low Leakage Current (Note 5)	V_{OUT} = 0.4V		–10	µA
I_{OZH}	Output High Leakage Current (Note 5)	V_{OUT} = V_{DD}, V_{DDB}		10	µA
Digital Input Voltage for 3.3 V Signaling					
V_{IL}	Input LOW Voltage		–0.5	0.325 V_{DDB}	V
V_{IH}	Input HIGH Voltage		0.475 V_{DDB}	V_{DDB} + 0.5	V
Digital Output Voltage for 3.3 V Signaling					
V_{OL}	Output LOW Voltage	I_{OL} = 1.5 mA		0.1 V_{DDB}	V
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = –0.5 mA	0.9 V_{DDB}		V
Digital Input Leakage Current for 3.3 V Signaling					
I_{IX}	Input Low Leakage Current	V_{IN} = 0 V, V_{DD} = V_{DDB} = 3.3 V (Note 4)	–10	10	µA
Digital Output Leakage Current for 3.3 V Signaling					
I_{OZL}	Output Low Leakage Current (Note 5)	V_{OUT} = 0.4V		–10	µA
I_{OZH}	Output High Leakage Current (Note 5)	V_{OUT} = V_{DD}, V_{DDB}		10	µA

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified (continued)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Units
Crystal Input Current						
V_{ILX}	XTAL1 Input LOW Voltage Threshold	V_{IN} = External Clock		–0.5	0.8	V
V_{IHX}	XTAL1 Input HIGH Voltage Threshold	V_{IN} = External Clock		VDD – 0.8	VDD + 0.5	V
I_{ILX}	XTAL1 Input LOW Current	V_{IN} = External Clock	Active	–120	0	µA
		V_{IN} = VSS	Sleep	–10	+10	µA
I_{IHX}	XTAL1 Input HIGH Current	V_{IN} = External Clock	Active	0	120	µA
		V_{IN} = VDD	Sleep		400	µA
Power Supply Current						
I_{DD}	Active Power Supply Current	XTAL1 = 20 MHz, CLK = 33 MHz			90	mA
I_{DDCOMA}	Sleep Mode Power Supply Current	SLEEP active AWAKE = 0 (BCR2, bit 2)			200	µA
$I_{DDSNOOZE}$	Auto Wake Mode Power Supply Current	SLEEP active AWAKE = 1 (BCR2, bit 2)			10	mA
$I_{DDMAGIC0}$	Magic Packet Mode Power Supply Current	CLK = 0 MHz (Note 10)			47	mA
$I_{DDMAGIC33}$	Magic Packet Mode Power Supply Current	CLK = 33 MHz (Note 10)			80	mA
Pin Capacitance						
C_{IN}	Input Pin Capacitance	FC = 1 MHz (Note 6)			10	pF
C_{IDSEL}	IDSEL Pin Capacitance	FC = 1 MHz (Note 6)			8	pF
C_O	I/O or Output Pin Capacitance	FC = 1 MHz (Note 6)			10	pF
C_{CLK}	CLK Pin Capacitance	FC = 1 MHz (Note 6)		5	12	pF
Twisted Pair Interface (10BASE-T)						
I_{IRXD}	Input Current at RXD±	$AV_{SS} < V_{IN} < AV_{DD}$		–500	500	µA
R_{RXD}	RXD± Differential Input Resistance			10		KΩ
V_{TIVB}	RXD+, RXD– Open Circuit I_{IN} = 0 mA Input Voltage (Bias)			AV_{DD}–3.0	AV_{DD}–1.5	V
V_{TIDV}	Differential Mode Input Voltage Range (RXD±)	AV_{DD} = 5.0 V		–3.1	3.1	V
V_{TSQ+}	RXD Positive Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 0 (CSR15, bit 9)		300	520	mV
$V_{TSQ–}$	RXD Negative Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 0 (CSR15, bit 9)		–520	–300	mV
V_{THS+}	RXD Post-Squelch Positive Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 0 (CSR15, bit 9)		150	293	mV
$V_{THS–}$	RXD Post-Squelch Negative Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 0 (CSR15, bit 9)		–293	–150	mV
V_{LTSQ+}	RXD Positive Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 1 (CSR15, bit 9)		180	312	mV
$V_{LTSQ–}$	RXD Negative Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 1 (CSR15, bit 9)		–312	–180	mV
V_{LTHS+}	RXD Post-Squelch Positive Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 1 (CSR15, bit 9)		90	176	mV
$V_{LTHS–}$	RXD Post-Squelch Negative Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤ 10 MHz LRT = 1 (CSR15, bit 9)		–176	–90	mV

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Twisted Pair Interface (10BASE-T) (Continued)					
V_{RXDTH}	RXD Switching Threshold	(Note 6)	–35	35	mV
V_{TXH}	TXD± and TXP± Output HIGH Voltage	AV_{SS}= 0 V	AV_{DD}–0.6	AV_{DD}	V
V_{TXL}	TXD± and TXP± Output LOW Voltage	AV_{DD} = 5 V	AV_{SS}	AV_{SS}+0.6	V
V_{TXI}	TXD± and TXP± Differential Output Voltage Imbalance		–40	40	mV
V_{TXOFF}	TXD± and TXP± Idle Output Voltage			40	mV
R_{TX}	TXD±, TXP± Differential Driver Output Impedance	(Note 6)		80	Ω
Attachment Unit Interface (AUI)					
I_{IAXD}	Input Current at DI+ and DI–	$-1V < V_{IN} < AV_{DD} + 0.5$ V	–500	+500	µA
I_{IAXC}	Input Current at CI+ and CI–	$-1V < V_{IN} < AV_{DD} + 0.5$ V	–500	+500	µA
V_{AOD}	Differential Output Voltage |(DO+)–(DO–)|	R_L = 78 Ω	630	1200	mV
V_{AODOFF}	Transmit Differential Output Idle Voltage	R_L = 78 Ω (Note 9)	–40	40	mV
I_{AODOFF}	Transmit Differential Output Idle Current	R_L = 78 Ω (Note 8)	–1	1	mA
V_{CMT}	Transmit Output Common Mode Voltage	R_L = 78 Ω	2.5	AV_{DD}	V
V_{ODI}	DO± Transmit Differential Output Voltage Imbalance	R_L = 78 Ω (Note 7)		25	mV
V_{ATH}	Receive Data Differential Input Threshold		–35	35	mV
V_{ASQ}	DI± and CI± Differential Input Threshold (Squelch)	–275	–160	mV	
V_{IRDVD}	DI± and CI± Differential Mode Input Voltage Range	–1.5	1.5	V	
V_{ICM}	DI± and CI± Input Bias Voltage	I_{IN} = 0 mA	AV_{DD}–3.0	AV_{DD}–1.0	V
V_{OPD}	DO± Undershoot Voltage at ZERO Differential on Transmit Return to ZERO (ETD)	(Note 9)		–100	mV

Notes:

1. *I_{OL1} applies to AD[31:0], C/$\overline{BE}$[3:0], PAR and* $\overline{REQ}$.
   I_{OL2} applies to $\overline{DEVSEL}$, $\overline{FRAME}$, $\overline{INTA}$, $\overline{IRDY}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{STOP}$, $\overline{TRDY}$*, EECS, ERA[7:0], ERACLK,* $\overline{EROE}$*, DXCVR/NOUT, ERD7/TXDAT, ERD6/TXEN and TDO.*
   I_{OL3} applies to EESK/$\overline{LED1}$*/SFBD,* $\overline{LED2}$*/SRDCLK, EEDO/*$\overline{LED3}$*/SRD, and EEDI/*$\overline{LNKST}$.
2. *V_{OH} does not apply to open-drain output pins.*
3. *Outputs are CMOS and will be driven to rail if the load is not resistive.*
4. *I_{IX} applies to all input pins except XTAL1.*
5. *I_{OZL} and I_{OZH} apply to all three-state output pins and bi-directional pins.*
6. *Parameter not tested. Value determined by characterization.*
7. *Tested, but to values in excess of limits. Test accuracy not sufficient to allow screening guard bands.*
8. *Correlated to other tested parameters–-not tested directly.*
9. *Test not implemented to data sheet specification.*
10. *The power supply current in Magic Packet mode is linear. For example, at CLK = 20 MHz the maximum Magic Packet mode power supply current would be 67 mA.*

SWITCHING CHARACTERISTICS: Bus Interface (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock Timing					
F_{CLK}	CLK Frequency		0	33	MHz
t_{CYC}	CLK Period	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	30	∝	ns
t_{HIGH}	CLK High Time	@ 2.0 V for V_{DDB} = 5 V @ 0.475 V_{DDB} for V_{DDB} = 3.3 V	12		ns
t_{LOW}	CLK Low Time	@ 0.8 V for V_{DDB} = 5 V @ 0.325 V_{DDB} for V_{DDB} = 3.3 V	12		ns
t_{FALL}	CLK Fall Time	Over 2 V p-p for V_{DDB} = 5 V Over 0.4 V_{DDB} p–p for V_{DDB} = 3.3 V (Note 1)	1	4	V/ns
t_{RISE}	CLK Rise Time	Over 2 V p-p for V_{DDB} = 5 V Over 0.4 V_{DDB} p–p for V_{DDB} = 3.3 V (Note 1)	1	4	V/ns
Output and Float Delay Timing					
t_{VAL}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$ Valid Delay	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	2	11	ns
t_{VAL} ($\overline{REQ}$)	$\overline{REQ}$ Valid Delay	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	2	12	ns
t_{ON}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{DEVSEL}$ Active Delay	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	2	11	ns
t_{OFF}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{DEVSEL}$ Float Delay	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V		28	ns
Setup and Hold Timing					
t_{SU}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$, IDSEL Setup Time	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	7		ns
t_H	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$, IDSEL Hold Time	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	0		ns
t_{SU} ($\overline{GNT}$)	$\overline{GNT}$ Setup Time	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	10		ns
t_H ($\overline{GNT}$)	$\overline{GNT}$ Hold Time	@ 1.5 V for V_{DDB} = 5 V @ 0.4 V_{DDB} for V_{DDB} = 3.3 V	0		ns

SWITCHING CHARACTERISTICS: Bus Interface (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
EEPROM Timing					
f_{EESK} (EESK)	EESK Frequency	@ 1.5 V for V (Note 2)		650	KHz
t_{HIGH} (EESK)	EESK High Time	@ 0.2 V	780		ns
t_{LOW}	EESK Low Time	@ 0.8 V	780		ns
t_{VAL} (EEDI)	EEDI Valid Output Delay from EESK	@ 1.5 V for V (Note 2)	–15	15	ns
t_{VAL} (EESK)	EECS Valid Output Delay from EESK	@ 1.5 V for V (Note 2)	–15	15	ns
t_{LOW} (EECS)	EECS Low Time	@ 1.5 V for V (Note 2)	1550		ns
t_{SU} (EEDO)	EEDO Setup Time to EESK	@ 1.5 V for V (Note 2)	50		ns
t_H (EEDO)	EEDO Hold Time from EESK	@ 1.5 V for V (Note 2)	0		ns
Expansion ROM Interface Timing					
t_{VAL} (ERA)	ERA Valid Delay from CLK	@ 1.5 V			ns
t_{VAL} (EROE)	EROE Valid Delay from CLK	@ 1.5 V			ns
t_{VAL} (ERACLK)	ERACLK Valid Delay from CLK	@ 1.5 V			ns
t_{SU} (ERD)	ERD Setup Time to CLK	@ 1.5 V			ns
t_H (ERD)	ERD Hold Time to CLK	@ 1.5 V			ns
JTAG (IEEE 1149.1) Test Signal Timing					
t_{J1}	TCK Frequency			10	MHz
t_{J2}	TCK Period		100		
t_{J3}	TCK High Time	@ 2.0 V	45		ns
t_{J4}	TCK Low Time	@ 0.8 V	45		ns
t_{J5}	TCK Rise Time			4	ns
t_{J6}	TCK Fall Time			4	ns
t_{J7}	TDI, TMS Setup Time		8		ns
t_{J8}	TDI, TMS Hold Time		10		ns
t_9	TDO Valid Delay		3	30	ns
t_{J9}	TDO Float Delay			50	ns
t_{J11}	All Outputs (Non-Test) Valid Delay		3	25	ns
t_{J12}	All Outputs (Non-Test) Float Delay			36	ns
t_{J13}	All Outputs (Non-Test) Setup Time		8		ns
t_{J4}	All Outputs (Non-Test) Hold Time		7		ns

Note:

1. *Not tested; parameter guaranteed by characterization.*
2. *Parameter value is given for automatic EEPROM read operation. When EEPROM port (BCR19) is used to access the EEPROM, software is responsible for meeting EEPROM timing requirements.*

SWITCHING CHARACTERISTICS: 10BASE-T Interface (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Transmit Timing					
t_{TETD}	Transmit Start of Idle		250	350	ns
t_{TR}	Transmitter Rise Time	(10% to 90%)		5.5	ns
t_{TF}	Transmitter Fall Time	(90% to 10%)		5.5	ns
t_{TM}	Transmitter Rise and Fall Time Mismatch	($t_{TM} = \|t_{TR} - t_{TF}\|$)		1	ns
t_{XMTON}	XMT Asserted Delay			100	ns
t_{XMTOFF}	XMT Deasserted Delay		20	62	ms
t_{PERLP}	Idle Signal Period		8	24	ms
t_{PWLP}	Idle Link Pulse Width	(Note 1)	75	120	ns
t_{PWPLP}	Predistortion Idle Link Pulse Width	(Note 1)	45	55	ns
t_{JA}	Transmit Jabber Activation Time		20	150	ms
t_{JR}	Transmit Jabber Reset Time		250	750	ms
t_{JREC}	Transmit Jabber Recovery Time (Minimum time gap between transmitted frames to prevent jabber activation)		1.0		µs
Receiving Timing					
t_{PWNRD}	RXD Pulse Width Not to Turn Off Internal Carrier Sense	$V_{IN} > V_{THS}$ (min)	136		ns
t_{PWROFF}	RXD Pulse Width To Turn Off	$V_{IN} > V_{THS}$ (min)		200	ns
t_{RETD}	Receive Start of Idle		200		ns
t_{RCVON}	RCV Asserted Delay		TRON –50	TRON +100	ns
t_{RCVON}	RCV Deasserted Delay		20	62	ms
Collision Detection and SQE Test					
t_{COLON}	COL Asserted Delay		750	900	ns
t_{COLOFF}	COL Deasserted Delay		20	62	ms

Note:

1. Not tested; parameter guaranteed by characterization.

SWITCHING CHARACTERISTICS: AUI (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
AUI Port					
t_{DOTR}	DO+, DO– Rise Time (10% to 90%)		2.5	5.0	ns
t_{DOTF}	DO+, DO– Fall Time (10% to 90%)		2.5	5.0	ns
t_{DORM}	DO+, DO– Rise and Fall Time Mismatch			1.0	ns
t_{DOETD}	DO± End of Transmission		200	375	ns
t_{PWODI}	DI Pulse Width Accept/Reject Threshold	$\|V_{IN}\| > \|VASQ\|$ (Note 1)	15	45	ns
t_{PWKDI}	DI Pulse Width Maintain/Turn-Off Threshold	$\|V_{IN}\| > \|VASQ\|$ (Note 2)	136	200	ns
t_{PWOCI}	CI Pulse Width Accept/Reject Threshold	$\|V_{IN}\| > \|VASQ\|$ (Note 3)	10	26	ns
t_{PWKCI}	CI Pulse Width Maintain/Turn-Off Threshold	$\|V_{IN}\| > \|VASQ\|$ (Note 4)	90	160	ns
Internal MENDEC Clock Timing					
t_{X1}	XTAL1 Period	V_{IN} = External Clock	49.995	50.001	ns
t_{X1H}	XTAL1 HIGH Pulse Width	V_{IN} = External Clock	20		ns
t_{X1L}	XTAL1 LOW Pulse Width	V_{IN} = External Clock	20		ns
t_{X1R}	XTAL1 Rise Time	V_{IN} = External Clock		5	ns
t_{X1F}	XTAL1 Fall Time	V_{IN} = External Clock		5	ns

Note:

1. *DI pulses narrower than t_{PWODI} (min) will be rejected; pulses wider than t_{PWODI} (max) will turn internal DI carrier sense on.*
2. *DI pulses narrower than t_{PWKDI} (min) will maintain internal DI carrier sense on; pulses wider than t_{PWKDI} (max) will turn internal DI carrier sense off.*
3. *CI pulses narrower than t_{PWOCI} (min) will be rejected; pulses wider than t_{PWOCI} (max) will turn internal CI carrier sense on.*
4. *CI pulses narrower than t_{PWKCI} (min) will maintain internal CI carrier sense on; pulses wider than t_{PWKCI} (max) will turn internal CI carrier sense off.*

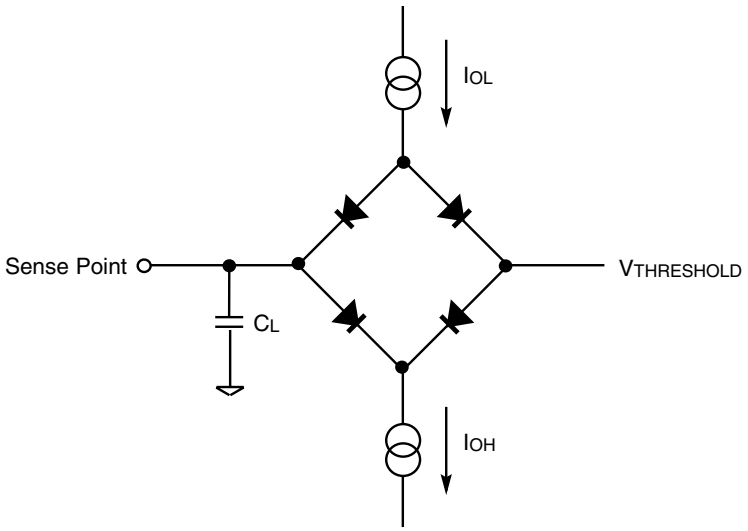
SWITCHING CHARACTERISTICS: EADI (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{EAD1}	SRD Setup to SRDCLK	@ 1.5 V	40		ns
t_{EAD2}	SRD Hold to SRDCLK	@ 1.5 V	40		ns
t_{EAD3}	SF/BD Change to SRDCLK	@ 1.5 V	–15	+15	ns
t_{EAD4}	$\overline{EAR}$ Deassertion to SRDCLK (First Rising Edge)	@ 1.5 V	50		ns
t_{EAD5}	$\overline{EAR}$ Assertion after SFD Event (Frame Rejection)	@ 1.5 V	200	51,090	ns
t_{EAD6}	$\overline{EAR}$ Assertion	@ 1.5 V	110		ns

A KEY TO SWITCHING WAVEFORMS

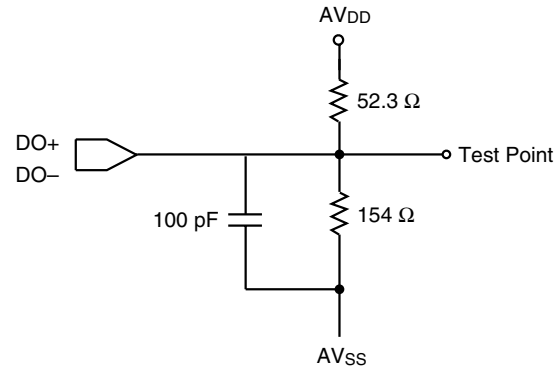
WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

SWITCHING TEST CIRCUITS

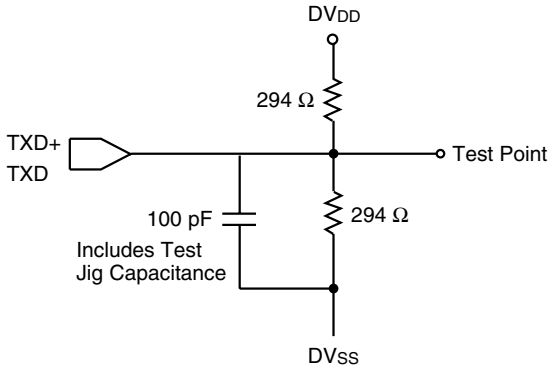


Normal and Tri-State OutPuts

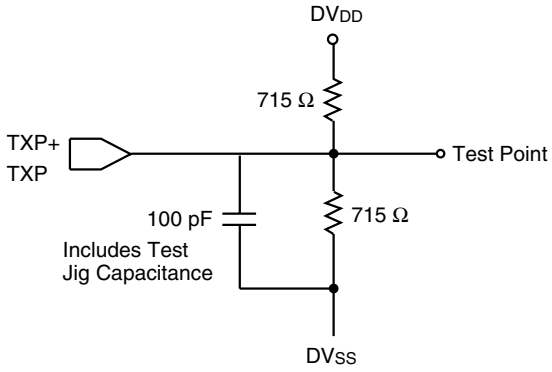
SWITCHING TEST CIRCUITS



AUI DO Switching Test Circuit

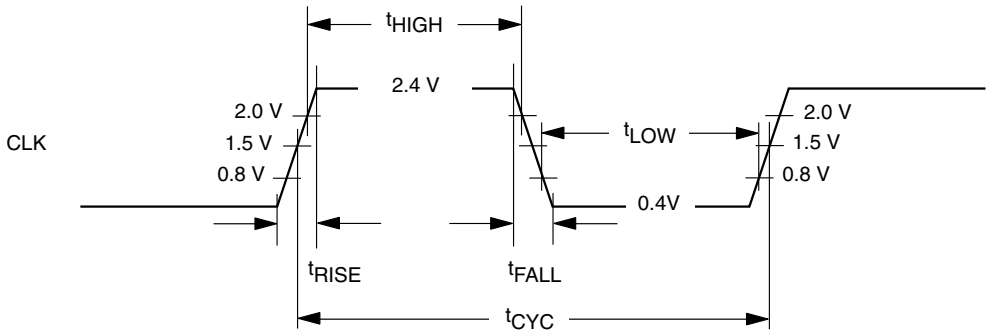


TXD Switching Test Circuit

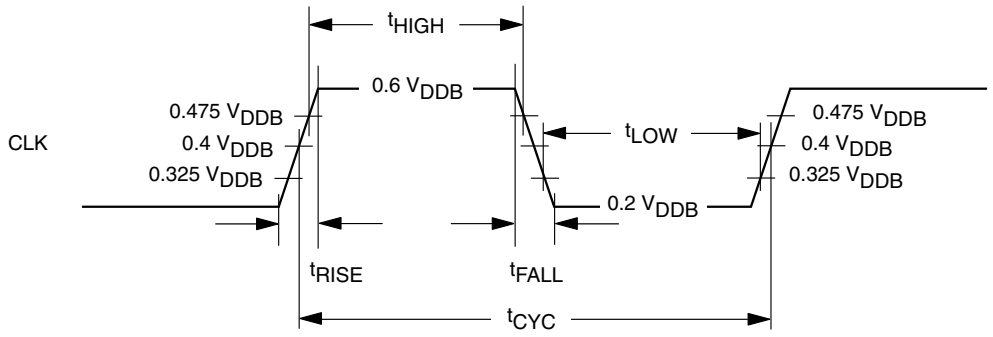


TXP Outputs Test Circuit

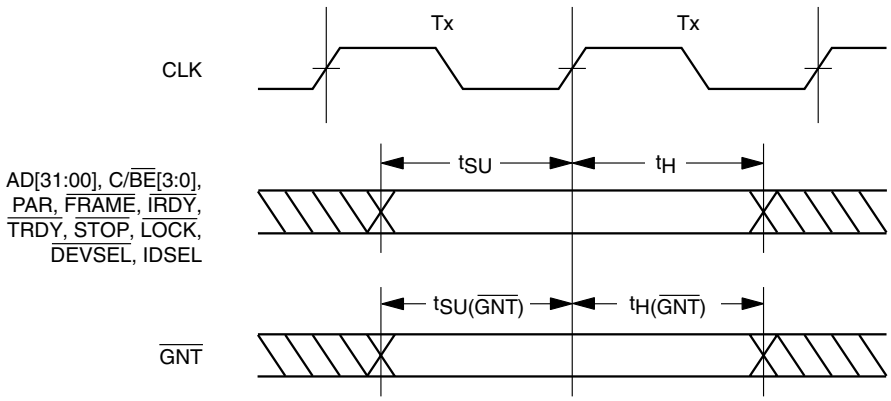
SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE



CLK Waveform for 5 V Signaling

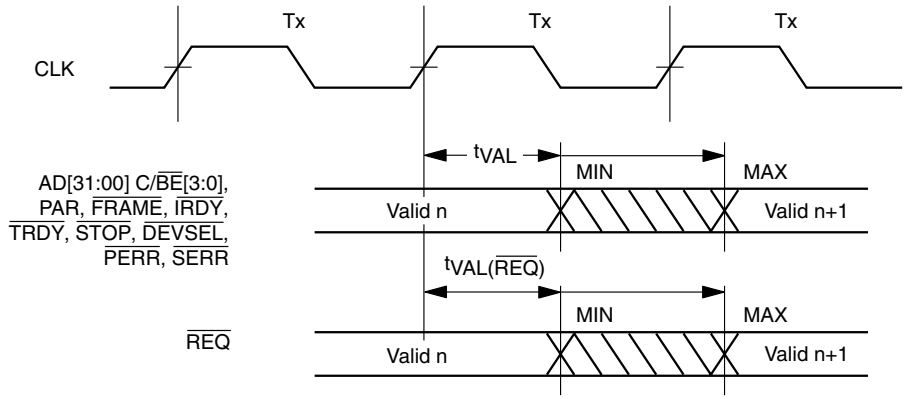


CLK Waveform for 3.3 V Signaling

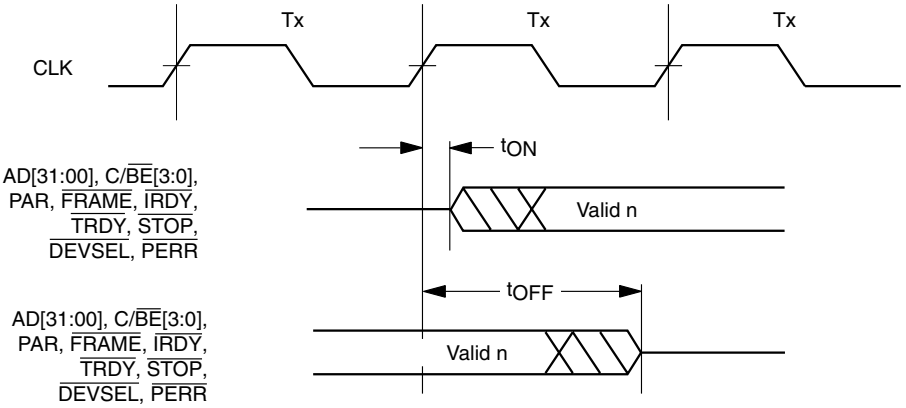


Input Setup and Hold Timing

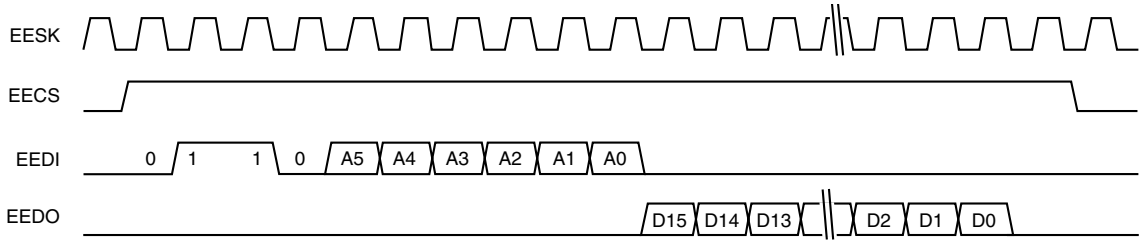
SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE



Output Valid Delay Timing

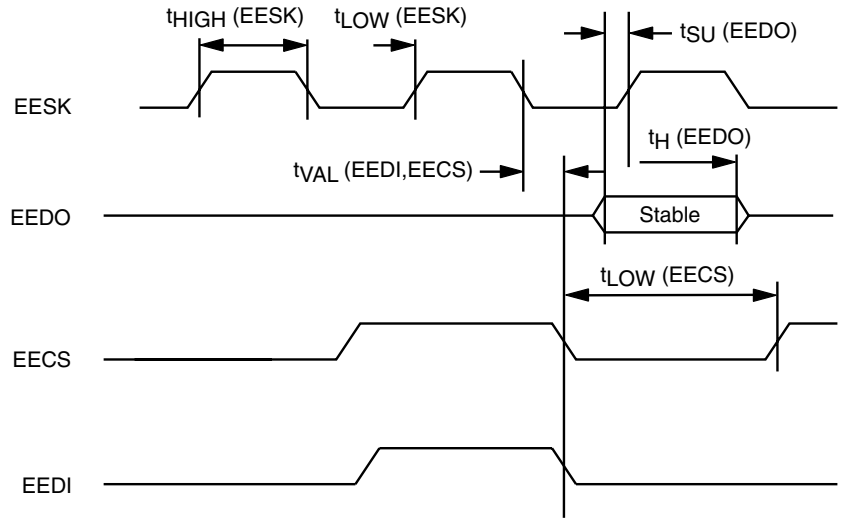


Output Tri-state Delay Timing

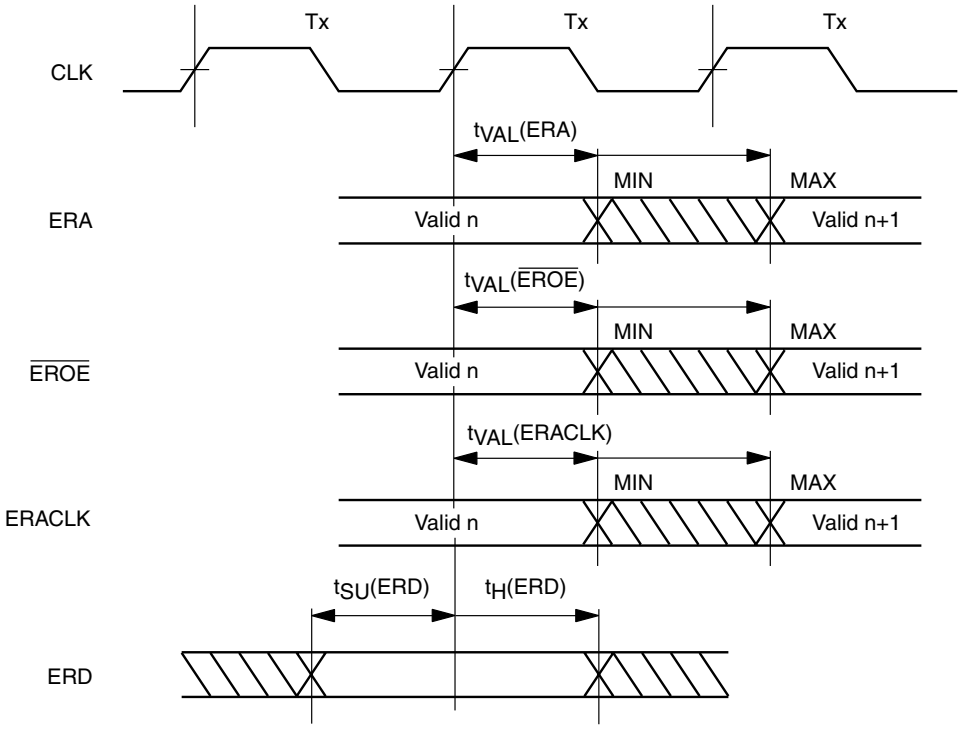


Automatic EEPROM Read Functional Timing

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE

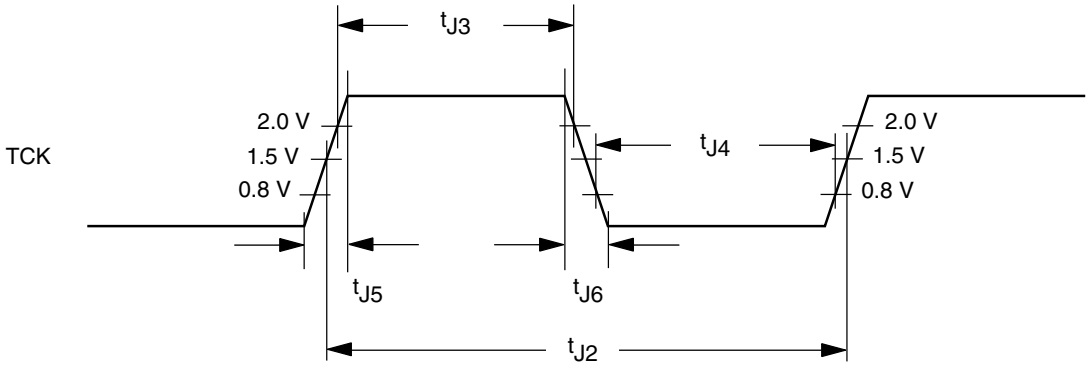


Automatic EEPROM Read Timing

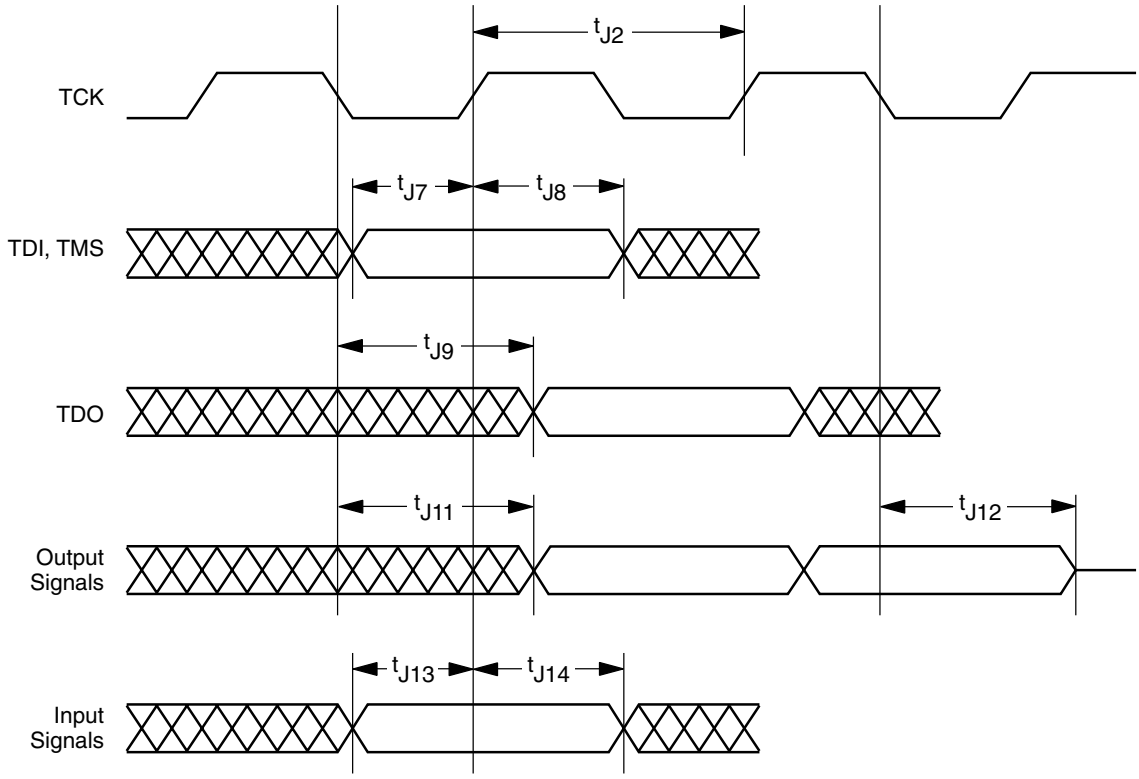


Expansion ROM Read Timing

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE

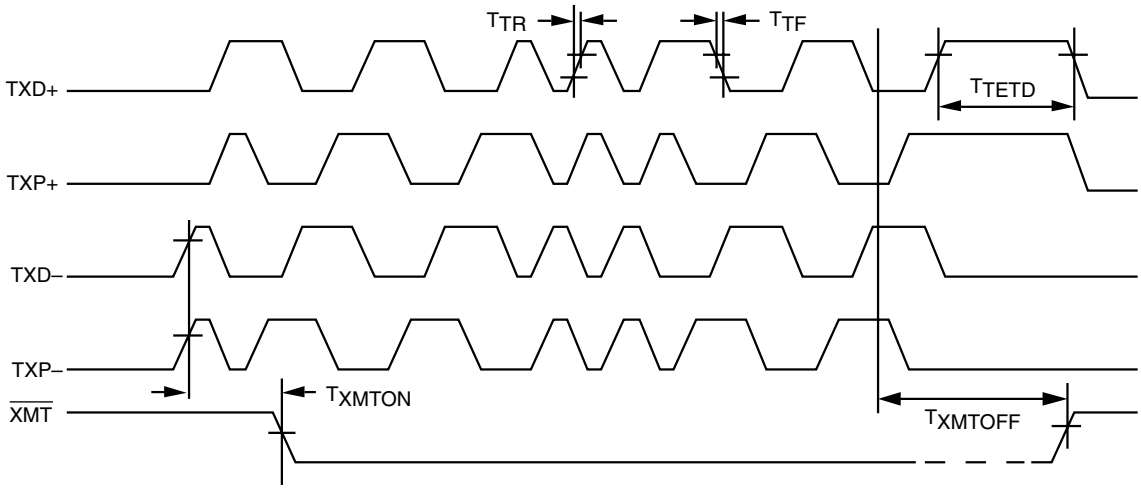


JTAG (IEEE 1149.1) TCK Waveform for 5 V Signaling

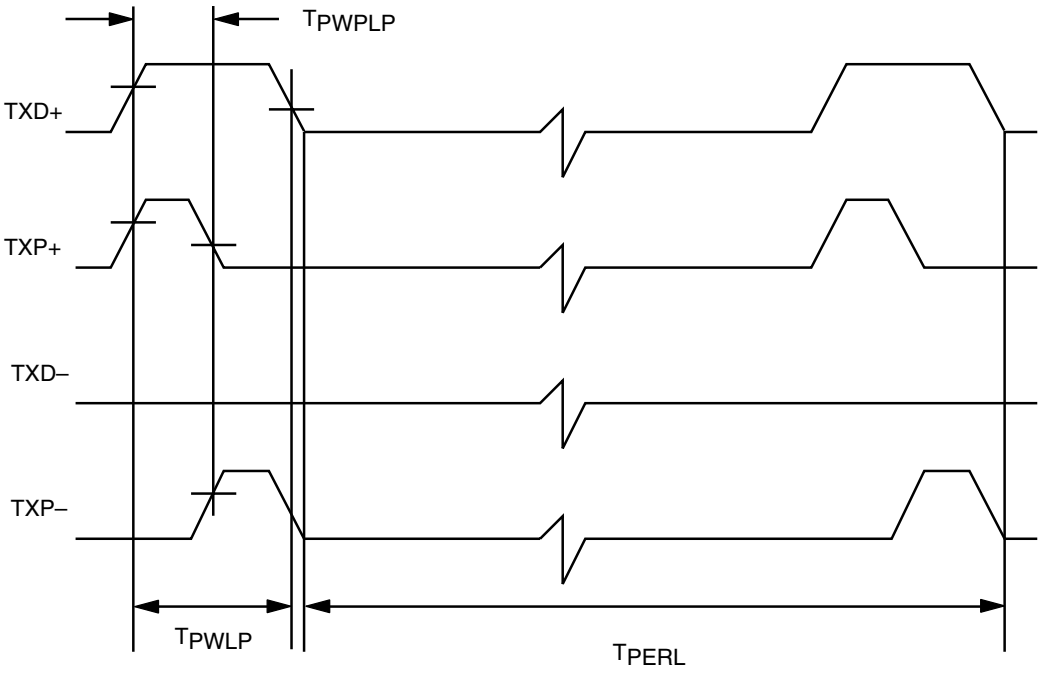


JTAG (IEEE 1149.1) Test Signal Timing

SWITCHING WAVEFORMS: 10BASE-T INTERFACE

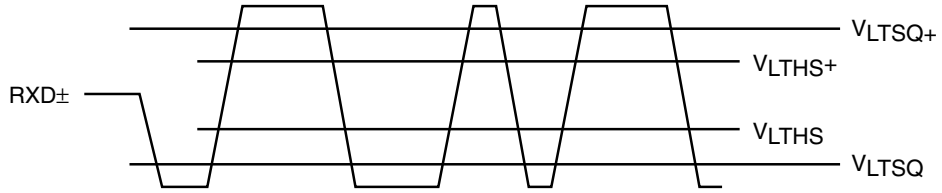


Transmit Timing

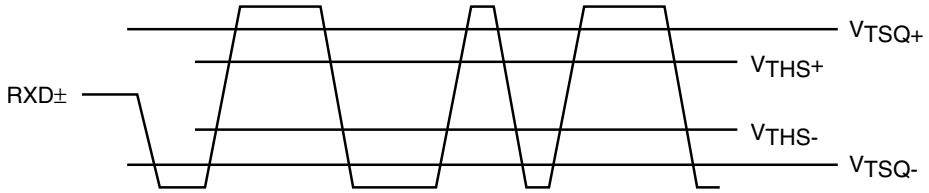


Idle Link Test Pulse

SWITCHING WAVEFORMS: 10BASE-T INTERFACE

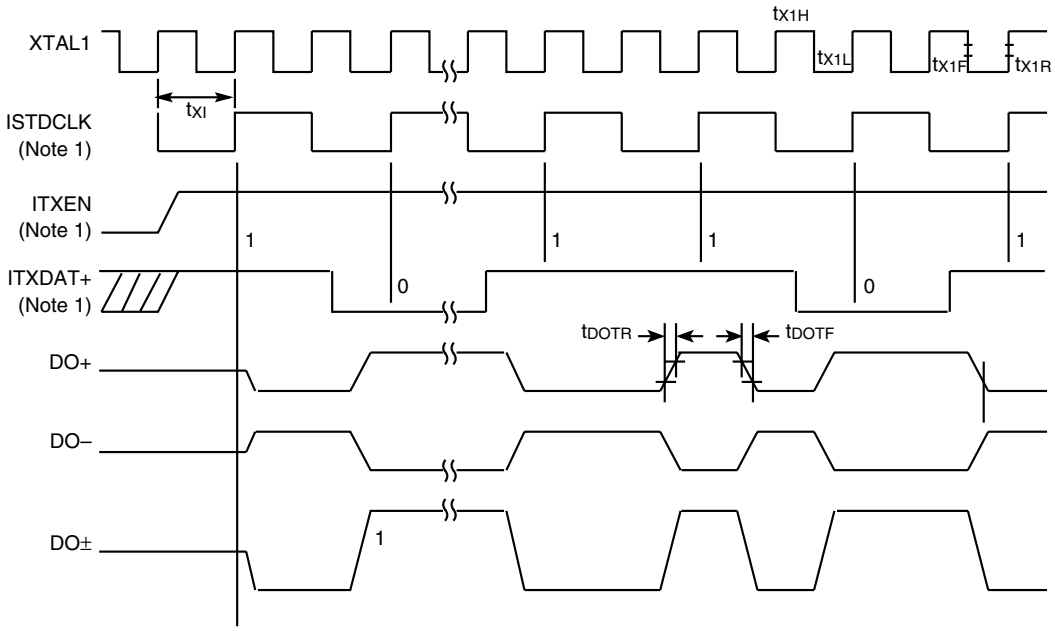


Receive Thresholds (LRT = 1)



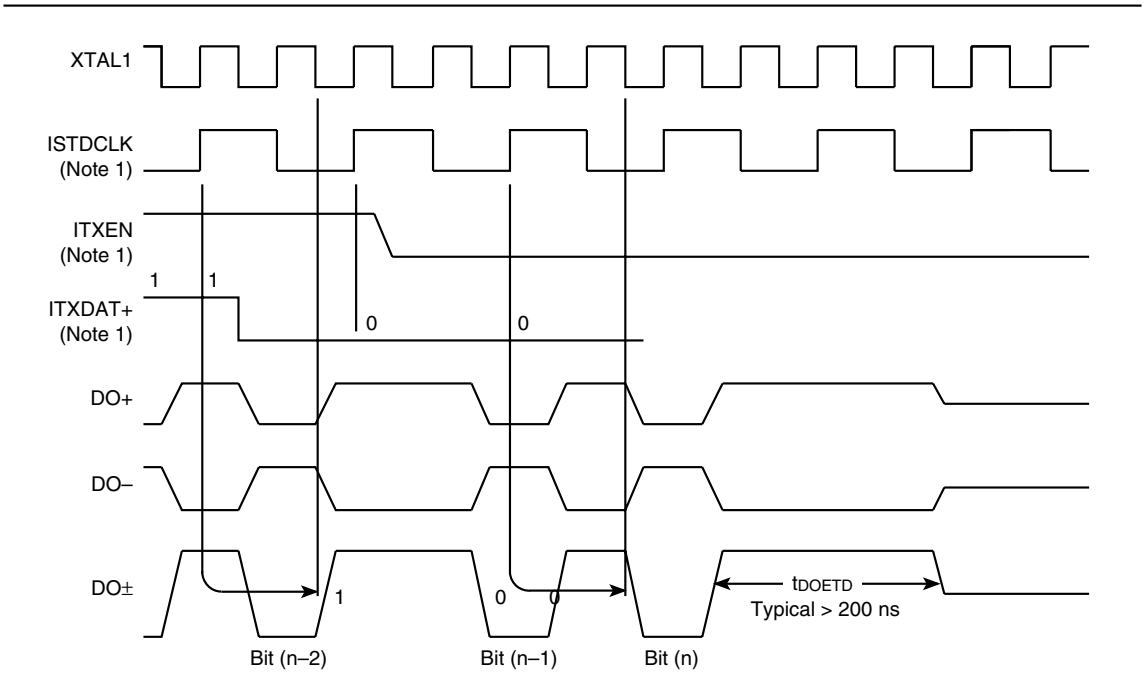
Receive Thresholds (LRT = 0)

SWITCHING WAVEFORMS: AUI



Note 1:
Internal signal and is shown for clarification only.

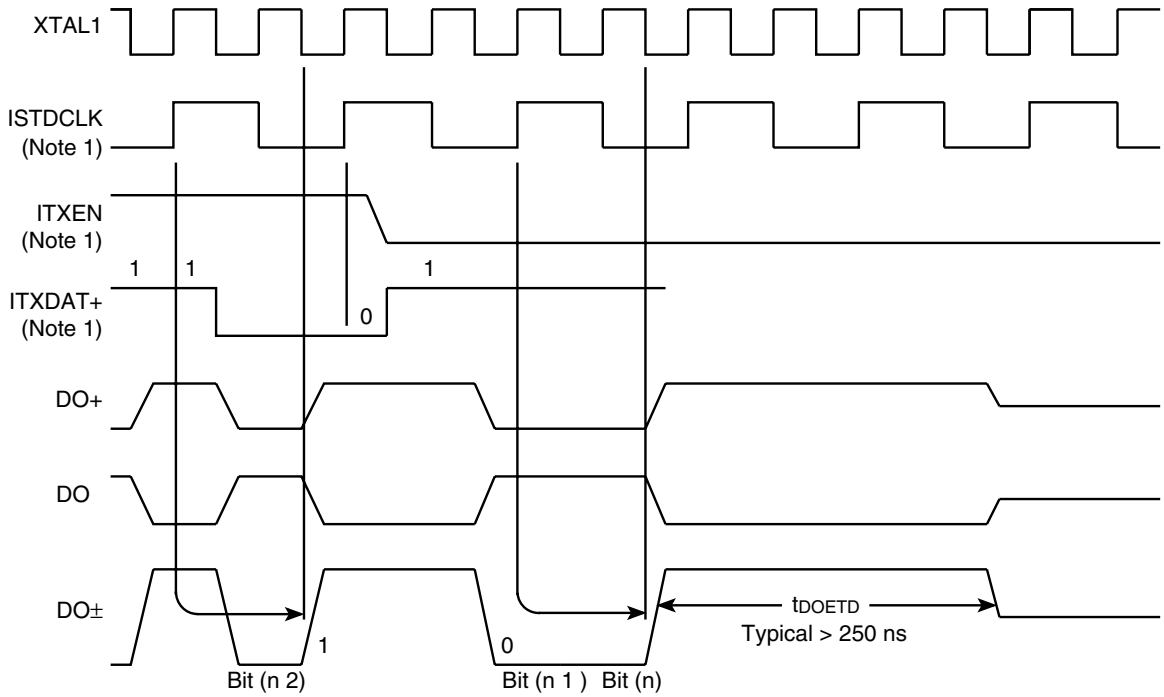
Transmit Timing—Start of Packet



Note 1:
Internal signal and is shown for clarification only.

Transmit Timing—End of Packet (Last Bit = 0)

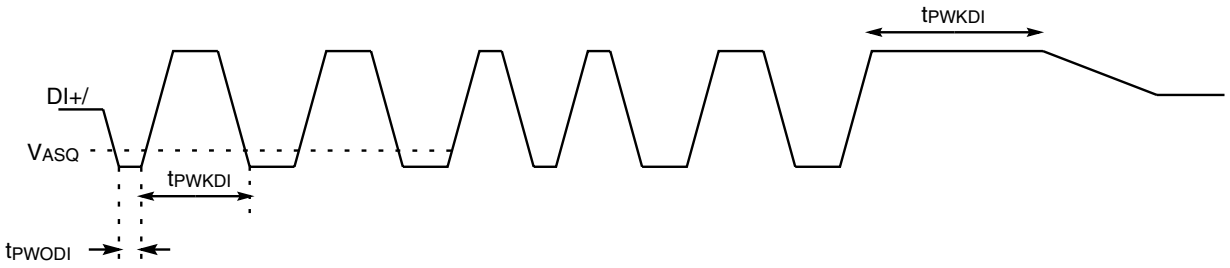
SWITCHING WAVEFORMS: AUI



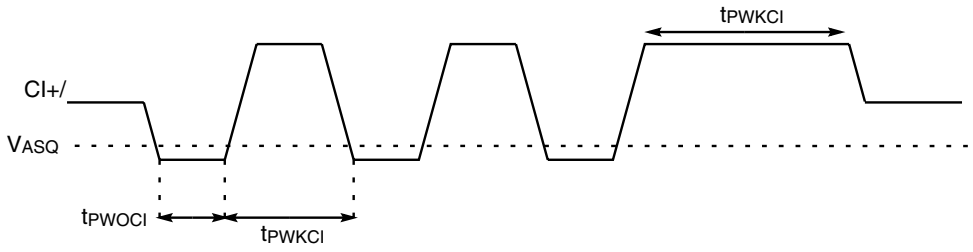
Note 1:
Internal signal and is shown for clarification only.

Transmit Timing—End of Packet (Last Bit = 1)

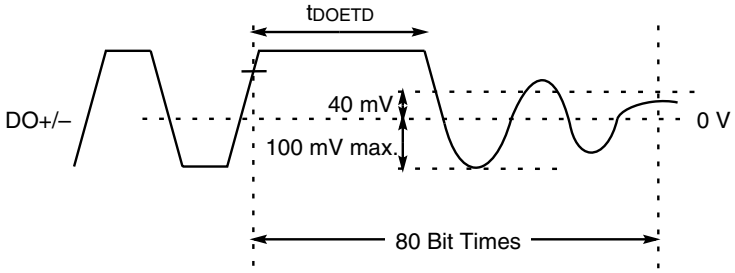
SWITCHING WAVEFORMS: AUI



Receive Timing Diagram

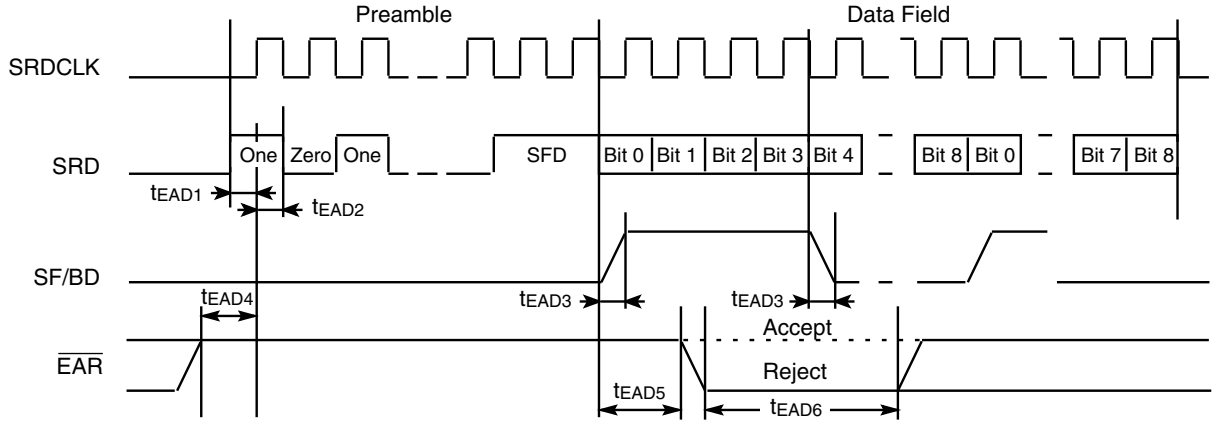


Collision Timing Diagram



Port DO ETD Waveform

SWITCHING WAVEFORMS: EADI



EADI Reject Timing