

Binary to 1-8 Decoder (Low)

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer to units.

$P_D = 315 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 4.0 \text{ ns typ}$
 $t_r, t_f = 2.0 \text{ ns typ (20\%--80\%)}$

MC10161



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

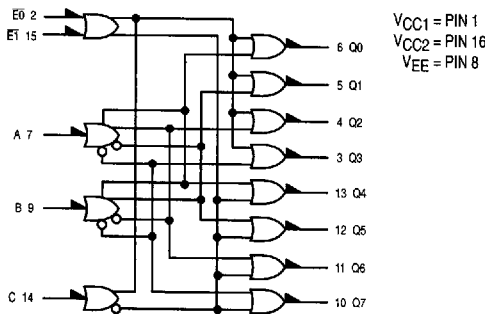


P SUFFIX
PLASTIC PACKAGE
CASE 648-08

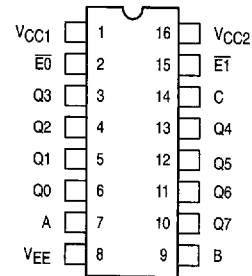


FN SUFFIX
PLCC
CASE 775-02

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H
L	L	L	H	L	H	H	H	L	H	H	H	H
L	L	L	L	L	H	H	H	H	L	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H
L	L	L	H	H	L	H	H	H	H	H	H	L
L	L	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C		+85°C			
			Min	Max	Min	Typ	Max	Min		Max
Power Supply Drain Current	I _E	8		84		61	76		84	mAdc
Input Current	I _{inH}	14		350			220		220	μAdc
	I _{inL}	14	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	13	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		13	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	V _{OL}	13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	13	-1.080		-0.980			-0.910		Vdc
		13	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	V _{OLA}	13		-1.655			-1.630		-1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t ₁₄₊₁₃₋ t ₁₄₋₁₃₊	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns
		13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
Rise Time (20 to 80%)	t ₁₃₊	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	ns
Fall Time (20 to 80%)	t ₁₃₋	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	ns

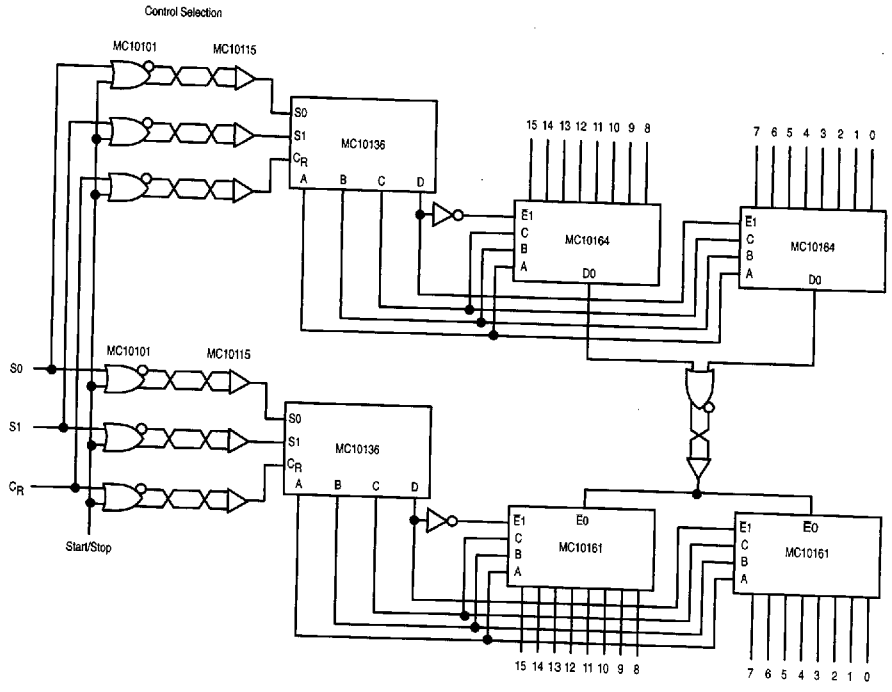
ELECTRICAL CHARACTERISTICS (continued)

3

			TEST VOLTAGE VALUES (Volts)					
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
@ Test Temperature								
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I _E	8	2,7,9,14,15				8	1,16
Input Current	I _{inH}	14	14				8	1,16
	I _{inL}	14		14			8	1,16
Output Voltage Logic 1	V _{OH}	13	2				8	1,16
		13	15				8	1,16
Output Voltage Logic 0	V _{OL}	13	14				8	1,16
Threshold Voltage Logic 1	V _{OHA}	13			2		8	1,16
		13			15		8	1,16
Threshold Voltage Logic 0	V _{OLA}	13			14		8	1,16
Switching Times (50Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₁₄₊₁₃₋ t ₁₄₋₁₃₊	13			14	13	8	1,16
		13			14	13	8	1,16
Rise Time (20 to 80%)	t ₁₃₊	13			14	13	8	1,16
Fall Time (20 to 80%)	t ₁₃₋	13			14	13	8	1,16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



3