A27C256
256K (32K x 8) CHMOS EPROM
Automotive

- **Extended Automotive Temperature Range: −40°C to +125°C**
- **CHMOS/NMOS Microcontroller and Microprocessor Compatible**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **120 ns Maximum Access Time**
- **CMOS and TTL Compatible**
- **Low Power**
  - **30 mA Max. Active**
  - **100 μA Max. Standby**
- **Fast Programming**
  - **Quick-Pulse Programming Algorithm**
  - **Programming Time as Fast as 4 Seconds**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity through EPI Processing**
- **Available in 28-Pin Cerdip Package**
  - **28-Pin Plastic Dip Package**
  - **Compact 32-Lead PLCC**

Intel's A27C256 is a 5V only, 262,144-bit Erasable Programmable Read Only Memory, organized as 32,768 words of 8 bits. Its standard pinouts provide for simple upgrades to 512 Kbits in the future in both DIP and SMT.

The A27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-wait-state operation with the 12 MHz 80286. The A27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run 1-wait-state on a 16 MHz 386™ microprocessor.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 28-pin DIP package, Intel also offers a 32-lead PLCC version of the A27C256. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The A27C256 is equally at home in both TTL and CMOS environments. The Quick-Pulse programming algorithm improves speed as much as 100 times over older methods, further reducing cost for system manufacturers.

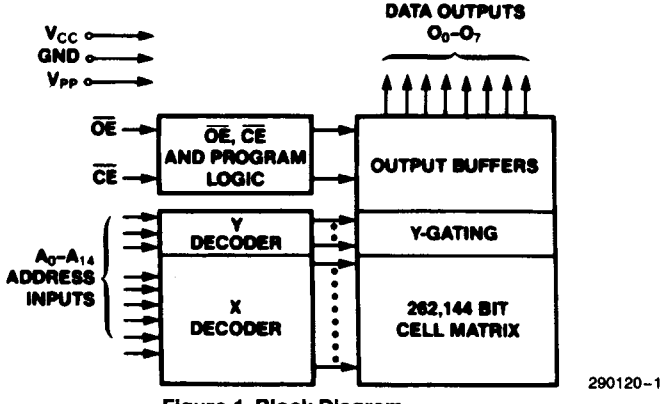


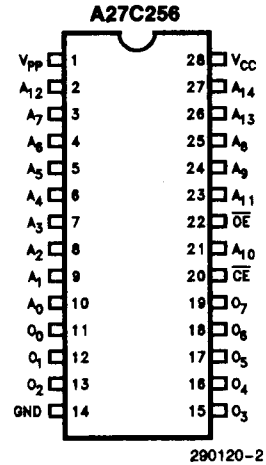
Figure 1. Block Diagram

September 1992
Order Number: 290120-005

Pin Names

A_0–A_{15}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
$\overline{PGM}$	PROGRAM
NC	NO CONNECT
DU	DON'T USE

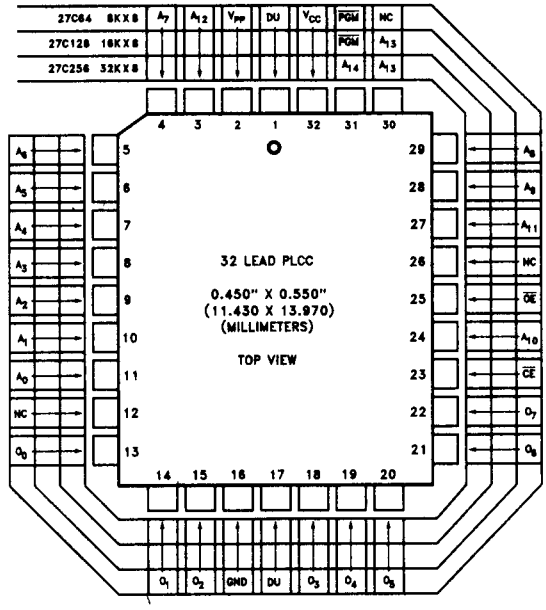
27512 27C512	27128A 27C128	2764A 27C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290120-2

2716	2732A	27C64 27C64	27128A 27C128	27512 27C512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A_{14}
V_{CC}	V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration



290120-3

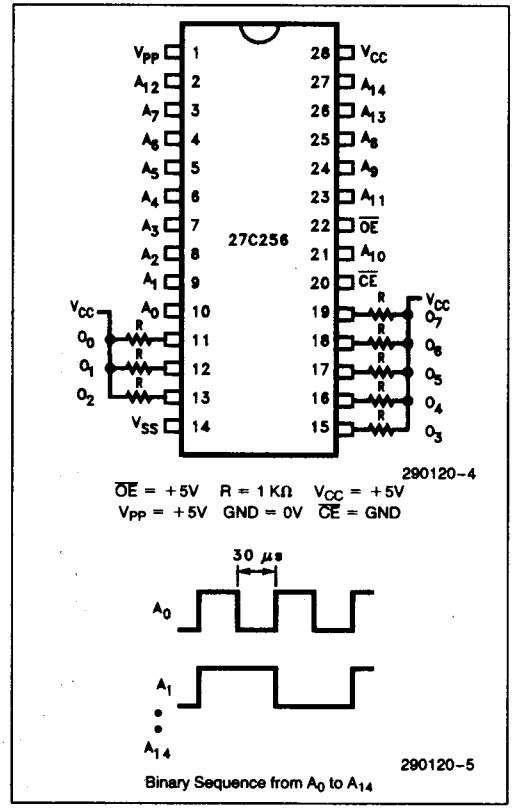
Figure 3. PLCC Lead Configuration

AUTOMOTIVE TEMPERATURE EPROMs

The Intel AUTOMOTIVE EPROM family receives additional processing to enhance product characteristics. AUTOMOTIVE processing is available for several densities allowing the appropriate memory size to match system requirements. AUTOMOTIVE EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications. The AUTOMOTIVE product family is available in −40°C to 125°C operating temperature range versions. Like all Intel EPROMs, the AUTOMOTIVE EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

Options

Speed	Packaging		
	CerDIP	PLCC	PDIP
−120V10	AD	AN	AP
−200V10	AD	AN	AP



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −40°C to 125°C
Temperature Under Bias ..... −40°C to 125°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −2V to 7V(2)
Voltage on A_9 with Respect to GND ..... −2V to 13.5V(2)
V_{PP} Supply Voltage with Respect to GND ..... −2V to 14.0V(2)
V_{CC} Supply Voltage with Respect to GND ..... −2V to 7.0V(2)
Maximum Junction Temperature (T_J) ..... 140°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz
I_{PP}	V_{PP} Operating Current	3			200	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

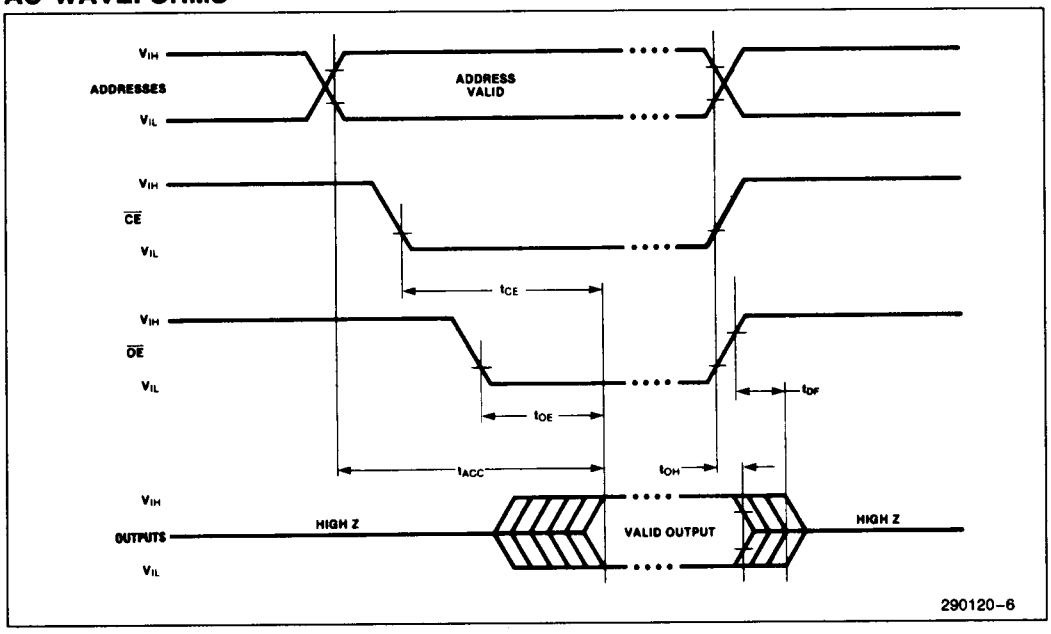
NOTES:
1. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
2. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0 to O_7 unloaded.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
5. Sampled, not 100% tested.
6. Typical limits are at V_{CC} = 5V, T_A = 25°C.

READ OPERATION AC CHARACTERISTICS(1) V_{CC} = 5.0V ± 10%

Versions		V_{CC} ±10%	A27C256-120V10		A27C256-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			120		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		55		75	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		30		55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.

AC WAVEFORMS



CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled, not 100% tested.

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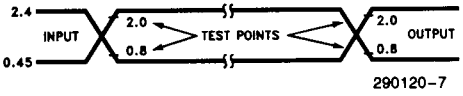
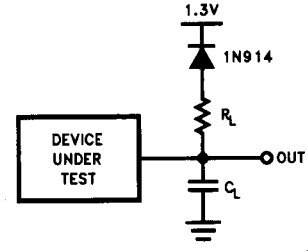
AC INPUT/OUTPUT REFERENCE WAVEFORM



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

DEVICE OPERATION

The Mode Selection table lists A27C256 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during Intelligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	1	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby		V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	2	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	V_{CP}	HIGH Z
Intelligent Identifier -Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89 H
Intelligent Identifier -Device	2, 3, 4	V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	V_{CC}	8D H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10-14} = V_{IL}.
4. Programming equipment may also refer to this device as the A27C256A. Older devices may have device ID = 8CH.

Read Mode

The A27C256 has two control functions, both must be enabed to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" are programmed, the data word can contain both "1's" and "0's". Ultraviolet light erasure is the only way to change "0's" to "1's".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE} = V_{IH}$ programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

Intelligent Identifier Mode

The Intelligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V + 0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{14} at V_{IL}, $A_0 = V_{IL}$ will present the manufacturer code and $A_0 = V_{IH}$ the device code. This mode functions in the 25°C ± 5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to the 512 Kbit density is easily accomplished due to the standardized pin configuration of the A27C256. A jumper between A_{15} and V_{CC} allows upgrade using the V_{PP} pin. Systems designed for 256 Kbit program memories today can be upgraded to 512 Kbit in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain flourescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

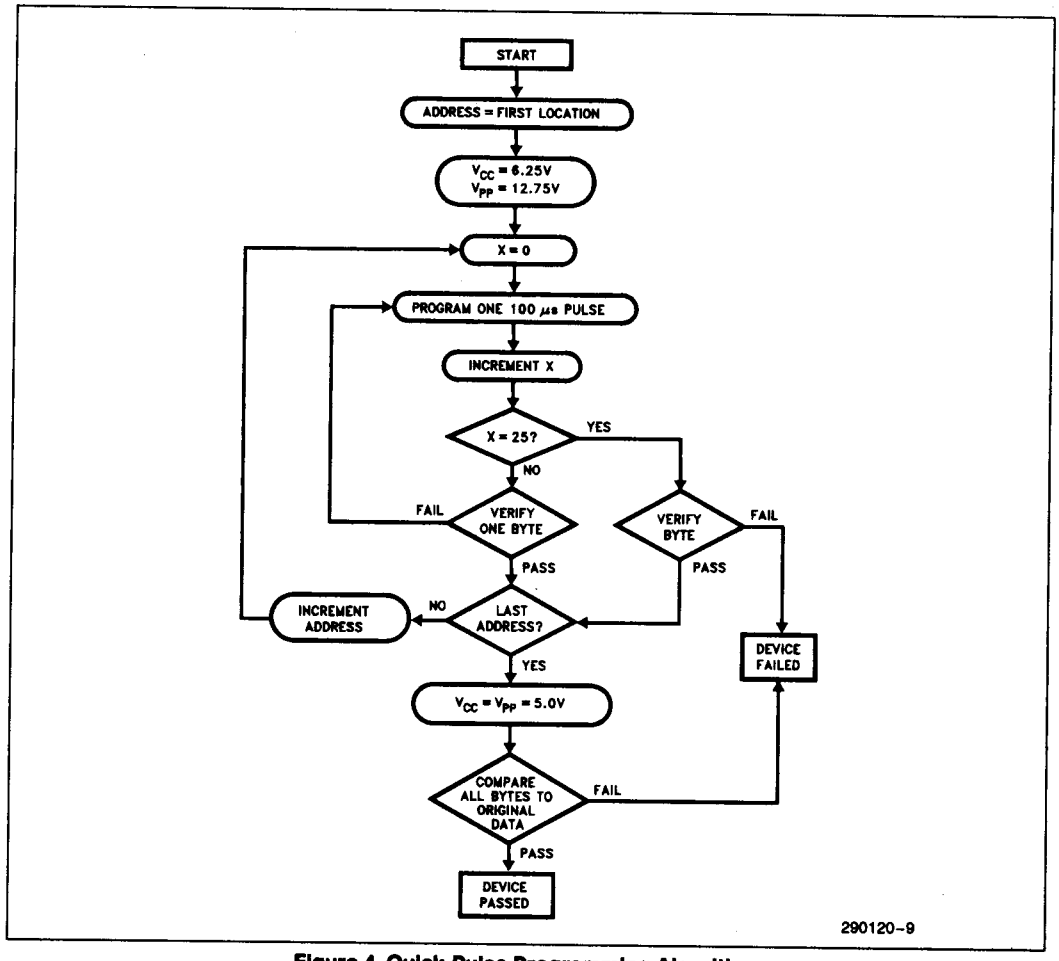


Figure 4. Quick-Pulse Programming Algorithm

Quick-Pulse Programming Algorithm

The Quick-Pulse Programming algorithm programs Intel's A27C256. Developed to substantially reduce programming throughput, this algorithm can program the A27C256 as fast as 4 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 µs pulse followed by a byte verification to determine when the addressed byte has been sucessfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, the A27C256 has also been characterized for the Quick-Board Programming Algorithm. The Quick-Board Programming Algorithm was developed for specific automotive applications using Intel's 1.0 micron EPROM products. Contact the factory or an automotive sales representative for any information regarding the Quick-Board Programming Algorithm.

DC PROGRAMMING CHARACTERISTICS T_A = 25°C ±5°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			30	mA	$\overline{CE} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage (Verify)		3.5			V	I_{OH} = −2.5 mA
V_{ID}	A_9 Intelligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) T_A = 25°C ±5°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current value is with outputs O_0 to O_7 unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurments.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

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PROGRAMMING WAVEFORMS