SN54H78, SN54L78, SN54LS78A, SN74H78, SN74LS78A

Dual J-K Flip-Flops

The ‘H78 and ‘L78 contain two J-K flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The ‘H78 and ‘L78 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The ‘LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

DUAL J–K FLIP–FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

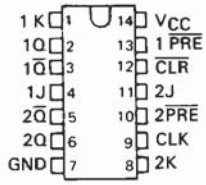
The 'H78 and 'L78 contain two J-K flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The 'H78 and 'L78 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

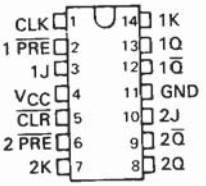
The SN54H78, SN54L78, and the SN54LS78A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H78 and the SN74LS78A are characterized for operation from 0°C to 70°C.

FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY

SN54H78 . . . J PACKAGE
SN74H78 . . . J OR N PACKAGE
(TOP VIEW)



SN54L78 . . . J PACKAGE
SN54LS78A . . . J OR W PACKAGE
SN74LS78A . . . D, J OR N PACKAGE
(TOP VIEW)



'H78, 'L78
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓	L	L	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

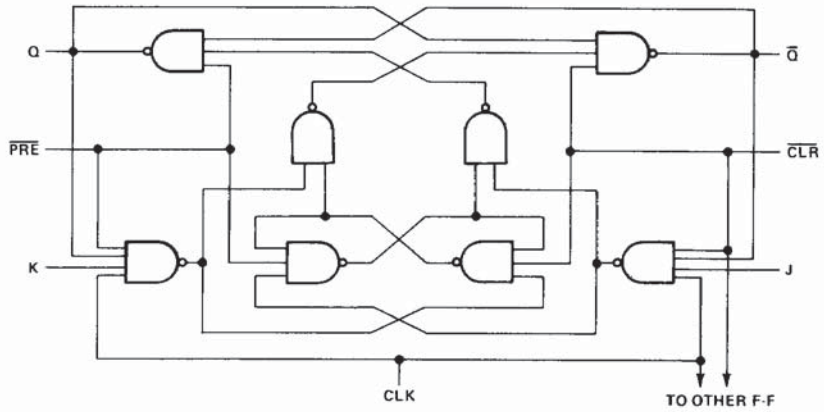
'LS78A

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

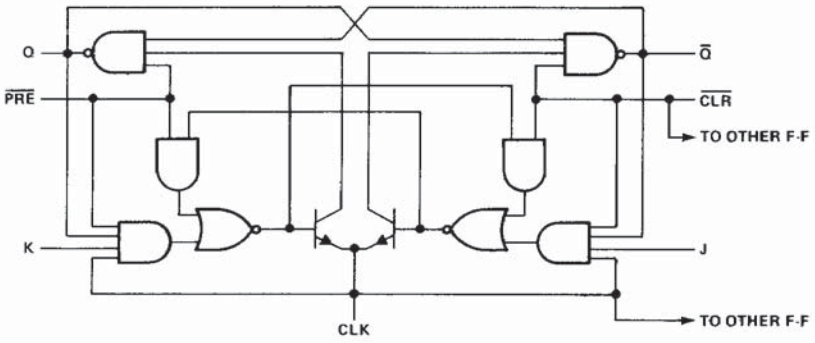
† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

logic diagrams

'H78



'L78



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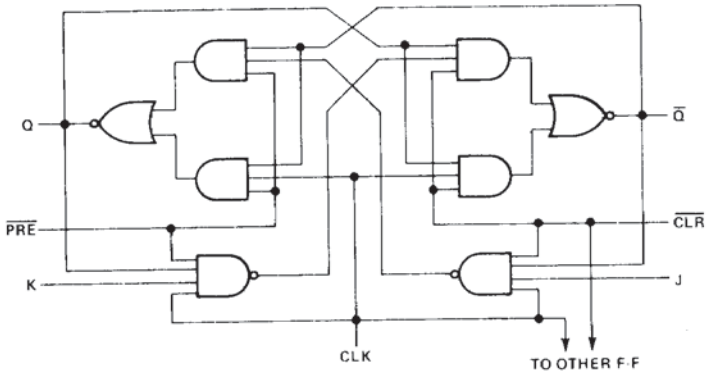
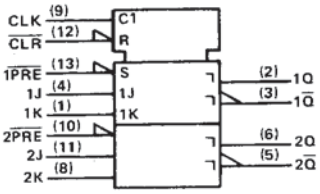
logic diagrams (continued)

'LS78A



logic symbols

'H78



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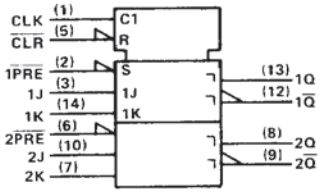
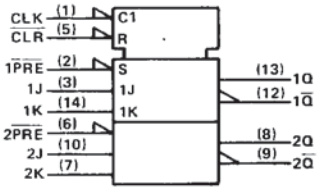


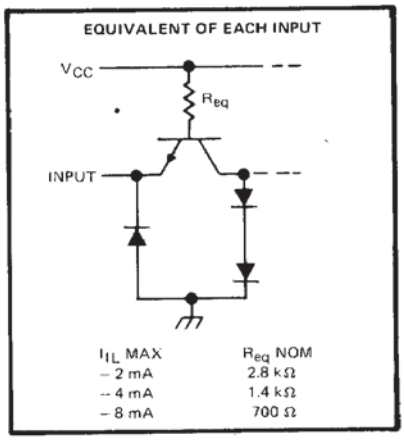
'LS78A



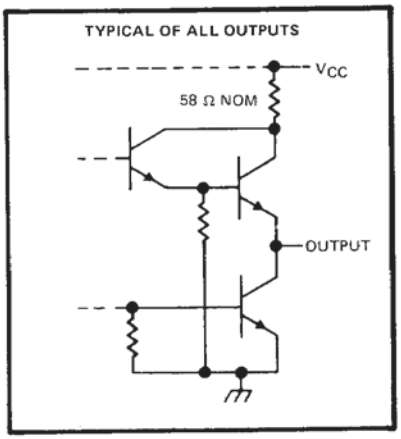
Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs

'H78

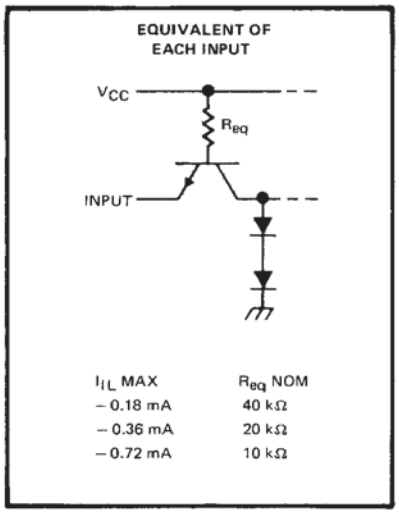


'H78

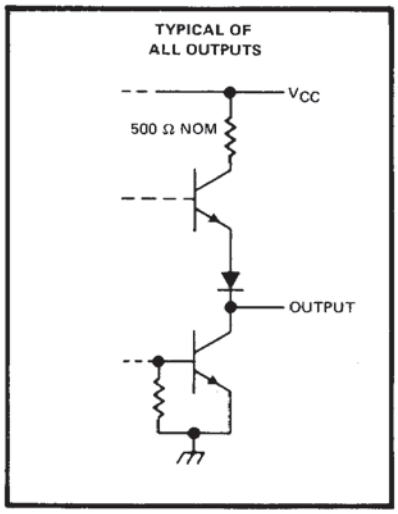


schematics of inputs and outputs (continued)

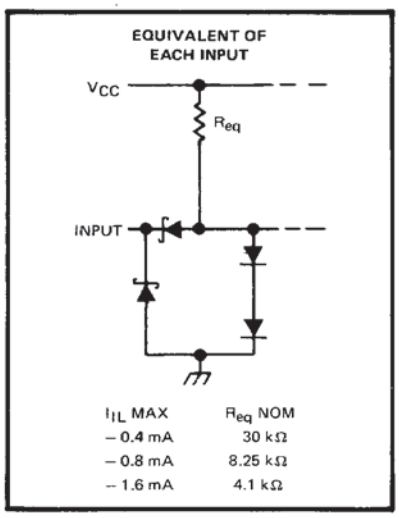
'L78



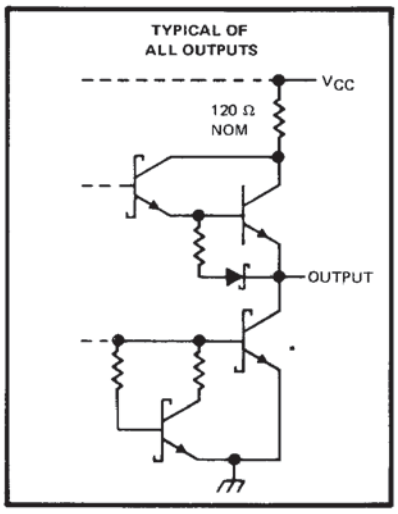
I_{IL} MAX	R_{eq} NOM
−0.18 mA	40 kΩ
−0.36 mA	20 kΩ
−0.72 mA	10 kΩ



'LS78A



I_{IL} MAX	R_{eq} NOM
−0.4 mA	30 kΩ
−0.8 mA	8.25 kΩ
−1.6 mA	4.1 kΩ



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: 'H78, 'L78 . . . . . 5.5 V
'LS78A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54H78			SN74H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.5			−0.5	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	12			12			ns
		CLK low	28			28			
		$\overline{CLR}$ or $\overline{PRE}$ low	16			16			
t_{su}	Setup time before CLK ↑	data high or low	0			0			ns
t_h	Hold time-data after CLK ↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54H78			SN74H78			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −8 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.5 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.4 V				50			50	μA
	CLR						200			200	
	$\overline{PRE}$ or CLK						100			100	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−2			−2	mA
	$\overline{CLR}$★						−8			−8	
	$\overline{PRE}$★						−4			−4	
	CLK						−4			−4	
I_{OS}§		V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CC}		V_{CC} = MAX,	See Note 2			16	25		16	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than output should be shorted at a time, and the duration of the short circuit should not exceed one second.
★ Clear is tested with preset high and preset is tested with clear high.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 25 pF	25	30		MHz
t_{PLH}	$\overline{CLR}$ or $\overline{PRE}$	Q or $\overline{Q}$			6	13	ns
t_{PHL}					12	24	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	21	ns
t_{PHL}					22	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	Clock input			0.6	V
		All other inputs			0.7	
I_{OH}	High-level output current				−0.1	mA
I_{OL}	Low-level output current				2	mA
t_w	Pulse duration	CLK high or low	200			ns
		$\overline{CLR}$ or $\overline{PRE}$ low	100			
t_{su}	Setup time before CLK ↑		0			ns
t_h	Hold time-data after CLK ↓		0			ns
T_A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.1 mA	2.4	3.3		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OL} = 2 mA		0.15		V
I_I	J or K	V_{CC} = MAX, V_I = 5.5 V			0.1	mA
	$\overline{PRE}$				0.2	
	CLK or $\overline{CLR}$				0.4	
I_{IH}	J or K	V_{CC} = MAX, V_I = 2.4 V			10	μA
	$\overline{CLR}$				40	
	$\overline{PRE}$				20	
	CLK				−400	
I_{IL}	J or K	V_{CC} = MAX, V_I = 0.3 V			−0.18	mA
	$\overline{PRE}$				−0.36	
	CLK or $\overline{CLR}$				−0.72	
I_{OS}		V_{CC} = MAX	−3		−15	mA
I_{CC}		V_{CC} = MAX, See Note 2		0.76	1.44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 4 kΩ, C_L = 50 pF	2.5	3		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			35	75	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			60	150	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)					200	
t_{PLH}	CLK	Q or $\overline{Q}$		10	35	75	ns
t_{PHL}				10	60	150	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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recommended operating conditions

			SN54LS78A			SN74LS78A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK ↓	data high or low	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	20			20			
t_h	Hold time-data after CLK ↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS78A			SN74LS78A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.7 V,	2.5	3.4					V
		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,				2.7	3.4		
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	J or K	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$						0.6			0.6	
	$\overline{PRE}$						0.3			0.3	
	CLK						0.8			0.8	
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$						120			120	
	$\overline{PRE}$						60			60	
	CLK						160			160	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$						−1.6			−1.6	
	$\overline{PRE}$						−0.8			−0.8	
	CLK						−1.6			−1.6	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC}		V_{CC} = MAX,	See Note 2			4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
t_{PLH}	$\overline{PRE}$, $\overline{CLR}$ or CLK	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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