Sound Processor Series for FPD TVs

Sound Processor with built-in Loudness

BD3869AF

●**Description**

BD3869AF is a 2ch sound processor with built-in loudness and volume control. It has low noise and low distortion due to the resistor ladder configuration. The IC current consumption is 3mA. The device is packaged in SOP18.

●**Features**

1) Resistor ladder type circuit, used for Volume and Tone control, achieving low noises and low distortion and reduced switching shock sound.
2) The I^2C BUS can control up to 3 devices. For Dolby digital applications, the 6ch can be used simultaneously.
3) High-performance functions are integrated into a compact package, idea for surround speakers and sub-woofers.
4) The center frequency and Q value in Bass characteristics can be changed by external components.

●**Applications**

TV units such as DVD, PC, Hi-vision, Karaoke, digital broadcasting and CATV. Also for car and portable audio.

● **Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Limits	Unit
Applied voltage	VCC	10.0	V
Input voltage	Vin	VCC+0.3～GND-0.3	V
Power Dissipation	Pd	680 *1	mW
Operating temperature	Topr	-40～+85 *2	°C
Storage temperature	Tastg	-55～+150	°C

*1 Reduced by 5.5 mW/°C at 25°C or higher.
Thermal resistance θja = 181.8 (°C/W). (when Rohm standard board is mounted.)
Rohm standard board: Size: 70×70×1.6 (mm^3)
Material: FR4 glass-epoxy substrate (copper foil area: not more than 3%).

*2 As long as voltage stays within operating voltage range, certain circuit operation is guaranteed in the operating temperature range.
Allowable power loss conditions are related to temperature, to which care must be taken.
In addition though the standard value of its electrical characteristics cannot be guaranteed under the conditions other than those specified, basic functions are maintained.

● **Operating voltage range**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage *3	VCC	5.3	9.0	9.5	V

Basic operation at Ta=25°C.

*3 As long as temperature and operating voltage meet specifications
In addition, though the standard value of its electrical characteristics cannot be guaranteed under the conditions other than those specified, basic functions are maintained.

● **Electric characteristics** (BD3869AF)

Unless specified: Ta=25℃, VCC=9V, f=1kHz, Vin=1Vrms, Rg=600Ω, RL=10kΩ, front volume = 0dB, Rear volume = 0dB, Bass = 0dB, Treble = 0dB, Loudness = OFF

	Parameter	Symbol	Limits			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Circuit current upon no signal	IQ	-	3	7	mA	Vin=0Vrms
	Maximum input voltage	VIM	2.2	2.5	-	Vrms	Front Volume = -6dB, THD(Vout)=1%
	Maximum output voltage	VOM	2.1	2.5	-	Vrms	THD=1%
	Voltage gain	GV	-2	0	2	dB	Gv=20log(Vout/Vin)
	Channel balance	CB	-1.5	0	1.5	dB	CB = Gv1-Gv2
	Total harmonic distortion	THD	-	0.01	0.2	%	Vout=1Vrms, BPF=400-30kHz
	Output noise voltage *	VNO	-	2.3	15	μVrms	BPF = IHF-A, Rg=0Ω
	Residual noise voltage *	VMNO	-	1.4	10	μVrms	Front Volume = -89dB Rear Volume = -∞, BPF = IHF-A, Rg=0Ω
	Cross talk *	CT	70	95	-	dB	CT = 20log(Vin/Vout), BPF=IHF-A
	Input impedance	RIN	42	60	78	KΩ	In case of no external loudness
VOLUME	Front volume control range	VATTF	-92	-89	-86	dB	VATT=20log(Vout/Vin), BPF=IHF-A
	Front volume switching step	SVFC	-	1	-	dB	
	Front volume set error 1	EVFC1	-2	0	+2	dB	0dB to –63dB
	Front volume set error 2	EVFC2	-3	0	+3	dB	-64dB to –89dB
	Rear volume control range	V_{ATTR}	-	-100	-90	dB	V_{ATT}=20log(Vout/Vin), BPF=IHF-A
	Rear volume switching step 1	SVRC1	-	1	-	dB	0dB to –10dB
	Rear volume switching step 2	SVRC2	-	2	-	dB	-10dB to –20dB
	Rear volume switching step 3	SVRC3	-	5	-	dB	-20dB to –35dB
	Rear volume switching step 4	SVRC4	-	10	-	dB	-35dB to –45dB
	Rear volume switching step 5	SVRC5	-	15	-	dB	-45dB to –60dB
	Rear volume set error 1	EVRC1	-2	0	+2	dB	0dB to –35dB
	Rear volume set error 2	EVRC2	-3	0	+3	dB	-45dB , -60dB
	Volume maximum attenuation	A_{TTMAX}	-	-114	-90	dB	Front Volume=-89dB Rear Volume=-∞ A_{TTMAX}=20log(Vout/Vin), BPF=IHP-A
BASS	Bass boost control range	V_{BBMAX}	+11	+14	+17	dB	f=80Hz, Vin=100mVrms Bass = +14dB, V_{BBMAX}=20log(Vout/Vin)
	Bass cut control range	V_{BCMAX}	-17	-14	-11	dB	f=80Hz, Vin=100mVrms Bass = -14dB, V_{BBMAX}=20log(Vout/Vin)
	Bass control step	SBC	-	2	-	dB	f=80Hz
	Bass set error (0dB-8dB)	EBS1	-2	0	2	dB	
	Bass set error (10dB-14dB))	EBS2	-3	0	3	dB	
TREBLE	Treble boost control range	V_{TBMAX}	+11	+14	+17	dB	f=15kHz, Vin=100mVrms Treble = +14dB, V_{TMAX}=20log(Vout/Vin)
	Treble cut control range	V_{TCMAX}	-17	-14	-11	dB	f=15kHz, Vin=100mVrms Treble = -14dB, V_{TMAX}=20log(Vout/Vin)
	Treble control step	STC	-	2	-	dB	f=15kHz
	Treble set error (0dB-8dB)	ETS1	-2	0	2	dB	
	Treble set error (10dB-14dB)	ETS2	-3	0	3	dB	
I^2C BUS	ACK LOW level output voltage	VOL	0	-	0.4	V	Sink current =3mA
	SCL、SDA input HI level	VIHI	3.0	5	5.5	V	
	SCL、SDA input LOW level	VILO	-0.5	0	1.5	V	

＊VP-9690A (Average value detection, effective value display) IHF-A filter by Matsushita Communication is used for measurement.

＊Phase of I/O signal terminals is the same.

＊This IC is not designed to be radiation-resistant.

● **Timing chart**

Electric specifications and timing of bus line and I/O stages

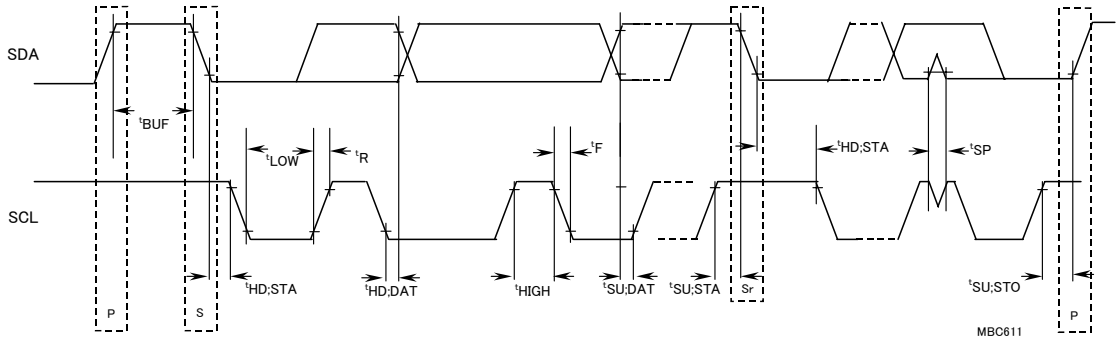


Fig.-1 Timing definition on I^2C BUS

Table 1: Characteristics of the SDA and SCL BUS lines for I^2C BUS devices

Parameter		Symbol	Standard mode I^2C BUS		Unit
			Min.	Max.	
1	SCL clock frequency	f_{SCL}	0	100	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	4.7	-	µs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD};S_{TA}$	4.0	-	µs
4	LOW period of the SCL clock	t_{LOW}	4.7	-	µs
5	HIGH period of the SCL clock	t_{HIGH}	4.0	-	µs
6	Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	µs
7	Data hold time	$t_{HD;DAT}$	0*	-	µs
8	Data set-up time	$t_{SU;\ DAT}$	250	-	ns
9	Rise time of both SDA and SCL signals	t_R	-	1000	ns
10	Fall time of both SDA and SCL signals	t_F	-	300	ns
11	Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	µs
12	Capacitive load for each bus line	Cb	-	400	pF

Above numerical values all correspond to $V_{IH\ min}$ and $V_{IL\ max}$ levels (see Table 2).

*The transmitter must internally provide at least 300 ns hold-time for SDA signals (at $V_{IH\ min}$ of SCL signals) in order to cross over undefined region at the fall-end of SCL.

Table 2: Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

Parameter		Symbol	Standard mode I^2C BUS		Unit
			Min.	Max.	
13	Low-level input voltage: fixed input levels	V_{IL}	-0.5	1.0	V
14	Low-level input voltage: fixed input levels	V_{IH}	2.3	-	V
15	Hysteresis of Schmitt trigger inputs: fixed input levels	V_{hys}	n/a	n/a	V
16	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	n/a	n/a	ns
17	Low-level output voltage (open drain): at 3mA sink current	V_{OL1}	0	0.4	V
18	Output fall time from VIHmin. to VIHmax. with a bus capacitance from 10 pF to 400pF: with up to 3mA sink current at VOL1	t_{OF}	-	250	ns
19	Input current each I/O pin with an input voltage between 0.4V and 0.9 VCCmax.	Ii	-10	10	µA
20	Capacitance for each I/O pin	Ci	-	10	pF

n/a = not applicable

●**Data format**

Slave addresses

Since slave address can be changed by the setting of CHIP(7pin), a maximum of 3 pcs can be used at the same time.

CHIP(pin7) Condition	MSB			Slave Address				LSB
	A6	A5	A4	A3	A2	A1	A0	R/W
GND - 0.2×Vcc	1	0	0	0	0	0	0	0
0.4×Vcc - 0.6×Vcc	1	0	0	0	0	0	1	0
0.8×Vcc – Vcc	1	0	0	0	0	1	0	0

Set the voltage of 7pin to within the defined conditions.

Select addresses

Parameter		MSB			Select Address				LSB
		D7	D6	D5	D4	D3	D2	D1	D0
0	Front Volume	0	0	0	0	0	0	0	0
1	Rear Volume	0	0	0	0	0	0	0	1
2	Bass / Treble	0	0	0	0	0	0	1	0

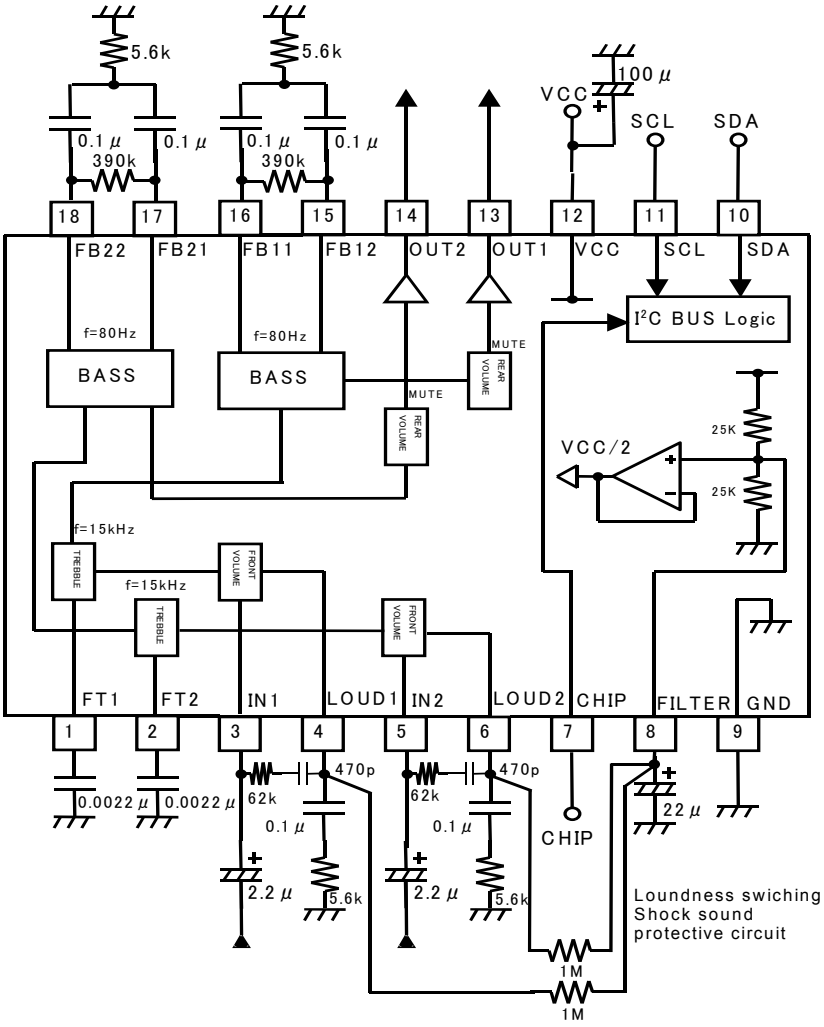
Data format

Parameter		Select Address	MSB			Data				LSB
			D7	D6	D5	D4	D3	D2	D1	D0
0	Front Volume	00H	Loud	Front Volume B		Front Volume A				
1	Rear Volume	01H	*	Channel Select		Rear Volume				
2	Bass / Treble	02H	Bass Gain				Treble Gain			

●**Operation Notes**

1. Numbers and data in entries are representative design values and are not guaranteed values of the items.
2. Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.
3. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
4. GND potential
   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
5. Thermal design
   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.
6. Short circuit between terminals and erroneous mounting
   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
7. Operation in strong electromagnetic field
   Using the ICs in a strong electromagnetic field can cause operation malfunction.

●**Application circuit diagram**



Unit
R : [Ω]
C : [F]

Fig. 2 Examination of application circuit

Terminal No.	Terminal name	Description of terminal	Terminal No.	Terminal name	Description of terminal
1	FT1	CH1 treble filter set terminal	10	SDA	I^2C communication terminal
2	FT2	CH2 treble filter set terminal	11	SCL	I^2C communication clock terminal
3	IN1	CH1 input terminal	12	VCC	Power supply terminal
4	LOUD1	CH1 loudness filter set terminal	13	OUT1	CH1 output terminal
5	IN2	CH2 input terminal	14	OUT2	CH2 output terminal
6	LOUD2	CH2 loudness filter set terminal	15	FB11	CH1 bus filter set terminal
7	CHIP	Chip select terminal	16	FB12	CH1 bus filter set terminal
8	FILTER	1/2VCC terminal	17	FB21	CH2 bus filter set terminal
9	GND	Ground terminal	18	FB22	CH2 bus filter set terminal

●**Reference data**

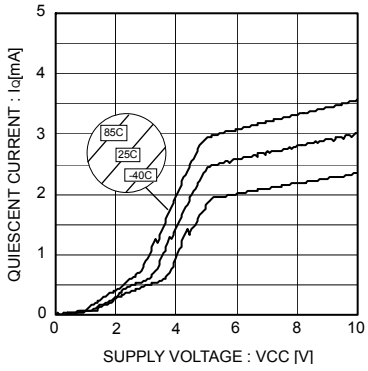


Fig.3 Quiescent current vs Supply voltage

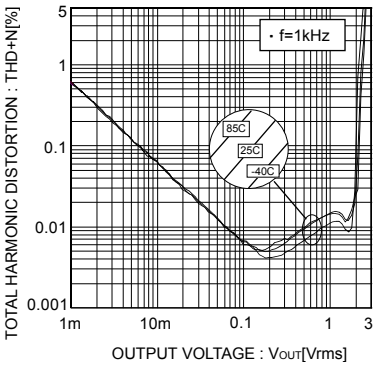


Fig.4 Total harmonic distortion vs Output voltage

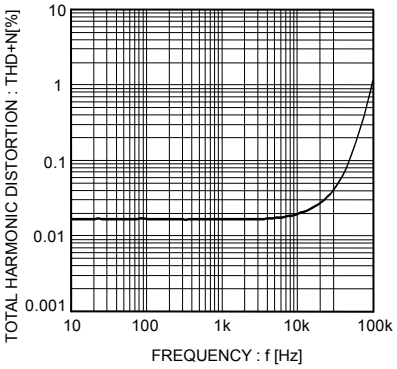


Fig.5 Total harmonic distortion vs Frequency

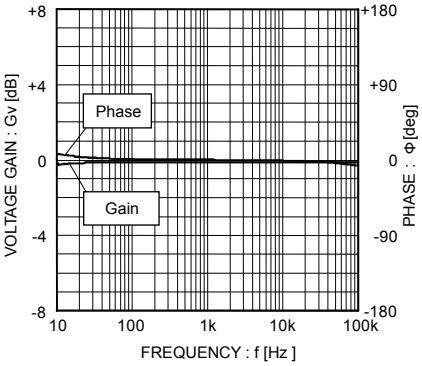


Fig.6 Voltage gain/phase vs. Frequency

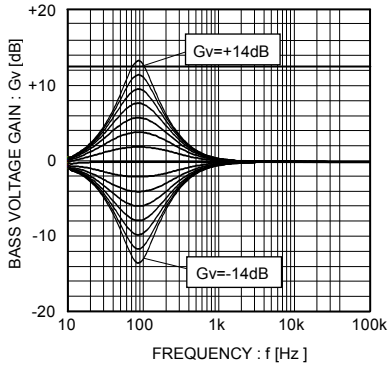


Fig.7 Bass Voltage gain vs Frequency

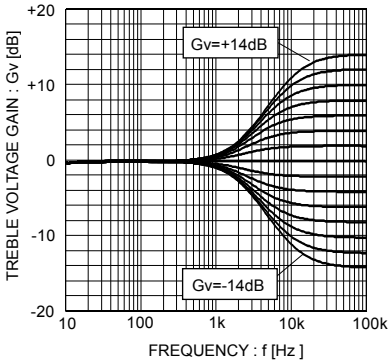


Fig.8 Treble Voltage gain vs Frequency

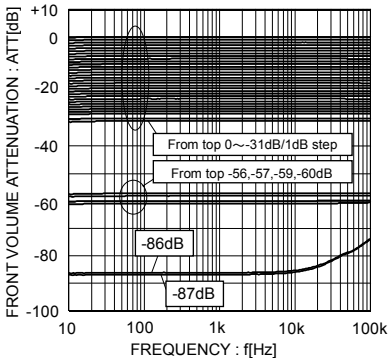


Fig.9 Front volume attenuation vs Frequency (loudness=OFF)

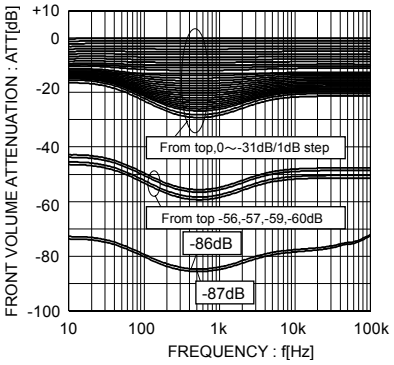


Fig.10 Front volume attenuation vs Frequency (loudness =ON)

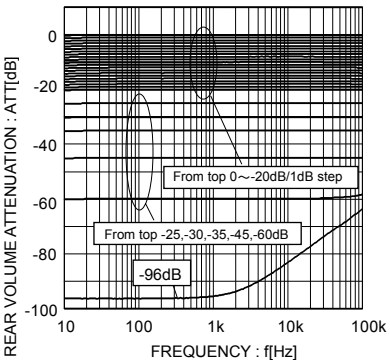


Fig.11 Rear volume attenuation vs Frequency

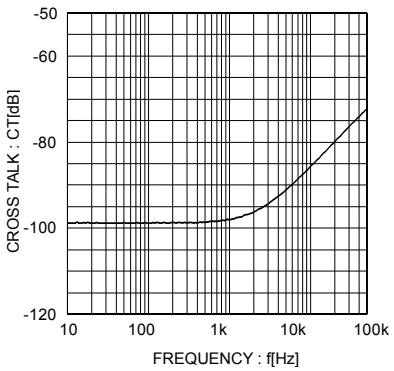


Fig.12 Cross talk vs Frequency

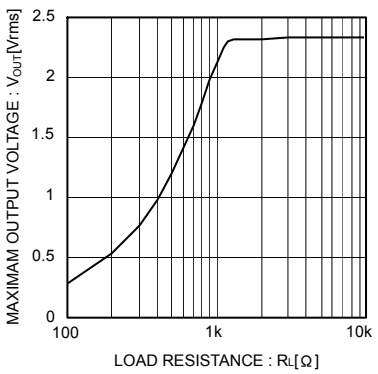


Fig.13 Maximum output voltage vs Load resistance

●**Selection of order type**

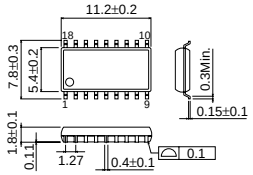
B	D	3	8	6	9	A	F	—	E	2

Part No.
BD3869AF

Tape and Reel information
BD3869AF E2

SOP18

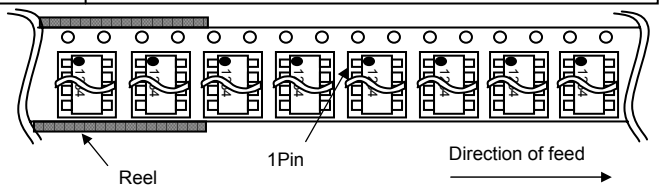
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (Correct direction: 1pin of product should be at the upper left when you hold reel on the left hand, and you pull out the tape on the right hand)



※Orders are available in complete units only.

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