Sound Processor Series for Car Audios

Sound processors with built-in 2-band Equalizer

BD3481FS, BD3482FS

●Description

BD3481FS/BD3482FS are sound processor having in it the stereo 4ch input selector, gain amplifier, stereo primary volume, 4ch fader volume, 2-band equalizer. There is no need for any particular microcomputer control In order to reduce various shock sounds of switching. Therefore, work to develop software can be reduced drastically.

●Features

1. Reduce the shock sounds of switching of Primary / Fader Volume attenuation and Tone by using advanst switching circuit.
2. Taking in a filter of bass and treble inside can reduce the external parts.
3. Bi-CMOS process
4. Reduce the noise of through mode by using tone-pass route.
5. Built-in ground isolation amplifier input, suited for external stereo input.
6. The package of this IC is SSOP-A20/SSOP-A24. It gathers a sound input terminals, sound output terminals respectively and it arranges them, to be arranging facilitates the laying-out of PCB pattern and reduces PCB area to one-way in the flow of the signal.

●Use

Best suited for car audio, and can be used for other audio units including TV, mini compo and micro compo.

●Product Lineup

Item	BD3481FS	BD3482FS
Output terminal of Input Gain	—	○
PKG	SSOP-A20	SSOP-A24

1) Data format of I^2C BUS is common for BD3481FS/BD3482FS.
2) Pin configuration are almost same for BD3481FS/BD3482FS.

●Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Limit	Unit
Impressed Voltage	VCC	10.0	V
Input Voltage	VIN	VCC+0.3～GND-0.3	V
Power Dissipation	BD3481FS	940 ※1	mW
	BD3482FS	1000 ※2	
Storage Temperature	Tastg	-55～+150	℃

※1 At Ta＝25°C or higher, this value is decreaced to 7.5mW/°C. Thermal resistance θja=133.3 (℃/W)
※2 At Ta＝25°C or higher, this value is decreaced to 8mW/°C. Thermal resistance θja=125.0 (℃/W)
When Rohm standard board is mounted.
Rohm standard board: size: 70×70×1.6 (mm^3)
material: FR4 glass-epoxy substrate (copper foil area: not more than 3%).

●Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	7.0	–	9.5	V
Temperature	Topr	-40	–	+85	℃

※ Design against radiation-proof isn't made.

Mar. 2007

●Electrical Characteristic

(Unless specified particularly, Ta=25℃, VCC=8.5V, f=1kHz, Vin=1Vrms, Rg=600Ω, RL=10kΩ, A input, Input gain 0dB, Primary Volume 0dB, Bass 0dB, Treble 0dB, Fader Volume 0dB)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Current upon no signal	IQ	–	15	30	mA	No signal
	Voltage gain	G_V	-1.5	0	1.5	dB	Gv = 20log(VOUT/VIN)
	Channel balance	CB	-1.5	0	1.5	dB	CB = GV1-GV2
	Total harmonic distortion	THD+N	–	0.005	0.05	%	VOUT = 1Vrms, BW = 400-30KHz
	Output noise voltage ＊	V_{NO}	–	6	25	μVrms	Rg = 0Ω, BW = IHF-A
	Residual output noise voltage ＊	V_{NOR}	–	2	10	μVrms	Fader = -∞dB, Rg = 0Ω BW = IHF-A
	Cross-talk between channels ＊	CTC	–	-100	-90	dB	Rg = 0Ω, BW = IHF-A CTC = 20log(VOUT/VOUT)
	Ripple rejection	RR	–	-70	-40	dB	Rg=0Ω f=100Hz VRR=100mVrms RR=20log(VOUT/VCCIN)
INPUT SELECTOR	Input impedance (A,B,C)	R_{IN}	70	100	130	kΩ	
	Input impedance (D)	R_{IN}	35	50	65	kΩ	
	Maximum input voltage	V_{IM}	2.1	2.3	–	Vrms	VIM at THD+N(VOUT)=1% BW = 400-30KHz
	Cross-talk between selectors ＊	CTS	–	-100	-90	dB	Rg = 0Ω, BW = IHF-A CTS = 20log(VOUT/VOUT)
	Common mode rejection ratio ＊	CMRR	50	65	–	dB	DP1 and DN input DP2 and DN input, BW = IHF-A CMRR = 20log(VOUT/VIN)
INPUT GAIN	Minimum input gain	$G_{IN\ MIN}$	-2	0	+2	dB	Input gain = 0dB, VIN = 200mVrms Gin = 20log(VOUT/VIN)
	Maximum input gain	$G_{IN\ MAX}$	18	20	22	dB	Input gain = 20dB VIN = 100mVrms Gin = 20log(VOUT/VIN)
	Step resolution	$G_{IN\ STEP}$	–	1	–	dB	Input gain = 0dB～+20dB
	Gain set error	$G_{IN\ ERR}$	-2	0	+2	dB	
MUTE	Mute attenuation ＊	G_{MUTE}	–	-105	-85	dB	Mute ON Gmute=20log(VOUT/VIN) BW = IHF-A
PRIMARY VOLUME	Maximum gain	$G_{V\ MAX}$	+10	+12	+14	dB	Volume = +12dB VIN=100mVrms Gv=20log(VOUT/VIN)
	Maximum attenuation	$G_{V\ MIN}$	-43	-40	-37	dB	Volume = -40dB Gv=20log(VOUT/VIN)
	Step resolution	$G_{V\ STEP}$	–	1	–	dB	GAIN & ATT=+12dB～-40dB
	Attenuation set error 1	$G_{V\ ERR1}$	-2	0	2	dB	GAIN & ATT=+12dB～-15dB
	Attenuation set error 2	$G_{V\ ERR2}$	-3	0	3	dB	ATT=-16dB～-40dB
BASS	Maximum boost gain	$G_{B\ BST}$	18	20	22	dB	Gain = 20dB, f = 100Hz VIN = 100mVrms Gb = 20log(VOUT/VIN)
	Maximum cut gain	$G_{B\ CUT}$	-22	-20	-18	dB	Gain = -20dB, f = 100Hz VIN = 2Vrms Gb = 20log(VOUT/VIN)
	Step resolution	$G_{B\ STEP}$	–	1	–	dB	f = 100Hz
	Gain set error	$G_{B\ ERR}$	-2	0	2	dB	f = 100Hz
	Center frequency	f_B	–	100	–	Hz	Gain = +20dB
	Quality factor	Q_B	–	1	–	–	f = 100Hz Gain = +20dB
TREBLE	Maximum boost gain	$G_{T\ BST}$	18	20	22	dB	Gain = +20dB, f = 10kHz VIN=100mVrms Gt = 20log(VOUT/VIN)
	Maximum cut gain	$G_{T\ CUT}$	-22	-20	-18	dB	Gain = -20dB, f = 10kHz VIN=2Vrms Gt = 20log(VOUT/VIN)
	Step resolution	$G_{T\ STEP}$	–	1	–	dB	f = 10kHz
	Gain set error	$G_{T\ ERR}$	-2	0	2	dB	f = 10kHz
	Center frequency	f_T	–	10	–	kHz	Gain = +20dB
	Quality factor	Q_T	–	1	–	–	f = 10kHz, Gain = +20dB

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Fader Volume	Maximum attenuation ＊	$G_{F\ MIN}$	–	-100	-90	dB	Gf = 20log(VOUT/VIN) BW = IHF-A, Att. = -∞dB
	Step resolution	$G_{F\ STEP}$	–	1	–	dB	Att. = 0～-62dB
	Attenuation set error 1	$G_{F\ ERR1}$	-2	0	2	dB	Att. = 0～-15dB
	Attenuation set error 2	$G_{F\ ERR2}$	-3	0	3	dB	Att. = -16～-47dB
	Attenuation set error 3	$G_{F\ ERR3}$	-4	0	4	dB	Att=-48～-62dB
OUTPUT	Output impedance	R_{OUT}	–	–	50	Ω	VIN=100mVrms
	Maximum output voltage	V_{OM}	2.0	2.2	–	Vrms	THD+N=1%, BW=400-30KHz
ADVANST SWITCHING	Advanst switching time of mute	T_{M1}	–	0.6	–	msec	Advanst switching ON
		T_{M2}	–	1.0	–		
		T_{M3}	–	1.4	–		
		T_{M4}	–	3.2	–		
	Advanst switching time of Volume, Fader, Tone gain and att.	T_{SFT1}	–	4.6	–	msec	Advanst switching ON
		T_{SFT2}	–	9.3	–		
		T_{SFT3}	–	18.6	–		
		T_{SFT4}	–	37.2	–		

※ VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for ＊ measurement.
※ Phase between input / output is same.

●Timing chart

Electrical specifications and timing for bus lines and I/O stages

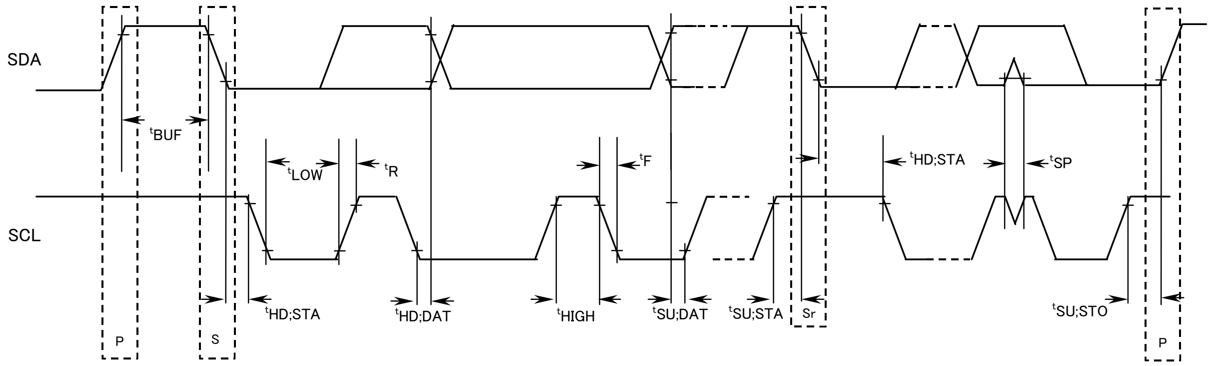


Fig.1 Definition of timing on the I^2C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I^2C-bus devices

	Parameter	Symbol	Fast-mode I^2C-bus Min.	Fast-mode I^2C-bus Max.	Unit
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between a STOP and START condition	tBUF	1.3	–	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	–	μS
4	LOW period of the SCL clock	tLOW	1.3	–	μS
5	HIGH period of the SCL clock	tHIGH	0.6	–	μS
6	Set-up time for a repeated START condition	tSU;STA	0.6	–	μS
7	Data hold time:	tHD;DAT	0*	–	μS
8	Data set-up time	tSU; DAT	100	–	ns
9	Rise time of both SDA and SCL signals	tR	20+Cb	300	ns
10	Fall time of both SDA and SCL signals	tF	20+Cb	300	ns
11	Set-up time for STOP condition	tSU;STO	0.6	–	μS
12	Capacitive load for each bus line	Cb	–	400	pF

All values referred to VIH min. and VIL max. Levels (see Table 2).
* A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Table 2　Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

	Parameter	Symbol	Fast-mode devices Min.	Fast-mode devices Max.	Unit
13	LOW level input voltage : fixed input levels	VIL	-0.5	1	V
14	HIGH level input voltage : fixed input levels	VIH	2.3	–	V
15	Hysteresis of Schmitt trigger inputs : fixed input levels	Vhys	n/a	n/a	V
16	Pulse width of spikes which must be suppressed by the input filter.	Tsp	0	50	ns
17	LOW level output voltage (open drain or open collector) : at 3mA sink current	VOL1	0	0.4	V
18	Output fall time from VIHmin. to VIHmax.　with a bus capacitance from 10 pF to 400pF : with up to 3mA sink current at VOL1	tOF	20+0.1Cb *1)	250 *2)	ns
19	Input current each I/O pin with an input voltage between 0.4V and 0.9 VDDmax.	Ii	-10	10	μA
20	Capacitance for each I/O pin.	Ci	–	10	pF

n/a = not applicable
1) maximum $V_{IH}=V_{DDmax}+0.5V$, $V_{DDMAX}=5.5V$
2) Cb = capacitance of one bus line in pF.
3) Note that the maximum tF for the SDA and SCL bus lines quoted in Table 1 (300ns) is longer than the specified maximum tOF for the output stages (250ns).　This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig. 1 without exceeding the maximum specified tF.

●CONTROL SIGNAL SPECIFICATION

Data

Items to be set	Select Address (hex)	D7 (MSB)	D6	D5	D4 (Data)	D3	D2	D1	D0 (LSB)
Initial Setup 1	01	Advanst switching ON/OFF	0	Advanst switching time of Volume/Fader/Tone		0	0	Advanst switching time of Mute	
Input Selector	04	0	0	0	0	0	Input Selector		
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Primary Volume Gain / Attenuation							
Fader 1ch Front	28	Fader Volume Gain / Attenuation							
Fader 2ch Front	29	Fader Volume Gain / Attenuation							
Fader 1ch Rear	2A	Fader Volume Gain / Attenuation							
Fader 2ch Rear	2B	Fader Volume Gain / Attenuation							
Bass gain	51	Bass Boost/Cut	0	0	Bass Gain				
Treble gain	57	Treble Boost/Cut	0	0	Treble Gain				
Test Mode	F0	0	0	0	0	0	0	0	0
	F1	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

※In function changing of the hatching part, it works advanst switching.

Slave address

A6 (MSB)	A5	A4	A3	A2	A1	A0	R/W (LSB)
1	0	0	0	0	0	0	0

※Please refer to『BD3481FS/BD3482FS User's Manual for I^2C BUS communication』about the detail of control signal specification.

●Application Circuit Diagram (BD3481FS)

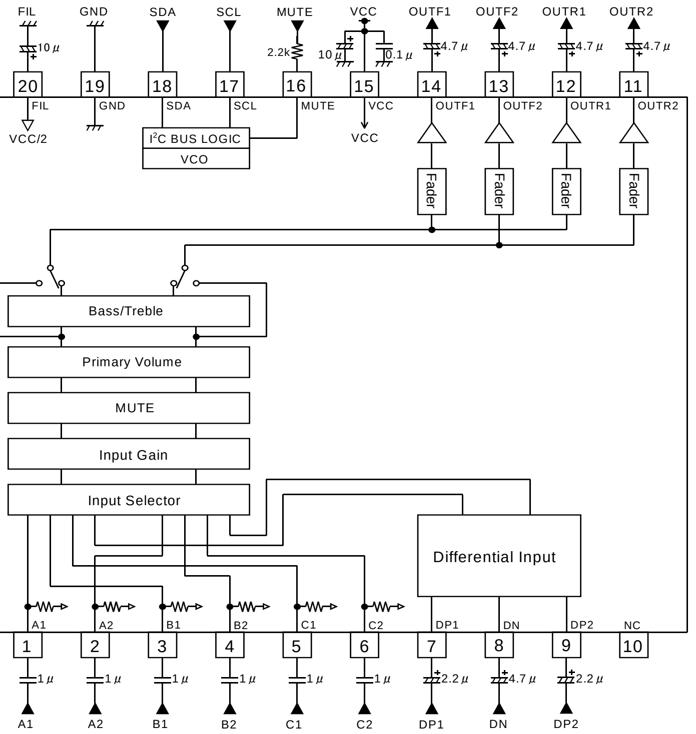


Fig.2 Application Circuit Diagram (BD3481FS)

●Descriptions of terminal

Terminal Number	Terminal Name	Description
1	A1	A input terminal of 1ch
2	A2	A input terminal of 2ch
3	B1	B input terminal of 1ch
4	B2	B input terminal of 2ch
5	C1	C input terminal of 1ch
6	C2	C input terminal of 2ch
7	DP1	D positive input terminal of 1ch
8	DN	D Negative input terminal
9	DP2	D positive input terminal of 2ch
10	NC	No connection terminal
11	OUTR2	Rear output terminal of 2ch
12	OUTR1	Rear output terminal of 1ch
13	OUTF2	Front output terminal of 2ch
14	OUTF1	Front output terminal of 1ch
15	VCC	Power supply terminal
16	MUTE	A terminal for external compulsory mute
17	SCL	Serial communication clock terminal
18	SDA	Serial communication data terminal
19	GND	GND terminal
20	FIL	VCC/2 terminal

● Application Circuit Diagram (BD3482FS)

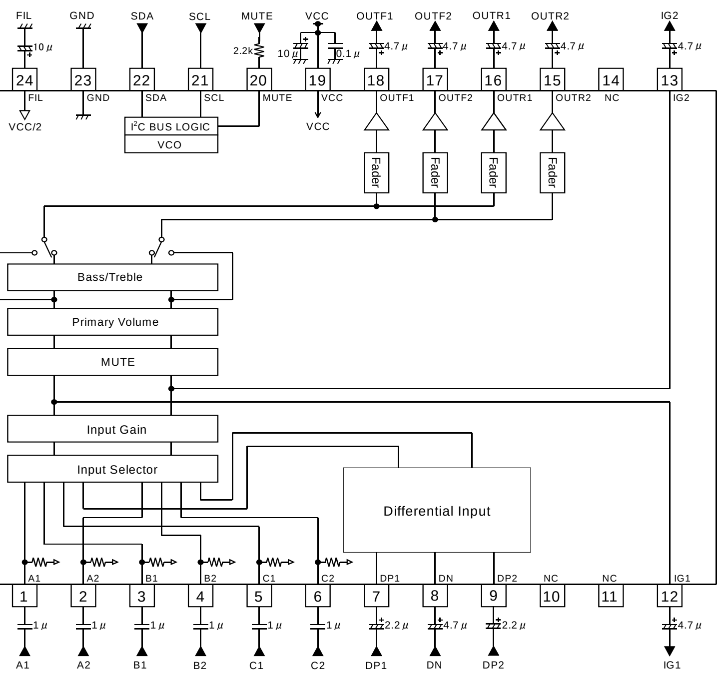


Fig.3 Application Circuit Diagram (BD3482FS)

Unit
R : [Ω]
C : [F]

Terminal Number	Terminal Name	Description
1	A1	A input terminal of 1ch
2	A2	A input terminal of 2ch
3	B1	B input terminal of 1ch
4	B2	B input terminal of 2ch
5	C1	C input terminal of 1ch
6	C2	C input terminal of 2ch
7	DP1	D positive input terminal of 1ch
8	DN	D negative input terminal
9	DP2	D positive input terminal of 2ch
10	NC	No connection terminal
11	NC	No connection terminal
12	IG1	Input gain terminal of 1ch
13	IG2	Input gain terminal of 2ch
14	NC	No connection terminal
15	OUTR2	Rear output terminal of 2ch
16	OUTR1	Rear output terminal of 1ch
17	OUTF2	Front output terminal of 2ch
18	OUTF1	Front output terminal of 1ch
19	VCC	Power supply terminal
20	MUTE	A terminal for external compulsory mute
21	SCL	Serial communication clock terminal
22	SDA	Serial communication data terminal
23	GND	Analog grounding terminal
24	FIL	VCC/2 terminal

●Data

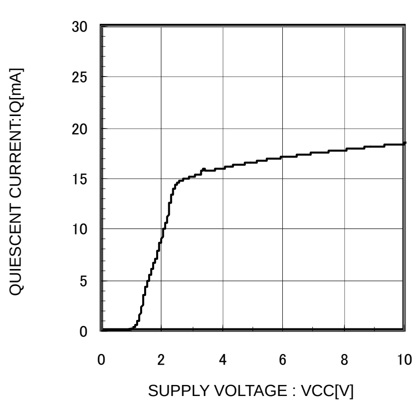


Fig.4 QUIESCENT CURRENT VS SUPPLY VOLTAGE

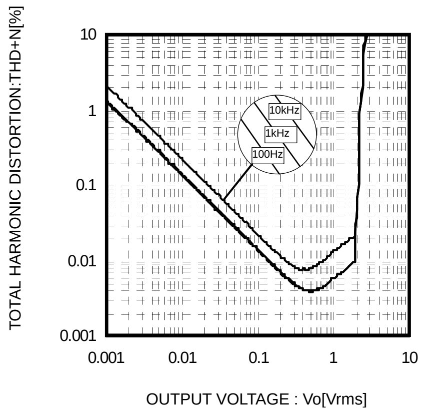


Fig.5 TOTAL HARMONIC DISTORTION VS OUTPUT VOLTAGE

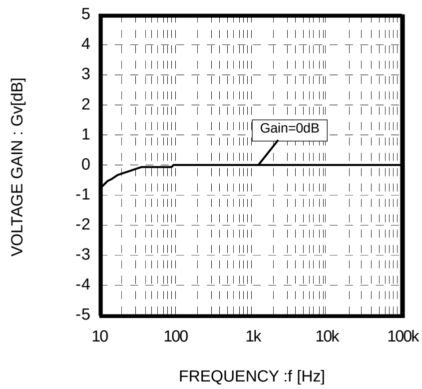


Fig.6 VOLTAGE GAIN VS FREQUENCY

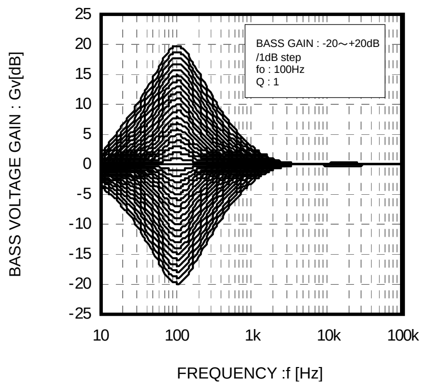


Fig.7 BASS VOLTAGE GAIN VS FREQUENCY

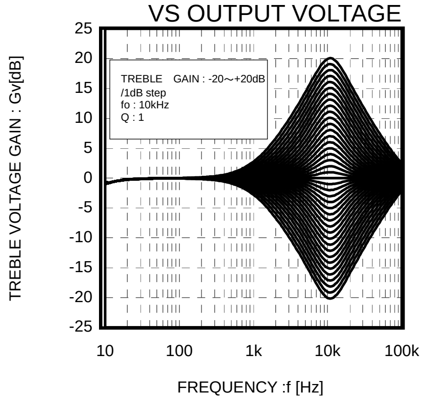


Fig.8 TREBLE VOLTAGE GAIN VS FREQUENCY

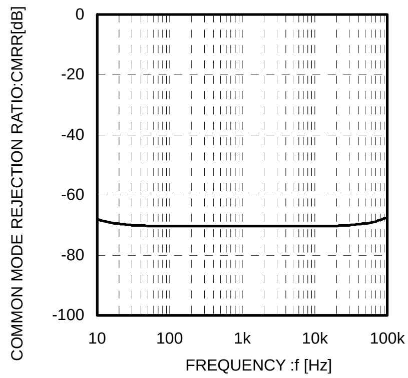


Fig.9 CMRR VS FREQUENCY

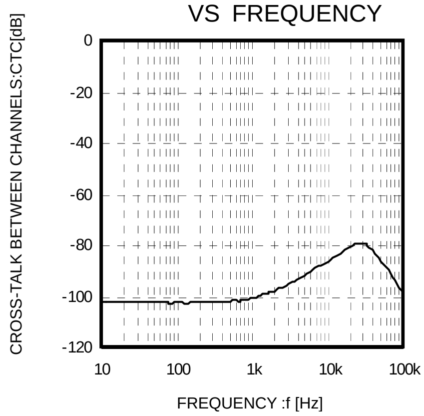


Fig.10 CROSS-TALK VS FREQUENCY

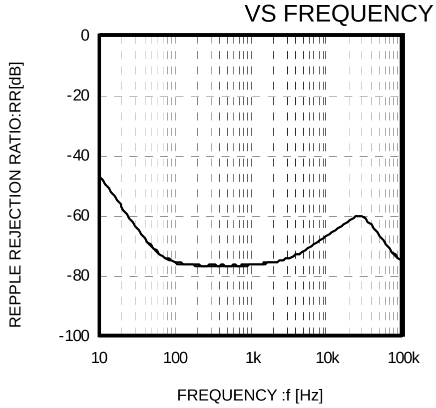


Fig.11 RIPPLE REJECTION RATIO VS FREQUENCY

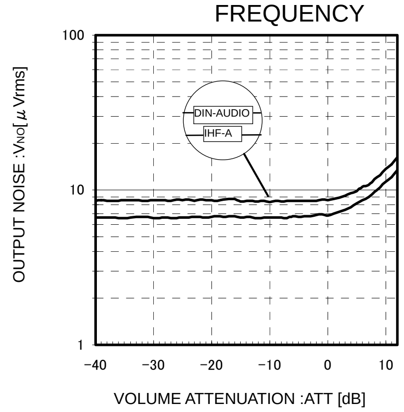


Fig.12 VOLUME ATTENUATION VS OUTPUT NOISE

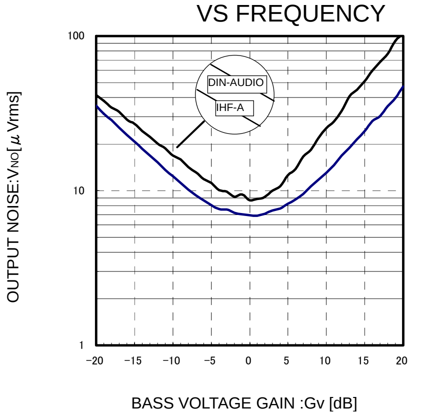


Fig.13 BASS VOLTAGE GAIN VS OUTPUT NOISE

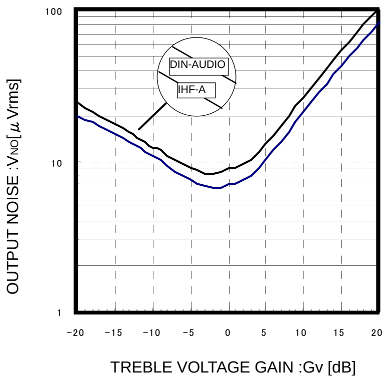


Fig.14 TREBLE VOLTAGE GAIN VS OUTPUT NOISE

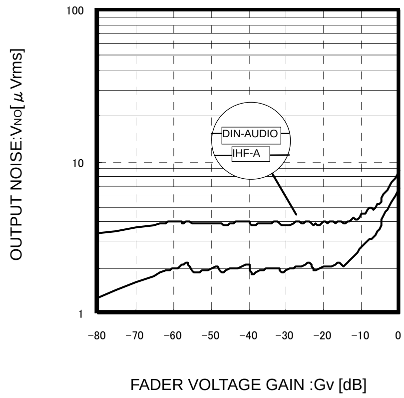


Fig.15 FADER VOLTAGE GAIN VS OUTPUT NOISE

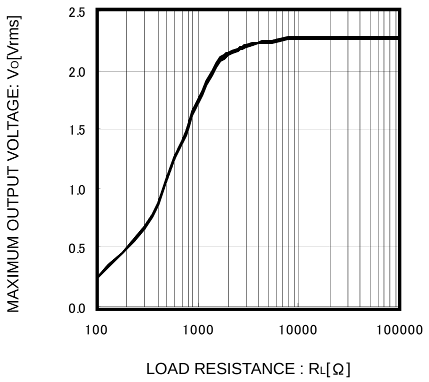


Fig.16 LOAD RESISTANCE VS MAXIMUM OUTPUT VOLTAGE

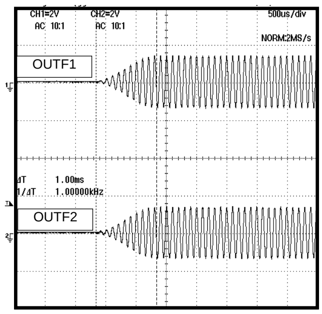


Fig.17 ADVANST SWITCHING WAVEFORM 1

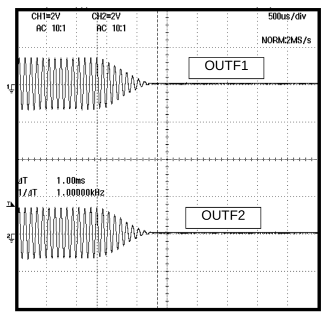


Fig.18 ADVANST SWITCHING WAVEFORM 2

●Cautions on use

(1) Data in entries are representative design values and are not guaranteed values of the items.

(2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.

(3) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to the LSI.

(4) GND potential

Make the GND pin voltage such that it is the lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including transient phenomena.

(5) Thermal design

Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

(6) Shorts between pins and misinstallation

When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is misinstalled and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and a GND.

(7) Operation in strong magnetic fields

Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

●Selection of order type

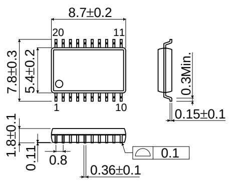
B	D	3	4	8	1	F	S	-	E	2

Part No. BD3482FS

Package and forming specification

SSOP-A20

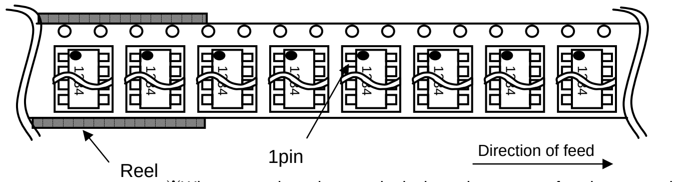
<Dimension>



(Unit:mm)

<Tape and Reel information>

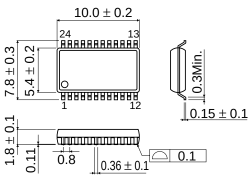
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SSOP-A24

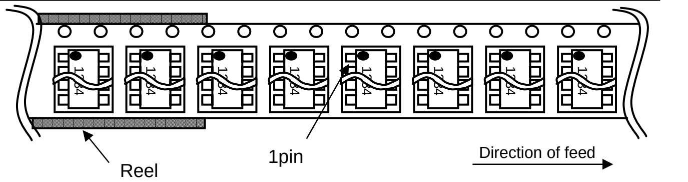
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

Contact us for further information about the products.

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