# Termination Regulators for DDR-SDRAMs

**BD3538F BD3538HFN**

## General Description

BD3538F/HFN is a termination regulator that complies with JEDEC requirements for DDR-SDRAM. This linear power supply uses a built-in N-channel MOSFET and high-speed OP-AMPS specially designed to provide excellent transient response. It has a sink/source current capability of up to 1A and has a power supply bias requirements of 3.3V to 5.0V for driving the N-channel MOSFET. By employing an independent reference voltage input (VDDQ) and a feedback pin (VTTS), this termination regulator provides excellent output voltage accuracy and load regulation as required by JEDEC standards. Additionally, BD3538 has a reference power supply output (VREF) for DDR-SDRAM or a memory controller. Unlike the VTT output that goes to "Hi-Z" state, the VREF output is kept unchanged when EN input is changed to "Low", making this IC suitable for DDR-SDRAM under "Self Refresh" state.

## Features

- Incorporates a push-pull power supply for termination (VTT)
- Incorporates a reference voltage circuit (VREF)
- Incorporates an enabler
- Incorporates an undervoltage lockout (UVLO)
- Incorporates a thermal shutdown protector (TSD)
- Compatible with Dual Channel (DDR-II)

## Applications

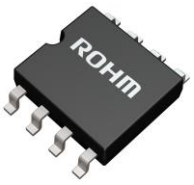
Power supply for DDR I / II - SDRAM

## Key Specifications

- Termination Input Voltage Range: 1.0V to 5.5V
- VCC Input Voltage Range: 2.7V to 5.5V
- VDDQ Reference Voltage Range: 1.0V to 2.75V
- Output Voltage: 1/2 x $V_{VDDQ}$ V(Typ)
- Output Current: 1.0A (Max)
- High side FET O-Resistance: 0.4Ω(Typ)
- Low side FET ON-Resistance: 0.4Ω(Typ)
- Standby Current: 0.5mA (Typ)
- Operating Temperature Range: -40°C to +105°C

## Packages

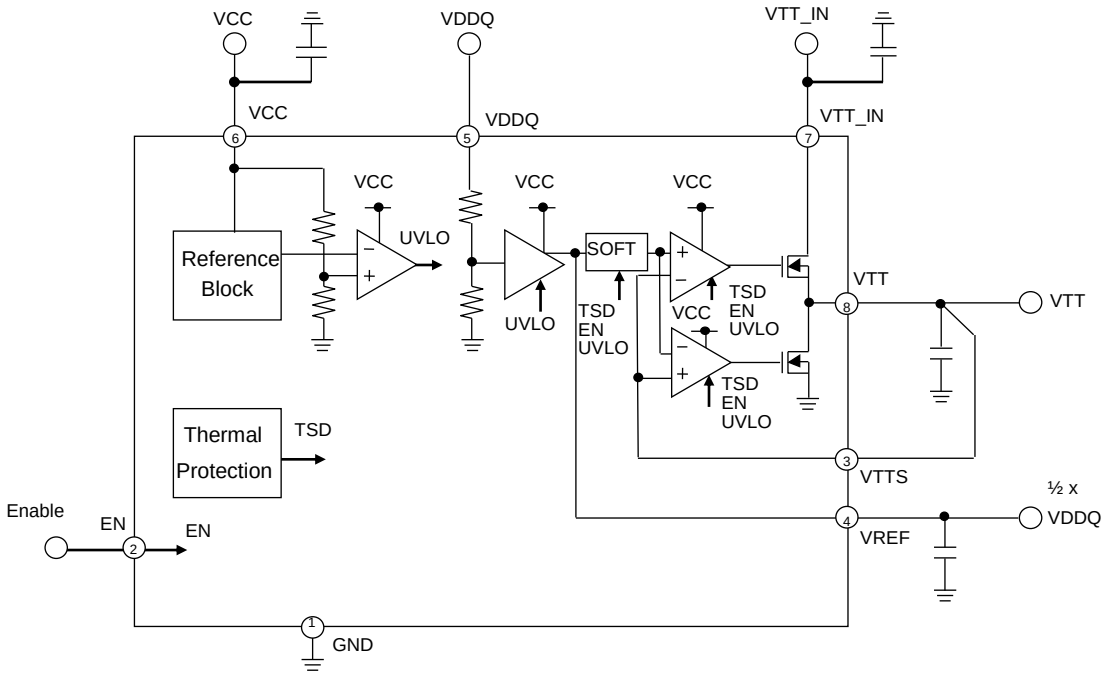
W(Typ) x D(Typ) x H(Max)




**SOP8**
5.00mm x 6.20mm x 1.71mm

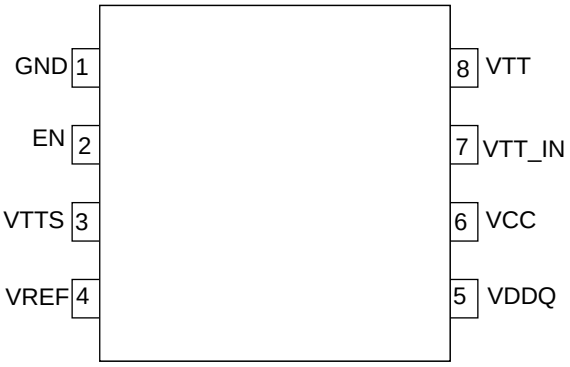

**HSON8**
2.90mm x 3.00mm x 0.60mm

## Typical Application Circuit, Block Diagram



## Pin Configuration

TOP VIEW




## Pin Descriptions

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | GND | GND pin |
| 2 | EN | Enable input pin |
| 3 | VTTS | Detector pin for termination voltage |
| 4 | VREF | Reference voltage output pin |
| 5 | VDDQ | Reference voltage input pin |
| 6 | VCC | VCC pin |
| 7 | VTT_IN | Termination input pin |
| 8 | VTT | Termination output pin |
| Bottom | FIN (Note 1) | Substraight<br>(Conntct to GND) |

(Note 1) Only BD3538HFN

## Description of Blocks

1. VCC
   The VCC pin is for the independent power supply input that operates the internal circuit of the IC. It is the voltage at this pin that drives the IC's amplifier circuits. The VCC input ranges from 3.3V to 5.5V and maximum current consumption is 4mA. A bypass capacitor of 1 µF or so should be connected to this pin when using the IC in an application circuit.

2. VDDQ
   This is the power supply input pin for an internal voltage divider network. The voltage at VDDQ is halved by two 50 kΩ internal voltage-divider resistors and the resulting voltage serves as reference for the VTT output. Since VTT = 1/2VDDQ, the JEDEC requirement for DDR-SDRAM can be satisfied by supplying the correct voltage to VDDQ. Noise input should be avoided at the VDDQ pin as it is also included by the voltage-divider at the output. An RC filter consisting of a resistor and a capacitor (220 Ω and 2.2 µF, for instance) may be used to reduce the noise input but make sure that it will not significantly effect the voltage-divider's output.

3. VTT_IN
   VTT_IN is a power supply input pin for VTT output. Voltage in the range between 1.0V to 5.5V, but consideration must be given to the current limit dictated by the ON-Resistance of the IC and to the change in allowable loss due to input/output voltage difference.
   Generally, the following voltages are supplied:
   - DDR I $V_{VTT\_IN}$ =2.5V
   - DDRII $V_{VTT\_IN}$ =1.8V

   Take note that a high impedance voltage input at VTT_IN may result in oscillation or degradation in ripple rejection, so connecting 10µF capacitor with minimal change in capacitance to VTT_IN terminal is recommended. However, this impedance may depend on the characteristics of the power supply input and the impedance of the PC board wiring, which must be carefully checked before use.

4. VREF
   BD3538 provides a constant voltage, VREF, which is independent from the VTT output and can serve as a reference input for memory controllers and DRAMs. The voltage level of VREF is kept constant even if the EN pin is at "Low" level, making the use of this IC compatible with "Self Refresh" state of DRAM.
   In order to stabilize the output voltage, connecting the correct combination of capacitor and resistor to VREF is necessary. For this purpose, a combination of 1.0µF to 2.2µF ceramic capacitor, characterized by minimal variation in capacitance and a 0.5Ω to 2.2Ω phase compensating resistor is recommended. The maximum current capability of the VREF pin is 20mA but for an application which consumes a small amount of VREF current, using a capacitance of 1 µF or less will do.

5. VTTS
   VTTS is a sense pin for the load regulation of the VTT output voltage. In case the wire connecting VTT pin and the load is too long, connecting VTTS pin to the part of the wire nearer to the load may improve load regulation.

6. VTT
   This is the output for the DDR memory termination voltage and it has a sink/source current capability of ±1.0A. VTT voltage tracks the voltage at VDDQ pin divided in half. The output is turned to OFF when EN pin is "Low" or when either the VCC UVLO or the thermal shutdown protection function is activated.
   Always connect a capacitor to VTT pin for loop gain and phase compensation and for reduction in output voltage variation in the event of sudden load change. Be careful in choosing the capacitor as sufficient capacitance may cause oscillation and high ESR (Equivalent Series Resistance) may result in increase d output voltage variation during a sudden change in load. A 220µF or so ceramic capacitor is recommended, though ambient temperature and other conditions should also be considered.

## Description of Blocks - continued

7. EN
A “High” input of 2.3V or higher to EN turns ON the VTT output. A “Low” input of 0.8V or less, on the other hand, turns VTT to a Hi-Z state. With a “Low” EN input, however, the VREF output remains ON, provided that sufficient VCC and VDDQ voltages have been established.

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | BD3538F | BD3538HFN | |
| Input Voltage | $V_{CC}$ | 7 (Note 2) (Note 3) | 7 (Note 2) (Note 3) | V |
| Enable Input Voltage | $V_{EN}$ | 7 (Note 2) (Note 3) | 7 (Note 2) (Note 3) | V |
| Termination Input Voltage | $V_{VTT\_IN}$ | 7 (Note 2) (Note 3) | 7 (Note 2) (Note 3) | V |
| VDDQ Reference Voltage | $V_{VDDQ}$ | 7 (Note 2) (Note 3) | 7 (Note 2) (Note 3) | V |
| Output Current | $I_{VTT}$ | 1 | 1 | A |
| Power Dissipation1 | Pd1 | 0.56 (Note 4) | 0.63 (Note 6) | W |
| Power Dissipation2 | Pd2 | 0.69 (Note 5) | 1.35 (Note 7) | W |
| Power Dissipation3 | Pd3 | - | 1.75 (Note 8) | W |
| Operating Temperature Range | Topr | -40 to +105 | -40 to +105 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | -55 to +150 | °C |
| Maximum Junction Temperature | Tjmax | +150 | +150 | °C |

(Note 2) Should not exceed Pd.
(Note 3) Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
(Note 4) Derate by 4.48mW/°C for Ta over 25°C (With no heat sink).
(Note 5) Derate by 5.52mW/°C for Ta over 25°C (When mounted on a board 70mm x 70mm x 1.6mm Glass-epoxyPCB).
(Note 6) Derate by 5.04mW/°C for Ta over 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 1-layer)
On less than 0.2% (percentage occupied by copper foil.
(Note 7) Derate by 10.8mW/°C for Ta over 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 1-layer)
On less than 7.0% (percentage occupied by copper foil.
(Note 8) Derate by 14.0mW/°C for Ta over 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 1-layer)
On less than 65.0% (percentage occupied by copper foil.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

## Recommended Operating Ratings (Ta=25°C)

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Input Voltage | $V_{CC}$ | 2.7 | 5.5 | V |
| Termination Input Voltage | $V_{VTT\_IN}$ | 1.0 | 5.5 | V |
| VDDQ Reference Voltage | $V_{VDDQ}$ | 1.0 | 2.75 | V |
| Enable Input Voltage | $V_{EN}$ | -0.3 | +5.5 | V |

## Electrical Characteristics

(Unless otherwise noted, Ta=25°C $V_{CC}$=3.3V $V_{EN}$=3V $V_{VDDQ}$=1.8V $V_{VTT\_IN}$=1.8V)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Standby Current | $I_{ST}$ | - | 0.5 | 1.0 | mA | $V_{EN}$=0V |
| Bias Current | $I_{CC}$ | - | 2 | 4 | mA | $V_{EN}$=3V |
| [Enable] | | | | | | |
| High Level Enable Input Voltage | $V_{ENHIGH}$ | 2.3 | - | 5.5 | V | |
| Low Level Enable Input Voltage | $V_{ENLOW}$ | -0.3 | - | +0.8 | V | |
| Enable Pin Input Current | $I_{EN}$ | - | 7 | 10 | µA | $V_{EN}$=3V |
| [Termination] | | | | | | |
| Termination Output Voltage 1 | $V_{VTT1}$ | $V_{VREF}$-30m | $V_{VREF}$ | $V_{VREF}$+30m | V | $I_{VTT}$=-1.0A to +1.0A<br>Ta=0°C to 105°C (Note 9) |
| Termination Output Voltage 2 | $V_{VTT2}$ | $V_{VREF}$-30m | $V_{VREF}$ | $V_{VREF}$+30m | V | $V_{CC}$=5V, $V_{VDDQ}$=2.5V<br>$V_{VTT\_IN}$=2.5V<br>$I_{VTT}$=-1.0A to +1.0A<br>Ta=0°C to 105°C (Note 9) |
| Source Current | $I_{VTT+}$ | 1.0 | - | - | A | |
| Sink Current | $I_{VTT-}$ | - | - | -1.0 | A | |
| Load Regulation | $\Delta V_{VTT}$ | - | - | 50 | mV | $I_{VTT}$=-1.0A to +1.0A |
| Line Regulation | Reg.I | - | 20 | 40 | mV | |
| Upper Side ON-Resistance 1 | $R_{HRON1}$ | - | 0.45 | 0.9 | Ω | |
| Lower Side ON-Resistance 1 | $R_{LRON1}$ | - | 0.45 | 0.9 | Ω | |
| Upper Side ON-Resistance 2 | $R_{HRON2}$ | - | 0.4 | 0.8 | Ω | $V_{CC}$=5V, $V_{VDDQ}$=2.5V<br>$V_{VTT\_IN}$=2.5V |
| Lower Side ON-Resistance 2 | $R_{LRON2}$ | - | 0.4 | 0.8 | Ω | $V_{CC}$=5V, $V_{VDDQ}$=2.5V<br>$V_{VTT\_IN}$=2.5V |
| [Reference Voltage Input] | | | | | | |
| Input Impedance | $Z_{VDDQ}$ | 70 | 100 | 130 | kΩ | |
| Output Voltage 1 | $V_{VREF1}$ | 1/2 x $V_{VDDQ}$ -18m | 1/2 x $V_{VDDQ}$ | 1/2 x $V_{VDDQ}$ +18m | V | $I_{REF}$=-5mA to +5mA<br>Ta=0°C to 105°C (Note 9) |
| Output Voltage 2 | $V_{VREF2}$ | 1/2 x $V_{VDDQ}$ -40m | 1/2 x $V_{VDDQ}$ | 1/2 x $V_{VDDQ}$ +40m | V | $I_{REF}$=-10mA to +10mA<br>Ta=0°C to 105°C (Note 9) |
| Output Voltage 3 | $V_{VREF3}$ | 1/2 x $V_{VDDQ}$ -25m | 1/2 x $V_{VDDQ}$ | 1/2 x $V_{VDDQ}$ +25m | V | $V_{CC}$=5V, $V_{VDDQ}$=2.5V<br>$V_{VTT\_IN}$=2.5V<br>$I_{VREF}$=-5mA to +5mA<br>Ta=0°C to 105°C (Note 9) |
| Output Voltage 4 | $V_{VREF4}$ | 1/2 x $V_{VDDQ}$ -40m | 1/2 x $V_{VDDQ}$ | 1/2 x $V_{VDDQ}$ +40m | V | $V_{CC}$=5V, $V_{VDDQ}$=2.5V<br>$V_{VTT\_IN}$=2.5V<br>$I_{VTT}$=-10mA to +10mA<br>Ta=0°C to 105°C (Note 9) |
| [UVLO] | | | | | | |
| Threshold Voltage | $V_{UVLO}$ | 2.40 | 2.55 | 2.70 | V | VCC : sweep up |
| Hysteresis Voltage | $\Delta V_{UVLO}$ | 100 | 160 | 220 | mV | VCC : sweep down |

(Note 9) No tested on outgoing inspection

**Typical Waveforms**

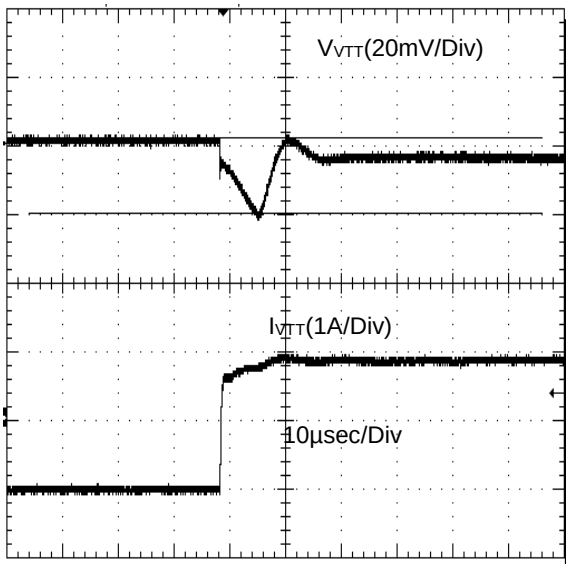



Figure 1. DDR1
(-1A → +1A)

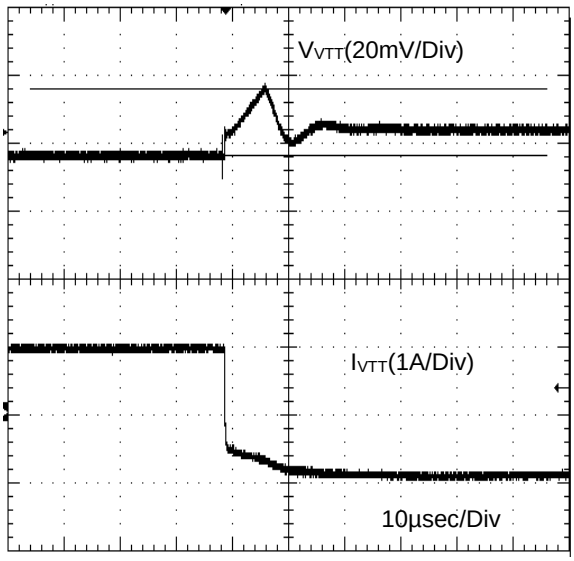



Figure 2. DDR1
(+1A → -1A)

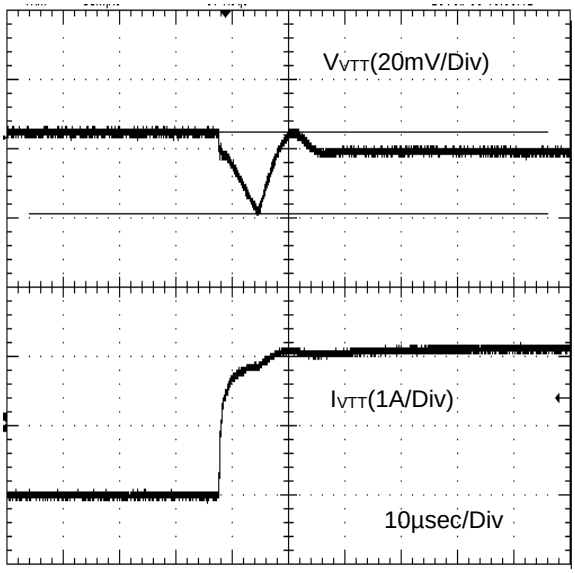



Figure 3. DDR2
(-1A → +1A)

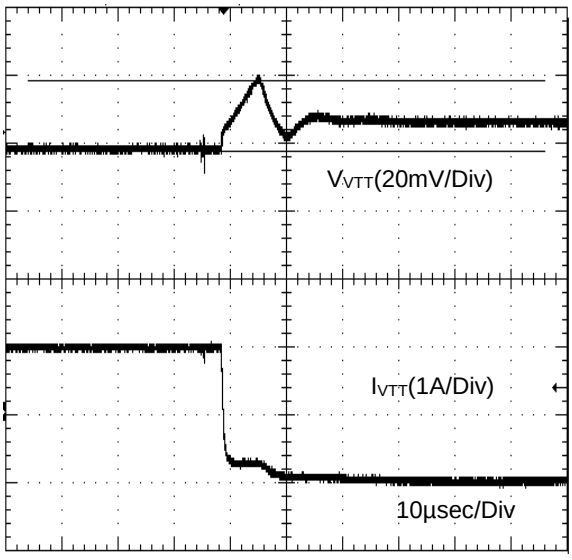



Figure 4. DDR2
(+1A → -1A)

**Typical Waveforms - continued**

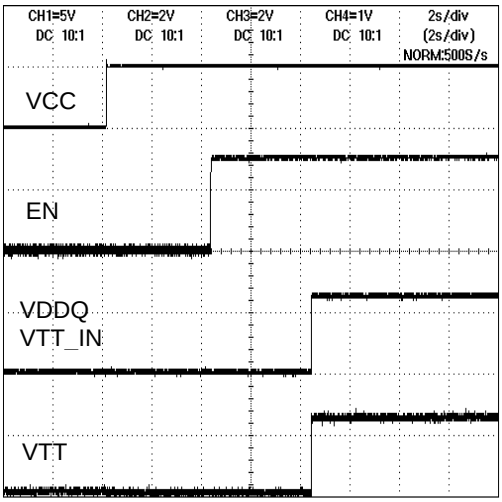



Figure 5. Input Sequence 1

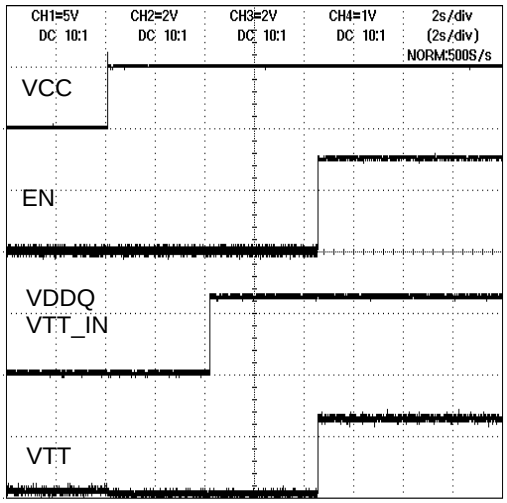



Figure 6. Input Sequence 2

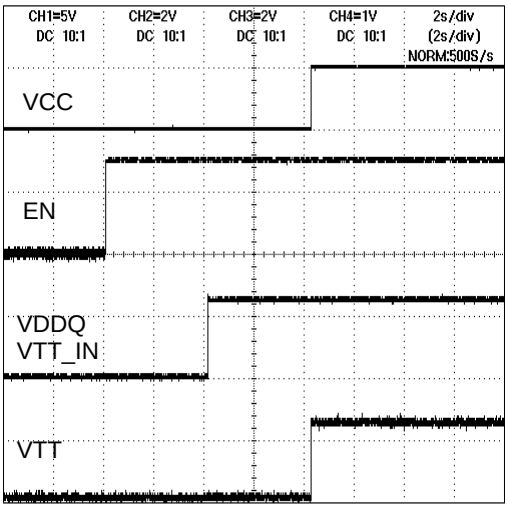



Figure 7. Input Sequence 3

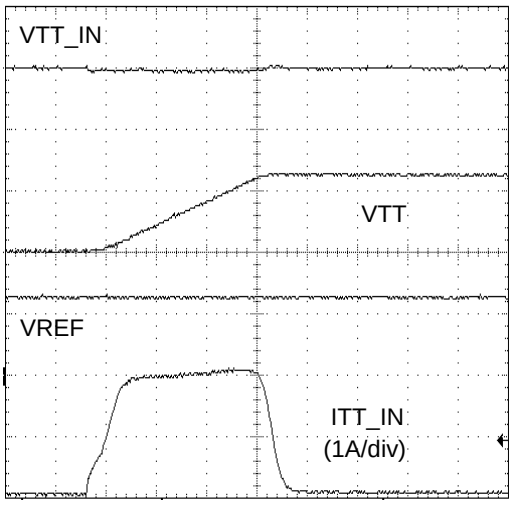



Figure 8. Start up Wave Form

## Typical Performance Curves

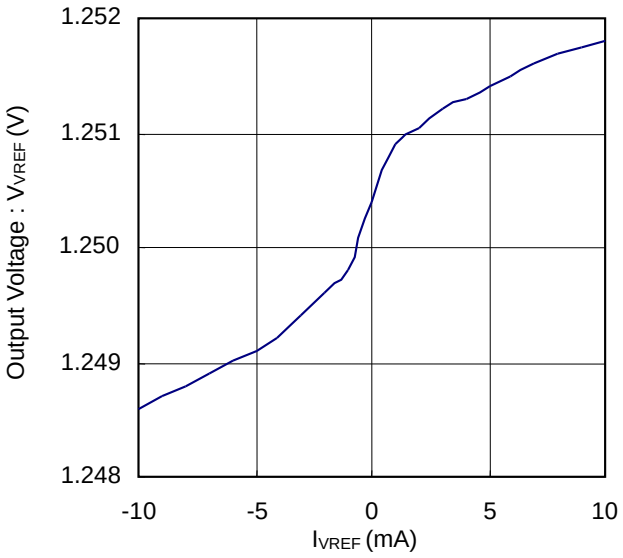



Figure 9. Output Voltage vs $I_{VREF}$ (DDR1)

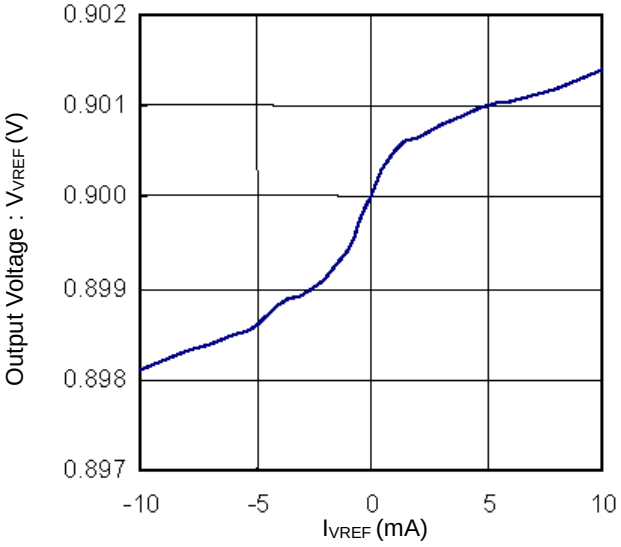



Figure 10. Output Voltage vs $I_{VREF}$ (DDR2)

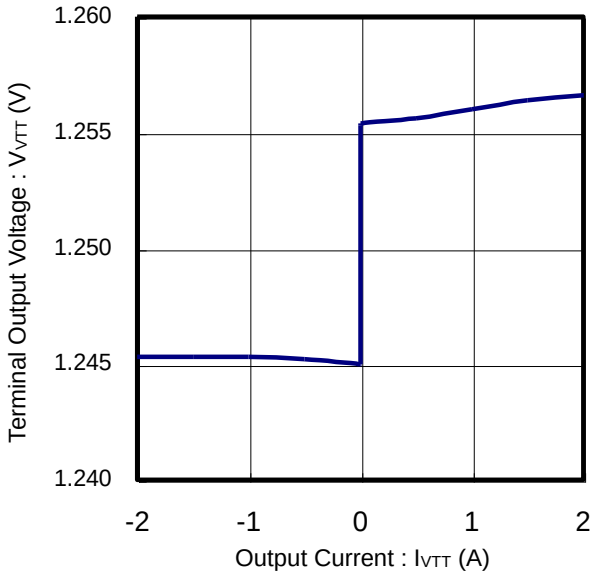



Figure 11. Terminal Output Voltage vs Output Current (DDR1)

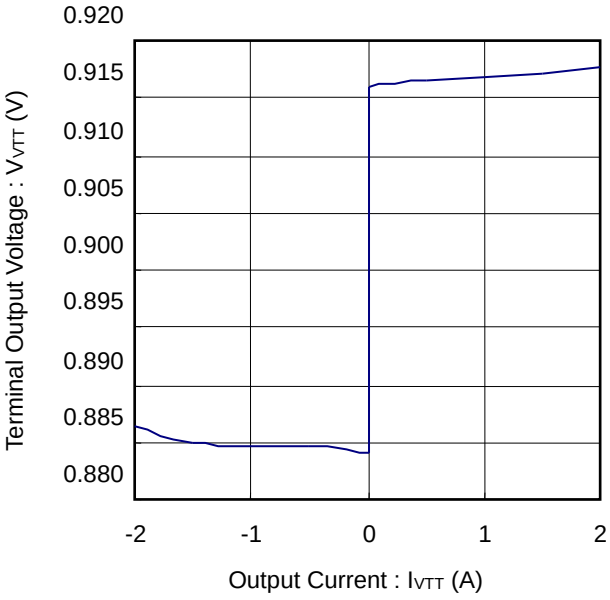
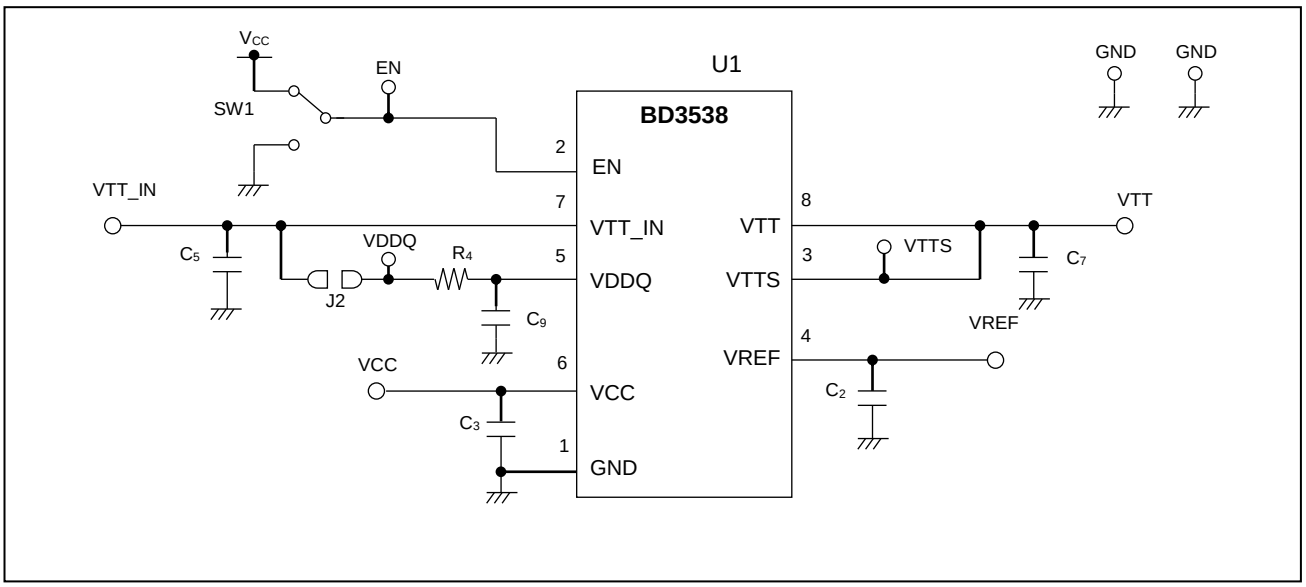



Figure 12. Terminal Output Voltage vs Output Current (DDR2)

## Application Information

### 1. Evaluation Board

■ BD3538 Evaluation Board Circuit




■ BD3538 Evaluation Board Application Components

| Part No | Value | Company | Parts Name |
|---|---|---|---|
| U1 | - | ROHM | BD3538 |
| $R_4$ | 220Ω | ROHM | MCR03 |
| J2 | 0Ω | - | - |
| $C_2$ | 10µF | MURATA | GRM21 Series |
| $C_3$ | 1µF | MURATA | GRM18 Series |
| $C_5$ | 10µF | MURATA | GRM21 Series |
| $C_7$ | 220µF | SANYO | 2R5TPE220MF |
| $C_9$ | 2.2µF | MURATA | GRM18 Series |

## 2. Power Dissipation

### Heat Loss

In thermal design, consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

(1) Ambient temperature Ta: 100°C or lower
(2) Chip junction temperature Tj: 150°C or lower

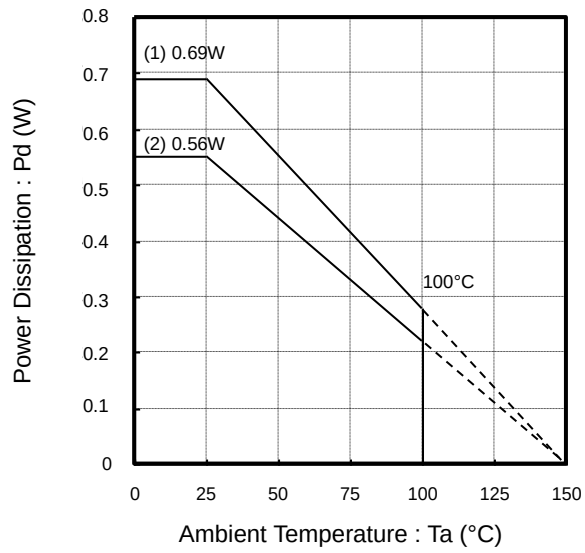
The chip junction temperature Tj can be considered as follows. See below diagrams for θja.
Since the package has FIN at the bottoms of IC, package power is considerably affected by the area of the copper foil where FIN is connected. In order to release heat, please make the board area large enough or add many through-holes to the inner layer pattern. Most of heat loss in BD3538 occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between IN and OUT by the output current. Since this IC is packaged for a high power applications. its thermal derating characteristics significantly depend on the PC board. So when designing, the size of the PC board to be used should be carefully considered.

$$Power\ dissipation(W) = \{Input\ voltage(V_{VTT\_IN}) - Output\ voltage(V_{VTT} = 1/2V_{VDDQ})\} \times I_{OUT}(Ave)$$

If $V_{VTT\_IN}$ = 1.8 volts, $V_{VDDQ}$=1.8 volts, and $I_{OUT}$ (Ave)=0.5 A, for instance, the power dissipation is determined as follows:

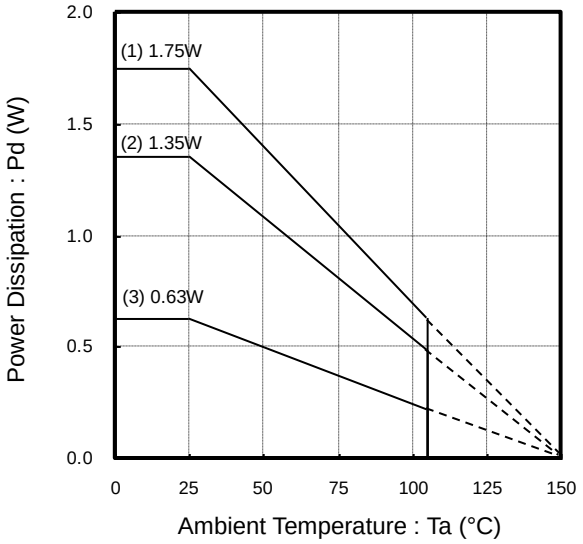
$$\text{Power dissipation}(W) = \{1.8(V) - 0.9(V)\} \times 0.5(A) = 0.4(W)$$

◎SOP8




(1) 70mm x 70mm x 1.6mm Glass-epoxy PCB
θj-c=181°C/W
(2) With no heat sink
θj-a=222°C/W

◎HSON8




(1) 1 layer (copper foil density : 65%)
θja=71.4°C/W
(2) 1 layer (copper foil density : 7%)
θja=92.4°C/W
(3) 1 layer (copper foil density : 0.2%)
θja=198.4°C/W

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**12. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

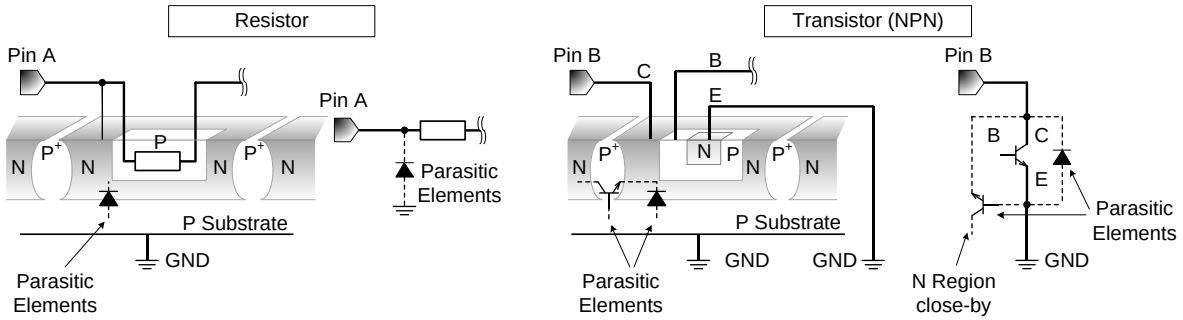



Figure 13. Example of monolithic IC structure

**13. Thermal Shutdown Circuit(TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will exceed 175°C which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

**14. Capacitor Across Output and GND**

If a large capacitor is connected between the output pin and ground pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or IN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 1000µF between output and ground.

**15. Output Capacitor Resistor**

Do not fail to connect a output capacitor to VREF output terminal for stabilization of output voltage. The capacitor connected to VREF output terminal works as a loop gain phase compensator. Insufficient capacitance may cause an oscillation. It is recommended to use a low temperature coefficient 1-10 µF ceramic capacitor, though it depends on ambient temperature and load conditions. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

**16. Output Capacitor**

Do not fail to connect a capacitor to VTT output pin for stabilization of output voltage. This output capacitor works as a loop gain phase compensator and an output voltage variation reducer in the event of sudden change in load. Insufficient capacitance may cause an oscillation. And if the equivalent series resistance (ESR) of this capacitor is high, the variation in output voltage increases in the event of sudden change in load. It is recommended to use a 220 µF functional polymer capacitor, though it depends on ambient temperature and load conditions. Using a low ESR ceramic capacitor may reduce a loop gain phase margin and cause an oscillation, which may be improved by connecting a resistor in series with the capacitor. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

## Operational Notes – continued

**17. Input capacitors**

These input capacitors are used to reduce the output impedance of power supply to be connected to the input terminals (VCC and VTT_IN). Increase in the power supply output impedance may result in oscillation or degradation in ripple rejecting characteristics. It is recommended to use a low temperature coefficient 1µF (for VCC) and 10µF (for VTT_IN) capacitor, but it depends on the characteristics of the power supply input, and the capacitance and impedance of the pc board wiring pattern. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

**18. Input terminals (VCC, VDDQ, VTT_IN and EN)**

VCC, VDDQ, VTT_IN and EN terminals of this IC are made up independent one another. To VCC terminal, the UVLO function is provided for malfunction protection. Irrespective of the input order of the inputs terminals, VTT output is activated to provide the output voltage when UVLO and EN voltages reach the threshold voltage while VREF output is activated when UVLO voltage reaches the threshold. If VDDQ and VTT_IN terminals have equal potential and common impedance, any change in current at VTT_IN terminal may result in variation of VTT_IN voltage, which affects VDDQ terminal and may cause variation in the output voltage. It is therefore required to perform wiring in such manner that VDDQ and VTT_IN terminals may not have common impedance. If impossible, take appropriate corrective measures including suitable CR filter to be inserted between VDDQ and VTT_IN terminals.

**19. VTTS Terminal**

This terminal used to improve load regulation of VTT output. Connection with VTT terminal must be done not to have common impedance with high current line, which may offer better load regulation of VTT output.

**20. Operating range**

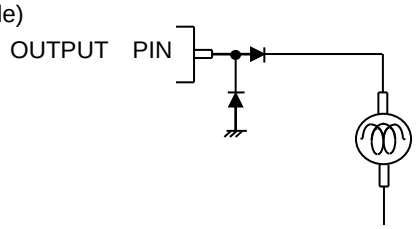
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

**21. Built-in thermal shutdown protection circuit**

Thermal shutdown protection circuit is built-in to prevent thermal breakdown. Turns VTT output to OFF when the thermal shutdown protection circuit activates. This thermal shutdown protection circuit is originally intended to protect the IC itself. It is therefore requested to conduct a thermal design not to exceed the temperature under which the thermal shutdown protection circuit can work.

**22.** In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is recommended to insert a protection diode.

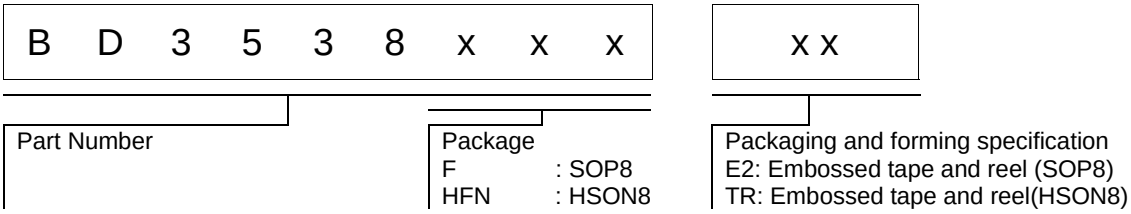
(Example)



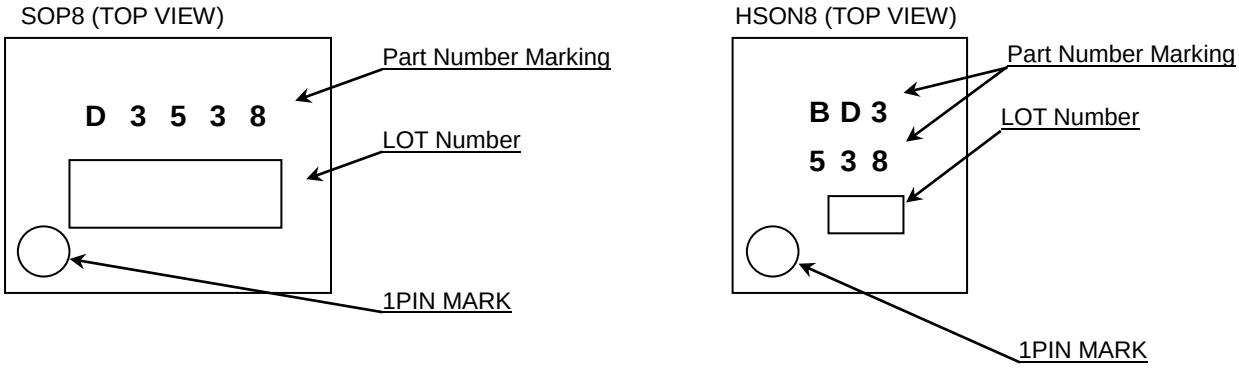

**23. Application Circuit**

Although we can recommend the application circuits contained herein with a relatively high degree of confidence, we ask that you verify all characteristics and specifications of the circuit as well as its performance under actual conditions. Please note that we cannot be held responsible for problems that may arise due to patent infringements or noncompliance with any and all applicable laws and regulations.

### Ordering Information

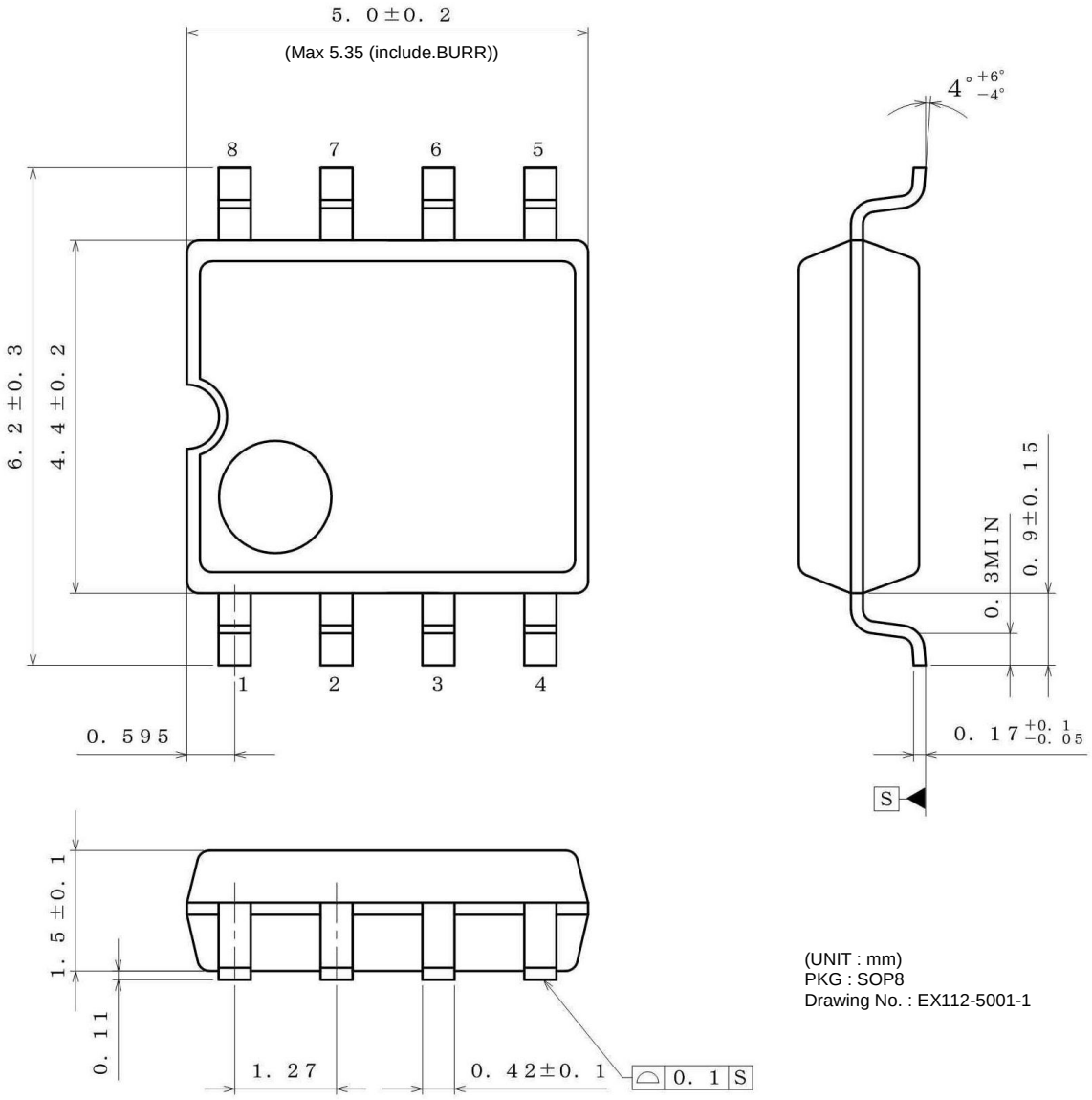



### Marking Diagrams



**Physical Dimension, Tape and Reel Information**

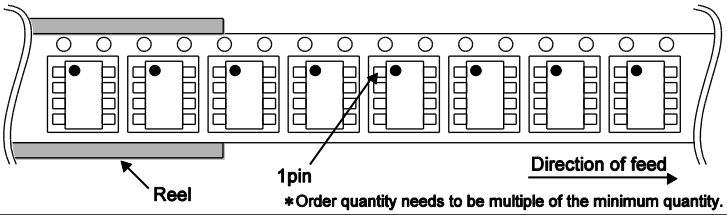
| Package Name | SOP8 |
|---|---|




(UNIT : mm)
PKG : SOP8
Drawing No. : EX112-5001-1

<Tape and Reel information>

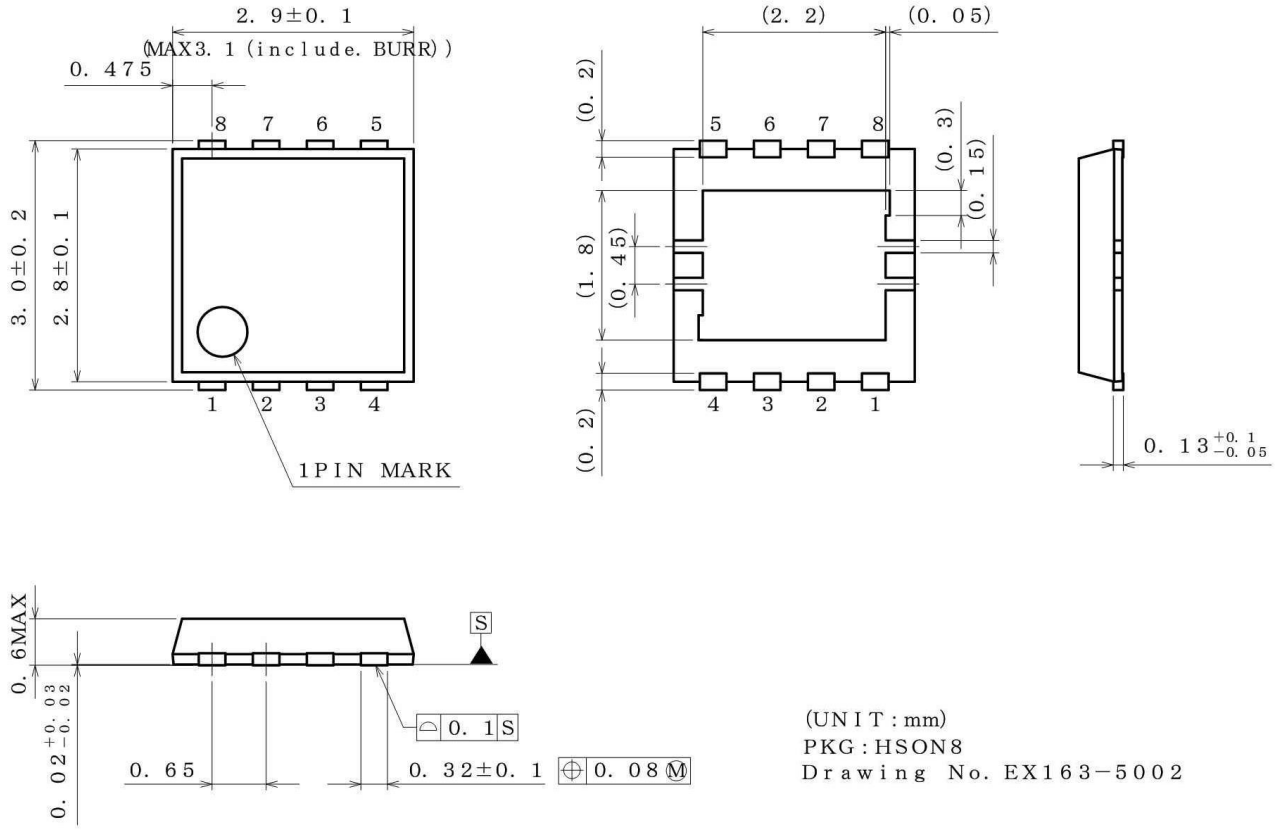
| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




*Order quantity needs to be multiple of the minimum quantity.

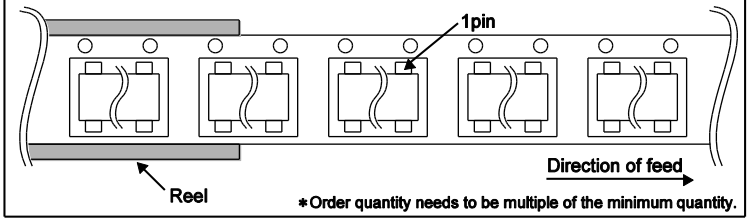
**Physical Dimension, Tape and Reel Information - continued**

| Package Name | HSON8 |
|---|---|




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




*Order quantity needs to be multiple of the minimum quantity.

**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 02.Nov.2015 | 001 | New Release |

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| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

### Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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