

V_{DSS}	30V
$R_{DS(on)}(Max.)$	23.7mΩ
I_D	±4.5A
P_D	1W

●Features

- 1) Low on - resistance.
- 2) High Power Package (TUMT6).
- 3) Pb-free lead plating ; RoHS compliant.
- 4) Halogen Free.

●Application

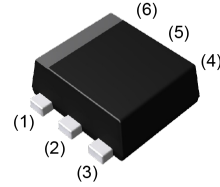
Switching

●Absolute maximum ratings ($T_a = 25^{\circ}C$)

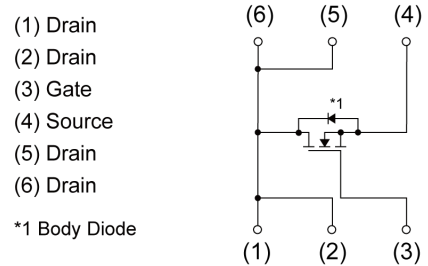
Parameter	Symbol	Value	Unit
Drain - Source voltage	V_{DSS}	30	V
Continuous drain current	I_D	±4.5	A
Pulsed drain current	$I_{D,pulse}^{*1}$	±18	A
Gate - Source voltage	V_{GSS}	±12	V
Power dissipation	P_D^{*2}	1	W
Junction temperature	T_j	150	°C
Range of storage temperature	T_{stg}	-55 to +150	°C

●Outline

TUMT6



●Inner circuit



●Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	8
	Basic ordering unit (pcs)	3000
	Taping code	TCR
	Marking	CJ

● Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	R_{thJA}^{*2}	-	-	125	°C/W

● Electrical characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 1mA$	30	-	-	V
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	$I_D = 1mA$ referenced to 25°C	-	18	-	mV/°C
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1	μA
Gate - Source leakage current	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1mA$	0.5	-	1.5	V
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	$I_D = 1mA$ referenced to 25°C	-	-2	-	mV/°C
Static drain - source on - state resistance	$R_{DS(on)}^{*3}$	$V_{GS} = 4.5V, I_D = 4.5A$	-	16.9	23.7	mΩ
		$V_{GS} = 2.5V, I_D = 4.5A$	-	23.9	33.5	
Gate input resistance	R_G	f=1MHz, open drain	-	2.7	-	Ω
Forward Transfer Admittance	$ Y_{fs} ^{*3}$	$V_{DS} = 5V, I_D = 4.5A$	6	-	-	S

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board (30×30×0.8mm)

*3 Pulsed

●Electrical characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	$V_{GS} = 0V$	-	900	-	pF
Output capacitance	C_{oss}	$V_{DS} = 15V$	-	100	-	
Reverse transfer capacitance	C_{rss}	$f = 1\text{MHz}$	-	70	-	
Turn - on delay time	$t_{d(on)}^{*3}$	$V_{DD} \approx 15V, V_{GS} = 4.5V$	-	15	-	ns
Rise time	t_r^{*3}	$I_D = 2.2A$	-	15	-	
Turn - off delay time	$t_{d(off)}^{*3}$	$R_L \approx 6.8\Omega$	-	40	-	
Fall time	t_f^{*3}	$R_G = 10\Omega$	-	10	-	

●Gate charge characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Total gate charge	Q_g^{*3}	$V_{DD} \approx 15V,$	-	8.1	-	nC
Gate - Source charge	Q_{gs}^{*3}	$I_D = 4.5A,$	-	2.1	-	
Gate - Drain charge	Q_{gd}^{*3}	$V_{GS} = 4.5V$	-	2.0	-	

●Body diode electrical characteristics (Source-Drain) ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous forward current	I_S	$T_a = 25^\circ\text{C}$	-	-	0.8	A
Body diode pulse current	I_{SP}^{*1}		-	-	18	A
Forward voltage	V_{SD}^{*3}	$V_{GS} = 0V, I_S = 0.8A$	-	-	1.2	V

●Electrical characteristic curves

Fig.1 Power Dissipation Derating Curve



Fig.2 Maximum Safe Operating Area

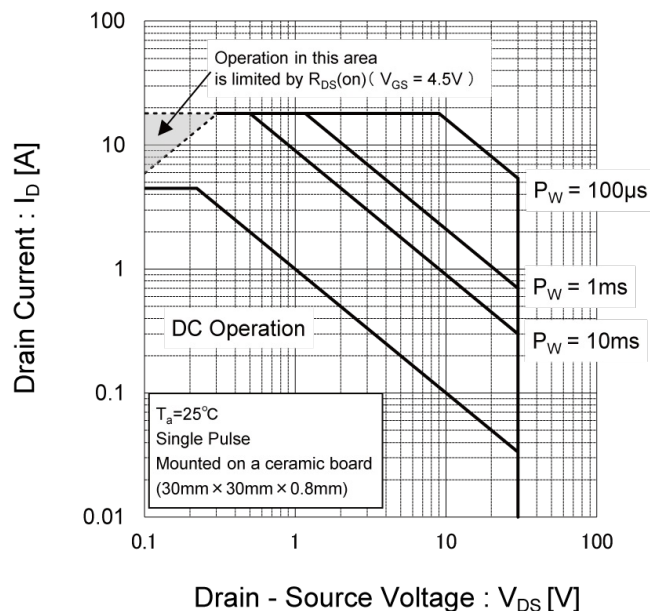


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

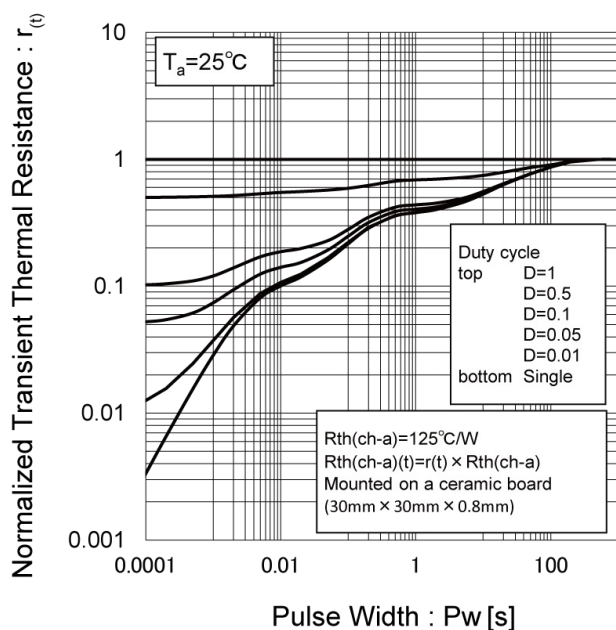
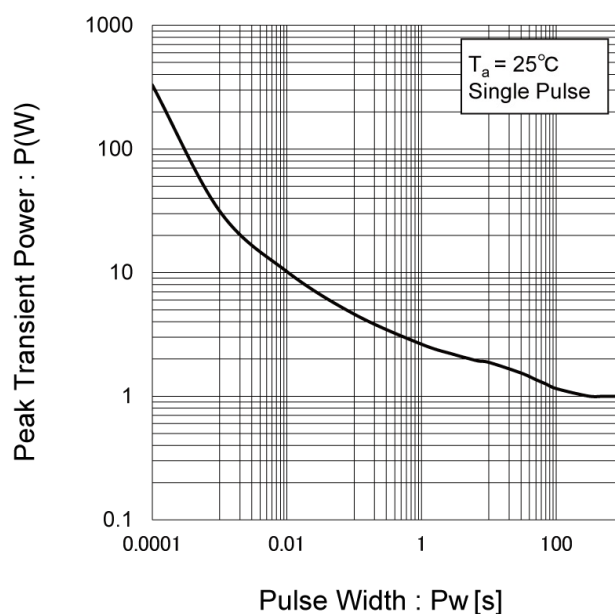


Fig.4 Single Pulse Maximum Power dissipation



●Electrical characteristic curves

Fig.5 Typical Output Characteristics(I)

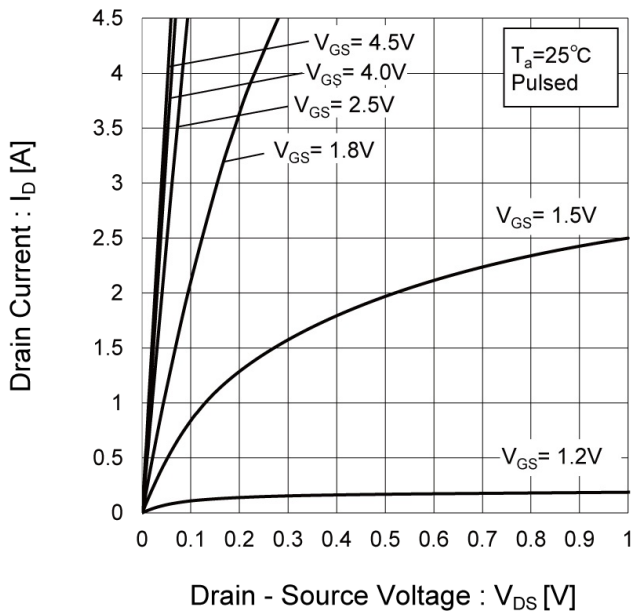


Fig.6 Typical Output Characteristics(II)

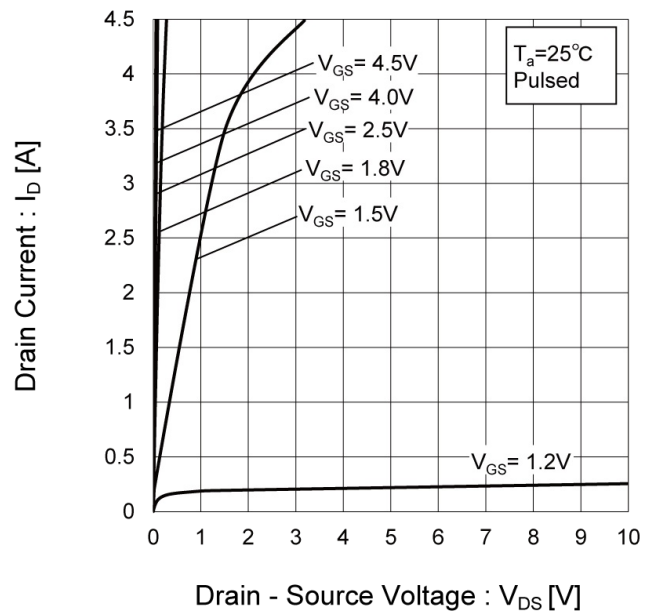
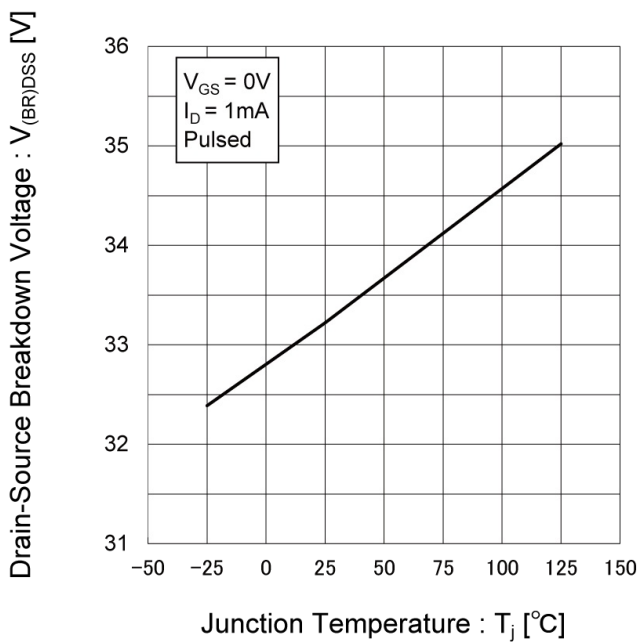


Fig.7 Breakdown Voltage vs. Junction Temperature



●Electrical characteristic curves

Fig.8 Typical Transfer Characteristics

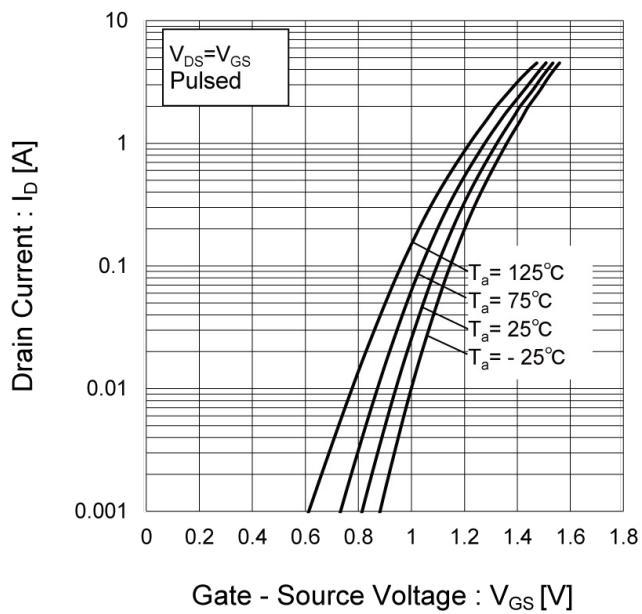


Fig.9 Gate Threshold Voltage vs. Junction Temperature

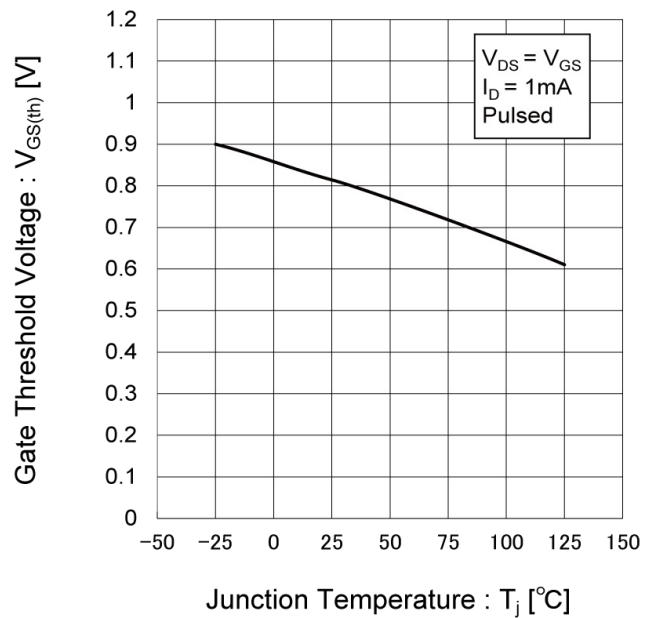
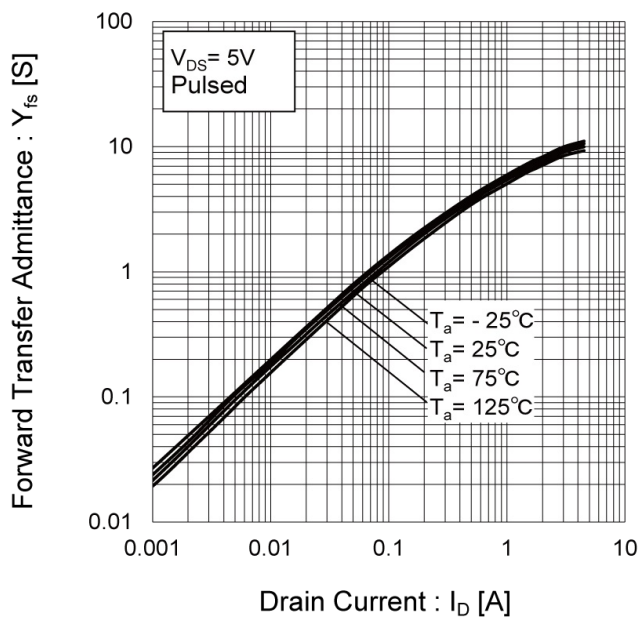


Fig.10 Transconductance vs. Drain Current



●Electrical characteristic curves

Fig.11 Drain Current Derating Curve

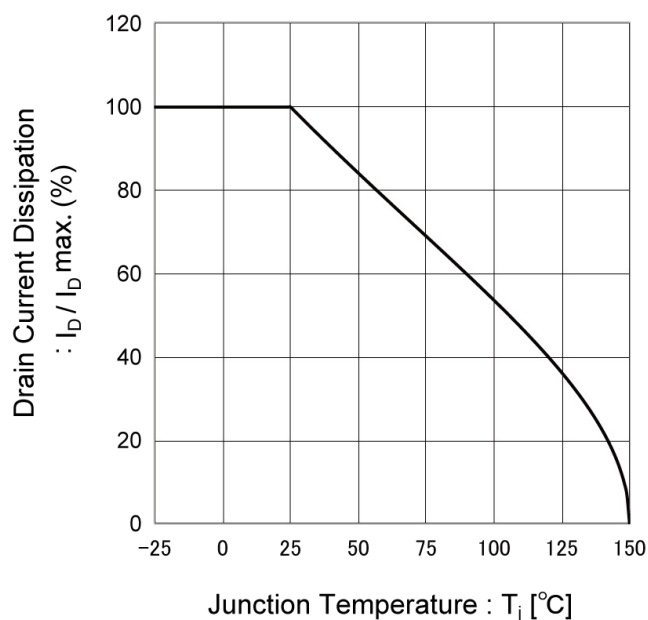


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

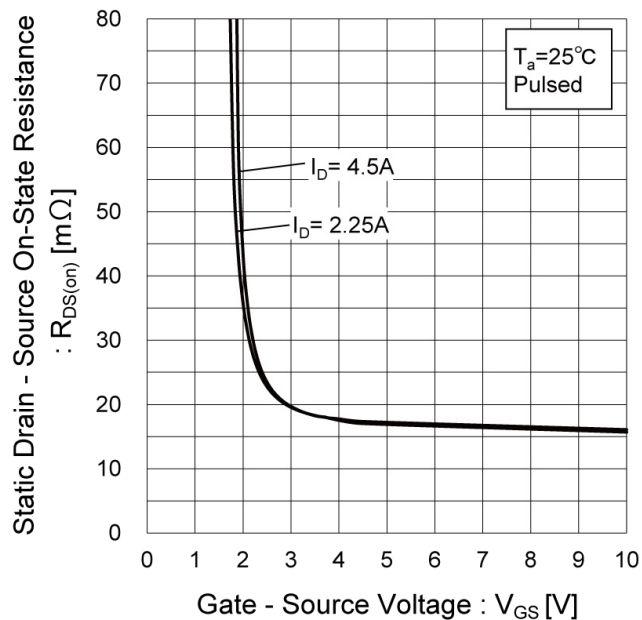
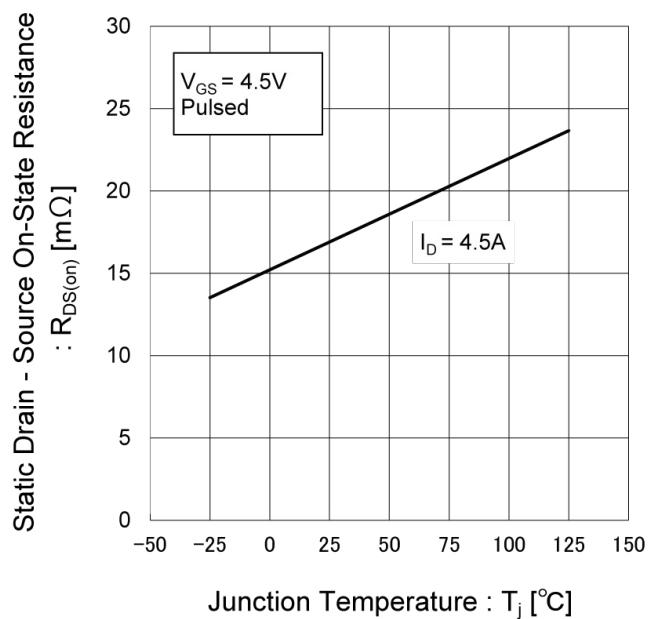


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



●Electrical characteristic curves

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current(I)

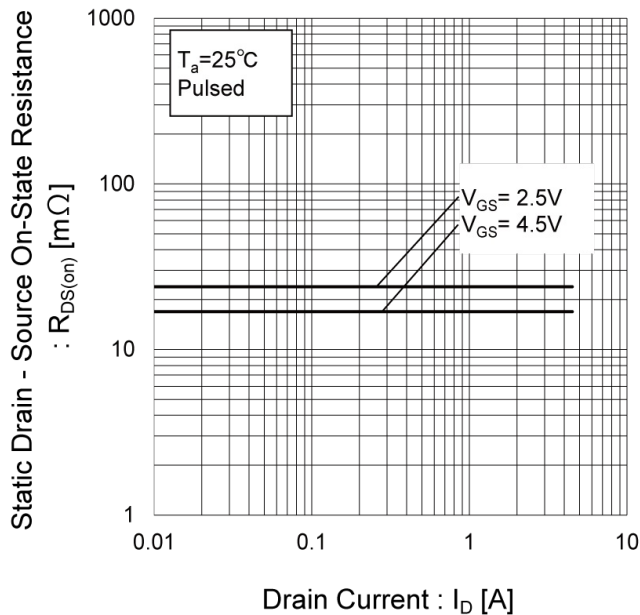


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current(II)

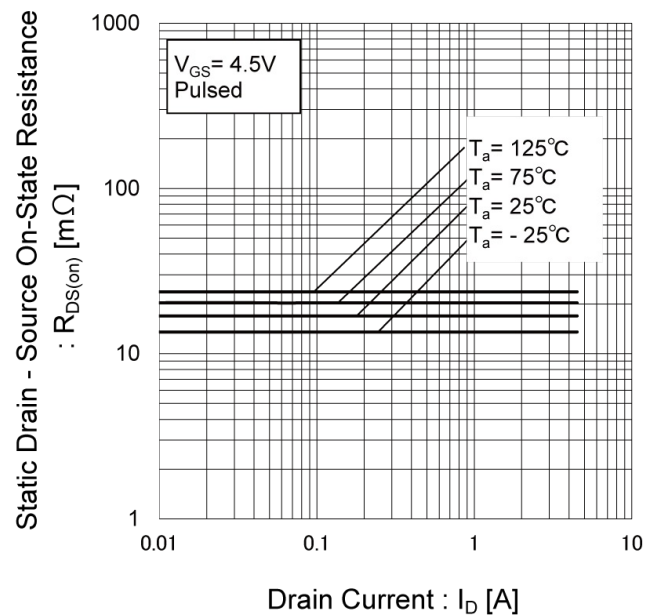
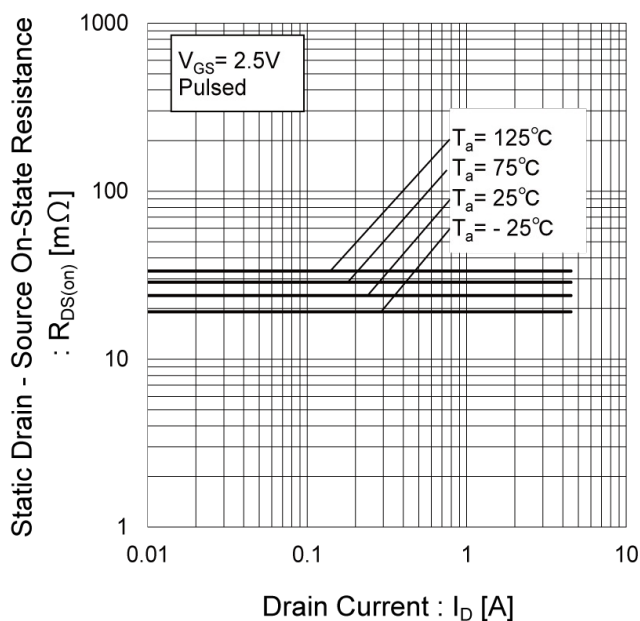


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current(III)



●Electrical characteristic curves

Fig.17 Typical Capacitance vs. Drain - Source Voltage

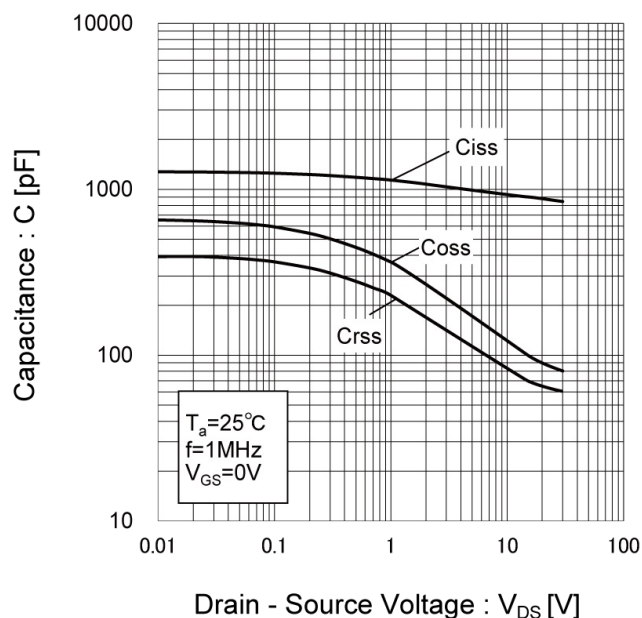


Fig.18 Switching Characteristics

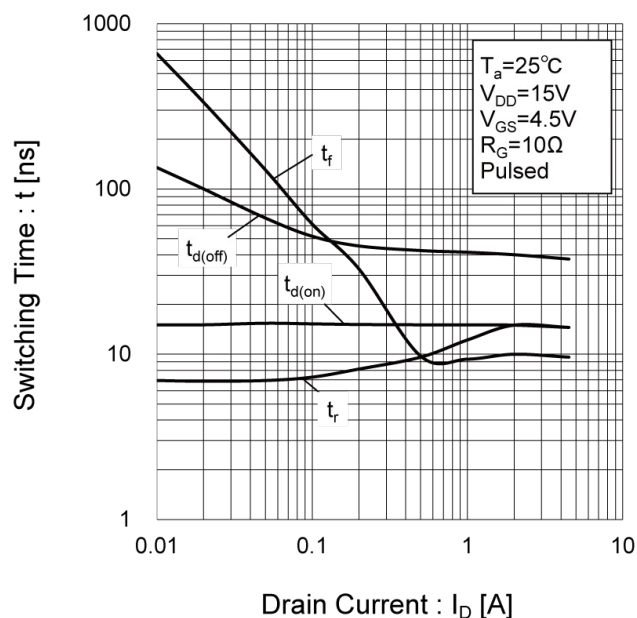


Fig.19 Dynamic Input Characteristics

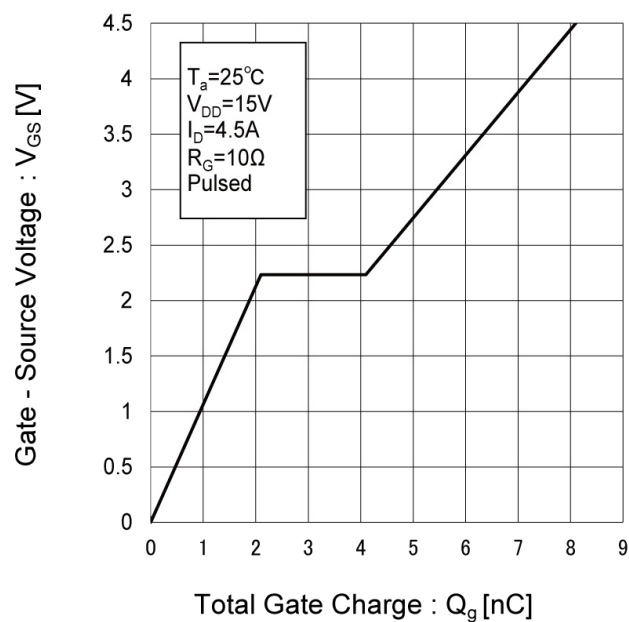
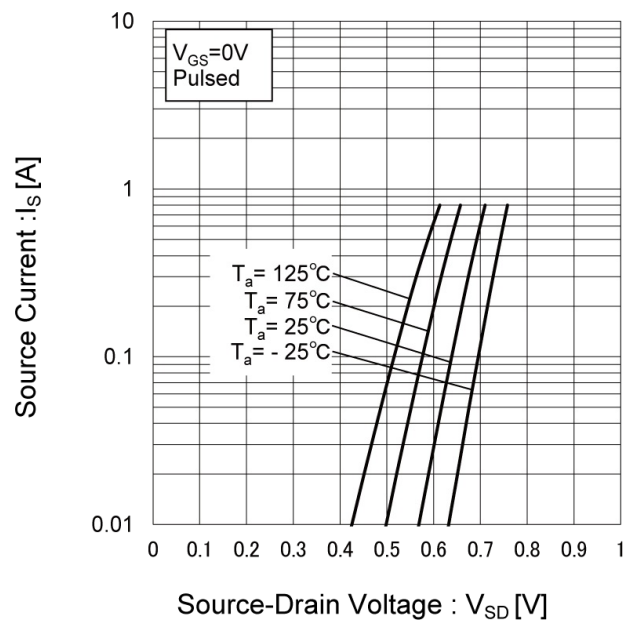


Fig.20 Source Current vs. Source Drain Voltage



● Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

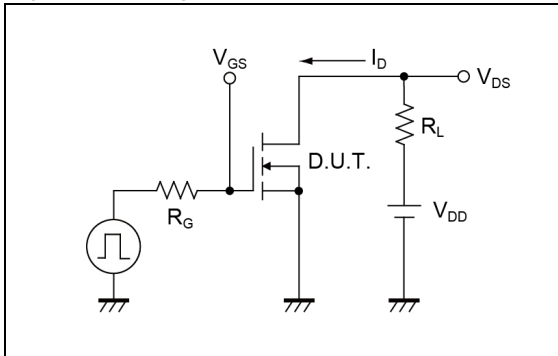


Fig.1-2 Switching Waveforms

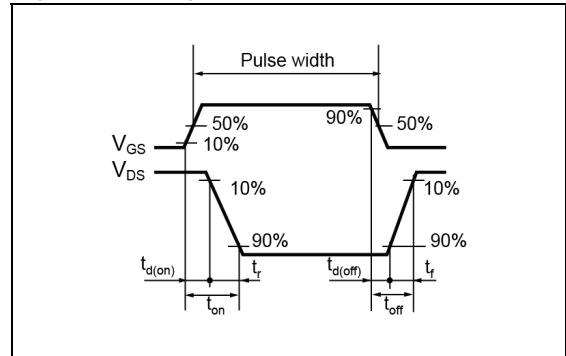


Fig.2-1 Gate Charge Measurement Circuit

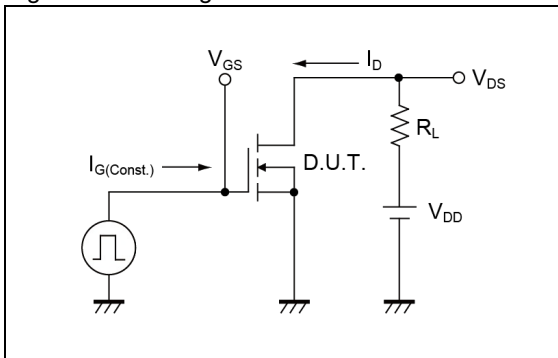
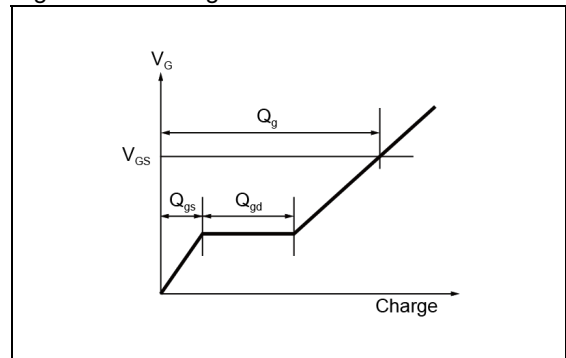


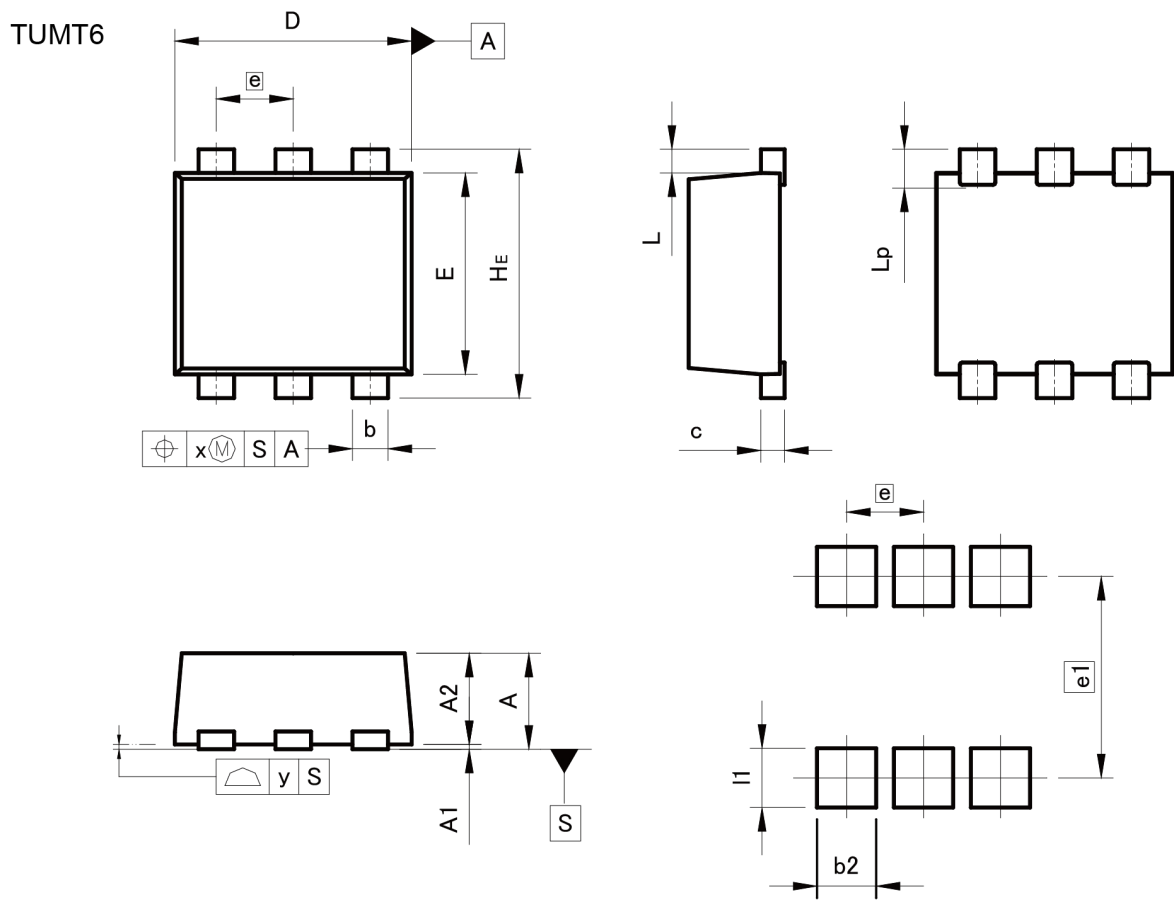
Fig.2-2 Gate Charge Waveform



● Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

●Dimensions



Pattern of terminal position areas
[Not a recommended pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	0.85	—	0.033
A1	0.00	0.10	0.000	0.004
A2	0.72	0.82	0.028	0.032
b	0.25	0.40	0.010	0.016
c	0.12	0.22	0.005	0.009
D	1.90	2.10	0.075	0.083
E	1.60	1.80	0.063	0.071
e	0.65		0.026	
HE	2.00	2.20	0.079	0.087
L	0.20		0.008	
Lp	—	0.40	—	0.016
x	—	0.10	—	0.004
y	—	0.10	—	0.004

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b2	—	0.50	—	0.020
e1	1.70		0.067	
l1	—	0.50	—	0.020

Dimension in mm/inches

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