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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

MOS INTEGRATED CIRCUIT

μPD720150

USB 2.0 HOST/PERIPHERAL CONTROLLER

μPD720150 is USB 2.0 Host/Peripheral controller, which complies with the universal serial bus specification revision 2.0. μPD720150 has 16 bit CPU interface with 2 DMA slave function and connects to various CPUs. μPD720150 is suitable for various embedded application.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μPD720150 User's Manual (Host Controller): S19374E

μPD720150 User's Manual (Peripheral Controller): S19375E

FEATURES

(1) 2 USB ports

- Host dedicated port & Host/Peripheral selectable port
- Host/Peripheral concurrent operation

<Configurable USB ports>

Port 1	Port 2
Host	–
–	Host
Host	Host
Host	Peripheral
–	Peripheral

- Integrates USB transceiver

(2) Low power consumption

- 1.5 V internal operating voltage
- Supports clock stop function during stand-by mode
- Reduces power consumption during Hi-Speed mode

(3) Integration of external parts

- On chip USB termination and pull-up/-down resistor
- On chip regulator for 1.5 V internal power supply

(4) 10 Configurable pipes

- Configurable transfer type for pipe1-9
- Supports all transfer types (Control/Bulk/Interrupt/Isochronous)
- Internal FIFO for transfer pipe

(5) Host Controller

- Supports High-/Full-/Low-Speed with auto detection
- Higher data transfer rate with DMA auto-continuation function in processing of multiple transactions
- USB hub support (limited usage)
- Auto scheduling of (μ)SOF and periodic transfer
- Automatic memory mapping
- Port power control and over current detection

(6) Peripheral Controller

- Supports High-/Full-Speed
- Interval setting for isochronous transfer
- Auto recovery of missing (μ)SOF
- Auto detection of Mass-storage class CBW command
- Supports USB remote wakeup

(7) Others

- 16-bit CPU bus Interface
  Separate / Multiplex bus selectable
  Supports little-/big-endian
  DMA 2ch (16/8 bit selectable)
- 6 GPIO pins
- System clock : 30 MHz crystal
- 3.3 V single power supply

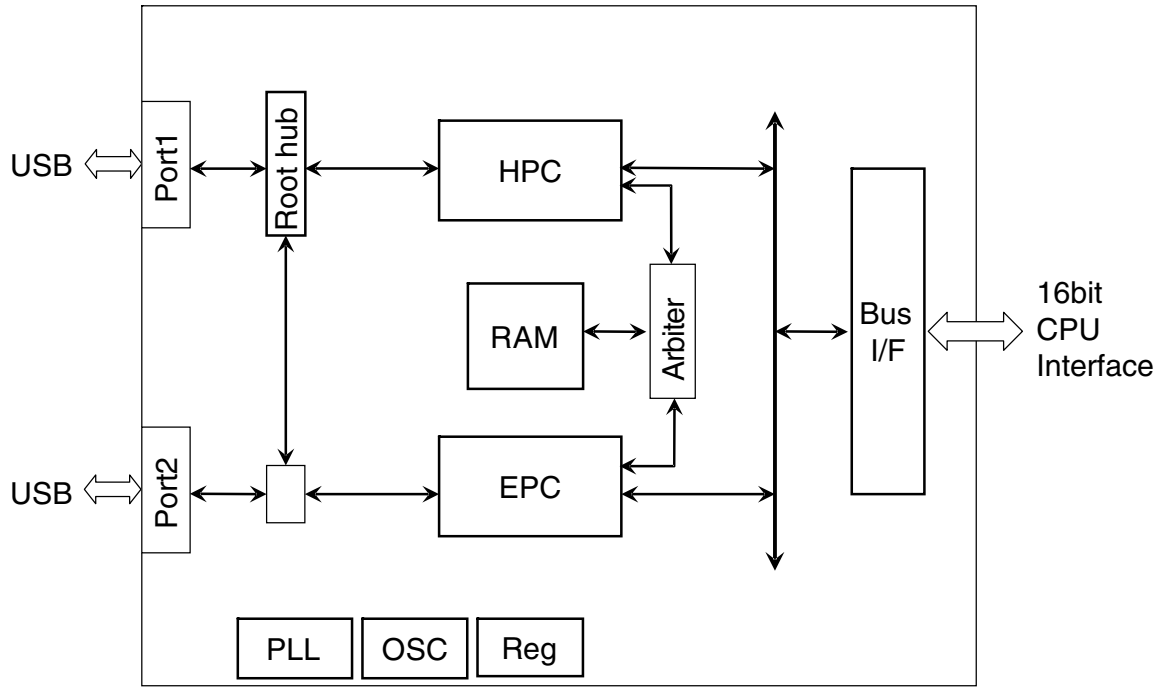
ORDERING INFORMATION

Part Number	Package	Remark
μPD720150GK-9EU-A	80-pin plastic TQFP (fine pitch) (12 × 12)	Lead-free product
μPD720150F1-BAE-A	84-pin plastic FBGA (6 × 6)	Lead-free product

Document No. R19DS0023EJ0300
(Previous No. S19338EJ2V0DS00)
Date Published March 2011 NS

The mark <R> shows major revised points.

BLOCK DIAGRAM



Bus I/F : 16bit CPU interface with 2 DMA slave mode. Bus mode can be selectable (Separate mode or multiplex mode).

HPC : Host controller block. This block handles frame scheduling, data transfer for USB devices, etc.

Root Hub : During host function, this block handles USB device connection and port power control.

EPC : Endpoint Controller. This block handles peripheral function and control all endpoints which required each USB transfer, such as Bulk, Control, Interrupt, Isochronous transfer.

RAM : Internal RAM for USB data transfer.

Arbiter : This block arbitrates the access to the internal RAM.

Port1 : Host only USB port.

Port2 : Host, peripheral selectable USB port.

PLL : Internal PLL.

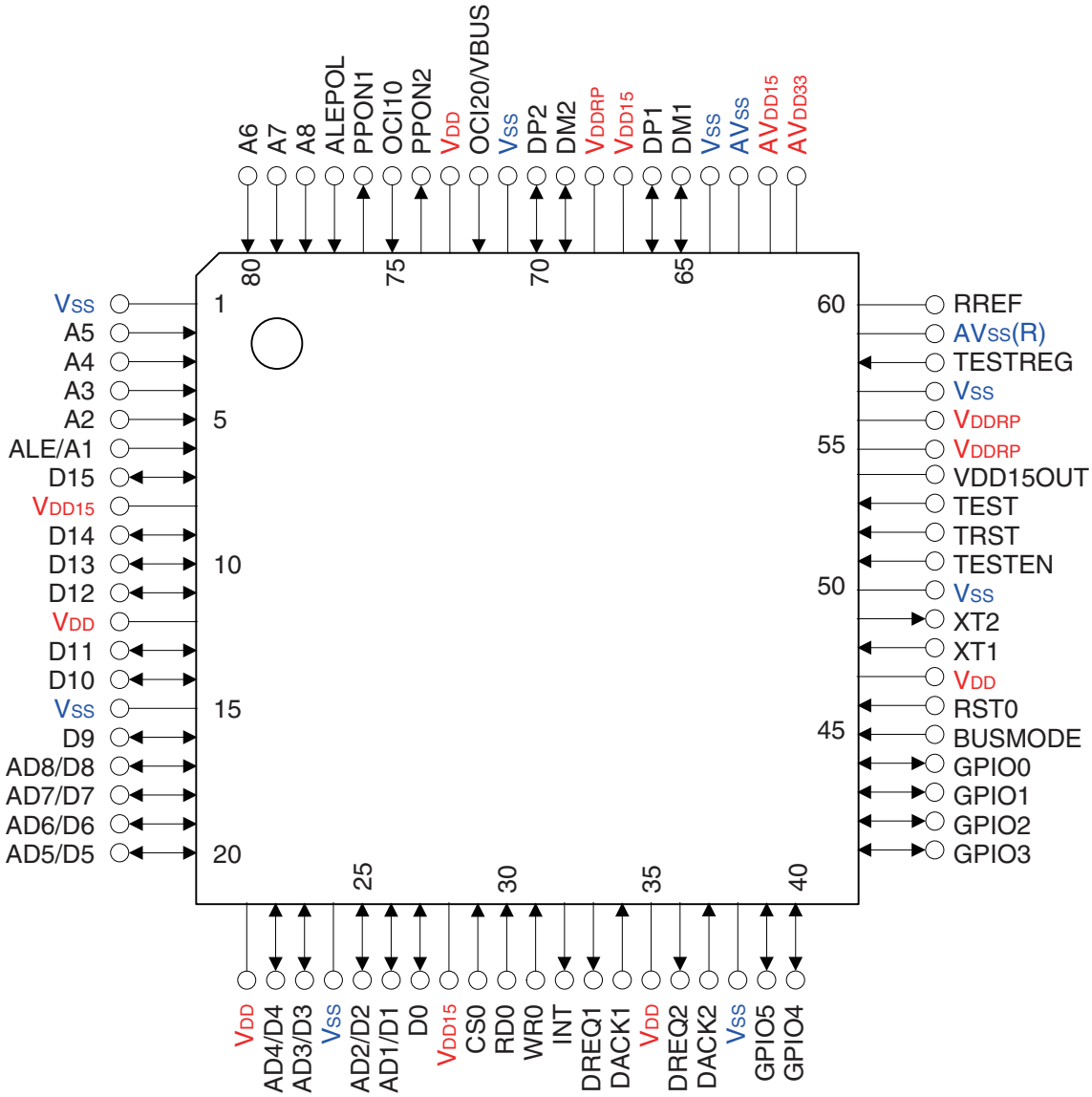
OSC : Internal oscillator block.

Reg : Internal voltage regulator for internal power supply.

PIN CONFIGURATION

- **80-pin plastic TQFP (fine pitch) (12 × 12)**
  μPD720150GK-9EU-A

Top View



Pin Name

- **80-pin plastic TQFP (fine pitch) (12 × 12)**
  μPD720150GK-9EU-A

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	21	V_{DD}	41	GPIO3	61	AV_{DD33}
2	A5	22	AD4/D4	42	GPIO2	62	AV_{DD15}
3	A4	23	AD3/D3	43	GPIO1	63	AV_{SS}
4	A3	24	V_{SS}	44	GPIO0	64	V_{SS}
5	A2	25	AD2/D2	45	BUSMODE	65	DM1
6	ALE/A1	26	AD1/D1	46	RST0	66	DP1
7	D15	27	D0	47	V_{DD}	67	V_{DD15}
8	V_{DD15}	28	V_{DD15}	48	XT1	68	V_{DDRP}
9	D14	29	CS0	49	XT2	69	DM2
10	D13	30	RD0	50	V_{SS}	70	DP2
11	D12	31	WR0	51	TESTEN	71	V_{SS}
12	V_{DD}	32	INT	52	TRST	72	OCI20/VBUS
13	D11	33	DREQ1	53	TEST	73	V_{DD}
14	D10	34	DACK1	54	VDD15OUT	74	PPON2
15	V_{SS}	35	V_{DD}	55	V_{DDRP}	75	OCI10
16	D9	36	DREQ2	56	V_{DDRP}	76	PPON1
17	AD8/D8	37	DACK2	57	V_{SS}	77	ALEPOL
18	AD7/D7	38	V_{SS}	58	TESTREG	78	A8
19	AD6/D6	39	GPIO5	59	$AV_{SS}(R)$	79	A7
20	AD5/D5	40	GPIO4	60	RREF	80	A6

Remark $AV_{SS}(R)$ should be used to connect RREF through 1 % precision reference resistor of 1.6 kΩ.

PIN CONFIGURATION

- **84-pin plastic FBGA (6 × 6)**
  μPD720150F1-BAE-A

	A	B	C	D	E	F	G	H	J	K	
10	RREF 28	AV_{SS}(R) 27	VDD15 OUT 26	V_{SS} 25	XT2 24	XT1 23	V_{DD} 22	GPIO1 21	GPIO3 20	GPIO4 19	10
9	V_{SS} 29	AV_{DD33} 58	TEST REG 57	TRST 56	TESTEN 55	BUS MODE 54	RST0 53	GPIO2 52	GPIO5 51	DACK2 18	9
8	DM1 30	AV_{SS} 59	AV_{DD15} 80	V_{DDRP} 79	V_{DD} 78	V_{DD} 77	V_{SS} 76	GPIO0 75	DREQ2 50	DACK1 17	8
7	DP1 31	V_{SS} 60	TEST 81					V_{SS} 74	INT 49	DREQ1 16	7
6	V_{DD15} 32	OCI20/ VBUS 61	V_{DDRP} 82					V_{DD} 73	RD0 48	WR0 15	6
5	DM2 33	PPON2 62	V_{DD} 83					V_{DD15} 72	D0 47	CS0 14	5
4	DP2 34	OCI10 63	V_{SS} 84					V_{SS} 71	AD2/D2 46	AD1/D1 13	4
3	V_{SS} 35	ALEPOL 64	V_{SS} 65	V_{DD15} 66	V_{DD} 67	V_{DD} 68	V_{SS} 69	V_{DD} 70	AD4/D4 45	AD3/D3 12	3
2	A8 36	PPON1 37	A5 38	A3 39	ALE/A1 40	D14 41	D11 42	D9 43	AD7/D7 44	AD5/D5 11	2
1	A7 1	A6 2	A4 3	A2 4	D15 5	D13 6	D12 7	D10 8	AD8/D8 9	AD6/D6 10	1
	A	B	C	D	E	F	G	H	J	K	

Top View

Pin Name

- **84-pin plastic FBGA (6 × 6)**
  μPD720150F1-BAE-A

Pin No.	Pin Name	Pin No.	Pin Name	Pin	Pin Name	Pin No.	Pin Name
1	A7	22	V_{DD}	43	D9	64	ALEPOL
2	A6	23	XT1	44	AD7/D7	65	V_{SS}
3	A4	24	XT2	45	AD4/D4	66	V_{DD15}
4	A2	25	V_{SS}	46	AD2/D2	67	V_{DD}
5	D15	26	VDD15OUT	47	D0	68	V_{DD}
6	D13	27	AV_{SS} (R)	48	RD0	69	V_{SS}
7	D12	28	RREF	49	INT	70	V_{DD}
8	D10	29	V_{SS}	50	DREQ2	71	V_{SS}
9	AD8/D8	30	DM1	51	GPIO5	72	V_{DD15}
10	AD6/D6	31	DP1	52	GPIO2	73	V_{DD}
11	AD5/D5	32	V_{DD15}	53	RST0	74	V_{SS}
12	AD3/D3	33	DM2	54	BUSMODE	75	GPIO0
13	AD1/D1	34	DP2	55	TESTEN	76	V_{SS}
14	CS0	35	V_{SS}	56	TRST	77	V_{DD}
15	WR0	36	A8	57	TESTREG	78	V_{DD}
16	DREQ1	37	PPON1	58	AV_{DD33}	79	V_{DDRP}
17	DACK1	38	A5	59	AV_{SS}	80	AV_{DD15}
18	DACK2	39	A3	60	V_{SS}	81	TEST
19	GPIO4	40	ALE/A1	61	OCI20/VBUS	82	V_{DDRP}
20	GPIO3	41	D14	62	PPON2	83	V_{DD}
21	GPIO1	42	D11	63	OCI10	84	V_{SS}

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 1.6 kΩ.

1. PIN FUNCTIONS

This section describes each pin functions.

1.1 Power supply

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
V_{DD}	_	Power	_	_	+3.3 V power supply for IO power.
V_{DDRP}	_	Power	_	_	+3.3 V power supply for USB and internal regulator.
V_{DD15}	_	Power	_	_	+1.5 V power supply. These pins must be supplied from VDD15OUT, output from internal regulator.
VDD15OUT	O	Regulator	_	1.5V	+1.5 V voltage output from internal regulator.
AV_{DD33}	_	Power	_	_	+3.3 V power supply for analog circuit.
AV_{DD15}	_	Power	_	_	+1.5 V power supply for analog circuit.
V_{SS}	_	Power	_	_	Ground
AV_{SS}	_	Power	_	_	Ground for analog circuit
AV_{SS}(R)	_	Power	_	_	Ground for reference resistor

1.2 Analog Signal

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
RREF	_	Analog	_	_	RREF must be connected to a 1% precision reference resistor of 1.6 k . The other side of the resistor must be connected to AV_{SS}(R) which must be connected to stable AV_{SS}.

1.3 System clock/Reset signal

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
XT1	I	OSC	_	_	Oscillator in Connect to 30 MHz crystal.
XT2	O	OSC	_	inverted XT1	Oscillator out Connect to 30 MHz crystal.
RST0	I	3.3V with schmitt	Low	_	Asynchronous reset signal

1.4 System Interface

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
A (8:2)	I	3.3V OR type	–	–	(Separate mode) Address bus (Multiplex mode) not used
ALE/A1	I	3.3V	(ALE signal) Depends on ALEPOL	–	(Separate mode) Address bus (Multiplex mode) Address strobe signal
ALEPOL	I	3.3V	–	–	ALE Active level select signal ALE 0: Low active 1: High active
D (15:9), D0	I/O	3.3V	–	Input	(Separate/Multiplex mode) Data bus
AD(8:1)/D(8:1)	I/O	3.3V	–	Input	(Separate mode) Data bus (Multiplex mode) Address/Data bus
CS0	I	3.3V	Low	–	Chip select signal
RD0	I	3.3V	Low	–	Read enable signal
WR0	I	3.3V	Low	–	Write enable signal
INT	O	3.3V	–	High	Interrupt request signal
DREQ (2:1)	O	3.3V	–	High	DMA request signal
DACK (2:1)	I	3.3V	–	–	DMA acknowledge signal
GPIO (5:0)	I/O	3.3V with pull-down	–	Input	General purpose I/O
BUSMODE	I	3.3V	–	–	Bus mode select signal (Separate/Multiplex). 0: Multiplex mode 1: Separate mode

1.5 USB Interface

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
DP (2:1)	I/O	USB	–	Pull-down	USB D+ signal
DM (2:1)	I/O	USB	–	Pull-down	USB D– signal
OCI10	I	3.3V	Low	–	(Host) Over-current status input of the down stream facing port 0: Over-current condition is detected 1: No over-current condition is detected.
OCI20/VBUS	I	3.3V with schmitt 5V tolerant	Low / High	–	(Host) Over-current status input of the down stream facing port 0: Over-current condition is detected 1: No over-current condition is detected. (Peripheral) VBUS monitoring signal 0: VBUS is not detected. 1: VBUS is detected.
PPON (2:1)	O	3.3V	High	Low	(Host) USB port power supply control output for downstream facing ports. 0: Power supply OFF 1: Power supply ON

1.6 Test signals

Pin Name	Direction	Buffer Type	Active Level	Reset	Function
TESTEN	I	3.3V with pull-down	–	–	Test signal This must be opened on board.
TEST	I	3.3V with pull-down	–	–	Test signal This must be opened on board.
TESTREG	I	3.3V with pull-down	–	–	Test signal This must be opened on board.
TRST	I	3.3V with pull-down	–	–	Test signal This must be opened on board.

2. HOW TO CONNECT TO EXTERNAL ELEMENTS

2.1 Handling Unused Pins

Unused pins shall be connected as shown below.

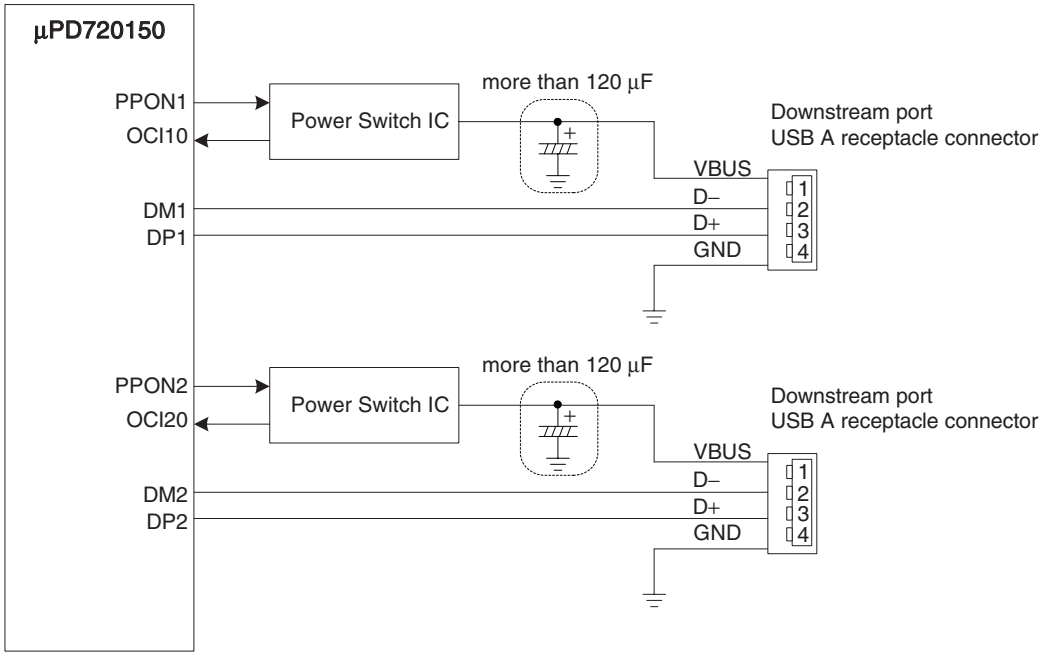
Table 2-1. Unused Pin Connection

Pin Name	Direction	Connection Method	Remark
DP(2:1)	I/O	No Connection (Open)	•For unused USB port. •During Peripheral mode, PPON2 must be open.
DM(2:1)	I/O	No Connection (Open)	
OCI10 OCI20/VBUS	I	Pull-up	
PPON(2:1)	O	No connection (Open)	
ALEPOL	I	Pull-down or Pull-up	During separate mode.
A (8:2)	I	Pull-down or Pull-up	During multiplex mode.
DREQ(2:1)	O	No connection (Open)	For unused DMA channel.
DACK(2:1)	I	Pull-up [Note]	For unused DMA channel.
GPIO(5:0)	I/O	No connection (Open)	For unused GPIO pins.
TESTEN	I	No connection (Open)	
TEST	I	No connection (Open)	
TRST	I	No connection (Open)	
TESTREG	I	No connection (Open)	

Note The polarity of this signal can be set from internal register. Set appropriate inactive level.

2.2 USB Port Connection (Host mode)

Figure 2–1. USB Downstream Port Connection (Host mode)



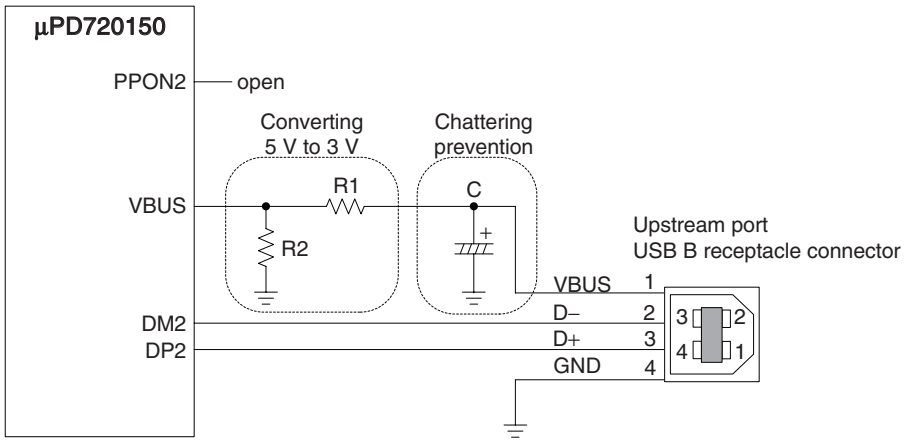
Caution Table 2-2 shows the pin description of PPON and OCI0. When power switch IC which supports different active level from μPD720150 is used, μPD720150 cannot control port power appropriately.

Table 2-2. PPON (2:1), OCI (2:1)0 pin description (Host mode)

Pin Name	Direction	Function	High level	Low level	Default value
PPON (2:1)	OUT	VBUS control	Port power ON	Port power OFF	Low level
OCI (2:1)0	IN	Over current detection	Normal	Over-current condition	–

2.3 USB Port Connection (Peripheral mode)

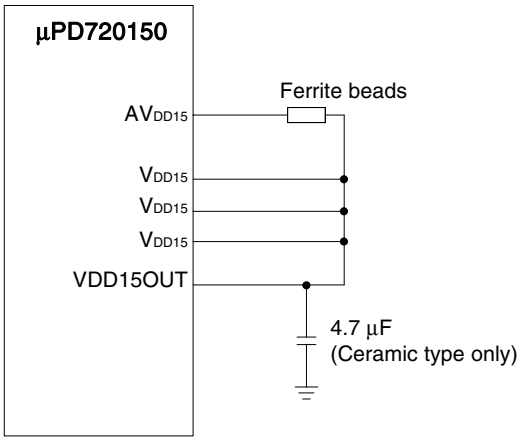
Figure 2–2. USB Downstream Port Connection (Peripheral mode)



Caution VBUS pin must be applied under +3.0 V when V_{DD} power = 0 V.

2.4 Internal Regulator Circuit Connection

Figure 2–3. Internal Regulator Circuit Connection

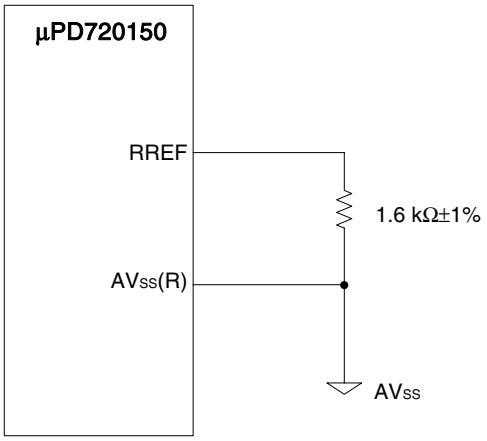


Caution VDD15OUT must be routed to only V_{DD15} (and AV_{DD15}). In case that VDD15OUT is also used for power supply of other ICs, this may cause unstable operation of the μPD720150.

Remark V_{DD15} is powered by VDD15OUT from internal regulator. It is not necessary to use an external regulator for V_{DD15}.

2.5 Analog Circuit Connection

Figure 2–4. Analog Circuit Connection

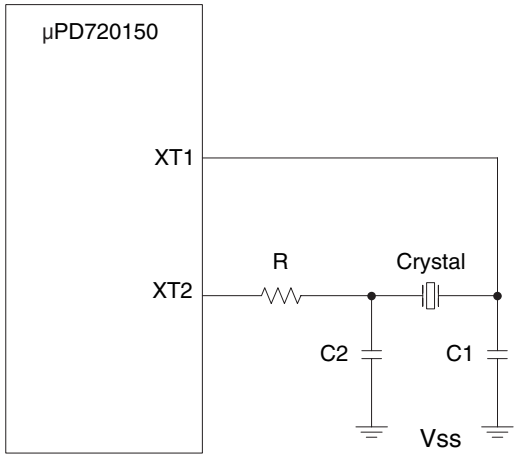


Caution The RREF register must be one 1.6 KΩ with 1% accuracy. It must NOT consist of two or more resisters (i.e. 1.5 KΩ + 100 Ω).

Remark The board layout should minimize the total path length from RREF through the resistor to AV_{SS}(R) and path length to AV_{SS} (analog ground). AV_{SS} must be stable.

2.6 Crystal Connection

Figure 2–5. Crystal Connection



The following crystals are evaluated on our reference design board. Table 2-3 shows the external parameters.

Table 2-3. External Parameters

Vender	Crystal			Oscillation circuit parameters		
	Type	Frequency [MHz]	Load Capacitance [pF]	R [Ω]	C1 [pF]	C2 [pF]
NDK Note 1	AT-41	30.000	5	470	8	8
	NX2520SA	30.000	7	1000	8	8
	NX2016AA	30.000	7	1000	8	8
KDS Note 2	DSX321G	30.000	5.7	680	5	5

Notes 1. NIHON DEMPA KOGYO CO., LTD.
2. DAISHINKU CORP.

In using these crystals, contact KDS or NDK to get the specification on external components to be used in conjunction with the crystal.

NDK's home page: http://www.ndk.com/en/
KDS's home page: http://www.kds.info/index_en.htm

3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 3.3 V input buffer
  A1/ALE, ALEPOL, CS0, RD0, WR0, DACK (2:1), BUSMODE, OCI10
- 3.3 V input buffer (OR-Type)
  A (8:2)
- 3.3 V input buffer (with pull-down resistor)
  TESTEN, TEST, TRST, TESTREG
- 3.3 V schmitt input buffer
  RST0
- 3.3 V I_{OL} = 6 mA bi-directional buffer
  D (15:0), AD (8:1)
- 3.3 V I_{OL} = 3 mA bi-directional buffer (with pull-down resistor)
  GPIO (5:0)
- 5V tolerant schmitt input buffer
  OCI20/VBUS
- 3.3 V IOL = 6mA output buffer
  INT, DREQ (2:1), PPON (2:1)
- 3.3 V oscillator Interface
  XT1, XT2
- USB interface, analog signal
  DP (2:1), DM (2:1), RREF

3.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}, V_{DDRP}, AV_{DD33}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}, V_{DDRP}, AV_{DD33}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input signal transition time from 0.1 x V_{DD} to 0.9 x V_{DD}.
Input fall time	t_{fi}	Indicates allowable input fall time to input signal transition time from 0.9 x V_{DD} to 0.1 x V_{DD}.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

3.3 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}, V_{DDRP}, AV_{DD33}		−0.5 to +4.6	V
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD}$ + 0.5 V	−0.5 to +4.6	V
		$V_I < V_{DD}$ + 3.0 V (5 V tolerant)	−0.5 to +6.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD}$ + 0.5 V	−0.5 to +4.6	V
Output current	I_O	3.3 V buffer (I_{OL} = 3 mA)	11	mA
		3.3 V buffer (I_{OL} = 6 mA)	21	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark 3.3 V must be applied to the I/O pins only after applying power supply voltage.

3.4 Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD} Note		2.7	3.3	3.6	V
	V_{DDRP} Note		3.0	3.3	3.6	V
	AV_{DD33} Note		3.0	3.3	3.6	V
High-level input voltage	V_{IH}					
3.3 V high-level input voltage		RST0	2.4		V_{DD}	V
<R>		OCI20/VBUS	2.4		5.5	V
		other input pins	2.0		V_{DD}	V
Low-level input voltage	V_{IL}					
3.3 V low-level input voltage		RST0	0		0.6	V
		other input pins	0		0.8	V
Hysteresis voltage	V_H					
3.3 V hysteresis voltage			0.3		1.5	V
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

Note V_{DD},V_{DDRP} and A_{VDD33} must turn on/off the power at the same time.

3.5 DC Characteristics (V_{DD} =2.7 to 3.6 V, T_A = –40 to +85°C)

3.5.1 Control pin block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		±10	μA
Low-level output current	I_{OL}	V_{OL} = 0.4 V			
3.3 V low-level output current (3 mA)			3.0		mA
3.3 V low-level output current (6 mA)			6.0		mA
High-level output current	I_{OH}	V_{OH} = 2.4 V			
3.3 V high-level output current (3 mA)			–3.0		mA
3.3 V high-level output current (6 mA)			–6.0		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA
3.3 V buffer with pull down resistor		$V_I = V_{DD}$	26	175	μA

3.5.2 USB interface block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}		40.5	49.5	Ω
Termination voltage for upstream facing port pullup (R_{PU})	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert(D+) - (D-)\rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling level	See **Figure 3–2**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10	+10	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		−900	−500	mV

Figure 3–1. Differential Input Sensitivity Range for Low-/full-speed

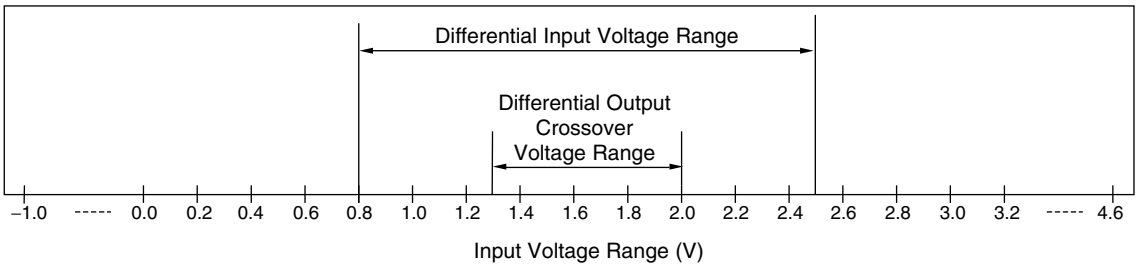


Figure 3–2. Receiver Sensitivity for Transceiver at DP/DM

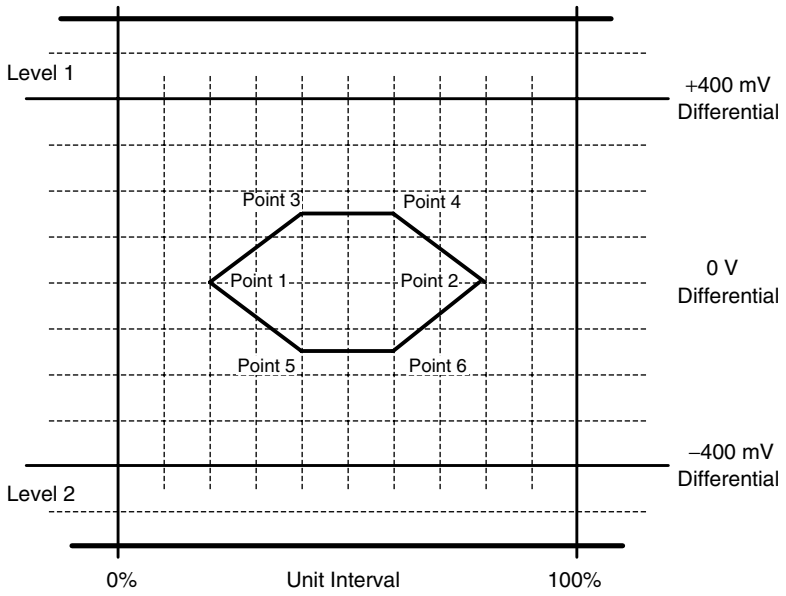
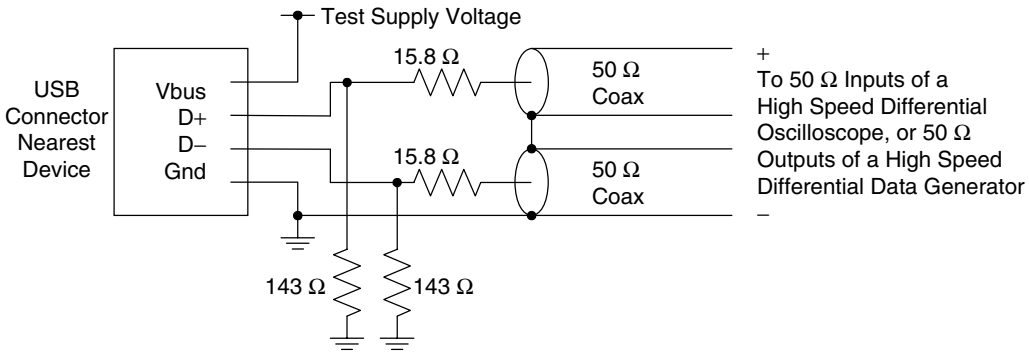


Figure 3–3. Receiver Measurement Fixtures



3.5.3 Power consumption

Hi-speed

Parameter	Mode	Condition	Typ.	Max.	Unit
Power Consumption	Host	Suspend	75		μA
		All the ports do not connect to any devices.	33		mA
		One device is connected (during data transfer)	49		mA
		Two devices are connected (during data transfer)	54		mA
	Peripheral	Suspend	210		μA
		Unconfigured (during Enumeration)	57		mA
		Configured (during data transfer)	58		mA
	Host / Peripheral concurrent operation	Suspend	215		μA
		during data transfer	85		mA

Full-speed

Parameter	Mode	Condition	Typ.	Max.	Unit
Power Consumption	Host	Suspend	75		μA
		All the ports do not connect to any devices.	33		mA
		One device is connected (during data transfer)	44		mA
		Two devices are connected (during data transfer)	50		mA
	Peripheral	Suspend	210		μA
		Unconfigured (during Enumeration)	30		mA
		Configured (during data transfer)	30		mA
	Host / Peripheral concurrent operation	Suspend	215		μA
		during data transfer	51		mA

Remark Typical conditions
Power supply voltage: 3.3 V
Operating ambient temperature: +25°C
Data throughput: 40 Mbps

3.5.4 Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_I	V_{DD} = 0 V, T_A = 25°C		8	pF
Output capacitance	C_O	f_C = 1 MHz		8	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		8	pF

3.6 AC Characteristics (V_{DD} = 2.7 to 3.6 V, T_A = –40 to +85°C)

3.6.1 System clock ratings

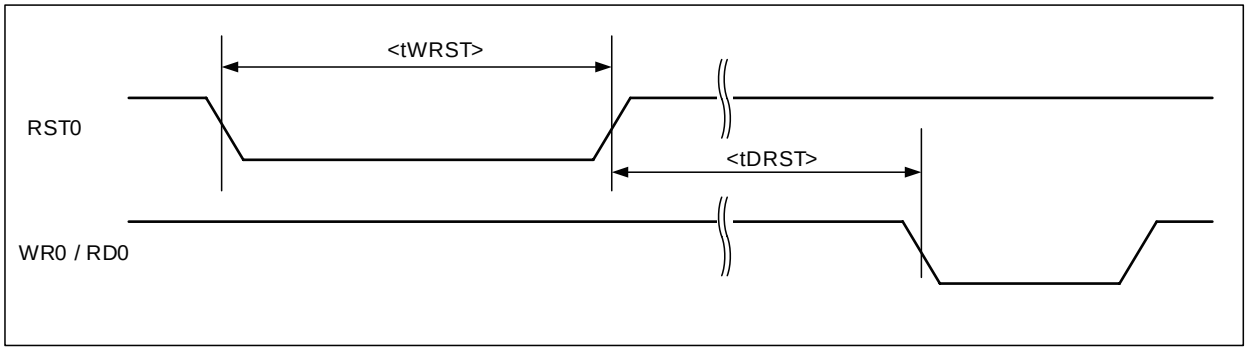
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	Crystal	–500 ppm	30	+500 ppm	MHz
Clock duty cycle	t_{DUTY}		40	50	60	%

Remarks 1. Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of crystal or oscillator block is including initial frequency accuracy, the spread of crystal capacitor loading, supply voltage, temperature, and aging, etc.

3.6.2 System reset

Parameter	Symbol	Condition	Min.	Max.	Unit
RST0 Active level width	tWRST		500	-	ns
RST0 Recovery time	tDRST		13	-	μs



3.6.3 System Interface

Separate Bus Read

Parameter	Symbol		Condition	Min.	Max.	Unit
Read Cycle time	<1>	tCYCR		79	-	ns
Address Setup time (to RD0↓)	<2>	tSAD		0	-	ns
Address Hold time (from RD0↓)	<3>	tHAD		62	-	ns
CS0 Setup time (to RD0↓)	<4>	tSCS		0	-	ns
CS0 Hold time (from RD0↑)	<5>	tHCS		0	-	ns
RD0 Active level width	<6>	tWRD1		62	-	ns
RD0 Inactive level width	<7>	tWRD2		17	-	ns
I/O Float delay time (from RD0↓)Note	<8>	tDIO		1	12	ns
Read Data Delay time (from RD0↓)	<9>	tDDT1	CL=50pF	-	61	ns
Read Data Hold time (from RD0↑)Note	<10>	tDDT2	CL=50pF	0	12	ns

Separate Bus Write

Parameter	Symbol		Condition	Min.	Max.	Unit
Write Cycle time	<11>	tCYCW		51	-	ns
Address Setup time (to WR0↓)	<12>	tSAD		0	-	ns
Address Hold time (from WR0↑)	<13>	tHAD		1	-	ns
CS0 Setup time (to WR0↓)	<14>	tSCS		0	-	ns
CS0 Hold time (from WR0↑)	<15>	tHCS		0	-	ns
WR0 Active level width	<16>	tWWR1		34	-	ns
WR0 Inactive level width	<17>	tWWR2		17	-	ns
Write Data Setup time (to WR0↑)Note	<18>	tSDT		5	-	ns
Write Data Hold time (from WR0↑)Note	<19>	tHDT		1	-	ns

Note In case of using DMA Type 2, please consider DACKn signal timing, instead of RD0/WR0.

Multiplex Bus Read

Parameter	Symbol		Condition	Min.	Max.	Unit
Read Cycle time	<20>	tCYCR		92	-	ns
Address Setup time (to ALE↓)	<21>	tSAD		17	-	ns
Address Hold time (from ALE↓)	<22>	tHAD		1	-	ns
CS0 Setup time (to ALE↓)	<23>	tSCS		17	-	ns
CS0 Hold time (from RD0↑)	<5>	tHCS		0	-	ns
RD0 Active level width	<6>	tWRD1		62	-	ns
I/O Float delay time (from RD0↓)Note	<8>	tDIO		1	12	ns
Read Data Delay time (from RD0↓)	<9>	tDDT1	CL=50pF	-	61	ns
Read Data Hold time (fromRD0↑)Note	<10>	tDDT2	CL=50pF	0	12	ns
ALE Active level width	<24>	tWAL		17	-	ns
RD0 Dalay time (from Address Release)	<25>	tDRD		0	-	ns

Multiplex Bus Write

Parameter	Symbol		Condition	Min.	Max.	Unit
Write Cycle time	<26>	tCYCW		52	-	ns
Address Setup time (to ALE↓)	<21>	tSAD		17	-	ns
Address Hold time (from ALE↓)	<22>	tHAD		1	-	ns
CS0 Setup time (to ALE↓)	<23>	tSCS		17	-	ns
CS0 Hold time (from WR0↑)	<15>	tHCS		0	-	ns
WR0 Active level width	<16>	tWWR1		34	-	ns
Write Data Setup time (to WR0↑)Note	<18>	tSDT		5	-	ns
Write Data Hold time (from WR0↑)Note	<19>	tHDT		1	-	ns
ALE Active level width	<24>	tWAL		17	-	ns
WR0 Delay time (from ALE↓)	<27>	tDWR		0	-	ns

Note In case of using DMA Type 2, please consider DACKn signal timing, instead of RD0/WR0.

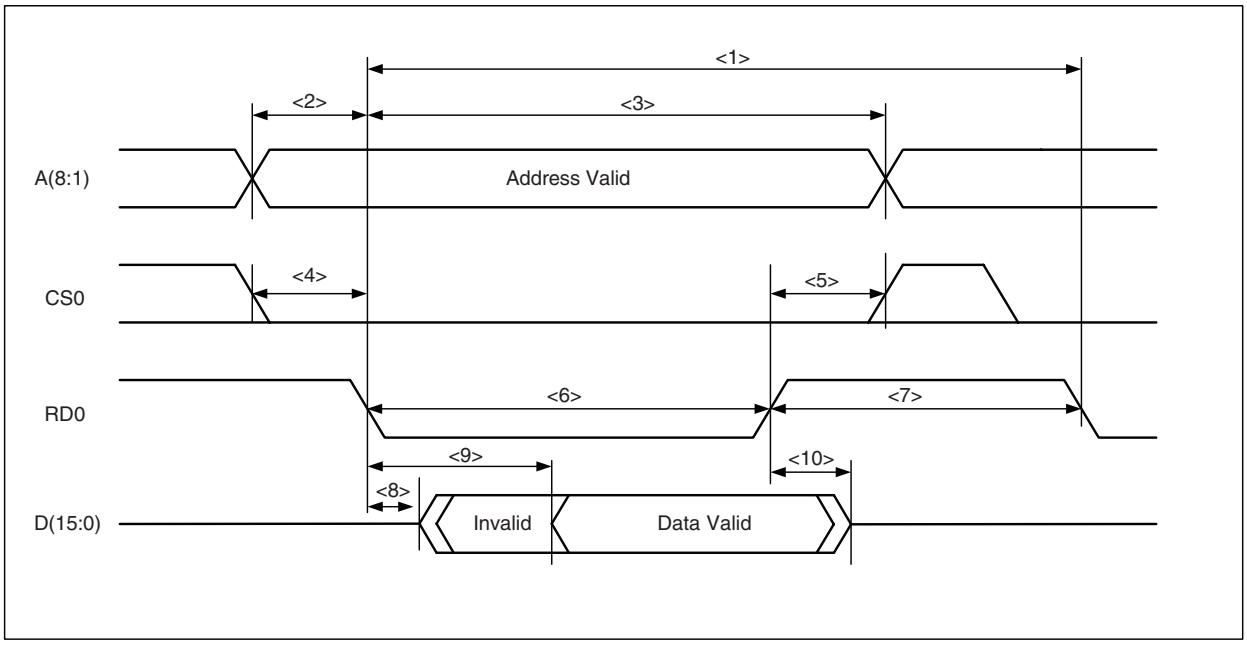
DMA transfer

Parameter	Symbol		Condition	Min.	Max.	Unit
DREQn Active level hold time (from DACKn assert) Note 1	<28>	tDDR1	Single / Burst2 mode	-	15	ns
DREQn Active level hold time (from WR0↓/RD0↓) Note 2	<29>	tDDR2	Burst1 mode	-	63	ns
DREQn Next assert time (from DACKn negate) Note 1	<31>	tDDR4	Single mode	34	66	ns
DMA Read enable Active level width	<32>	tDDA1	Type0,1: RD0 Type2: DACKn	34	-	ns
DMA Read enable Inactive level width	<33>	tDDA2	Type0,1: RD0 Type2: DACKn	17	-	ns
DMA Read Cycle time	<34>	tCYCDR		51	-	ns
Read Data Delay time (from RD0↓) Note 2	<35>	tDDT	CL=50pF	-	14	ns
DMA Write enable Active level width	<36>	tWDA1	Type0,1: WR0 Type2: DACKn			
DMA Write enable Inactive level width	<37>	tWDA2	Type0,1: WR0 Type2: DACKn	17	-	ns
DMA Write Cycle time	<38>	tCYCDW		51	-	ns
DACKn Setup time (to WR0/RD0↓)	<39>	tSDA		0	-	ns
DACKn Hold time (from WR0/RD0↑)	<40>	tHDA		0	-	ns
DREQn Active level hold time (from PIO WR0↑)	<41>	tDDR5	Forced DMA termination (burst 1 mode)	-	63	ns

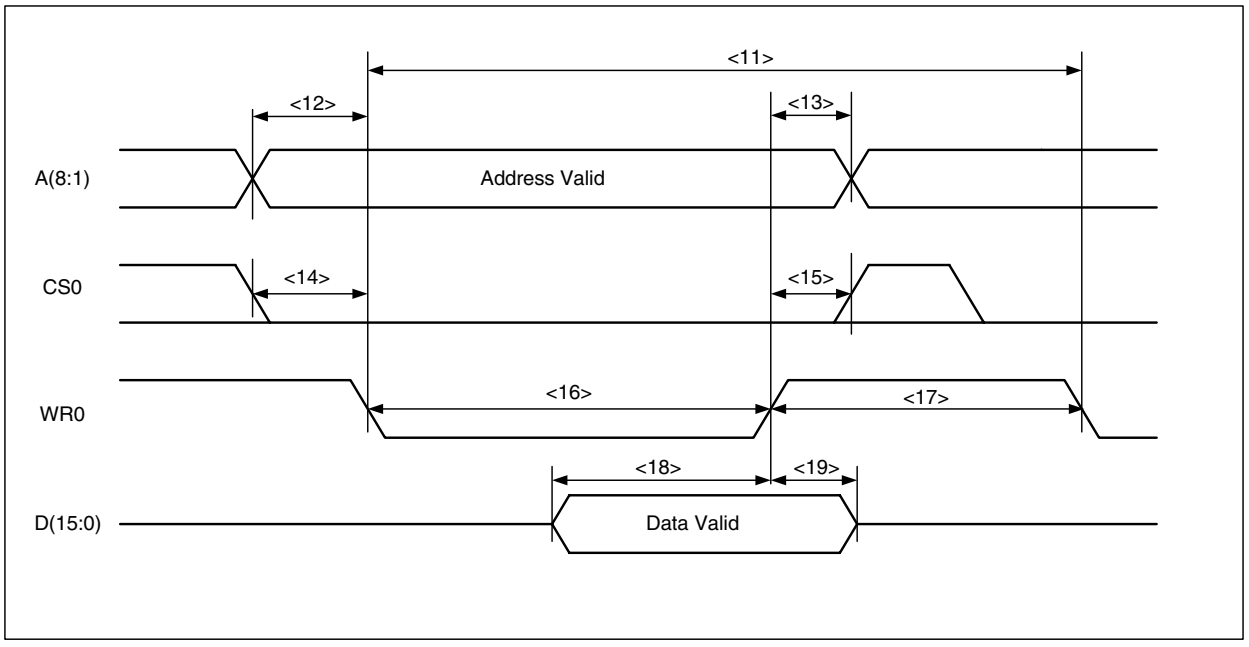
Notes 1. In case of using DMA Type 0, please consider RD0/WR0 signal timing, instead of DACKn.

2. In case of using DMA Type 2, please consider DACKn signal timing, instead of RD0/WR0.

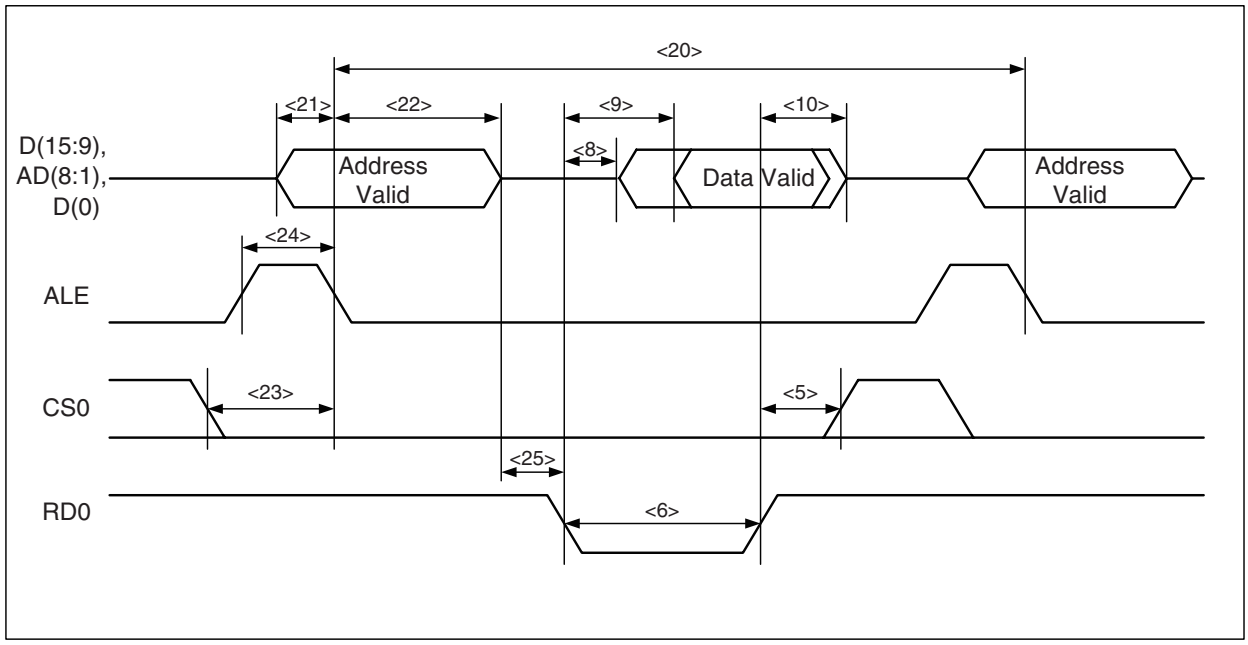
(1) PIO Read timing (Separate bus mode)



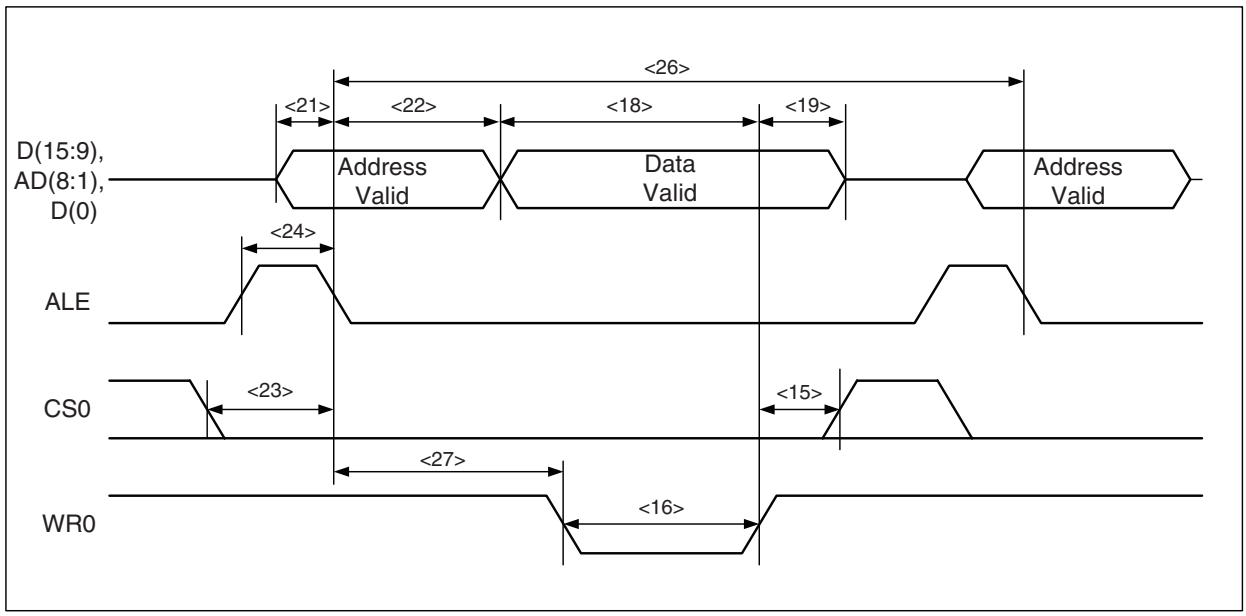
(2) PIO Write timing (Separate bus mode)



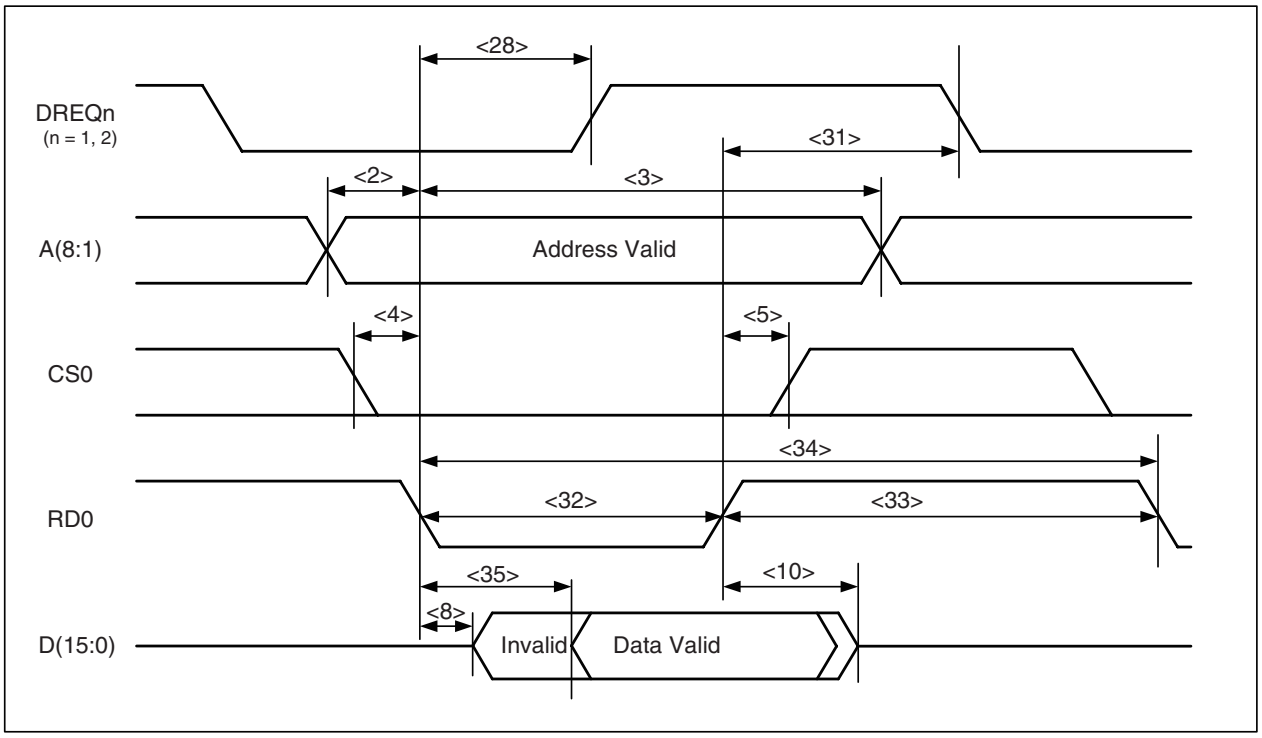
(3) PIO Read timing (Multiplex bus mode)



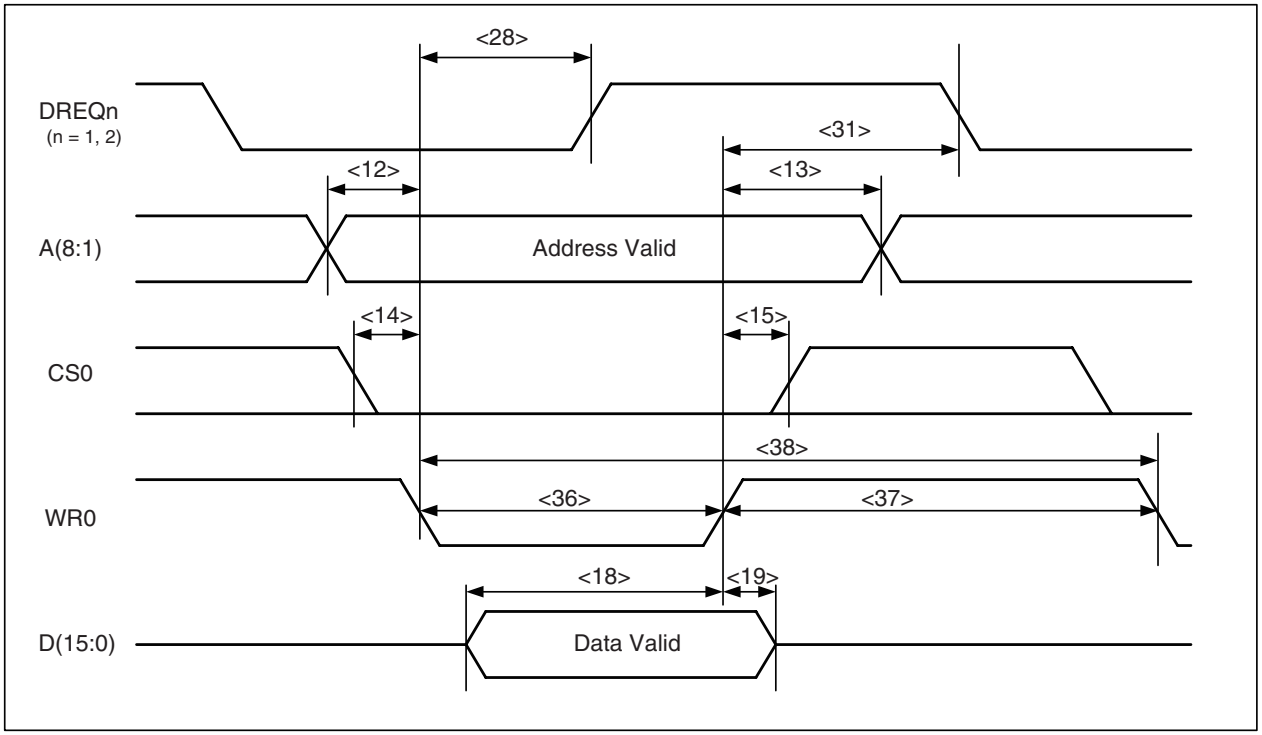
(4) PIO Write timing (Multiplex bus mode)



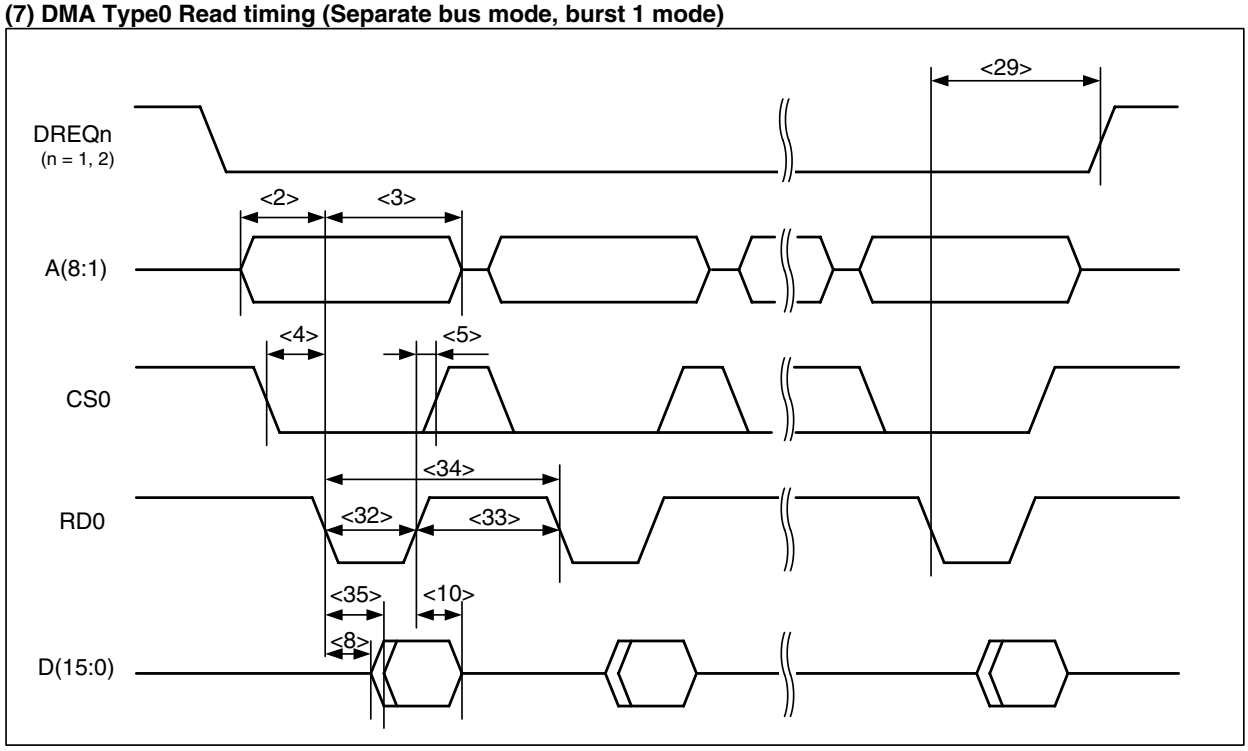
(5) DMA Type0 Read timing (Separate bus mode, single mode)



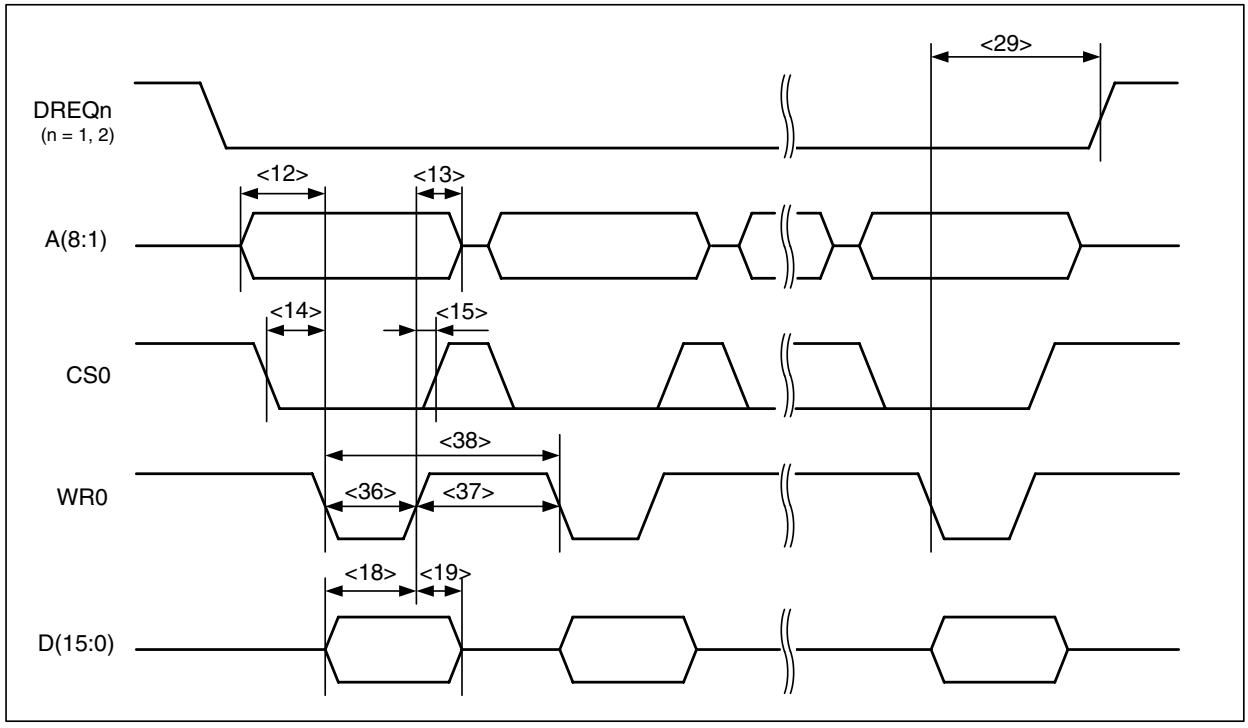
(6) DMA Type0 Read timing (Separate bus mode, single mode)



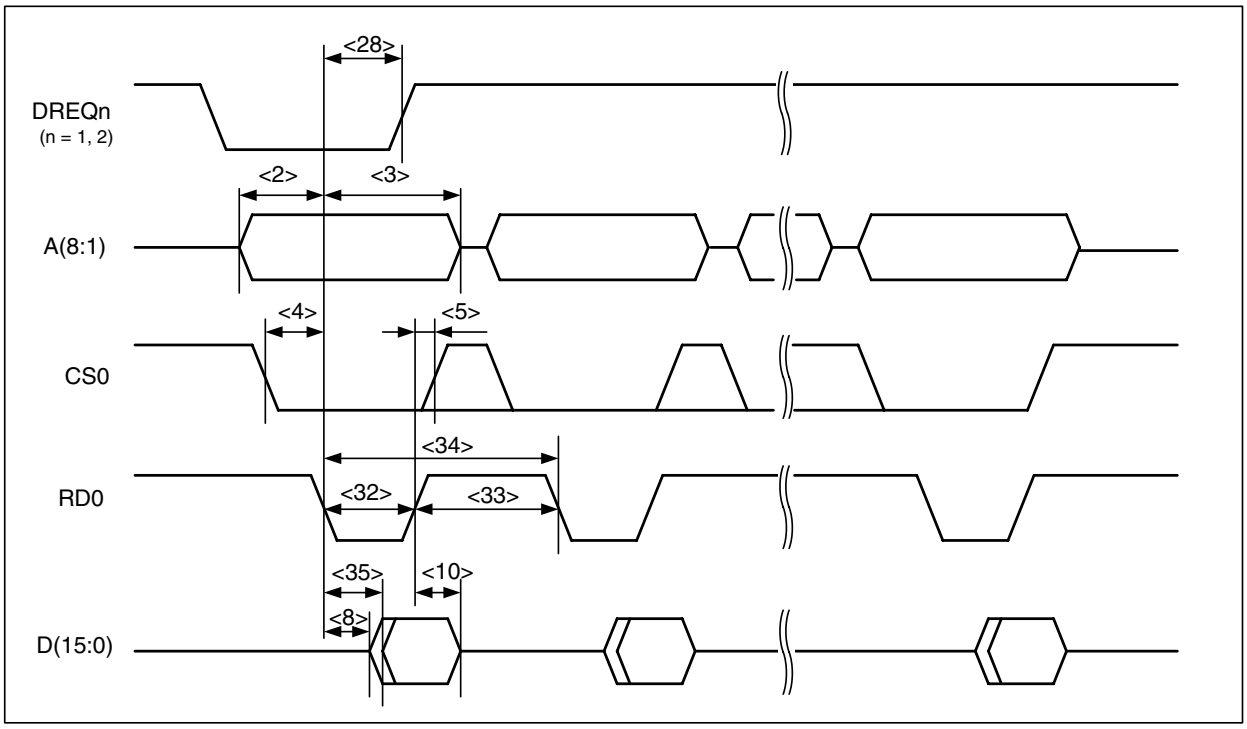
(7) DMA Type0 Read timing (Separate bus mode, burst 1 mode)



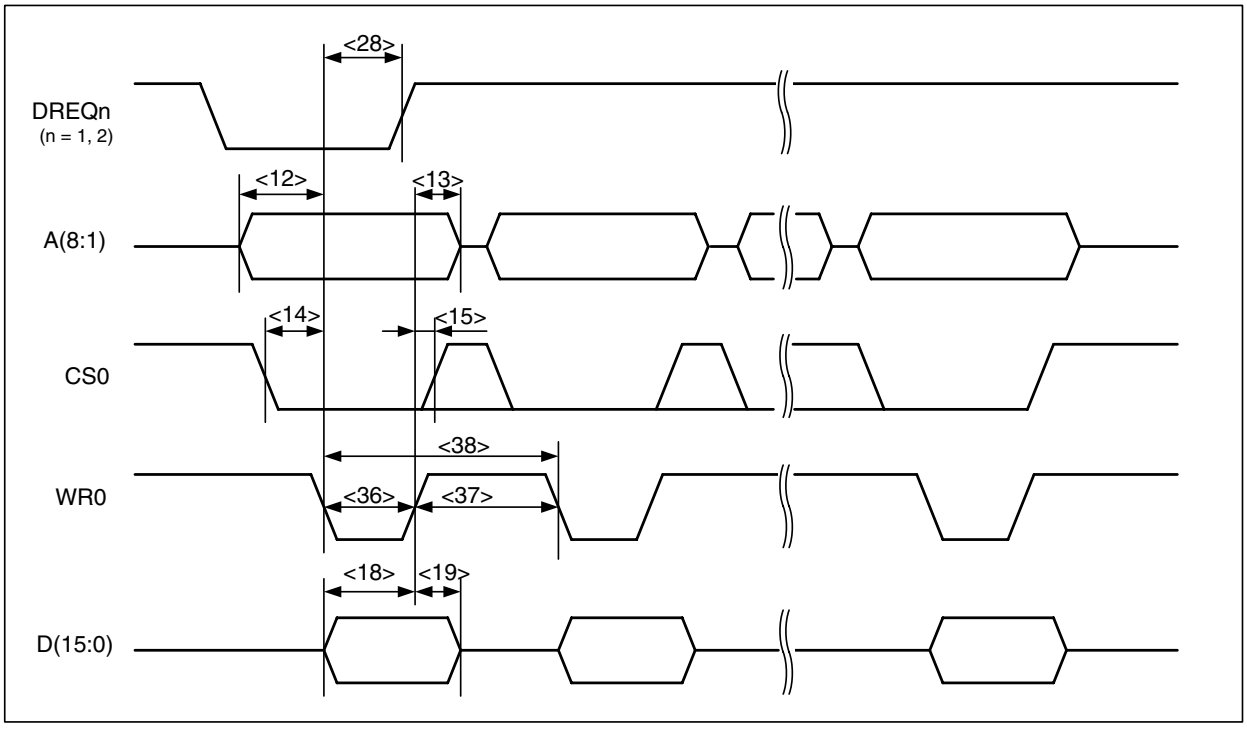
(8) DMA Type0 Write timing (Separate bus mode, burst 1 mode)



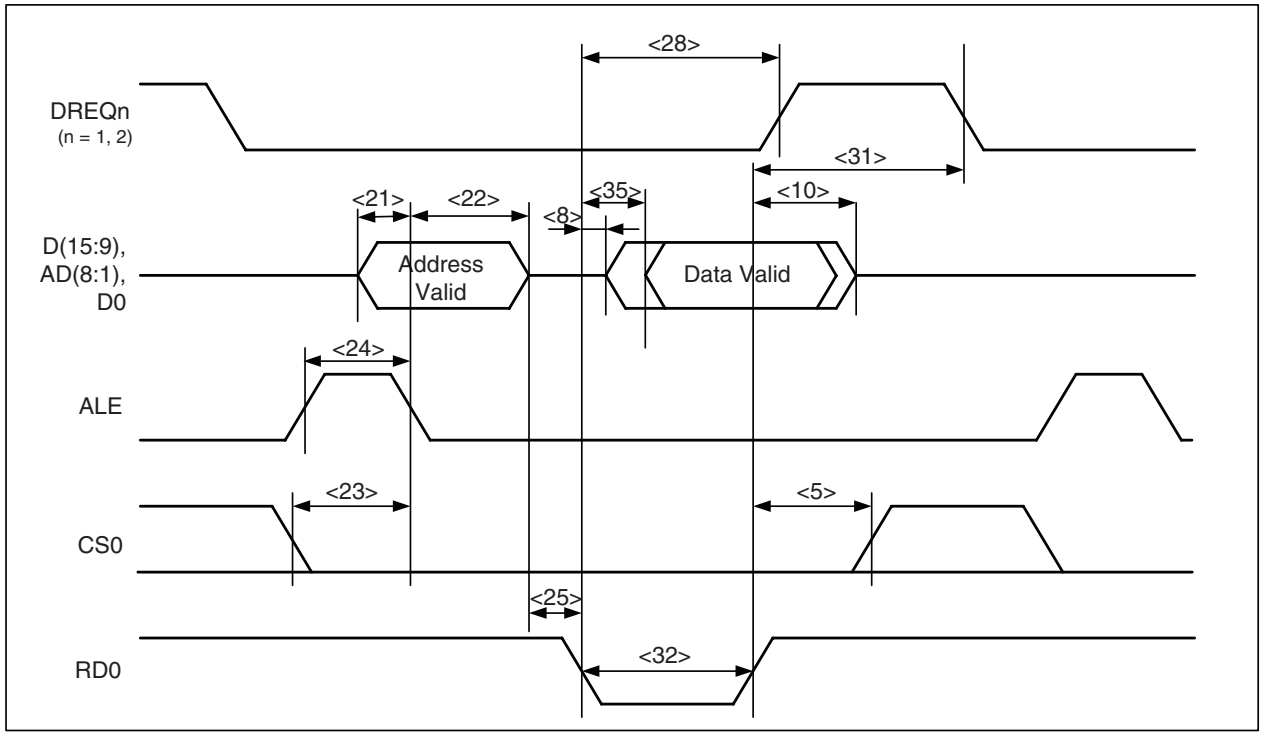
(9) DMA Type0 Read timing (Separate bus mode, burst 2 mode)



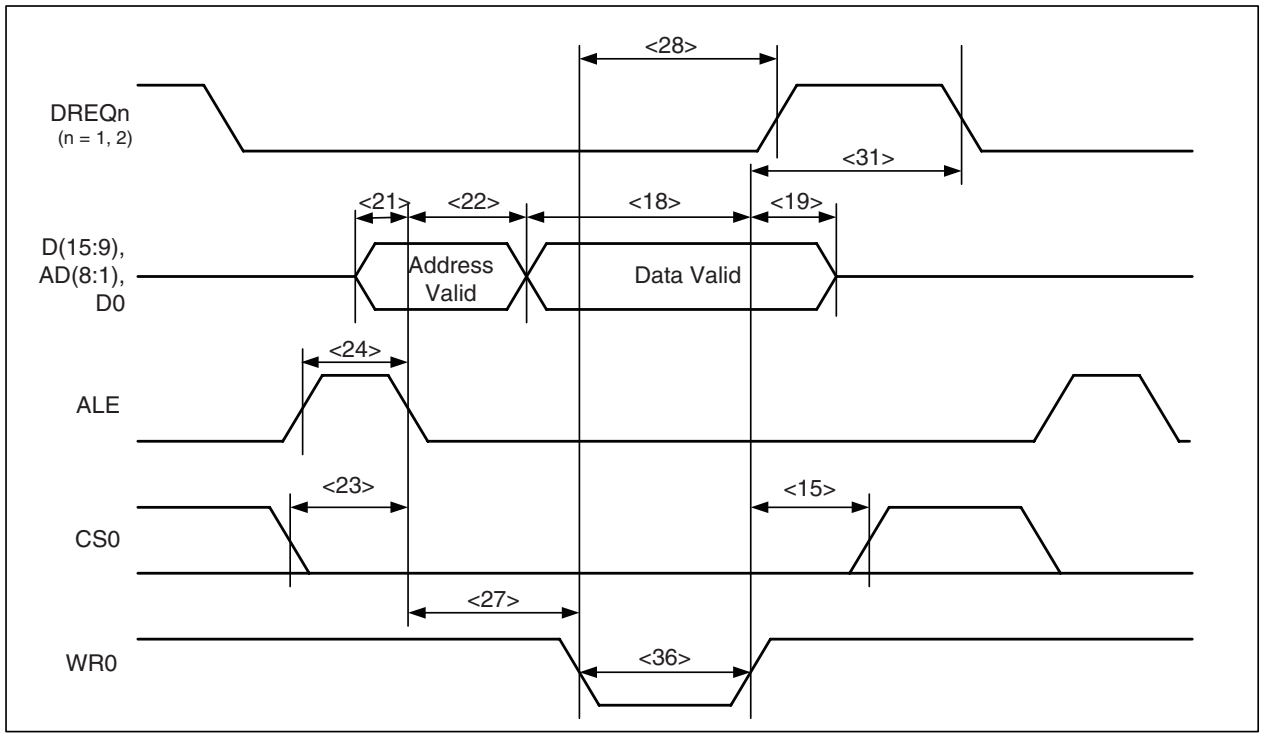
(10) DMA Type0 Write timing (Separate bus mode, burst 2 mode)



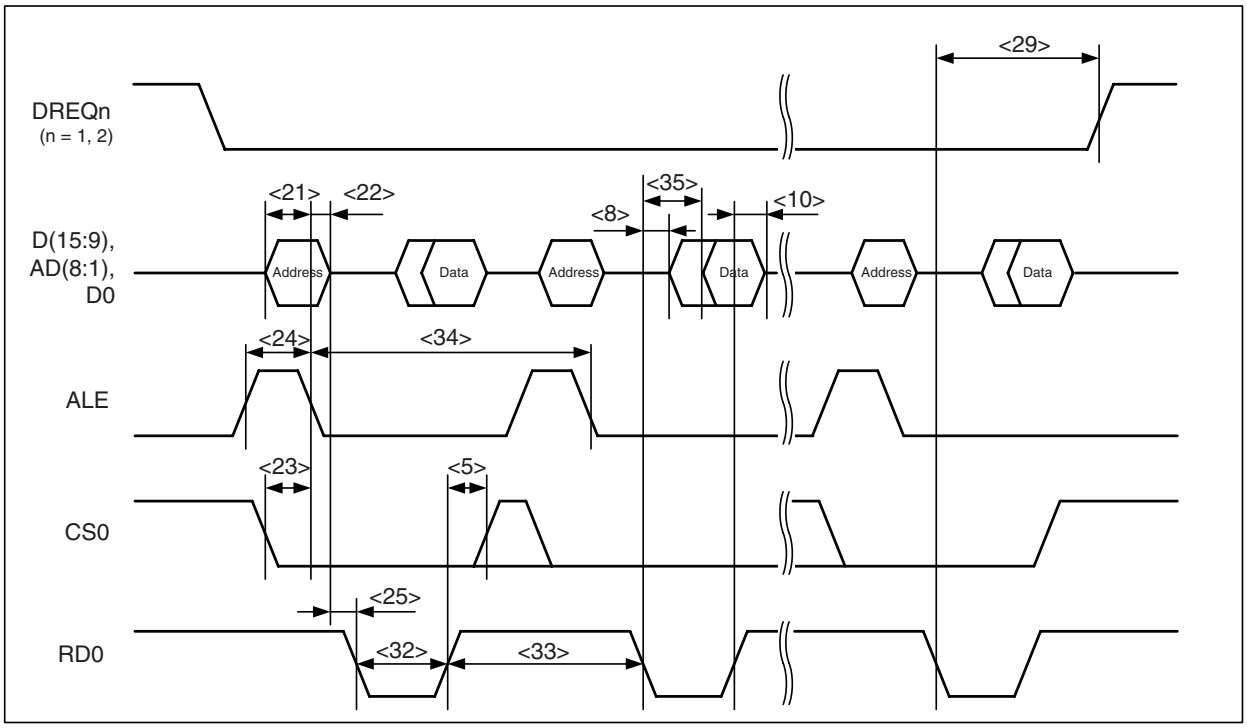
(11) DMA Type0 Read timing (Multiplex bus mode, single mode)



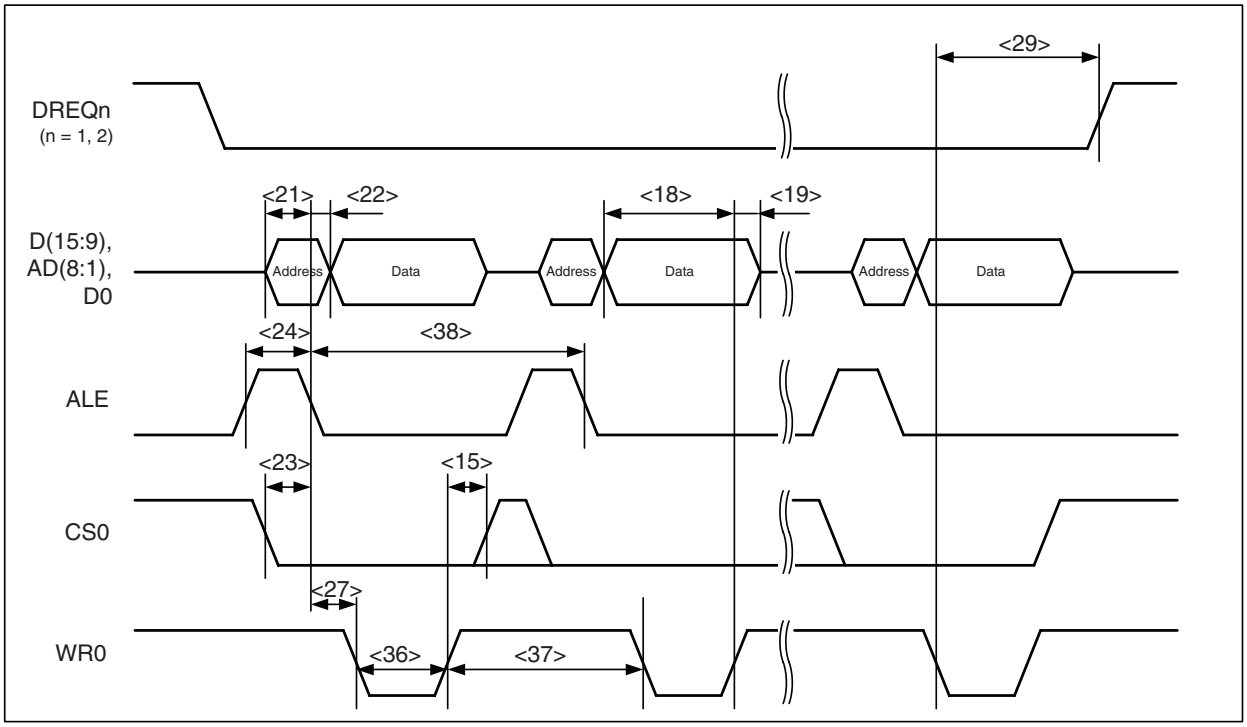
(12) DMA Type0 Write timing (Multiplex bus mode, single mode)



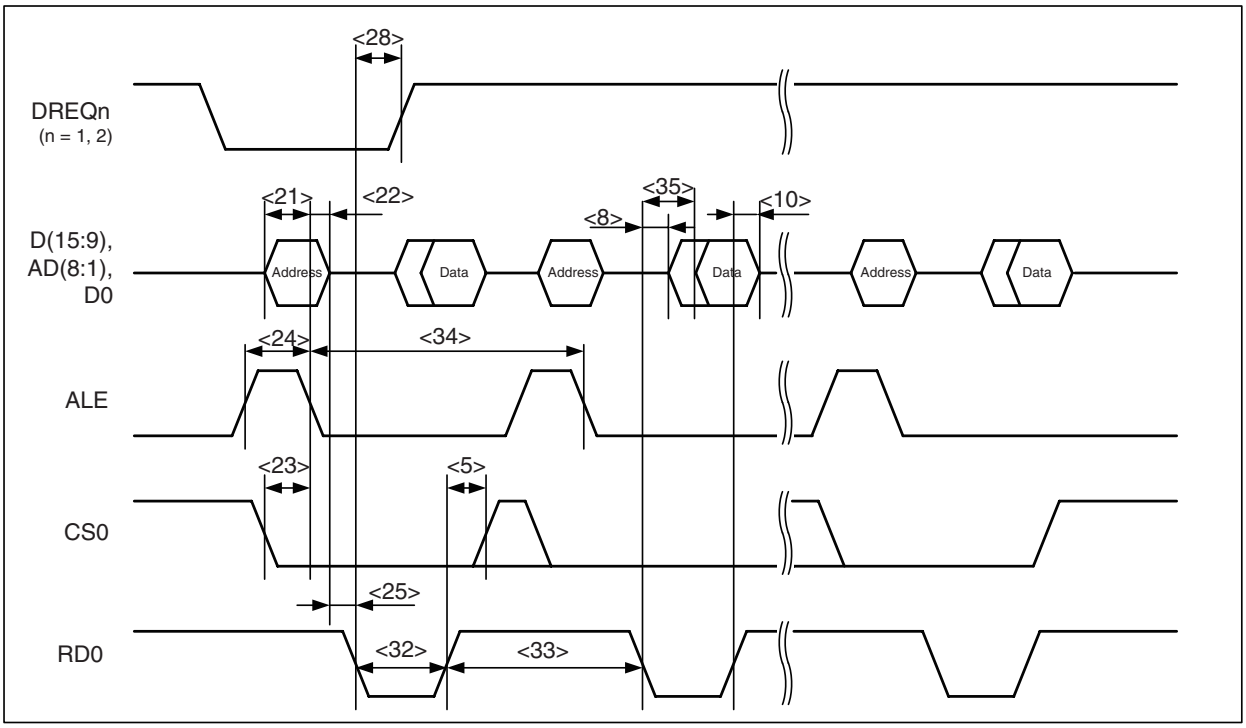
(13) DMA Type0 Read timing (Multiplex bus mode, burst 1 mode)



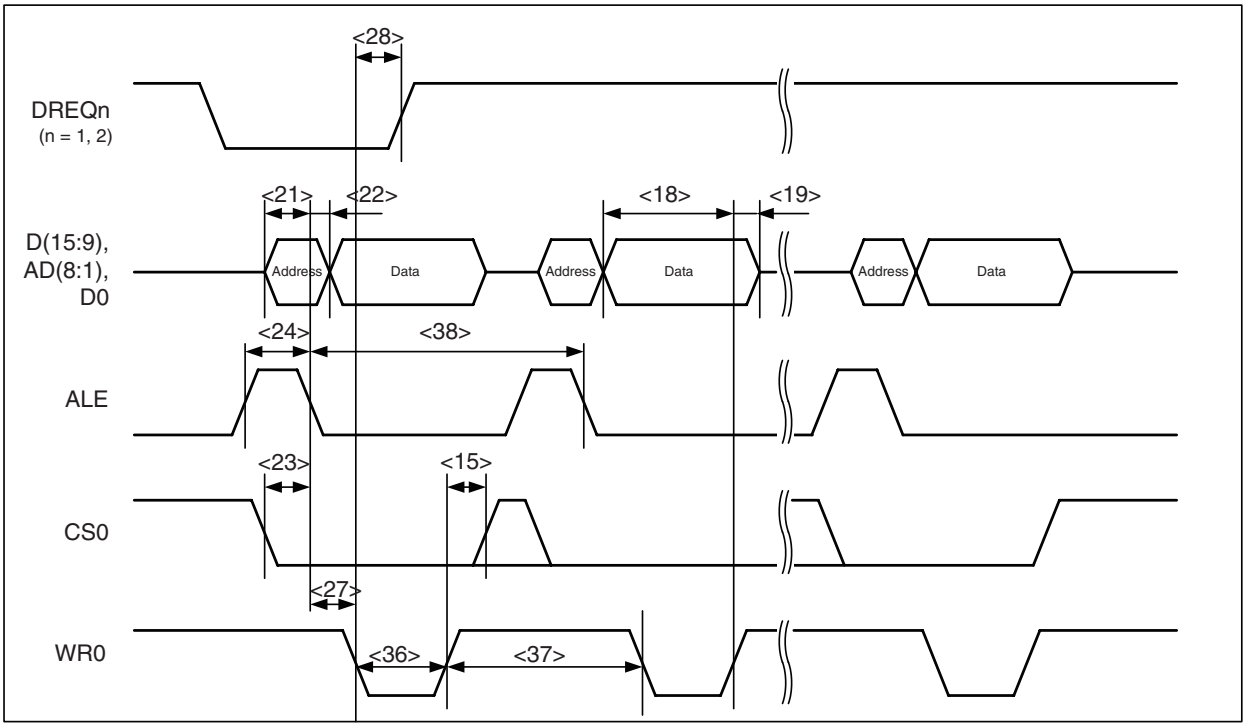
(14) DMA Type0 Write timing (Multiplex bus mode, burst 1 mode)



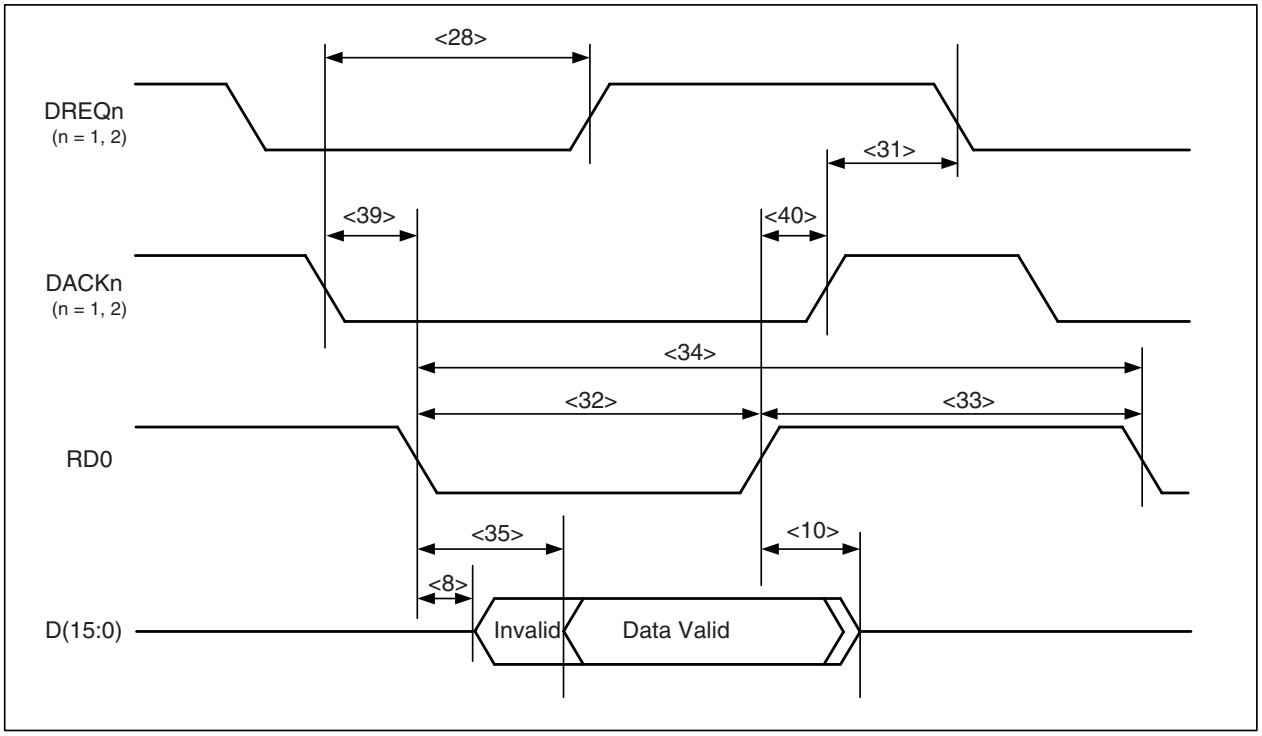
(15) DMA Type0 Read timing (Multiplex bus mode, burst 2 mode)



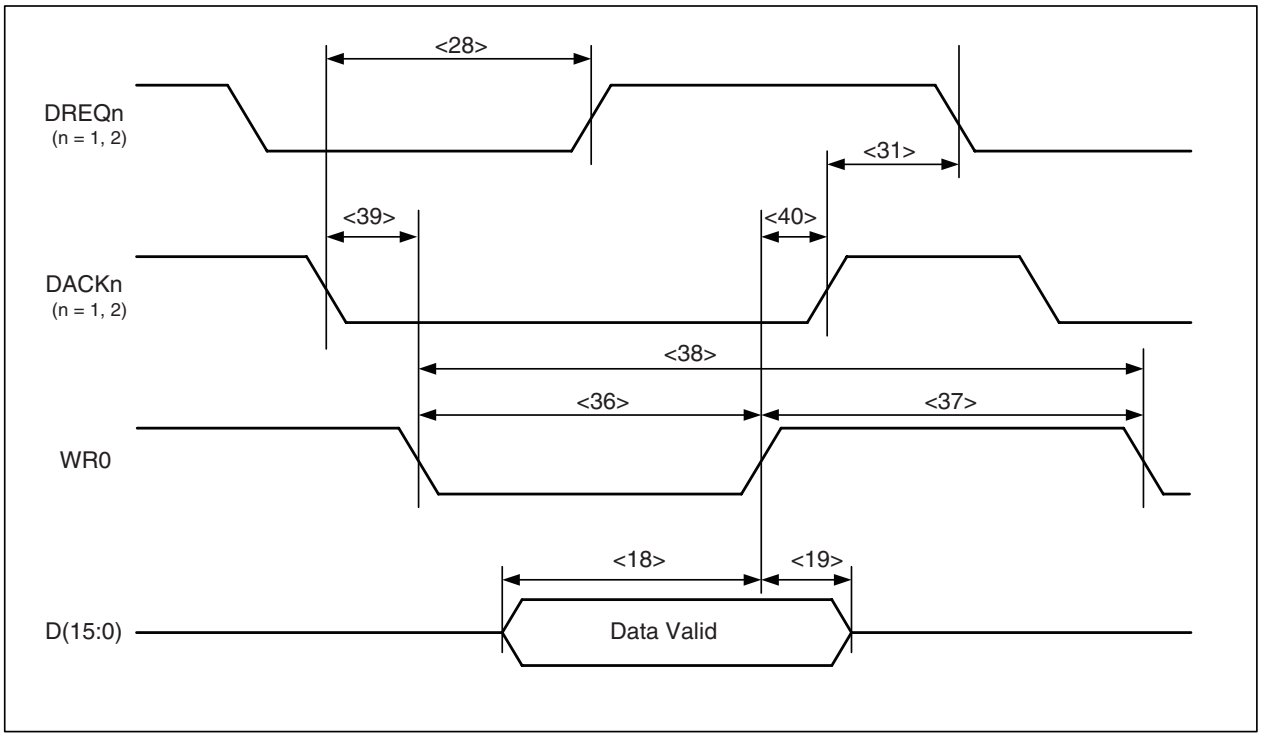
(16) DMA Type0 Write timing (Multiplex bus mode, burst 2 mode)



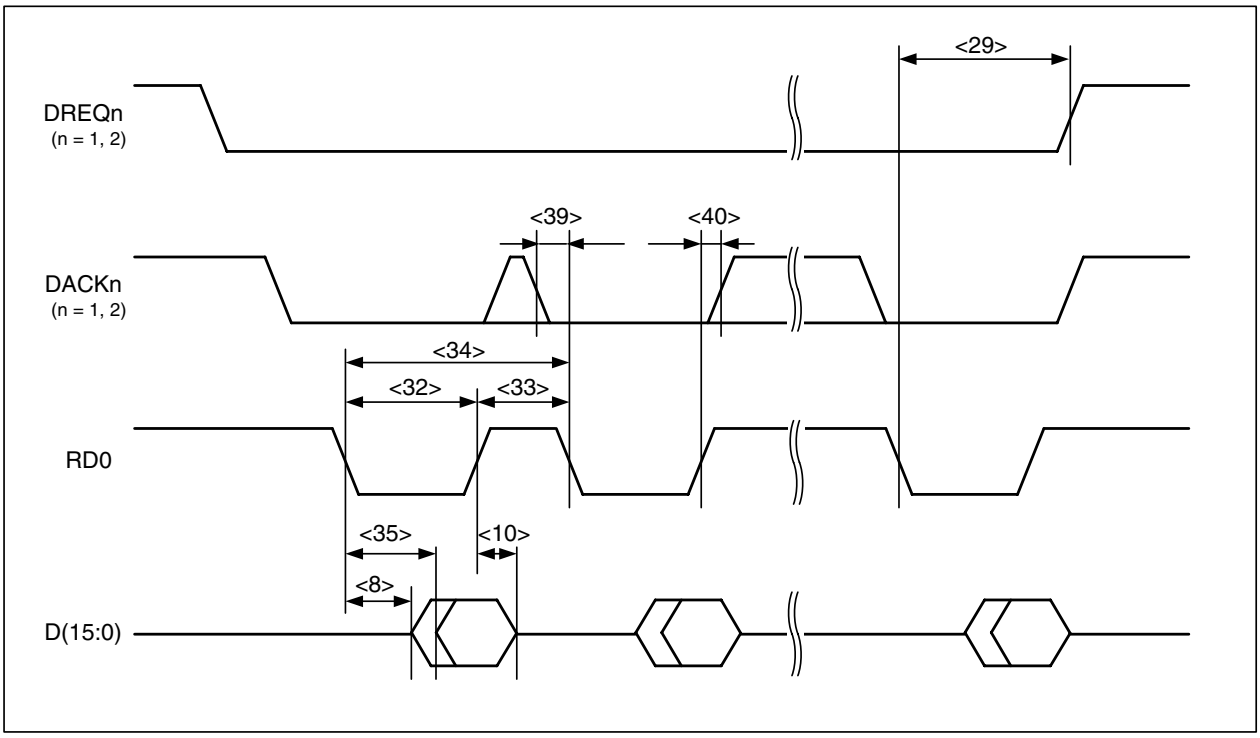
(17) DMA Type1 Read timing (single mode)



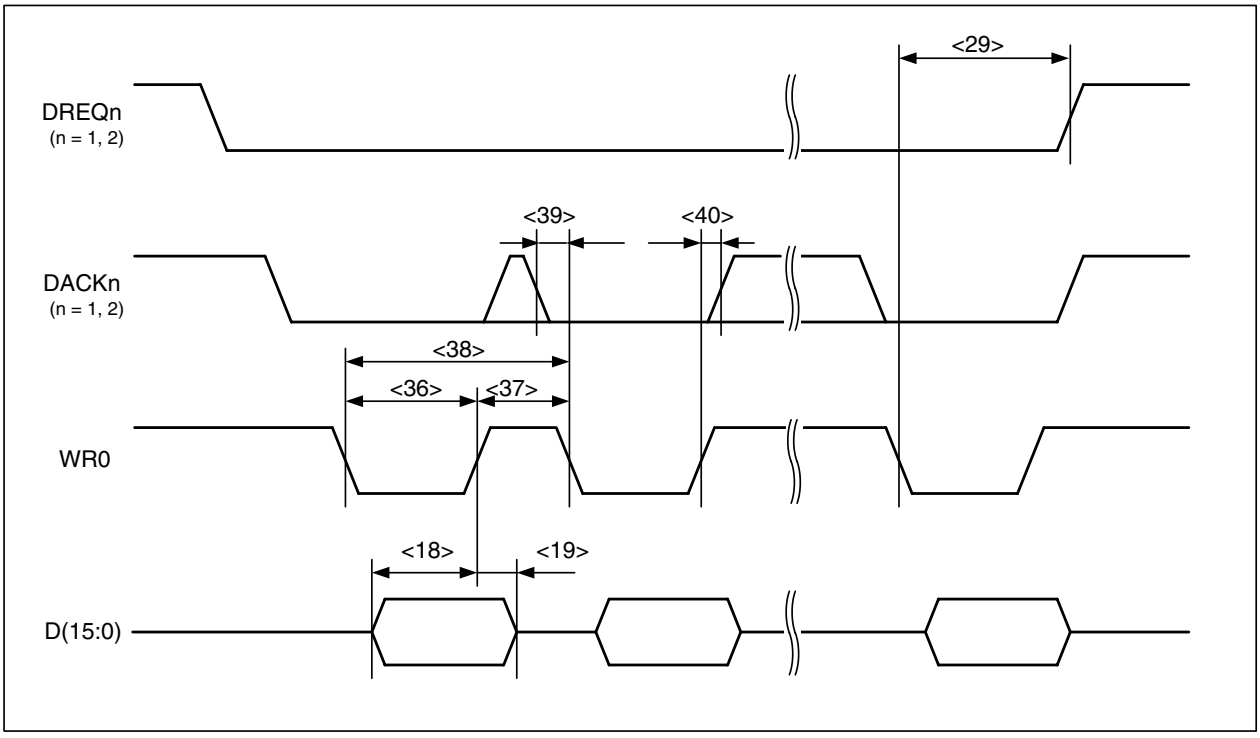
(18) DMA Type1 Write timing (single mode)



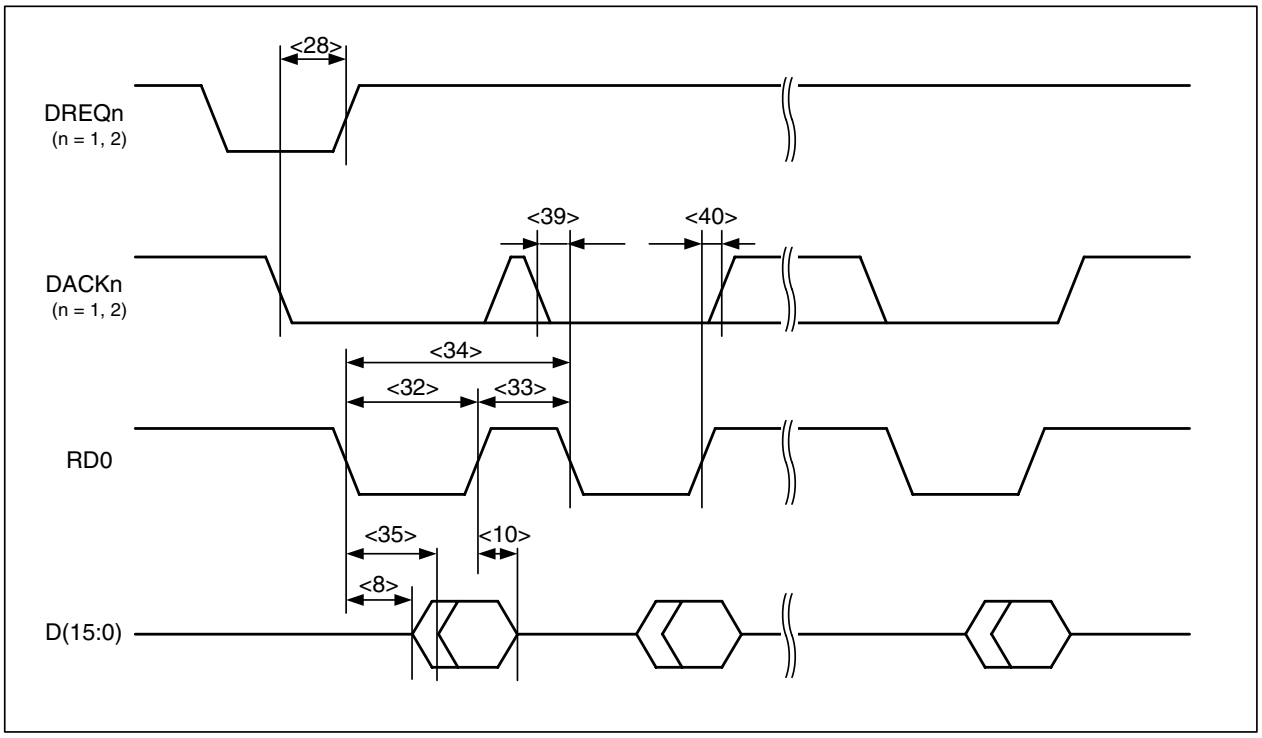
(19) DMA Type1 Read timing (burst 1 mode)



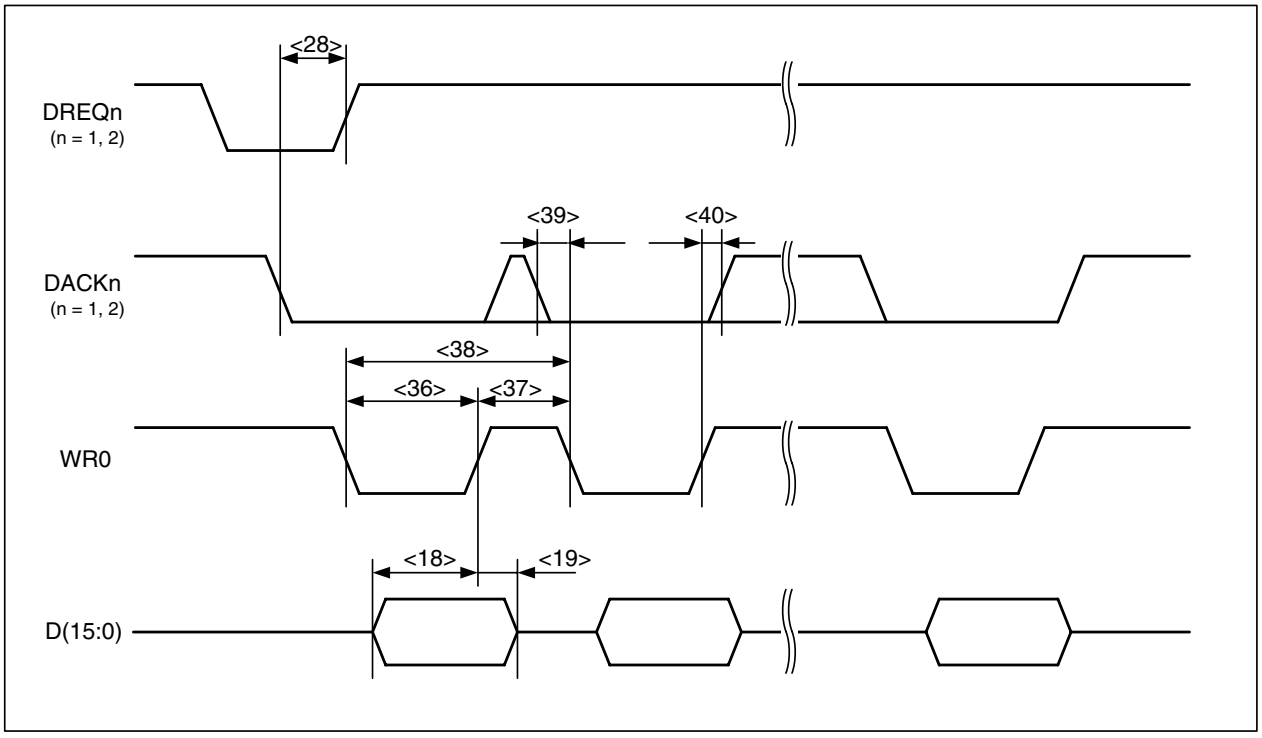
(20) DMA Type1 Write timing (burst 1 mode)



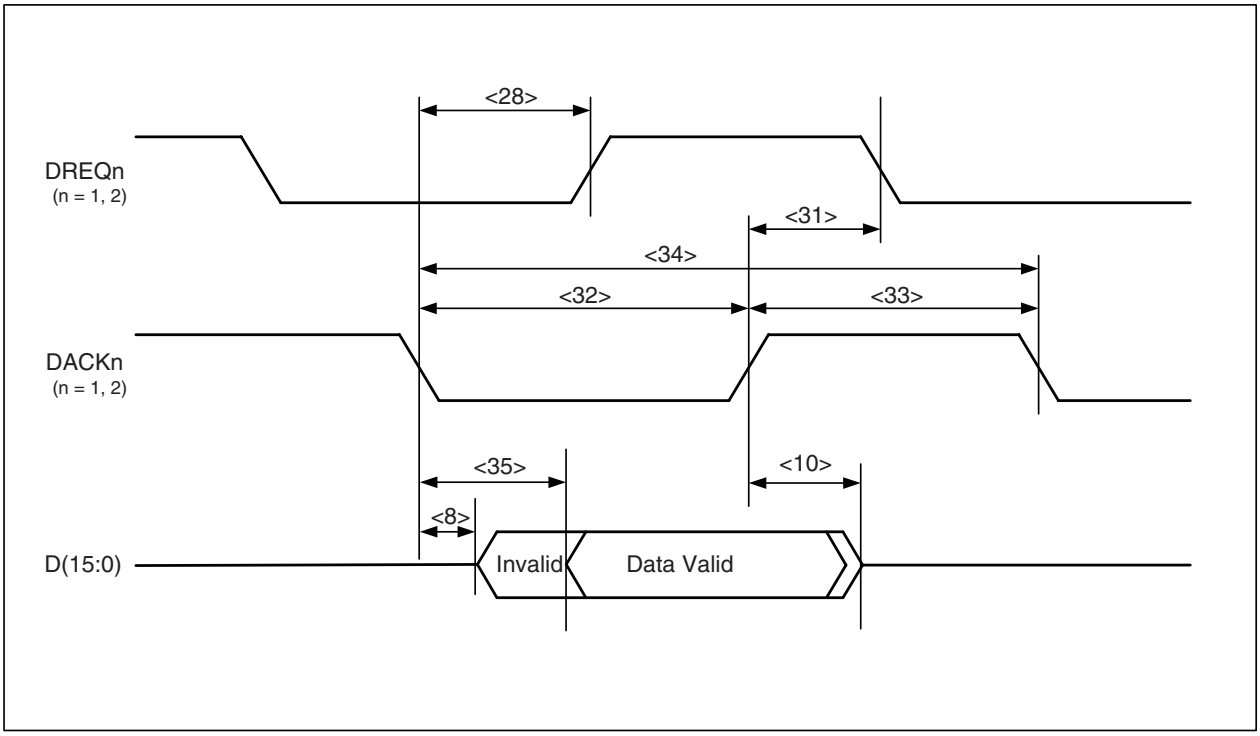
(21) DMA Type1 Read timing (burst 2 mode)



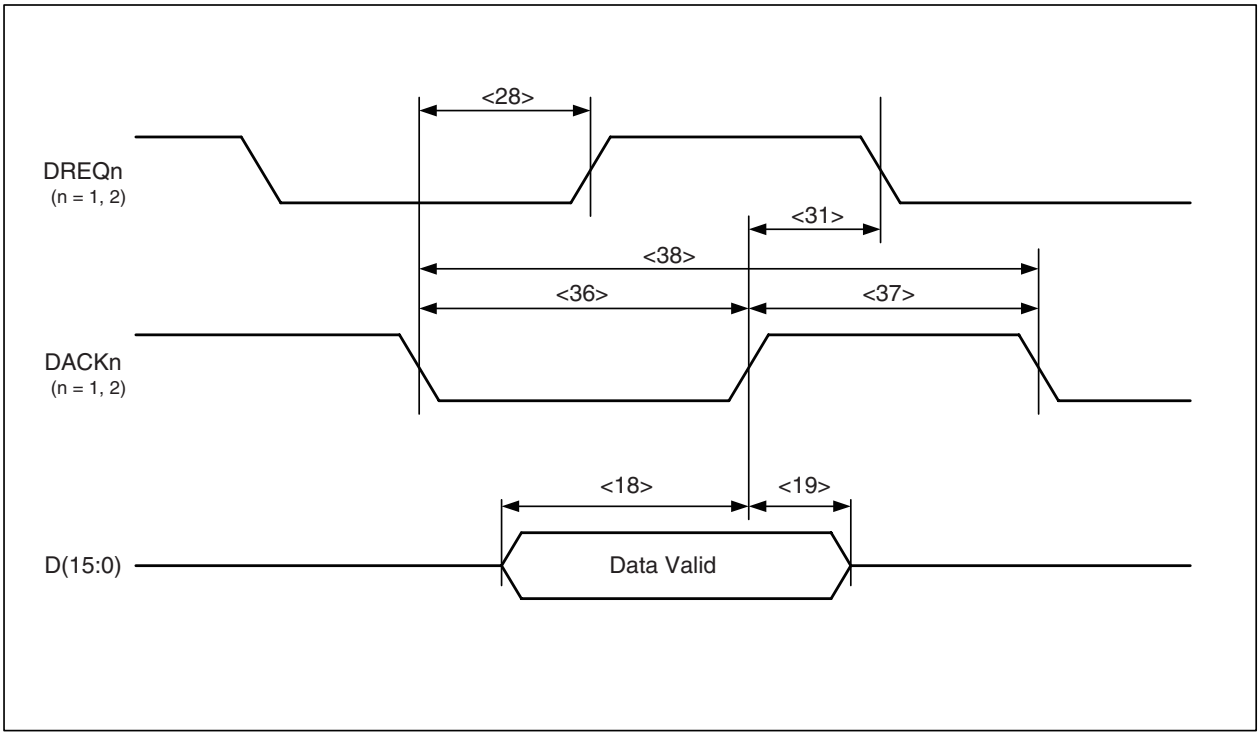
(22) DMA Type1 Write timing (burst 2 mode)



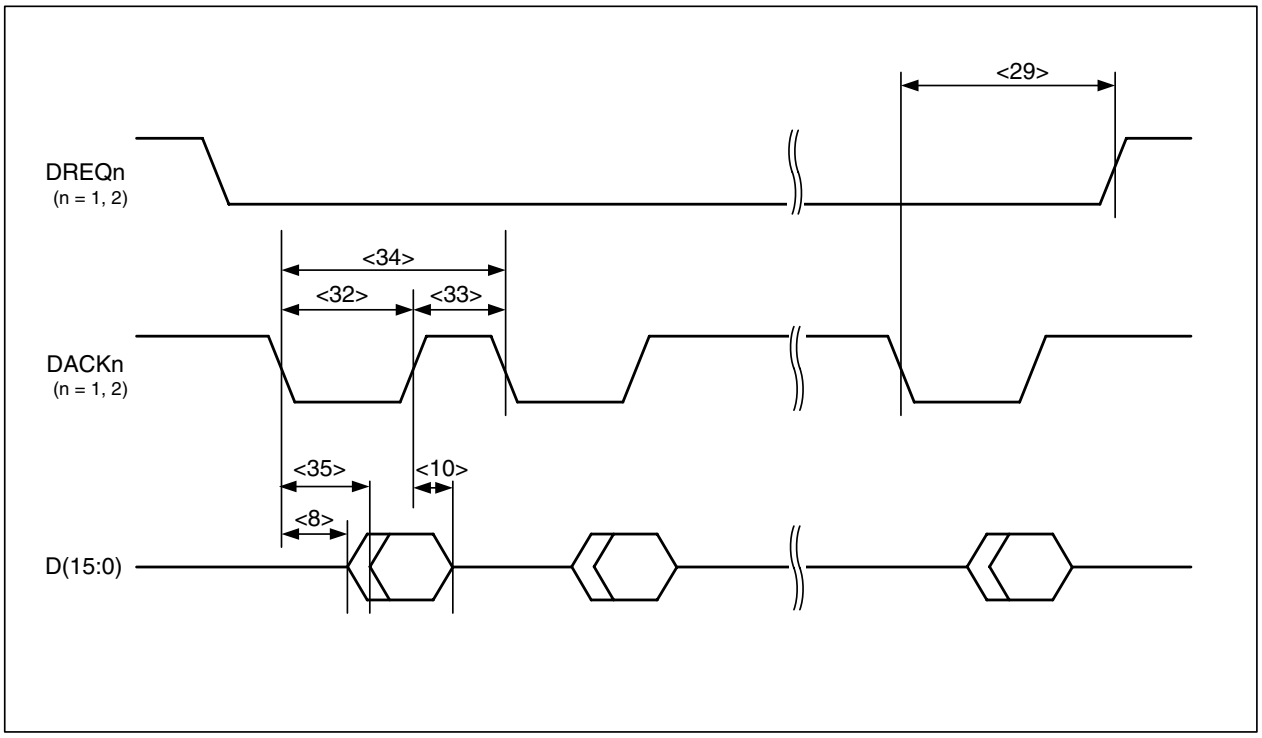
(23) DMA Type2 Read timing (single mode)



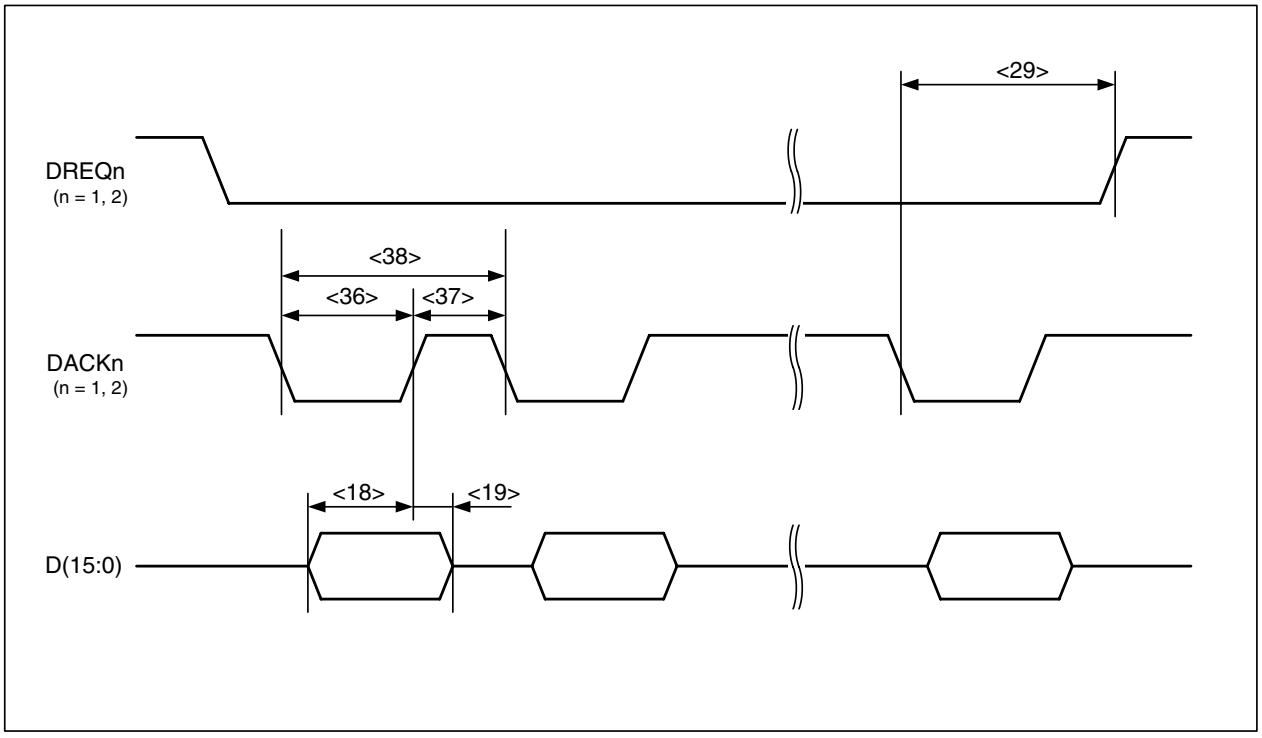
(24) DMA Type2 Write timing (single mode)



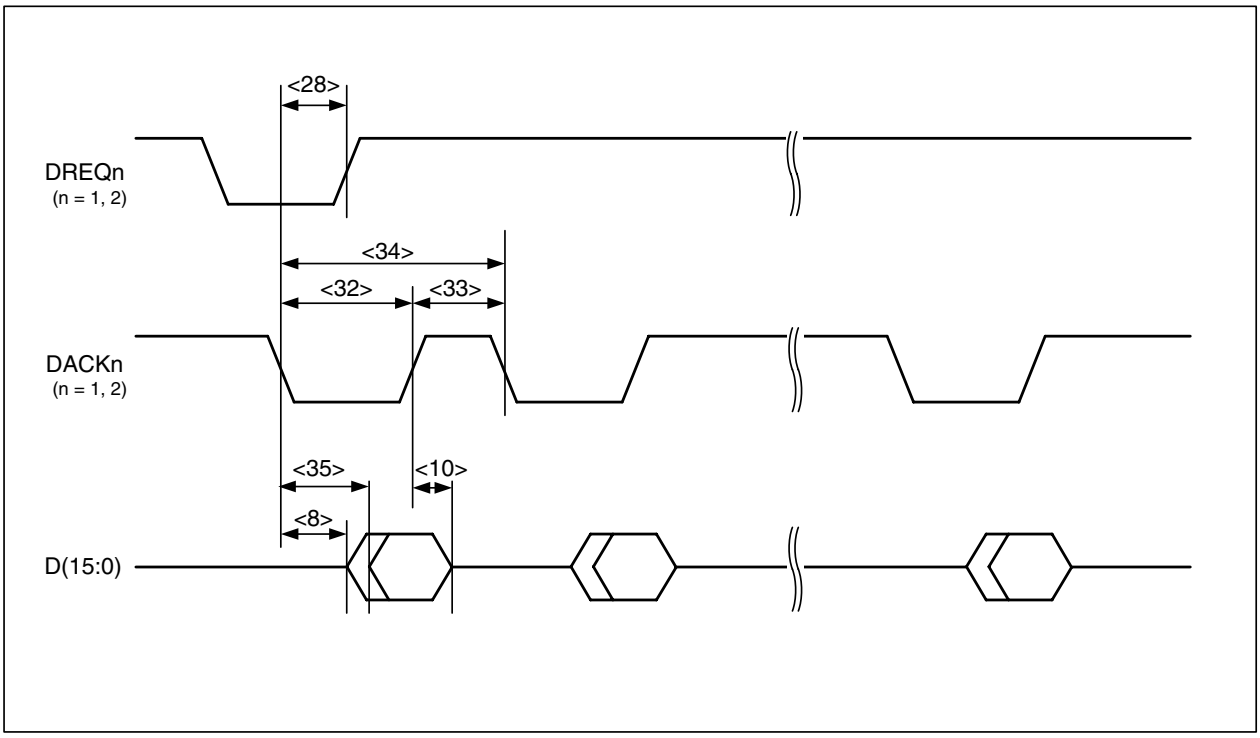
(25) DMA Type2 Read timing (burst 1 mode)



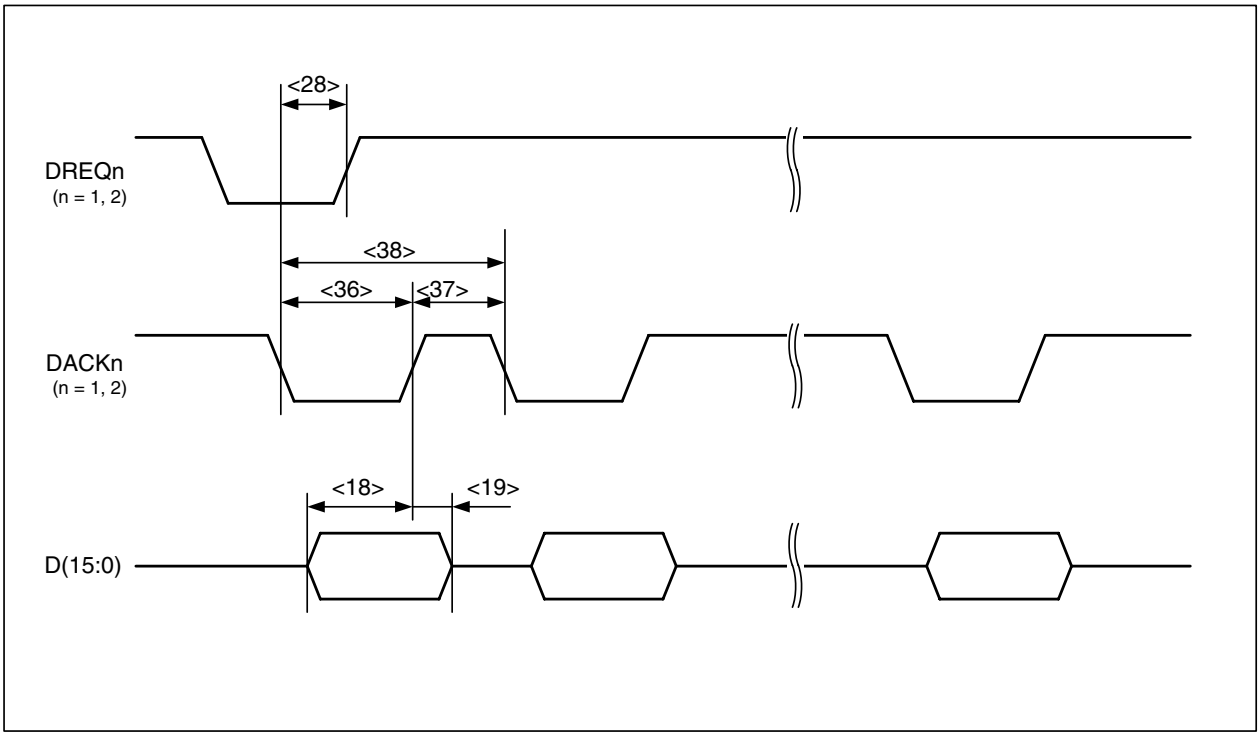
(26) DMA Type2 Write timing (burst 1 mode)



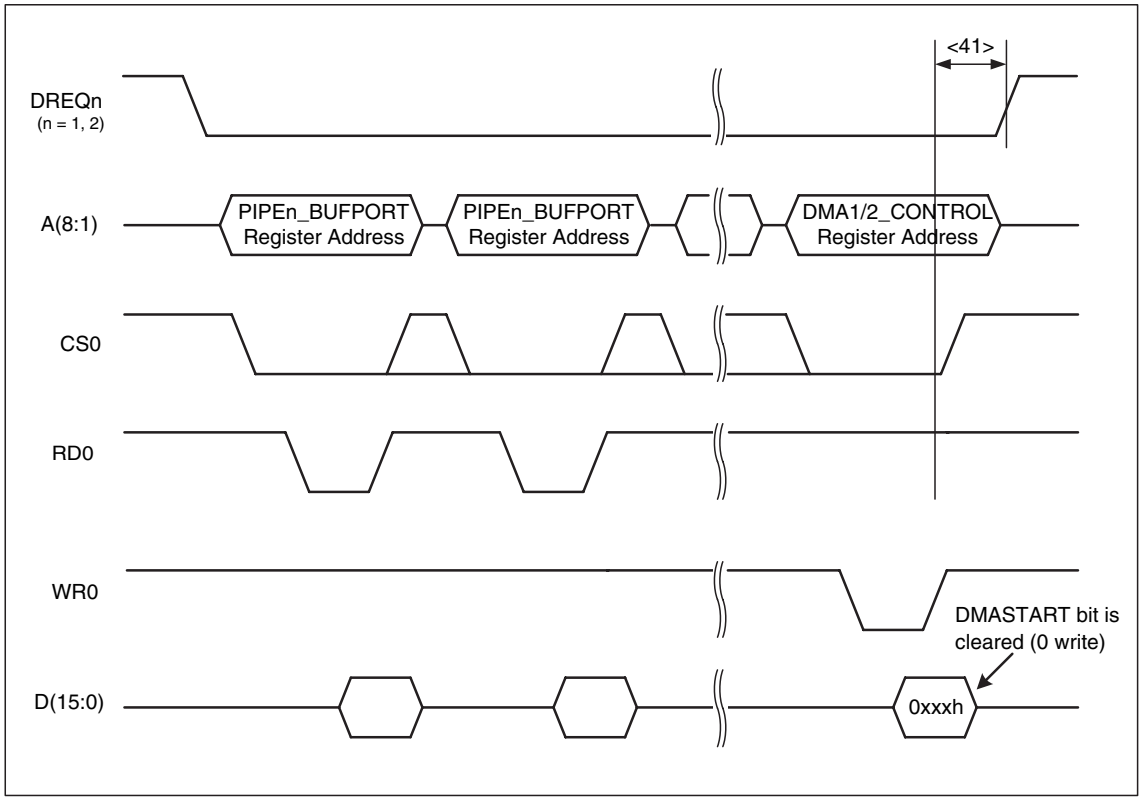
(27) DMA Type2 Read timing (burst 2 mode)



(28) DMA Type2 Write timing (burst 2 mode)

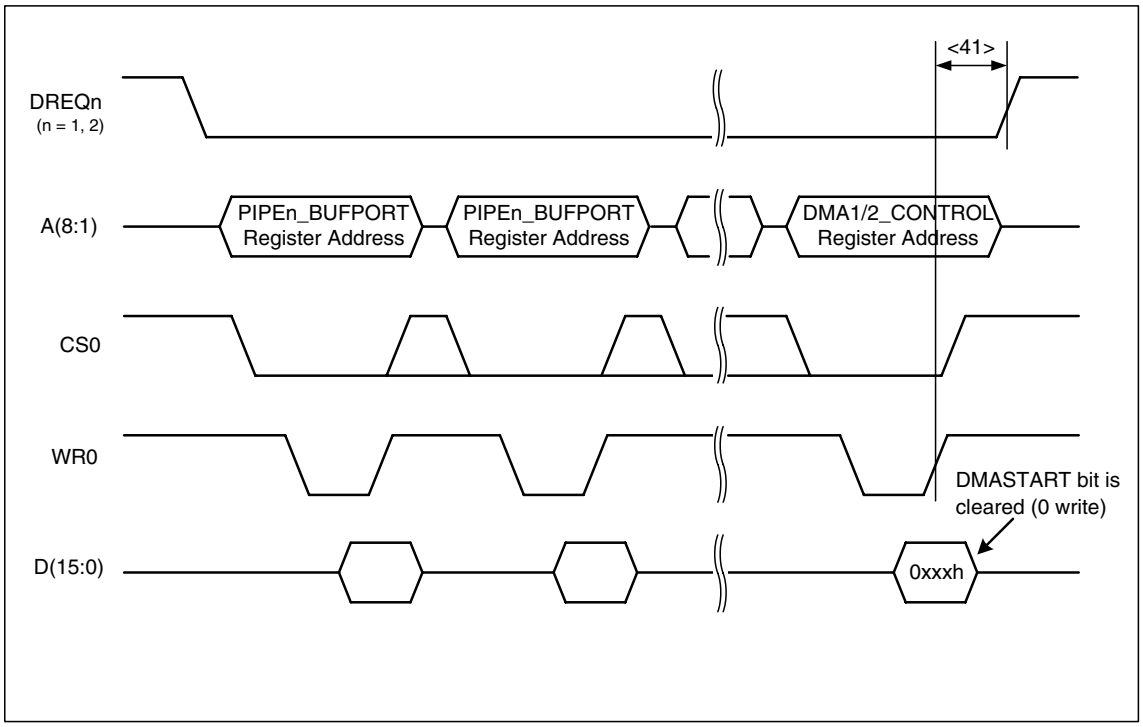


(29) DMA Read timing (burst 1 mode, forced DMA termination)



Remark This is the example in Type0 (separate bus mode).

(30) DMA Write timing (burst 1 mode, forced DMA termination)



Remark This is the example in Type0 (separate bus mode).

3.6.4 USB Interface

(1/3)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{LR}	C_L = 200 to 600 pF,	75	300	ns
Fall time (90 to 10%)	t_{LF}	C_L = 200 to 600 pF,	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF})	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Source jitter total (including frequency tolerance): To next transition For paired transitions	 t_{DDJ1} t_{DDJ2}		 −25 −14	 +25 +14	 ns ns
Source jitter for differential transition to SE0 transition	t_{LDEOP}		−40	+100	ns
Receiver jitter: To next transition For paired transitions	 t_{UJR1} t_{UJR2}		 −152 −200	 +152 +200	 ns ns
Source SE0 interval of EOP	t_{LEOPT}		1.25	1.50	μs
Receiver SE0 interval of EOP	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{FST}			210	ns
Full-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{FR}	C_L = 50 pF	4	20	ns
Fall time (90 to 10%)	t_{FF}	C_L = 50 pF	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance): To next transition For paired transitions	 t_{DJ1} t_{DJ2}		 −3.5 −4.0	 +3.5 +4.0	 ns ns
Source jitter for differential transition to SE0 transition	t_{FDEOP}		−2	+5	ns
Receiver jitter: To next transition For paired transitions	 t_{JR1} t_{JR2}		 −18.5 −9	 +18.5 +9	 ns ns
Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(2/3)

Parameter	Symbol	Conditions	Min.	Max.	Unit
High-speed Source Electrical Characteristics					
Rise time (10 to 90%)	t_{HSR}		500		ps
Fall time (90 to 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 3–4**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 3–4**.				
Receiver jitter tolerance	See **Figure 3–2**.				
Hub Event Timings					
Time to detect a downstream facing port connect event	t_{DCNN}		2.5	2000	μs
Time to detect a disconnect event at a hub's downstream facing port	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port	t_{DRSMDN}	Nominal	20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Inter-packet delay for packets traveling in same direction for high-speed	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay for packets traveling in opposite direction for high-speed	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for root hub response for high-speed	$t_{HSRSPIPD1}$			192	Bit times
Time for which a Chirp J or Chirp K must be continuously detected during reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs

(3/3)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Device Event Timings					
Time from internal power good to device pulling D+ beyond V_{IHZ} (min.) (signaling attached)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	t_{ATTDB}			100	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
Time for which a suspended highspeed capable device must see a continuous SE0 before beginning the high-speed detection handshake	$t_{FILTSE0}$		2.5		μs
Time a high-speed capable device operating in non-suspended fullspeed must wait after start of SE0 before beginning the high-speed detection handshake	$t_{WTRSTFS}$		2.5	3000	μs
Time a high-speed capable device operating in high-speed must wait after start of SE0 before reverting to full-speed	t_{WTREV}		3.0	3.125	ms
Time a device must wait after reverting to full-speed before sampling the bus state for SE0 and beginning the high-speed detection handshake	$t_{WTRSTHS}$		100	875	μs
Minimum duration of a Chirp K from a high-speed capable device within the reset protocol	t_{UCH}		1.0		ms
Time after start of SE0 by which a high-speed capable device is required to have completed its Chirp K within the reset protocol	t_{UCHEND}			7.0	ms
Time between detection of downstream chirp and entering high-speed state	t_{WTHS}			500	μs
Time after end of upstream chirp at which device reverts to fullspeed default state if no downstream chirp is detected	t_{WTFS}		1.0	2.5	ms

Figure 3–4. Transmit Waveform for Transceiver at DP/DM

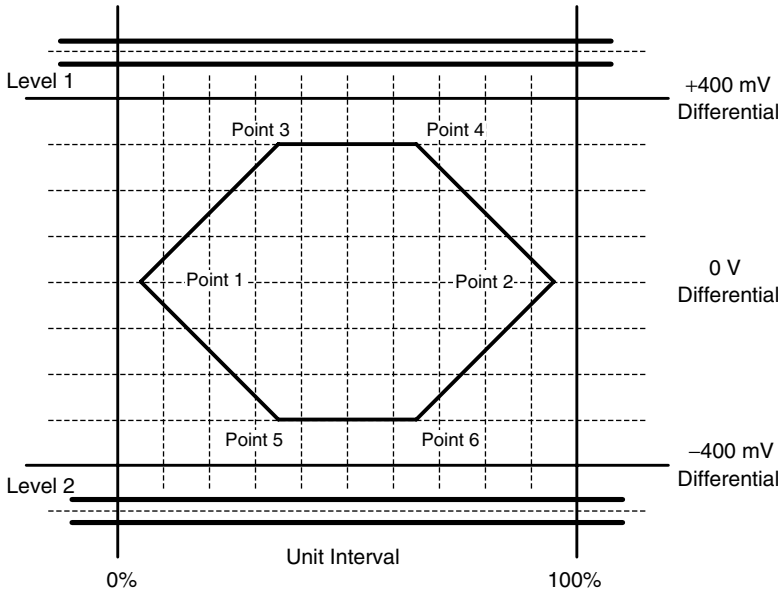
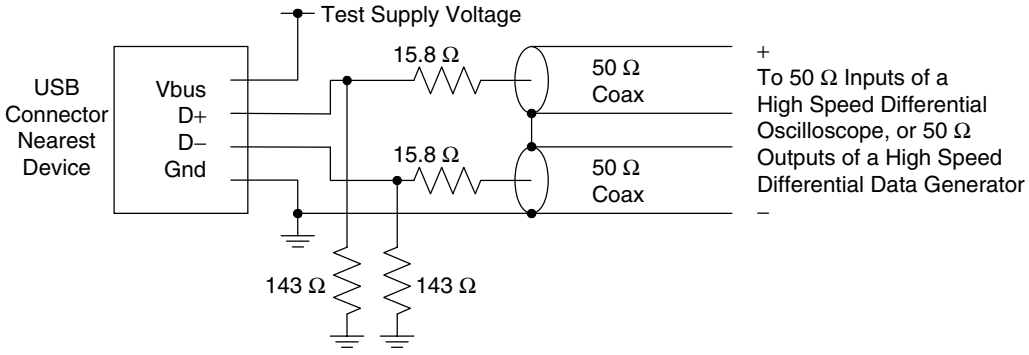
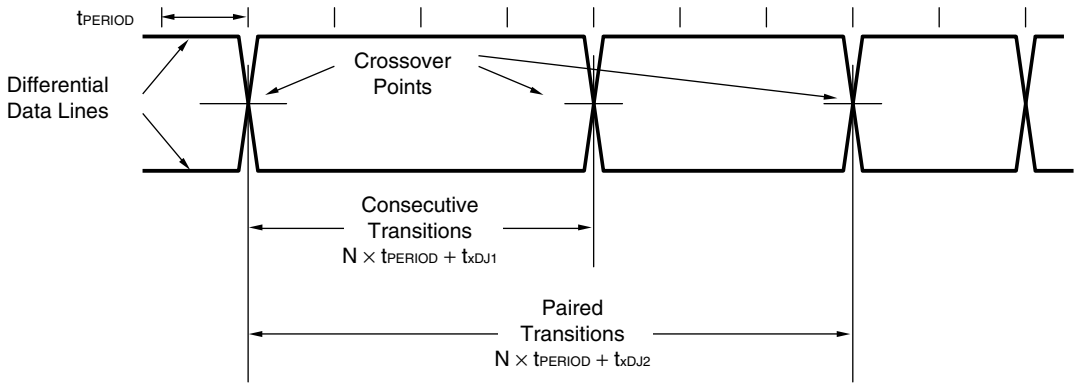


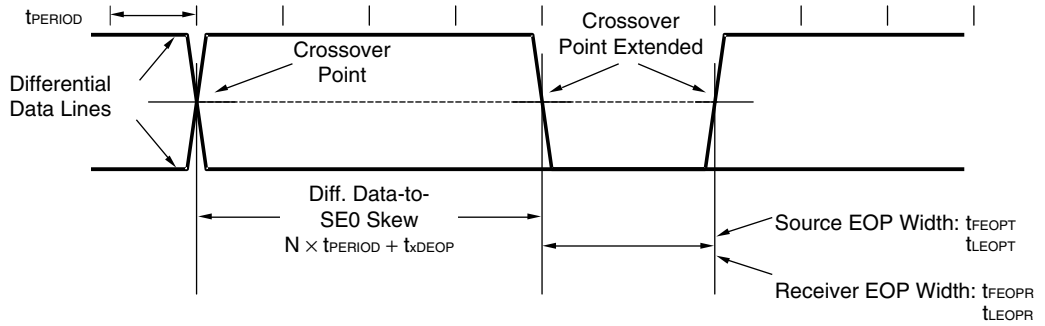
Figure 3–5. Transmitter Measurement Fixtures



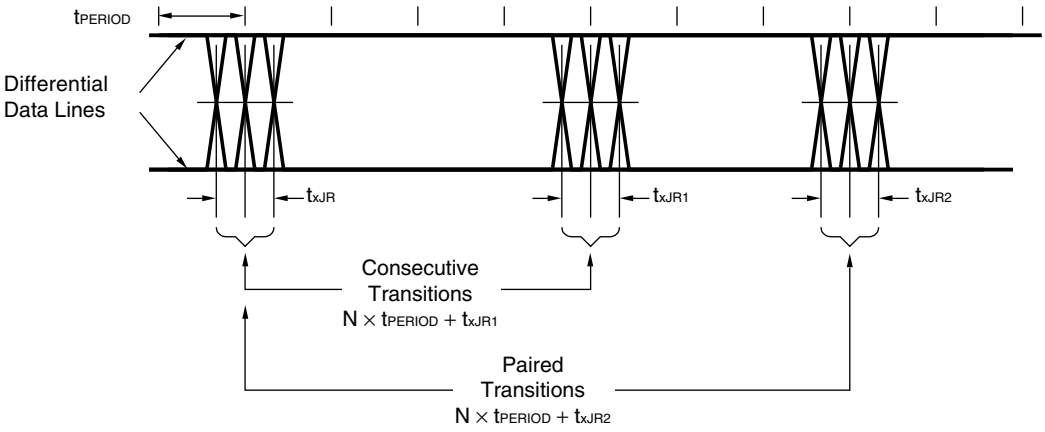
USB differential data jitter for full-speed



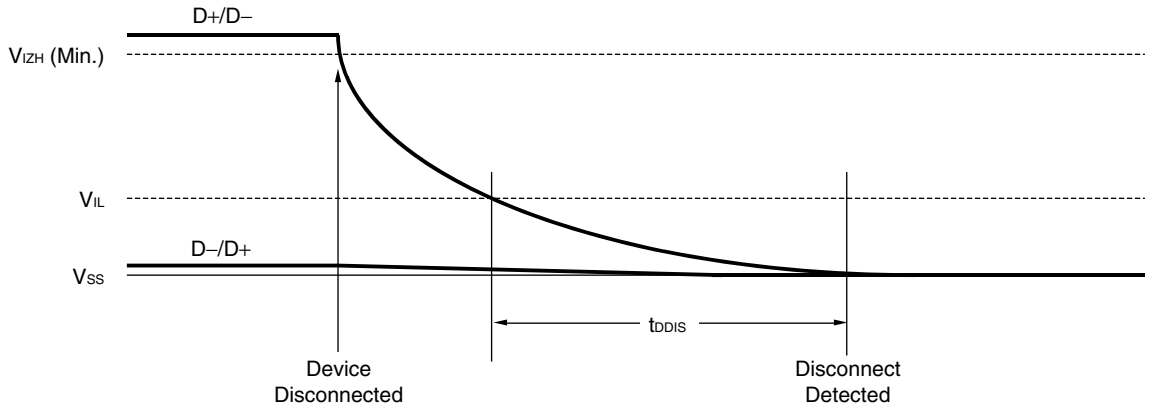
USB differential-to-EOP transition skew and EOP width for low-/full-speed



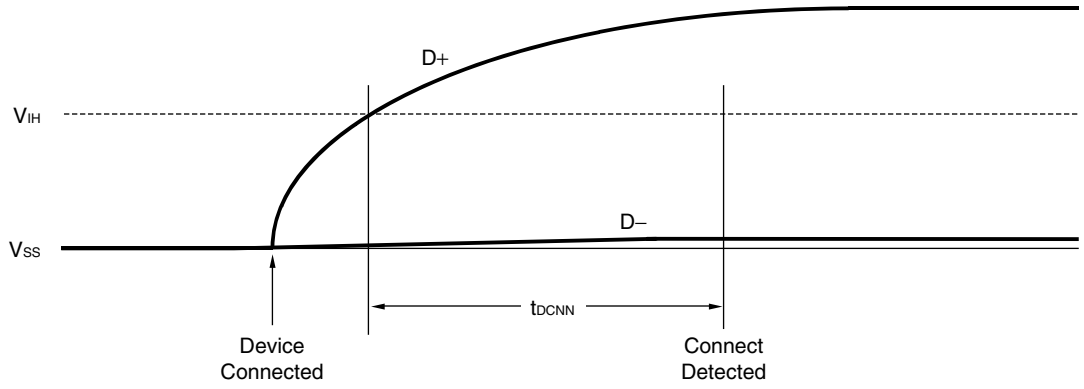
USB receiver jitter tolerance for low-/full-speed



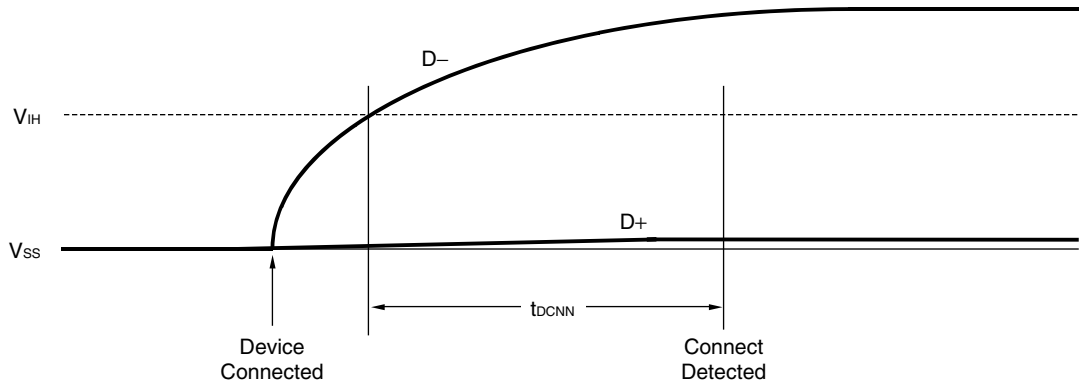
Low-/full-speed disconnect detection



Full-/high-speed device connect detection



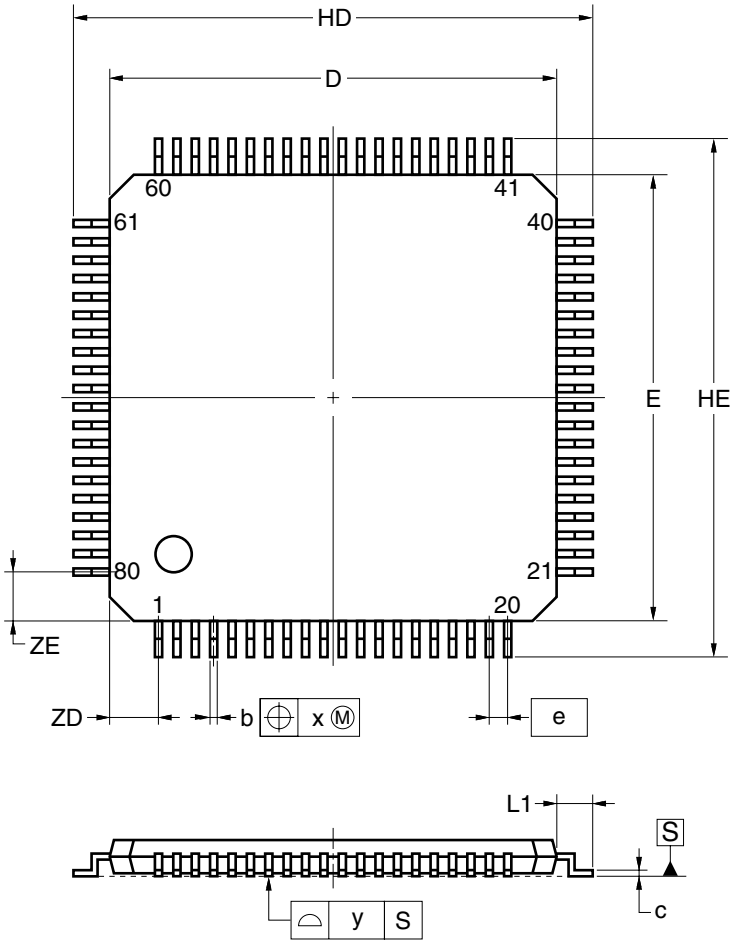
Low-speed device connect detection

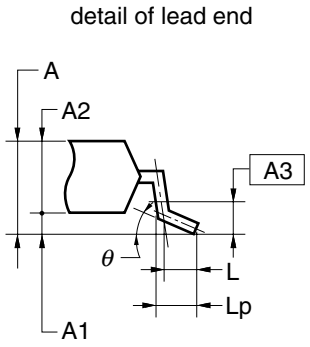


4. PACKAGE DRAWINGS

• μPD720150GK-9EU-A

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)





NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

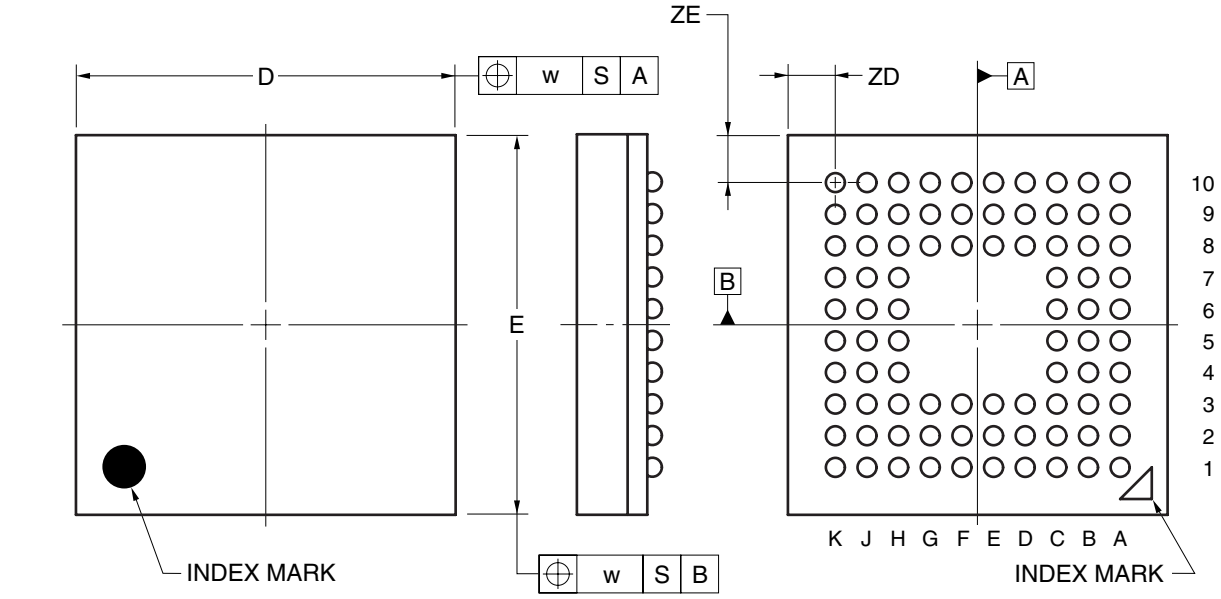
(UNIT:mm)

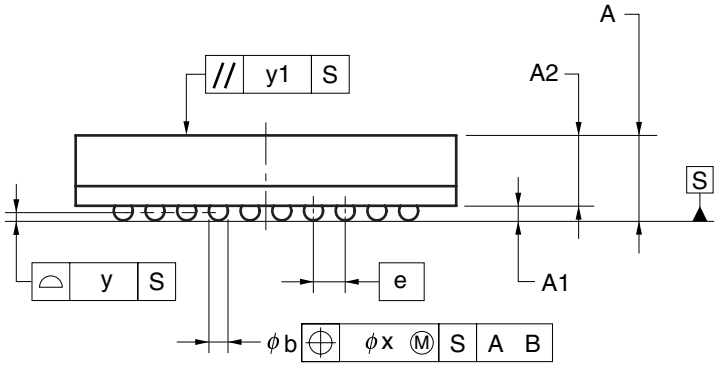
ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
A2	1.00
HD	14.00±0.20
HE	14.00±0.20
A	1.10±0.10
A1	0.10±0.05
A3	0.25
Lp	0.60±0.15
b	0.22±0.05
c	$0.17^{+0.03}_{-0.07}$
θ	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25
L	0.50
L1	1.00±0.20

K80GK-50-9EU

•μPD720150F1-BAE-A

84-PIN PLASTIC FBGA (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
w	0.20
A	1.32±0.10
A1	0.21±0.05
A2	1.11
e	0.50
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P84F1-50-BAE

5. RECOMMENDED SOLDERING CONDITIONS

The μPD720150 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

• μPD720150GK-9EU-A: 80-pin plastic TQFP (Fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit [Note]: 7 days (10 to 72 hours pre-backing is required at 125C° afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3
Partial heating method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (per each side of the device) , Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	–

Note The Maximum number of days during which the product can be stored at a temperature of 5 to 25°C and a relative humidity of 20 to 65% after dry-pack package is opened.

• μPD720150F1-BAE-A: 84-pin plastic FBGA (6 × 6)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3, Exposure limit [Note]: 7 days (10 to 72 hours pre-backing is required at 125C° afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3

Note The Maximum number of days during which the product can be stored at a temperature of 5 to 25°C and a relative humidity of 20 to 65% after dry-pack package is opened.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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