

### Description

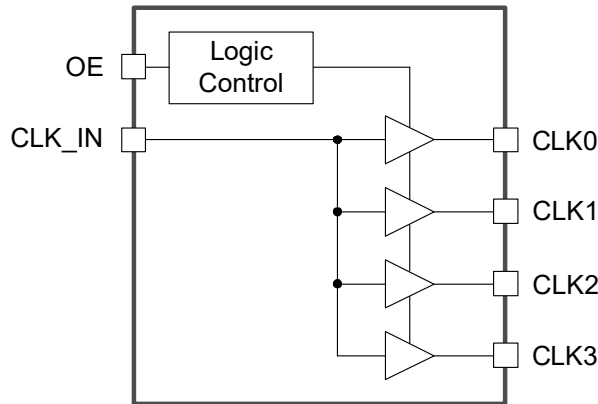
The 2304NZL is a high-performance, low skew, low jitter 1:4 LVCMOS clock buffer. The 2304NZL is ideal for PCI/PCI-X or networking applications.

The 2304NZL supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs.

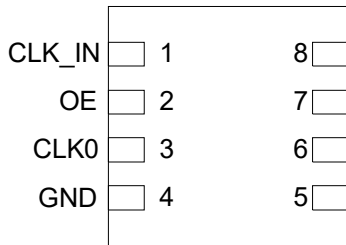
### Features

- Low input to output propagation delay (1.8ns, 3.3V)
- Low output skew: 40ps max
- Glitch-free Output Enable Function
- 1.8V to 3.3V power supply
- Packaged in small 8-pin 2 x 2 mm DFN package, as well as standard TSSOP and SOIC packages
- Industrial temperature range (-40°C to +85°C)

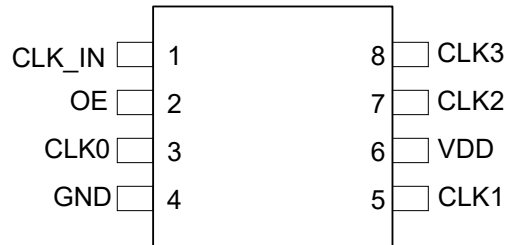
### Block Diagram



## Pin Assignment



8-pin DFN



8-pin TSSOP/SOIC

## Functionality Table

Inputs		Outputs
CLK_IN	OE	CLK(3:0)
0	0	Low
0	1	0
1	0	Low
1	1	1

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK_IN	Input	Clock input.
2	OE	Input	Output Enable for the clock outputs. Outputs are enabled when forced HIGH. Outputs are forced to logic LOW when OE is forced LOW.
3	CLK0	Output	Clock output 0.
4	GND	Power	Power supply ground.
5	CLK1	Output	Clock output 1.
6	VDD	Power	Connect +1.8V, +2.5V or +3.3V power supply.
7	CLK2	Output	Clock output 2.
8	CLK3	Output	Clock output 3.

## External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 $\mu$ F should be connected between VDD on pin 6 and GND on pin 4, as close to the device as possible. A termination resistor should be used on each clock output if the trace is longer than 1 inch. See the Test Loads section for recommended values.

To achieve the low output skew that the 2304NZL is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 2304NZL. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	Power supply			4.6	V
Output Enable and All Outputs	$V_{IO}$	With respect to GND	-0.5		$V_{DD}+0.5$	V
ICLK	$V_{IN}$	Input Voltage	-0.5		4.6	V
Ambient Operating Temperature	$T_{AMB}$	Industrial Temperature	-40		85	°C
Storage Temperature	$T_{STORE}$	Storage Temperature	-65		150	°C
Junction Temperature	$T_J$	Junction Temperature			125	°C
Soldering Temperature	$T_{SOLDER}$	Soldering Temperature			260	°C
ESD	ESD	Human Body Model	2000			V

## Recommended Operation Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Temperature	$T_{AMB}$	Ambient	-40	25	85	°C
Power Supply Voltage	$V_{DD}$	With respect to GND	1.7		3.465	V

## DC Electrical Characteristics

VDD = 1.8 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V <sub>DD</sub>		1.71	1.8	1.89	V
Input High Voltage (CLK_IN, OE)	V <sub>IH</sub>	Note 1	0.8xVDD		3.45	V
Input Low Voltage (CLK_IN, OE)	V <sub>IL</sub>	Note 1			0.2xVDD	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	0.9xVDD			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OH</sub> = 2 mA			0.1xVDD	V
Operating Supply Current	I <sub>DD</sub>	No load, 50MHz		8		mA
Nominal Output Impedance	Z <sub>O</sub>			20		Ω
Input Capacitance	C <sub>IN</sub>	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD = 2.5 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V <sub>DD</sub>		2.375	2.5	2.625	V
Input High Voltage(CLK_IN, OE)	V <sub>IH</sub>	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	V <sub>IL</sub>	Note 1			0.2xVDD	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	0.9xVDD			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OH</sub> = 2 mA			0.1xVDD	V
Operating Supply Current	I <sub>DD</sub>	No load, 50MHz		10		mA
Nominal Output Impedance	Z <sub>O</sub>			21		Ω
Input Capacitance	C <sub>IN</sub>	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD = 3.3 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V <sub>DD</sub>		3.135	3.3	3.465	V
Input High Voltage(CLK_IN, OE)	V <sub>IH</sub>	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	V <sub>IL</sub>	Note 1			0.2xVDD	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	0.9xVDD			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OH</sub> = 2 mA			0.1xVDD	V
Operating Supply Current	I <sub>DD</sub>	No load, 50MHz		12		mA
Nominal Output Impedance	Z <sub>O</sub>			25		Ω
Input Capacitance	C <sub>IN</sub>	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

## AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		170	MHz
Output Rise Time	t <sub>OR</sub>	20% to 80% of VDD, C <sub>L</sub> = 5 pF	0.7	1.1	1.5	ns
Output Fall Time	t <sub>OF</sub>	80% to 20% of VDD, C <sub>L</sub> = 5 pF	0.7	1.1	1.5	ns
Propagation Delay	Note 1		2.2	2.5	3.2	ns
Additive Phase Jitter, RMS		125MHz		100		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 2.5V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		200	MHz
Output Rise Time	t <sub>OR</sub>	20% to 80% of VDD, C <sub>L</sub> = 5 pF	0.6	1	1.5	ns
Output Fall Time	t <sub>OF</sub>	80% to 20% of VDD, C <sub>L</sub> = 5 pF	0.6	1	1.5	ns
Propagation Delay	Note 1		1.4	1.9	2.4	ns
Additive Phase Jitter, RMS		125MHz		50		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

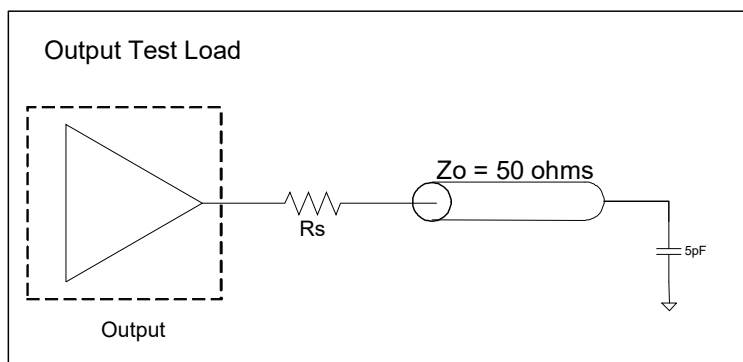
VDD = 3.3 V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		200	MHz
Output Rise Time	t <sub>OR</sub>	20% to 80% of VDD, C <sub>L</sub> = 5 pF	0.5	1	1.5	ns
Output Fall Time	t <sub>OF</sub>	80% to 20% of VDD, C <sub>L</sub> = 5 pF	0.5	1	1.5	ns
Propagation Delay	Note 1		1.1	1.7	2.1	ns
Additive Phase Jitter, RMS		125MHz		30		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Phase noise spec taken with Wenzel oscillator as reference input.

## Test Load and Circuit



VDD	Rs ( $\Omega$ )
1.8V	25
2.5V	29
3.3V	30

## Thermal Characteristics (8DFN)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		81		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	1 m/s air flow		73		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	3 m/s air flow		70		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	$\theta_{JC}$			10.6		$^{\circ}\text{C}/\text{W}$

## Thermal Characteristics (8TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		110		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	1 m/s air flow		100		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	3 m/s air flow		80		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	$\theta_{JC}$			35		$^{\circ}\text{C}/\text{W}$

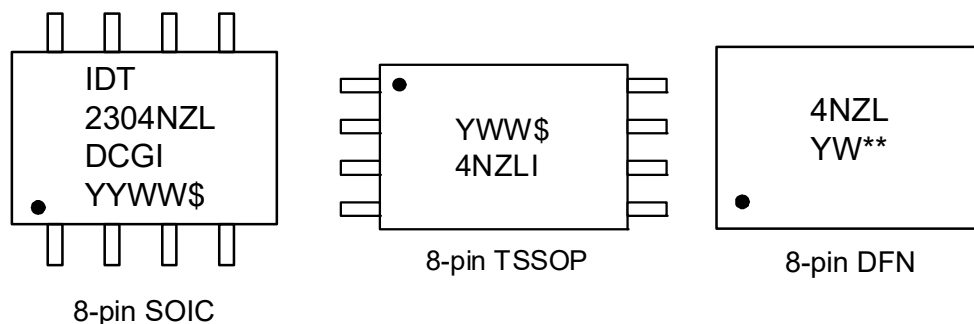
## Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		110		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	1 m/s air flow		100		$^{\circ}\text{C}/\text{W}$
	$\theta_{JA}$	3 m/s air flow		80		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	$\theta_{JC}$			35		$^{\circ}\text{C}/\text{W}$

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Marking Diagrams



### Notes:

1. “\*\*\*” is the lot number (DFN only).
2. “YYWW” or “YWW” or “YW” is the digits of the year and week that the part was assembled.
3. “\$” is the mark code.
4. “G” denotes RoHS compliant package.
5. “I” denotes industrial temperature range.
6. Bottom markings: lot number and country of origin for TSSOP; lot number for SOIC.

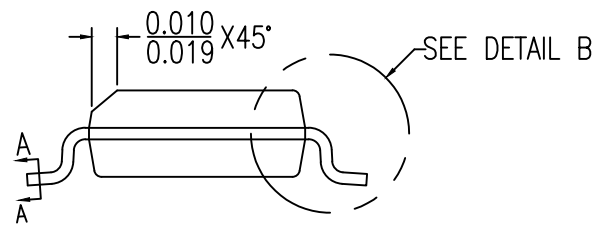
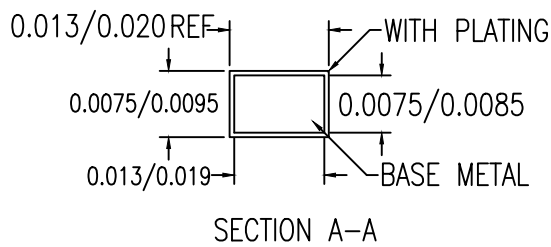
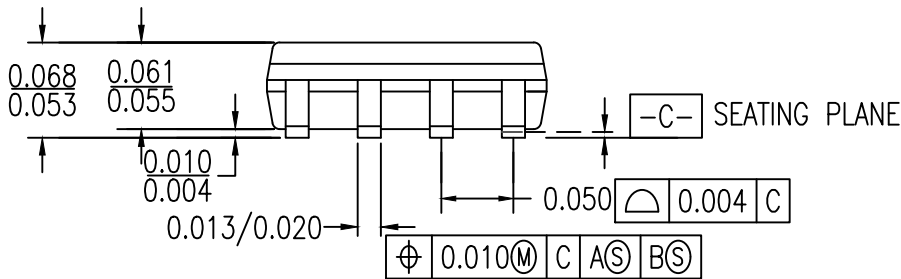
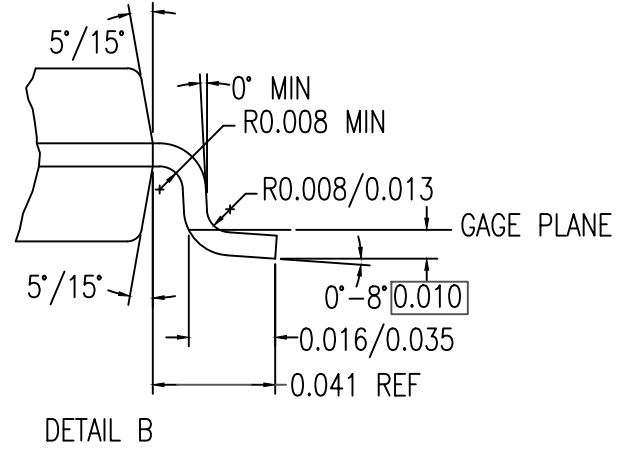
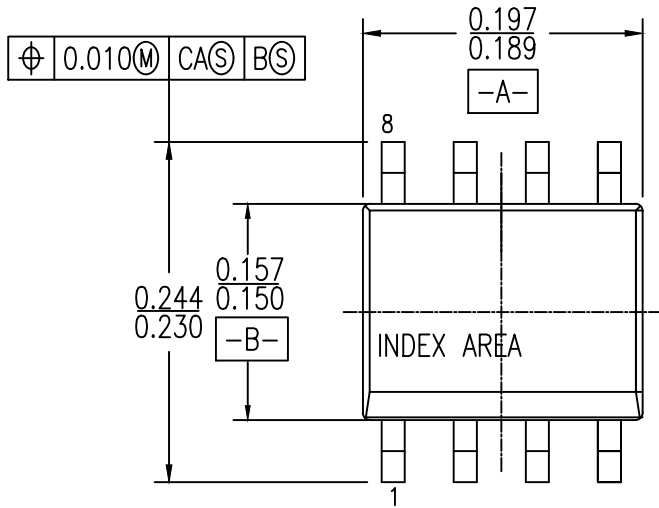
## Ordering Information

Part Number	Carrier Type	Package	Temperature Range
2304NZLDCGI	Tubes	0.150" body, 0.050" pitch <a href="#">8-SOIC</a>	-40 to +85°
2304NZLDCGI8	Tape and Reel	0.150" body, 0.050" pitch <a href="#">8-SOIC</a>	-40 to +85°
2304NZLPGGI	Tubes	4.4mm body, 0.65mm pitch <a href="#">8-TSSOP</a>	-40 to +85°
2304NZLPGGI8	Tape and Reel	4.4mm body, 0.65mm pitch <a href="#">8-TSSOP</a>	-40 to +85°
2304NZLNTGI	Tubes	2.0 × 2.0 × 0.75 mm <a href="#">8-DFN</a>	-40 to +85°
2304NZLNTGI8	Tape and Reel	2.0 × 2.0 × 0.75 mm <a href="#">8-DFN</a>	-40 to +85°

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

## Revision History

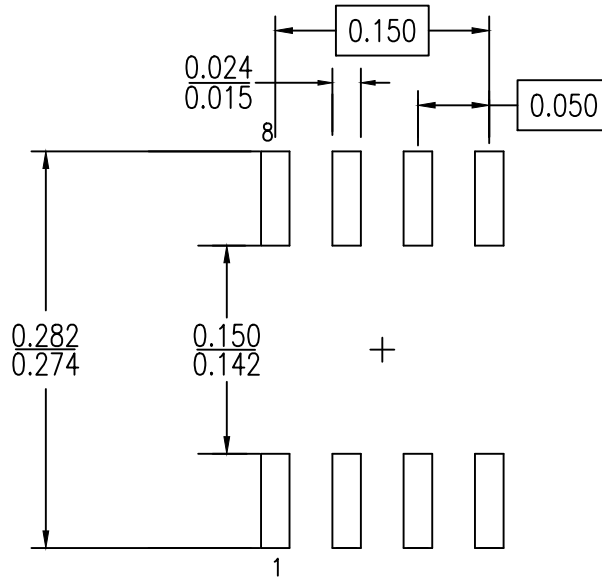
Date	Description
July 24, 2023	<ul style="list-style-type: none"> <li>• Updated TSSOP marking diagram.</li> <li>• Updated Package Outline Drawings section.</li> <li>• Added POD links to ordering Information.</li> <li>• Rebranded to Renesas.</li> </ul>
January 31, 2017	<ul style="list-style-type: none"> <li>• Updates to operating supply current and output impedance values in DC electrical tables.</li> <li>• Added Rs values to test loads.</li> </ul>
June 21, 2016	<ul style="list-style-type: none"> <li>• Added marking diagrams.</li> <li>• Moved to final.</li> </ul>



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES



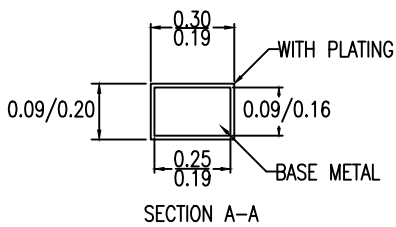
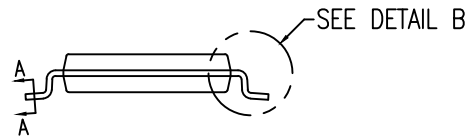
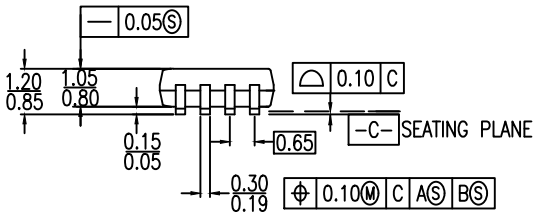
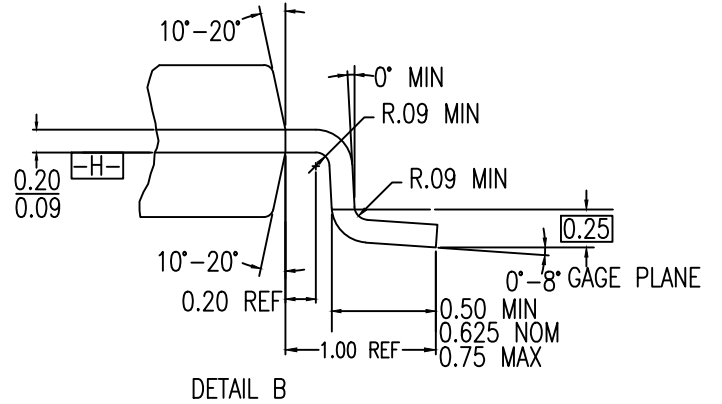
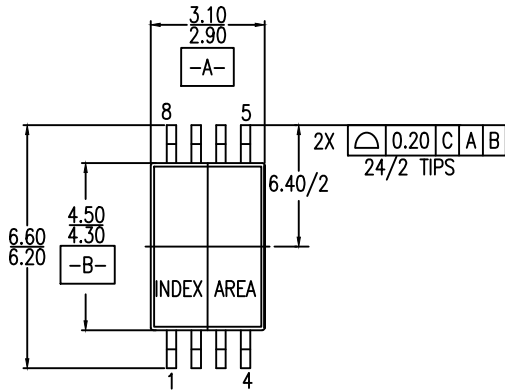


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

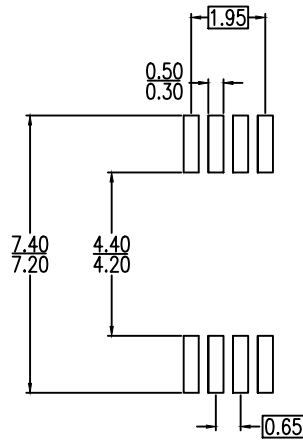
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES

Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 01	Dedicate to Package DCG8 Only
Feb 24, 2016	Rev 00	Initial Release



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

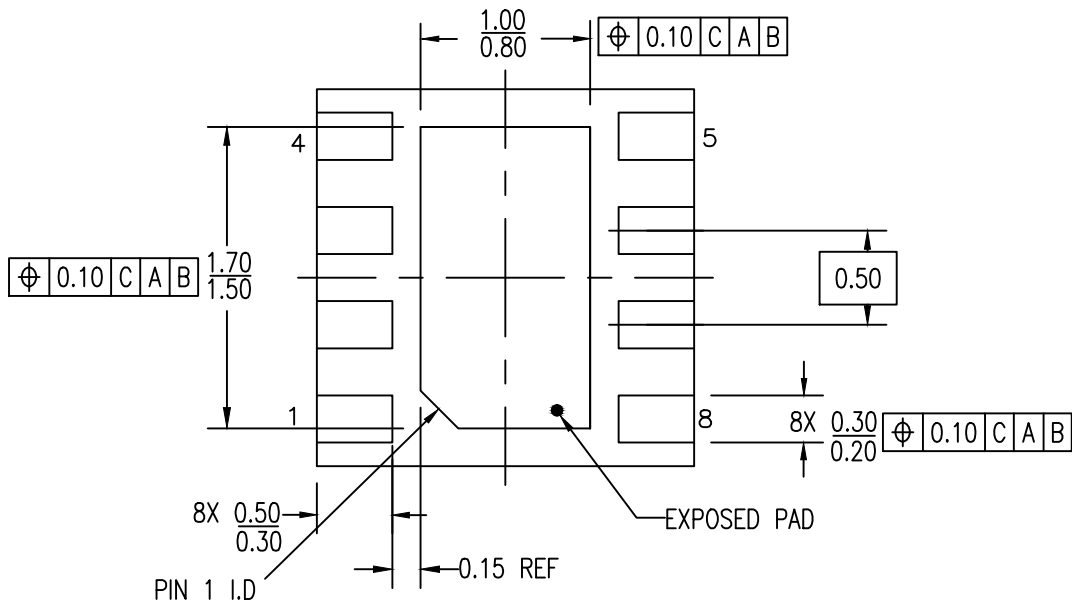
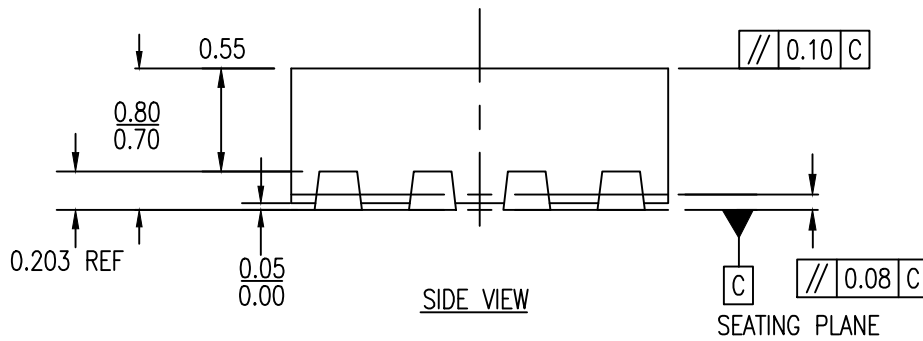
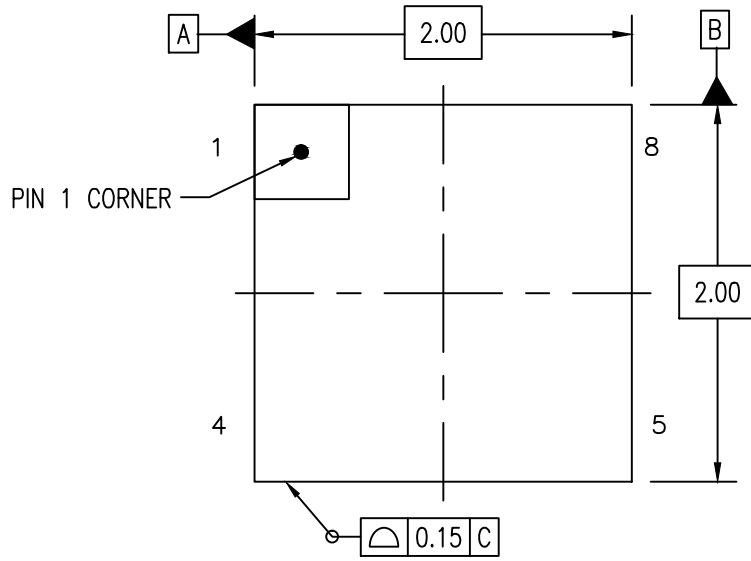


RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

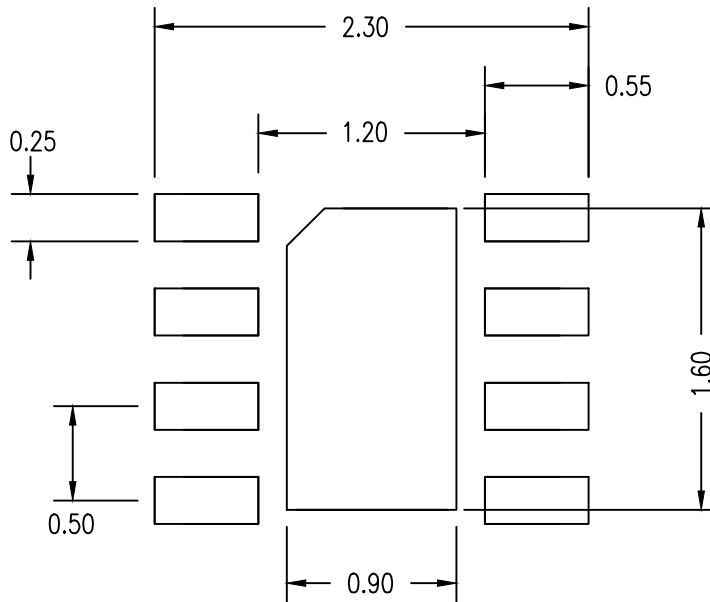
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 00	Initial Release



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Feb 12, 2018	Rev 01.	New Format, Change QFN to VFQFPN
April 12, 2018	Rev 02	Change from "VFQFPN" to "DFN"

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.