General Description

DA7400 is a high-performance, ultra-low-power, stereo hi-fi codec for USB-C™ and Bluetooth® headphone (HP), headset, or hearable applications.

With high-performance playback and record paths, DA7400 is designed for high dynamic range and minimum latency. An integrated, programmable, digital signal processor performs equalization, limiting, mixing, and gain control.

Key Features

- Stereo analog microphone or line input path with 95 dB dynamic range
- Stereo differential headphone path with 115 dB dynamic range
- JAS Hi-Res AUDIO compatible
- 4-wire digital audio interface with support for I²S, TDM, and other common audio formats:
  - Up to 32 bits per channel
  - Up to 384 kHz sample rate support
- Two stereo PDM inputs for digital microphones
- Integrated low-noise microphone bias
- Flexible DSP supporting mixing, gain, equalization, sidetone, and automatic gain control
- Bypassable asynchronous sample-rate converters
- Programmable fractional-N phase-locked loop (PLL)
- I²C compatible control interface
- WLCSP 32 ball, 3.29 mm x 1.75 mm, 0.4 mm pitch

Applications

- Headphones and headsets
- Internet of Things (IoT)
- Hearables
- Gaming and virtual reality (VR)

System Diagram

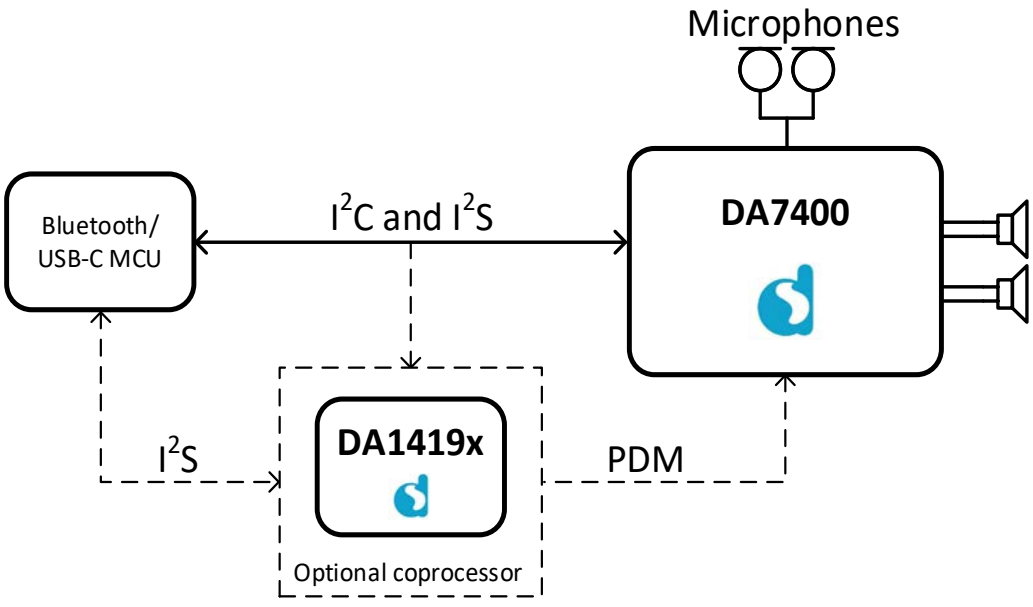

Figure 1: System Diagram

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1 Terms and Definitions

ADC	Analog to Digital Converter
ALC	Automatic Level Control
APU	Audio Processing Unit
BCLK	Bit Clock
BG	Bandgap
BW	Bandwidth
CLK	Clock
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DMIC	Digital microphone
DMIC IF	Digital Microphone Interface
DSP	Digital Signal Processor
EQ	Equalization
HP	Headphone
I^2C	Inter-Integrated Circuit
IF	Interface
IoT	Internet of Things
LDO	Low-Dropout Regulator
MCLK	Master Clock
MEMS	Micro-Electro-Mechanical Systems
OSC	Oscillator
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Binary Sequences
rms	Root Mean Square
SDM	Sigma-Delta Modulation
SR	Sample Rate
SRAM	Static Random-Access Memory
SRC	Sample Rate Converter
SRM	Sample Rate Matching
SSR	System Sample Rate (internal chip sample rate)
TDM	Time Division Multiplexing
VR	Virtual Reality
WCLK	Word Clock
WLCSP	Wafer Level Chip Scale Package

2 Block Diagram

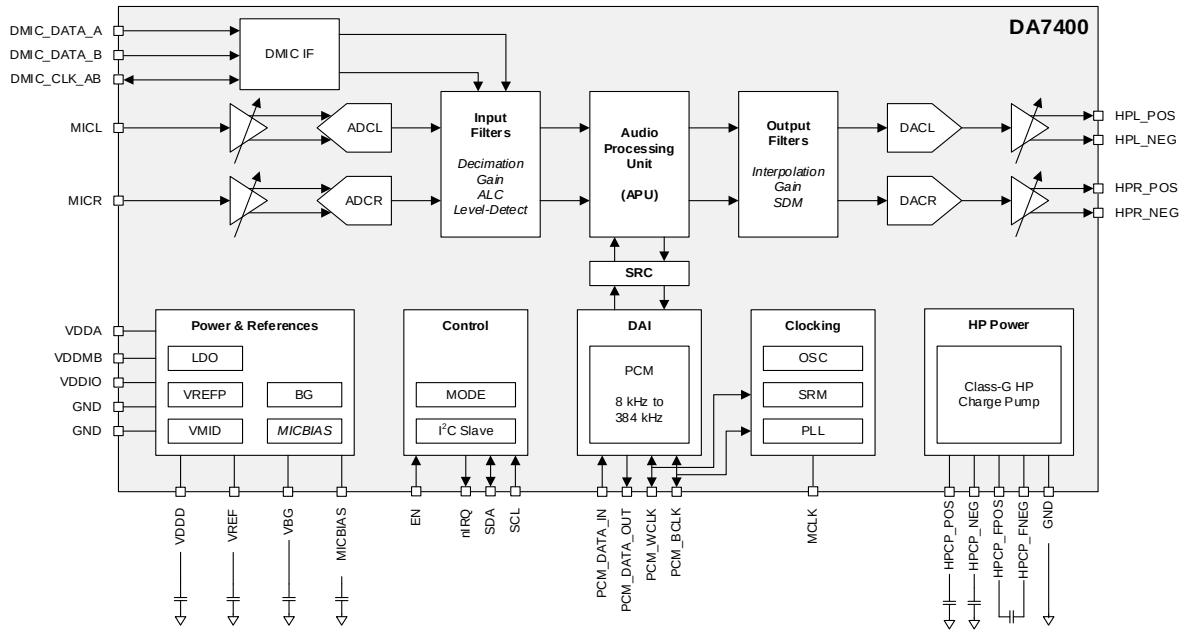


Figure 2: Block Diagram

2.1 Blocks Summary

Power and References: V_{DDA} is the main analog supply to the chip. V_{DDIO} is the input/output (IO) supply to the chip. The power and references block provides an internal low-dropout regulator (LDO) which generates V_{DDD} to supply the digital circuitry, the input to this LDO is V_{DDA}. Internal reference generators create the bandgap (BG) V_{BG}, and V_{REF} references; the V_{REF} and V_{BG} references must be externally decoupled. V_{DDD} can also be supplied from an external source.

Control: The I^2C slave is used for control and register access and an active-low interrupt pin (nIRQ) is used to inform an external host of events within the device that require host interaction. A system sequencer enables and disables the audio paths in a pop-and-click free manner.

Input Path: The analog-to-digital converters (ADCs) are high-performance sigma-delta converters. The dual microphone inputs support analog microphones as well as line input levels.

ADC data is decimated and routed to the audio processing unit (APU). The path has user-configurable gain, automatic level control (ALC) and a root-mean-square (rms) level detector.

Output Path: The digital-to-analog converters (DACs) are high-performance sigma-delta converters. The headphone driver is a differential output Class-G driver supplied with a positive and negative voltage from the headphone charge pump.

DAC data is sourced from the APU. It is interpolated and sigma-delta modulated (SDM) for the analog output path, which has configurable gain.

APU: Within the APU there is a custom programmable digital signal processor (DSP) core capable of performing many audio tasks including equalization, limiting, and low-latency sidetone filtering.

DMICs: The pulse density modulation (PDM) DMIC inputs support up to two digital micro-electro-mechanical systems (MEMS) microphones. The data line clocks in left and right channels on opposite edges of the clock.

Digital Audio Interface (DAI): The pulse code modulation (PCM) interface is the main synchronous audio interface to the host, operating in either master or slave configuration. It operates at a bit clock (BLCK) rate of up to 24.576 MHz, supporting a maximum sample rate of 384 kHz (stereo, 32 bits). It transmits the microphone data and receives stereo data for the headphone output.

An asynchronous sample-rate converter (SRC) sits between the DAI and the APU, and can be bypassed. The SRC converts the incoming audio data from the DAI sample rate to the 192 kHz sample rate used by the APU for low latency applications and the outgoing audio data from 192 kHz to the sample rate of the host. In applications where low latency is not required the SRC can be bypassed.

Clocking: A PLL acts as the core of the clocking block, taking its input reference from the MCLK pin or the PCM_BCLK pin.

When the DAI is operating in Slave mode, the PLL can also work with sample rate matching (SRM), a mechanism to track the sample rate, to lock to the incoming DAI word clock (WCLK).

3 Pinout

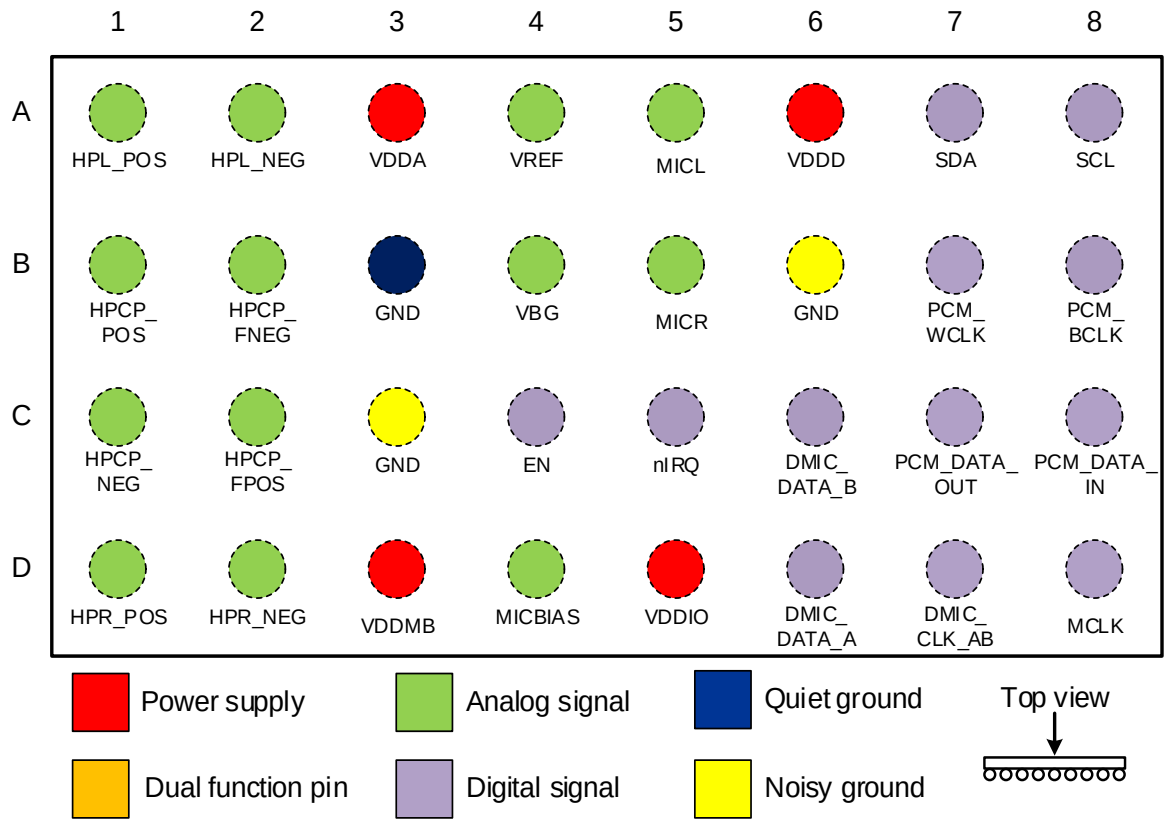


Figure 3: WLCSP Pinout Diagram (Top View)

Table 1: Pin Description

WLCSP Ball #	Name	Type (Table 2)	Description
A1	HPL_POS	AO	HP left channel positive output
A2	HPL_NEG	AO	HP left channel negative output
A3	VDDA	PWR	Analog supply input
A4	VREF	AO	Analog reference output
A5	MICL	AI	Microphone left input
A6	VDDD	PWR	Digital supply output
A7	SDA	DIOD	I^2C serial data (external pull-up)
A8	SCL	DI	I^2C serial clock (external pull-up)
B1	HPCP_POS	AO	HP charge-pump positive bulk capacitor
B2	HPCP_FNEG	AO	HP charge-pump negative flying capacitor
B3	GND	GND	Quiet ground
B4	VBG	AO	Bandgap reference output
B5	MICR	AI	Microphone right input
B7	PCM_WCLK	DIO	PCM word clock / sync / select
B8	PCM_BCLK	DIO	PCM bit clock

WLCSP Ball #	Name	Type (Table 2)	Description
C1	HPCP_NEG	AO	HP charge-pump negative bulk capacitor
C2	HPCP_FPOS	AO	HP charge-pump positive flying capacitor
C3	GND	GND	Noisy ground
C4	EN	DI	Device enable, active high
C5	nIRQ	DOD	Active low, open-drain interrupt (external pull-up)
C6	DMIC_DATA_B	DI	DMIC data input B
C7	PCM_DATA_OUT	DO	PCM data output
C8	PCM_DATA_IN	DI	PCM data input
D1	HPR_POS	AO	HP right channel positive output
D2	HPR_NEG	AO	HP right channel negative output
D3	VDDMB	PWR	MICBIAS supply
D4	MICBIAS	AO	MICBIAS output
D5	VDDIO	PWR	Digital IO supply input
D6	DMIC_DATA_A	DI	DMIC data input A
D7	DMIC_CLK_AB	DO	DMIC clock for DMIC_DATA_A and DMIC_DATA_B
D8	MCLK	DI	Master clock input

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input / output	AIO	Analog input / output
DIOD	Digital input / output open drain	DOD	Digital output open drain
PWR	Power	GND	Ground

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min		Max	Unit
T_{STG}	Storage temperature		-40		150	°C
V_{DDA}	Main analog supply	Relative to GND	-0.3		1.98	V
V_{DDIO}	Digital I/O supply	Relative to GND	-0.3		3.63	V
V_{DDMB}	MICBIAS supply	Relative to GND	-0.3		3.63	V

4.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient operating temperature	In air	-40		85	°C
V_{DDA}	Main analog supply	Relative to GND	1.71	1.8	1.89	V
V_{DDIO}	Digital I/O supply	Relative to GND	1.1	1.8	3.6	V
V_{DDMB}	MICBIAS supply	Relative to GND	1.71	3.3	3.6	V

Note 1 Within the specified limits, a lifetime of 10 years is guaranteed.

4.3 Electrical Characteristics

Unless otherwise noted, the parameters listed in Table 5 to Table 18 are valid for T_A = 25 ºC, V_{DDA} = 1.8 V, V_{DDIO} = 1.8 V, V_{DDMB} = 3.3 V, DAI sampling frequency (f_S) = 48 kHz, system sampling frequency (SSR) = 48 kHz, R_{HP_LD} = 32 Ω, input and output path gains = 0 dB, LP_MODE_SET<x> = 0x00, 24-bit audio data, input signal = 997 Hz, and bandwidth = 20 Hz to 20 kHz.

4.3.1 Reference Voltages

Table 5: Bandgap

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{BG}	Bandgap reference output voltage		1.19	1.2	1.21	V

Table 6: VREF

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{REFP}	V_{REFP} buffer output voltage			1.56		V

Table 7: LDO

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{DDD_0V9}	Output voltage	STANDBY mode	0.89	0.9	0.92	V
V_{DDD_1V2}	Output voltage	ACTIVE mode	1.17	1.2	1.23	V

4.3.2 Input Path Characteristics

Table 8: Input Path

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IN}	Full-scale input signal on MICL and MICR Note 1	Peak-to-peak		0.8 * VDDA		V
DR	Dynamic range Note 2	A-weighted	92	95	97.5	dB
THD+N	Total harmonic distortion plus noise Note 3	Input signal = -1 dBFS	-81	-85	-87.5	dB
XTLK	Channel-to-channel crosstalk	One channel input = -1 dBFS Other channel input = mute Both channels enabled		90		dB
$PSRR_{217Hz}$	Power supply rejection ratio from V_{DDA} to the ADC outputs	Measured at 217 Hz		60		dB
$PSRR_{1kHz}$	Power supply rejection ratio from V_{DDA} to the ADC outputs	Measured at 1 kHz		60		dB
$PSRR_{20kHz}$	Power supply rejection ratio from V_{DDA} to the ADC outputs	Measured at 20 kHz		50		dB
Z_{IN}	Input impedance			10		kΩ
A_{RNG}	Analog gain range		0		30	dB
A_{STP}	Analog gain step		5.8	6	6.2	dB

Note 1 V_{IN} yields 0 dBFS at the DAI output, when the path gain = 0 dB.

Note 2 DR is a ratio of the full-scale signal VIN to the integrated noise in the presence of a -60 dBFS, 997 Hz input signal.

Note 3 THD+N is the integrated noise plus distortion level relative to the given reference signal level.

Table 9: Input Filters

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$f_{PB\_8kHz\_96kHz}$	Passband frequency	SSR ≤ 96 kHz		0.45 * fS		Hz
f_{PB_192k}	Passband frequency	SSR = 176.4 kHz or 192 kHz		0.35 * fS		Hz
$A_{RPL\_PB\_8kHz\_32kHz}$	Passband gain ripple	SSR ≤ 32 kHz		+/-0.4		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
$A_{RPL\_PB\_44.1kHz\_192kHz}$	Passband gain ripple	SSR ≥ 44.1 kHz		+/-0.1		dB
$f_{SB\_8kHz\_96kHz}$	Stopband frequency	SSR ≤ 96 kHz		0.55 * fS		Hz
f_{SB_192kHz}	Stopband frequency	SSR = 176.4 kHz or 192 kHz		0.7 * fS		Hz
$A_{SB\_8kHz\_32kHz}$	Stopband attenuation	SSR ≤ 32 kz		80		dB
$A_{SB\_44.1kHz\_96kHz}$	Stopband attenuation	SSR = 44.1 kHz to 96 kHz		66		dB
A_{SB_192kHz}	Stopband attenuation	SSR = 176.4 kHz or 192 kHz		41		dB
$t_{D\_GRP\_8kHz\_32kHz}$	Group delay	SSR ≤ 32 kHz		4		samples
$t_{D\_GRP\_44.1kHz\_96kHz}$	Group delay	SSR = 44.1 kHz to 96 kHz		5		samples
$t_{D\_GRP\_192kHz}$	Group delay	SSR = 176.4 kHz or 192 kHz		5		samples

4.3.3 Automatic Level Control Characteristics

Table 10: Automatic Level Control

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{ATK}	Attack time	Per decibel	7.37 / fS		30197/ fS	s
t_{RLS}	Release time	Per decibel	29.49 / fS		30197 / fS	s
t_{HLD}	Hold time		62 / fS		2031616 / fS	s
ALC_{THR_MAX}	Maximum threshold	Full scale	-78		0	dBFS
ALC_{THR_MIN}	Minimum threshold	Full scale	-94.5		0	dBFS
ALC_{N_THR}	Noise threshold	Full scale	-94.5		0	dBFS
ALC_{THR_STP}	Threshold step size			1.5		dBFS
A_{TOT_MAX}	Maximum overall gain		0		72	dB
A_{MAX}	Maximum overall attenuation		0		78	dB
A_{ANA_MAX}	Maximum analog gain		0		30	dB
A_{ANA_MIN}	Minimum analog gain		0		30	dB

4.3.4 Microphone Bias Characteristics

Table 11: Microphone Bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
I_{LD}	Load current				2	mA
Electrical Performance						
$V_{MICBIAS}$	Output voltage	Programmable in eight steps (1.2, 1.4, 1.6, 1.8, 2.16, 2.4, 2.7, 2.98) V	1.2		3	V
V_{N_OUT}	Noise voltage at the output	RMS V_{DDMB} = 3.3 V $V_{MICBIAS}$ = 2.2 V		5		µV
I_{VDDMB}	Supply current	V_{DDMB} = 3.3 V No load			300	µA
$PSRR_{217Hz}$	Power supply rejection ratio	At 217 Hz $V_{MICBIAS}$ = 2.2 V Load = 2 mA		75		dB
$PSRR_{1kHz}$	Power supply rejection ratio	At 1 kHz $V_{MICBIAS}$ = 2.2 V Load = 2 mA		75		dB
$PSRR_{20kHz}$	Power supply rejection ratio	At 20 kHz $V_{MICBIAS}$ = 2.2 V Load = 2 mA		60		dB

4.3.5 Output Path Characteristics

Table 12: Output Path

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
R_{HP_LD}	Headphone output load resistance, per output		12	32		Ω
Electrical Performance						
V_{OUT}	Full-scale differential HP output signal level	Peak-to-peak		2.88		V
V_{OUT_OFS}	Output dc offset		-140	0	140	µV
$V_{N\_OUT\_24dB}$	Output noise	RMS HPPGA gain ≤ -24 dB Input < -60 dBFS Non-A-weighted R_{HP_LD} = 32 Ω to ∞ Ω		1.6		µV

Parameter	Description	Conditions	Min	Typ	Max	Unit
DR	Dynamic range	HPPGA gain = -24 dB to 0 dB A-weighted	112.5	115	117	dB
THD+N-1dbFS	Total harmonic distortion plus noise	HPPGA gain = 0 dB Input 1 kHz @ -1 dBFS	-84	-90	-92	dB
THD+N-20dBFS	Total harmonic distortion plus noise	HPPGA gain = 0 dB Input 1 kHz at -20 dBFS		-100		dB
P_{OUT}	Headphone driver load power, per output	THD+N ≤ 0.1 %		30		mW
A_{RPL}	Output path gain ripple	HPPGA gain = -24 dB to 0 dB		+/-0.5		dB
A_{RNG}	Output path analog gain range		-24		6	dB
A_{MUTE}	Output path analog mute attenuation				-50	dB
A_{STP}	Output path analog gain step		5.9	6	6.1	dB
A_{ERR}	Analog gain absolute error	HPPGA gain = -24 dB to 0 dB Input = 1 kHz at - 1 dBFS	-0.1		0.1	dB
$PSRR_{217Hz}$	Power supply rejection from VDDA to the HP output	Measured at 217 Hz		75		dB
$PSRR_{1kHz}$	Power supply rejection from VDDA to the HP output	Measured at 1 kHz		75		dB
$PSRR_{20kHz}$	Power supply rejection from VDDA to the HP output	Measured at 20 kHz		65		dB
XTLK	HP-to-HP channel-to-channel crosstalk	HPPGA gain = 0 dB -1 dBFS output from aggressor and -120 dBFS output from victim		-90		dB

Table 13: Output Filters

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$f_{PB\_8kHz\_96kHz}$	Passband frequency	SSR ≤ 96 kHz	0.4166*fS			Hz
$A_{RPL\_PB\_8kHz\_96kHz}$	Passband ripple	SSR ≤ 96 kHz Input = 20 Hz to 0.4166*f_S			0.11	dB
$f_{SB\_CUT\_OFF\_8kHz\_96kHz}$	Stopband cut-off frequency	SSR ≤ 96 kHz	0.58*fS			Hz
$A_{SB\_8kHz\_96kHz}$	Stopband attenuation	SSR ≤ 96 kHz	87			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
$t_{D\_GRP\_8kHz\_96kHz}$	Group delay	SSR ≤ 96 kHz Input = 1 kHz			58	µs
f_{PB_192kHz}	Passband frequency	SSR = 176.4 kHz to 192 kHz	0.2864 *fS			Hz
$A_{RPL\_PB\_192kHz}$	Passband ripple	SSR = 176.4 kHz to 192 kHz Input = 20 Hz to 0.2864*f_S			0.01	dB
$f_{SB\_CUT\_OFF\_192kHz}$	Stopband cut-off frequency	SSR = 176.4 kHz to 192 kHz	0.875* fS			Hz
A_{SB_192kHz}	Stopband attenuation	SSR = 176.4 kHz to 192 kHz	90			dB
$t_{D\_GRP\_192kHz}$	Group delay	SSR = 176.4 kHz to 192 kHz Input = 1 kHz			6.7	µs
A_{DIG_RNG}	Digital gain range		-77.25		18	dB
A_{DIG_STP}	Digital gain step			0.375		dB

4.3.6 Phase-Locked Loop Characteristics

Table 14: Phase-Locked Loop

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
f_{IN_CLK}	PLL input clock frequency		2.5		50	MHz
f_{REF_CLK}	PLL reference clock frequency		2.5		5	MHz
f_{WCLK}	Word clock frequency	Sample rates of (8, 12, 16, 24, 32, 48, 96, 192, 384) kHz and (11.025, 22.05, 44.1, 88.2, 176.4, 352.8) kHz supported	8	48	384	kHz
Electrical Performance						
f_{OUT}	Internal system clock frequency		65	98.304	125	MHz
$f_{OUT\_INT\_OSC}$	Internal oscillator clock frequency		34.5	35	35.5	MHz
t_{ON}	PLL lock time without SRM			0.1		ms
t_{ON_SRM}	PLL lock time with SRM			25		ms
$t_{JTR\_ABS\_PLL}$	Absolute jitter of PLL	50 Hz to 40 kHz integration range Clean input source f_{REF_CLK} = 5 MHz		104		ps
$t_{JTR\_ABS\_PLL}$	Absolute jitter of PLL	50 Hz to 40 kHz integration		171		ps

Parameter	Description	Conditions	Min	Typ	Max	Unit
		range Clean input source f_{REF_CLK} = 3.5 MHz				
$t_{JTR\_ABS\_PLL}$	Absolute jitter of PLL	50 Hz to 40 kHz integration range Clean input source f_{REF_CLK} = 2 MHz		250		ps
$t_{JTR\_PER\_OSC}$	Period jitter in internal oscillator			27		ps
f_{SRM}	SRM update frequency			1		kHz

4.3.7 Digital Audio Interface

Table 15: Digital Audio Interface

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
f_S	Sample rate		8	48	384	kHz
$f_{PCM\_BCLK\_IN}$	PCM_BCLK frequency	Slave mode	0.256		24.576	MHz
$D_{PCM\_BCLK\_IN}$	PCM_BCLK duty cycle ratio	Slave mode	45		55	%
$t_{RISE\_FALL\_IN}$	Rise/fall time on inputs PCM_BCLK, PCM_WCLK and PCM_DATA_IN			2	4	ns
$t_{HOLD\_PCM\_DATA\_IN}$	Hold time of PCM_DATA_IN with respect to PCM_BCLK active edge		4			ns
$t_{HOLD\_PCM\_WCLK}$	Hold time of PCM_WCLK with respect to PCM_BCLK active edge		4			ns
$t_{SETUP\_PCM\_DATA\_IN}$	Setup time of PCM_DATA_IN with respect to PCM_BCLK active edge		4			ns
$t_{SETUP\_PCM\_WCLK}$	Setup time of PCM_WCLK with respect to PCM_BCLK active edge		4			ns
Programmable Conditions						
$f_{PCM\_BCLK\_OUT}$	PCM_BCLK frequency	Master mode	0.256		24.576	MHz
$N_{PCM\_BCLK\_PER\_FRAME}$	Number of PCM_BCLK periods in a frame	master mode	32		256	-
N_{BITS_CH}	Number of bits per channel		16	24	32	-

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$t_{DLY\_DATA\_OUT\_DRV}$	Delay from PCM_BCLK inactive edge to PCM_DATA_OUT driving	VDDIO = 1.8 V At 2 ns drive setting			24	ns
$t_{DLY\_DATA\_OUT\_DRV\_1V2}$	Delay from PCM_BCLK inactive edge to PCM_DATA_OUT driving	VDDIO = 1.2 V At 2 ns drive setting			24	ns
$t_{DLY\_DATA\_OUT\_HIZ}$	Delay from PCM_BCLK active edge to PCM_DATA_OUT high-impedance	VDDIO = 1.8 V At 2 ns drive setting	5		17	ns
$t_{DLY\_DATA\_OUT\_HIZ\_1V2}$	Delay from PCM_BCLK active edge to PCM_DATA_OUT high-impedance	VDDIO = 1.2 V At 2 ns drive setting	5		17	ns
$t_{DLY\_WCLK\_DRV}$	Delay from PCM_BCLK inactive edge to PCM_WCLK driving	VDDIO = 1.8 V In master mode with 2 ns drive setting			14	ns
$t_{DLY\_WCLK\_DRV\_1V2}$	Delay from PCM_BCLK inactive edge to PCM_WCLK driving	VDDIO = 1.2 V In master mode with 2 ns drive setting			14	ns
$D_{PCM\_BCLK\_OUT}$	PCM_BCLK duty cycle ratio	Master mode D_{MCLK} = 50 %	45		55	%
t_{PULSE_WCLK}	PCM_WCLK pulse	Measured in PCM_BCLK periods	1			cycle

4.3.8 I²C

Table 16: I2C

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
C_{BUS}	Bus line capacitive load				150	pF
t_{SETUP_START}	Start condition setup time		260			ns
t_{HOLD_START}	Start condition hold time		260			ns
t_{LO_SCL}	SCL low time		500			ns
t_{HI_SCL}	SCL high time		260			ns
t_{RISE_SCL}	SCL and SDA rise time				120	ns
t_{FALL_SCL}	SCL and SDA fall time				120	ns
$t_{SETUP\_DATA\_IN}$	Data setup time		50			ns
$t_{HOLD\_DATA\_IN}$	Data hold time		0			ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{SETUP_STOP}	Stop condition setup time		260			ns
Standard						
f_{SCL}	SCL clock frequency				1000	kHz
t_{BUS}	Bus free time between a STOP and START condition		4.7			µs
Electrical Performance						
t_{RISE_SDA}	SCL and SDA rise time				120	ns
t_{FALL_SDA}	SCL and SDA fall time				120	ns
$t_{SETUP\_DATA\_OUT}$	Data setup time		50			ns
$t_{HOLD\_DATA\_OUT}$	Data hold time		0			ns

4.3.9 System Characteristics

Table 17: System Latency

Parameter	Description	Conditions	Min	Typ	Max	Unit
Timing Characteristics						
t_{ON_STDBY}	Turn on time	From OFF to STANDBY			10	ms
t_{ON_ACT}	Turn on time	From OFF to all paths enabled SRC enabled SRM enabled with fastest ramp setting		50		ms
t_{OFF_ACT}	Turn off time	From all paths enabled SRC enabled SRM enabled to OFF with fastest ramp setting		50		ms

Table 18: DA7400 System Power Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
P_{Q_OFF}	Quiescent power in OFF	EN pin = GND	5	10	30	µW
$P_{Q\_STANDBY}$	Quiescent power in STANDBY	EN pin = VDDIO	125	165	220	µW
$P_{Q\_STEREO\_PLB}$	Quiescent power in ACTIVE with headphone playback	SSR = DAI SR = 48 kHz Load = 32 Ω		9.5		mW

Parameter	Description	Conditions	Min	Typ	Max	Unit
		No signal LP_MODE_SET<x> = 1				
N_{PATH}	Internal path width	All digital paths		24		bits

5 Power and References

5.1 Introduction

A bandgap voltage (V_{BG}), a digital supply (V_{DDD}), and a main reference (V_{REF}) voltage are internally generated to supply the DA7400 analog and digital circuitry, see Figure 4.

5.2 Block Diagram

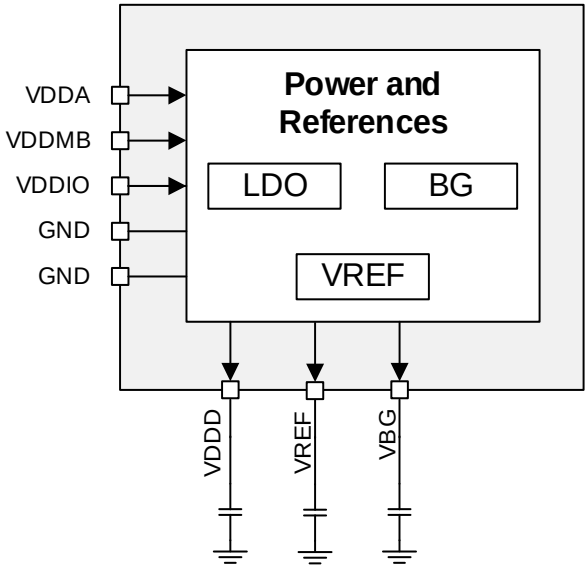


Figure 4: References Block Diagram

5.3 Digital Supply

V_{DDD} powers the digital logic circuitry. It is generated by an LDO powered from V_{DDA}. V_{DDD} is automatically enabled when needed. V_{DDD} can also be supplied from an external source.

5.4 Bandgap Voltage

V_{BG} provides a highly stable, temperature compensated reference. It is used by the microphone bias, digital LDO, and the PLL. Powered from V_{DDA}, V_{BG} is enabled automatically as required.

5.5 Main Reference Voltage

V_{REF} provides an accurate reference for the internal analog circuitry. V_{REFP} is generated from V_{DDA}.

6 Control Interface

6.1 Introduction

DA7400 is software-controlled through registers accessed via an I²C compatible serial control interface. Data is shifted in to, and out of, the DA7400 under the control of the host processor, which also provides the serial clock (SCL). An interrupt pin provides feedback to the host on events that occur within DA7400.

6.2 Features

- I²C compatible (Standard mode, Fast mode, and Fast-mode Plus)
- I²C speeds of up to 1 MHz
- Page reads and writes to reduce I²C traffic
- Interrupt pin

6.3 Block Architecture

6.3.1 I²C Control Interface

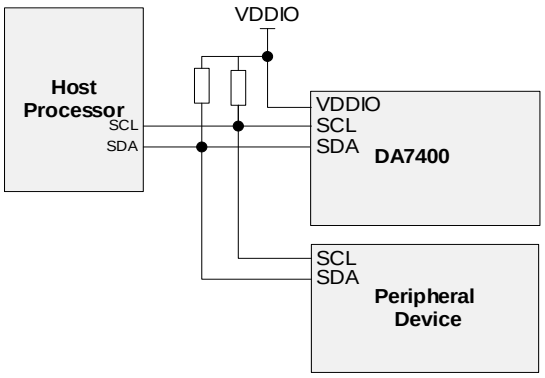


Figure 5: I²C Control Interface Bus

The 7-bit I²C slave address for DA7400 is 0x1A (0011010 binary), which is equivalent to 0x34 (8-bit address) for writing and 0x35 (8-bit address) for reading.

The I²C clock is supplied by the SCL line and the bidirectional I²C data is carried by the SDA line. The I²C interface is open drain, supporting multiple devices on a single line. The bus lines must be pulled high by external pull-up resistors (1 kΩ to 20 kΩ range). The attached devices only drive the bus lines low by connecting them to ground. This means that two devices cannot conflict if they drive the bus simultaneously.

DA7400 supports Standard-mode, Fast-mode, and Fast-mode Plus, with the highest frequency of the bus at 1 MHz in Fast-mode Plus. The exact frequency is determined by the application and does not have any relation to the DA7400 internal clock signals. DA7400 will follow the host's clock speed within the described limitations and does not arbitrate, or slow down, the clock.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. The DA7400 will only operate as a slave.

All data is transmitted across the I²C bus in groups of eight bits. A four-byte serial protocol is used containing one byte for the slave address, two bytes for the register address and one byte for data. Data and address transfers are transmitted MSB first for both read and write operations. All

transmission begins with the start condition (S) from the master while the bus is idle (the bus is free). A start condition is initiated by a high-to-low transition on the SDA line while the SCL is in the high state. Transmission ends with a stop condition (P) from the master. A stop condition is indicated by a low-to-high transition on the SDA line while the SCL line is in the high state. If a new START or STOP condition occurs within a message, the bus will return to idle.

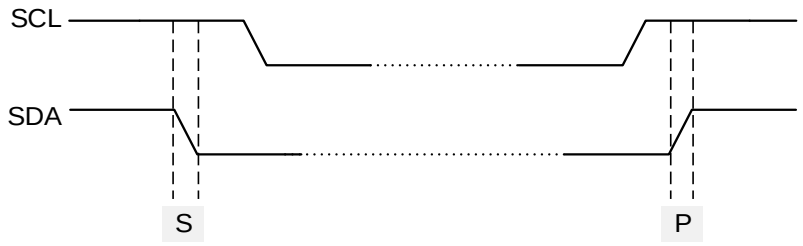


Figure 6: I²C Start and Stop Conditions

The I²C bus is monitored by DA7400 for a valid slave address whenever the interface is enabled. It responds with an acknowledge (A) immediately when it receives its own slave address. An acknowledge is indicated by the receiver pulling the SDA line low during the clock cycle immediately following the byte transmitted, see Figure 7 to Figure 10.

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 16-bit register address followed by eight bits of data terminated by a stop condition (DA7400 responds to all bytes with an acknowledge), see Figure 7.

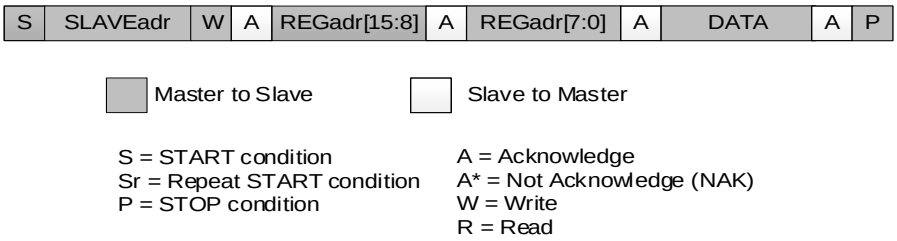


Figure 7: I²C Byte Write (SDA line)

Consecutive (Page) writes are supported if the master sends several data bytes following a slave register address. The I²C control block then increments the address pointer to the next I²C address, stores the received data and sends an acknowledge until the master sends the stop condition.

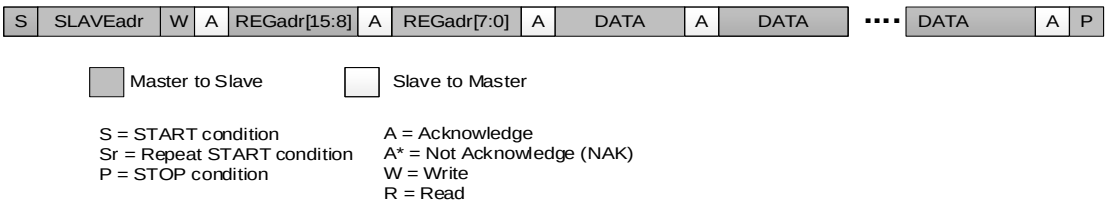


Figure 8: I²C Page Write (SDA line)

When the host reads data from a register it first has to write access DA7400 with the target register address and then read access DA7400 with a repeated start, or a second start condition. After receiving the data, the host sends a not acknowledge (A*) and terminates the transmission with a stop condition:

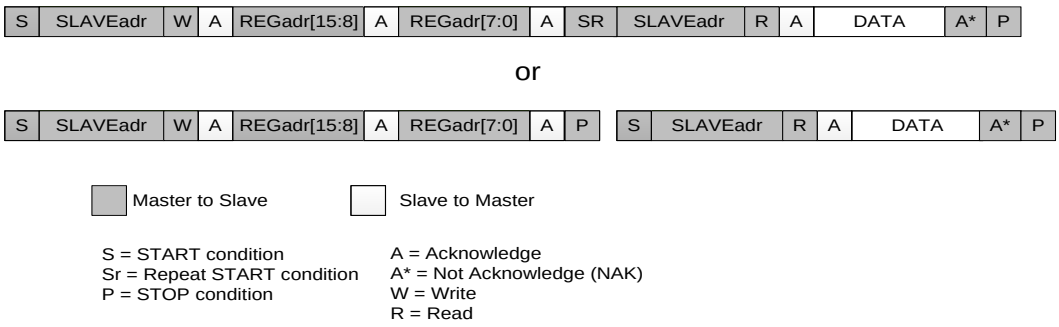


Figure 9: Examples of the I²C Byte Read (SDA line)

DA7400 supports page reads, this is initiated from the master by sending an acknowledge instead of not acknowledge after receipt of the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a not acknowledge directly after the receipt of data, followed by a subsequent stop condition. If a non-existent I²C address is read out, the DA7400 will return code zero.

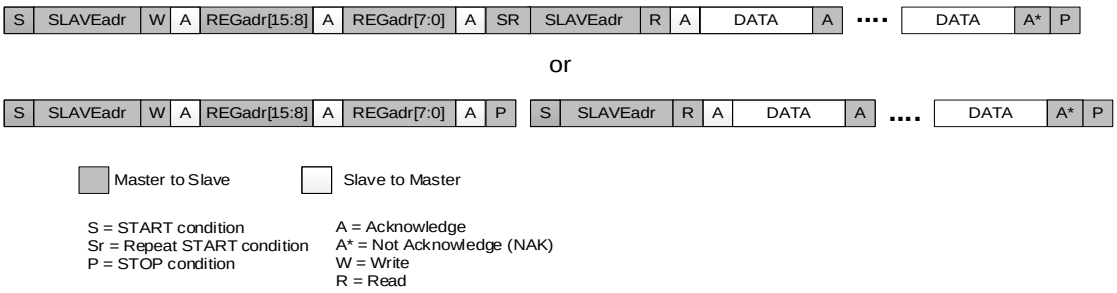


Figure 10: Examples of I²C Page Read (SDA line)

6.3.2 Interrupt

An open-drain, active-low interrupt (nIRQ) alerts the host to events occurring within the device. Events can be masked individually to prevent undesired interrupts. Interrupts are cleared by writing to the appropriate event register.

7 System Sequencers

7.1 Introduction

The system sequencers control the startup and shutdown sequence of DA7400. They also enable and disable the audio paths in a pop-and-click free manner.

7.2 Features

- Artifact-free audio path enable and disable
- Sequencers and audio paths selectively enabled to save power

7.3 Block Architecture

The system contains two sequencers, a power sequencer and an audio sequencer. The power sequencer controls the device startup and shutdown sequence. The audio sequencer enables and disables the audio paths, see Figure 11.

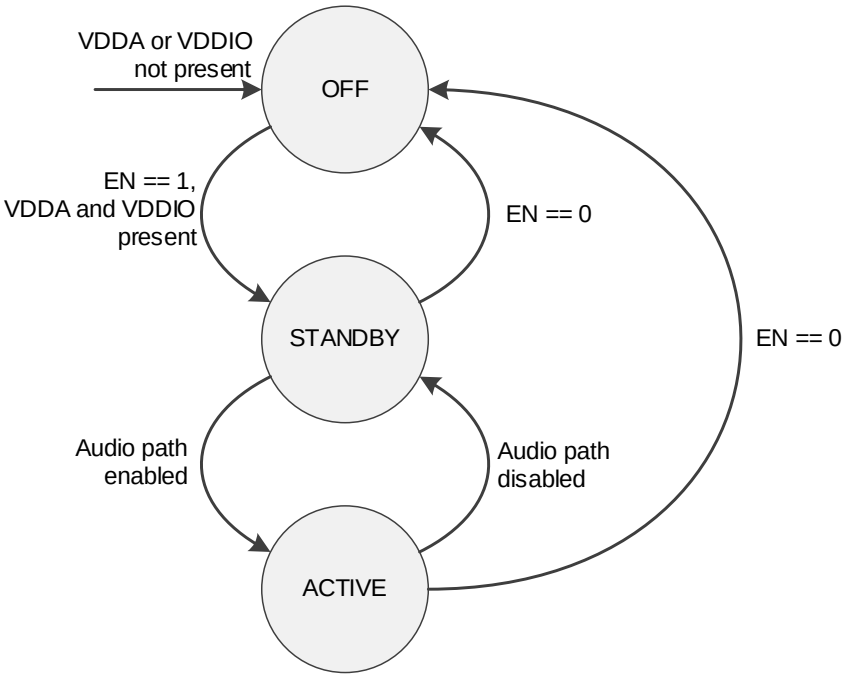


Figure 11: System Sequencer

7.4 Device Startup Sequence

The power sequencer controls the system startup and shutdown, see Figure 11. If any of V_{DDA}, V_{DDIO}, or EN are low then DA7400 is in the OFF state and is held in reset.

If the EN pin is asserted (pulled up to V_{DDIO}), EN = 1, the digital LDO and the digital core are enabled, then DA7400 transitions into the STANDBY state. I^2C communication is available after the turn on time from OFF to STANDBY (t_{ON_STBY}) has elapsed after asserting the EN pin.

Once the device has been programmed, see Section 15 the device enters the ACTIVE state **only** when an audio path is enabled by the audio sequencer, see Section 7.6.

7.5 Device Shutdown Sequence

The power sequencer also controls the shutdown sequence, see Figure 11.

If V_{DDA} or V_{DDIO} become unavailable, or the EN pin is deasserted the device enters the OFF state.

NOTE
Moving directly from the ACTIVE state to OFF may result in audible artefacts.

To ensure a pop-and-click free shutdown from the ACTIVE state initiate the STANDBY state via the audio sequencer, see Sections 7.6 and 15.2. Once the device returns to the STANDBY state EN can be deasserted and the device returns to the OFF state.

7.6 Audio Sequencer

The audio sequencer sets up the audio paths and initiates the ACTIVE state, see Section 15.2. To enable fast switching between audio applications two sequencer sets are available; for example, switching between SET0 for headphone playback and SET1 for a talk application such as a telephone call. Switching between sets is enabled quickly with one register write.

The active path can include the microphone, headphone, DAC, ADC, microphone bias, DAI, SRC, and digital microphone interfaces, as well as the appropriate SRAM program memory bank (PROG-0 or PROG-1). Paths are ramped on and off to ensure there are no audible artifacts.

DA7400 returns to the STANDBY state when the sequencer switches to a set with no active paths.

NOTE
To avoid audible artifacts do not write to the active sequencer set.

8 Clocking

8.1 Introduction

The DA7400 clocking block consists of a fractional-N phase locked loop (PLL) with sample rate matching (SRM), a 35 MHz internal oscillator, and a clock generator. It provides clocks for each of the key audio blocks, resulting in optimal power consumption and performance.

8.2 Features

- Supports input clock frequencies from 2.5 MHz to 50 MHz
- Fractional-N PLL generating a system clock up to 98.304 MHz
- SRM synchronizing the system clock with WCLK
- Reference clock detection and PLL status reporting
- 35 MHz standby oscillator

8.3 Block Diagram

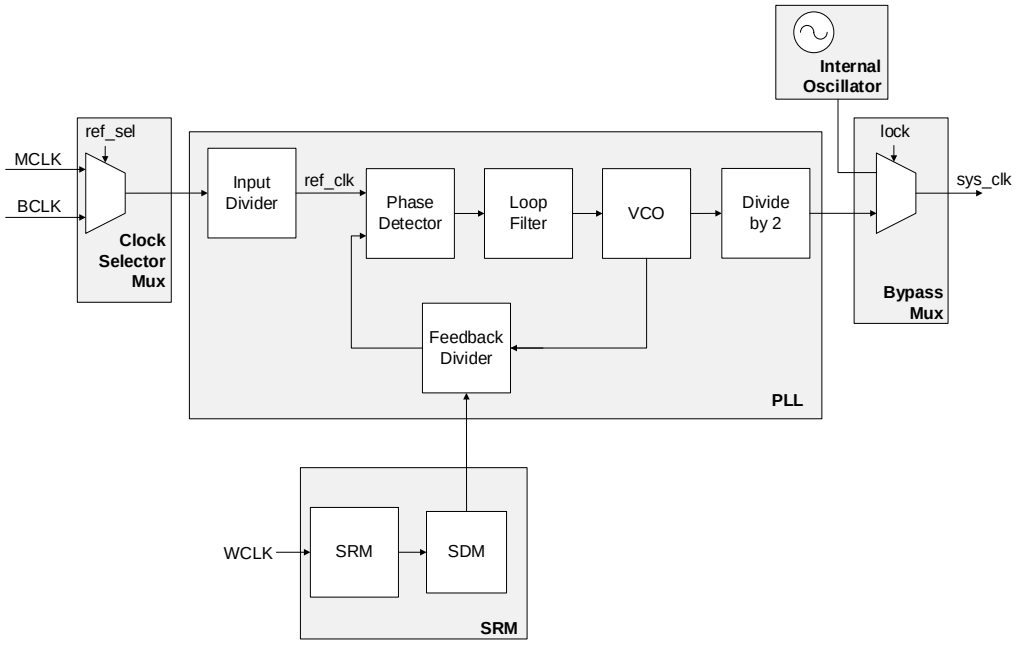


Figure 12: Clocking Block Diagram

8.4 Architecture

The clocking block consists of the following sub-blocks:

- PLL, see Section 8.5
- Clock Selector Mux, see Section 8.5.1.1
- Bypass Mux, see Section 8.5.1.5
- Clock Generator, see Section 8.6

8.4.1 Power Supplies

V_{DDD} supplies the digital circuitry, including the SRM and clock generator. An internal supply, derived from V_{DDA}, supplies the PLL, input divider, and internal oscillator.

NOTE
To minimize power consumption from the internal LDO, an external 1.2 V DCDC power supply can be connected. Please see application note AN-AU-075 for instructions on how to configure the device for an external digital supply.

8.5 Phase Locked Loop

The PLL generates the system clock (sys_clk) from a variety of clock sources. When the digital audio interface (DAI) is in Master mode (DA7400 generates bit clock (BCLK) and word clock (WCLK)) the PLL takes its clock input from the master clock (MCLK) pin.

When the DAI is in Slave mode (DA7400 receives BCLK and WCLK), or the DAI is unused, the PLL takes its clock input from MCLK or BCLK. When using BCLK as the PLL reference clock any signal on the MCLK pin is ignored.

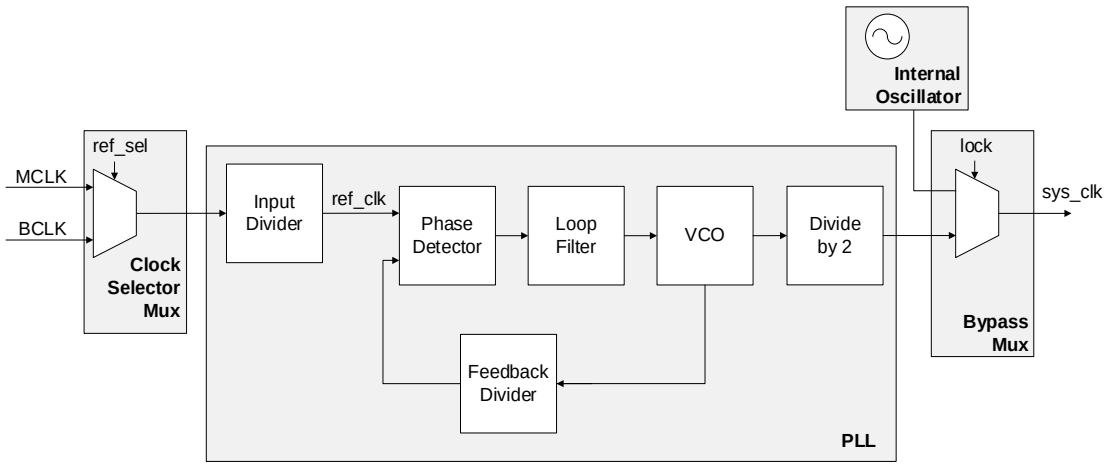


Figure 13: PLL Block Diagram

8.5.1 PLL Operation

8.5.1.1 Clock Selector Mux

The clock selector mux selects one of two clocks as the input to the PLL, see Section 15.3.1:

- MCLK - used in Master or Slave mode when MCLK > 2.5 MHz
- BCLK - used in Slave mode when BCLK > 2.5 MHz and is continuous

8.5.1.2 Input Divider

The configurable input divider generates a reference clock (ref_clk) for the PLL by dividing the input clock to be between 2.5 MHz to 5 MHz, see Section 15.3.2.

8.5.1.3 Phase Detector, Loop Filter, VCO, and Feedback Divider

The analog PLL consists of a phase detector, loop filter, voltage-controlled oscillator, and fractional feedback divider. It generates a phase-locked output clock (vco_out) of 180.6336 MHz, 195.942 MHz, or 196.608 MHz depending on the system sample rate (SSR) as shown in Table 19. The SSR is 192 kHz when the sample rate converter is enabled, otherwise it is equal to the DAI sample rate (WCLK), see Section12.3.1.1.

Table 19: PLL Output Clock Frequencies

PLL Output Clock Frequency (MHz)	System Sample Rate (kHz)	DAI Sample Rate (kHz)
180.6336	11.025, 22.05, 44.1, 88.2, or 176.4	11.025, 22.05, 44.1, 88.2, 176.4, or 352.8
195.942	192	11.025, 22.05, 44.1, 88.2, 176.4, or 352.8
196.608	12, 16, 24, 32, 48, 96, or 192	12, 16, 24, 32, 48, 96, 192, or 384

8.5.1.4 Divide-by-Two

The divide-by-two block reduces the VCO output clock (vco_out) frequency to the required sys_clk frequency of 90.3168 MHz, 97.9712 MHz, or 98.304 MHz.

8.5.1.5 PLL Bypass Mux

The PLL bypass mux is a glitch-free mux that connects the output of the PLL block to the clock generator when the PLL (and, when applicable, the SRM) is locked. If the PLL (or SRM) is unlocked, or loses lock, the PLL bypass mux will automatically switch to bypass the PLL and clock the device from the internal oscillator see Section 15.3.5.

8.5.2 PLL in Normal Mode (SRM Disabled)

Program the PLL to run in Normal mode when either of the following conditions are met:

1. The DAI is in Master mode.
2. The DAI is in Slave mode and BCLK > 2.5 MHz and is continuous.

8.5.2.1 DAI in Master Mode Using MCLK

When the DAI is in Master mode (DA7400 generates BCLK and WCLK) the PLL takes MCLK as its input and generates the sys_clk required for the selected SSR.

8.5.2.2 DAI in Slave Mode Using BCLK

When the DAI is in Slave mode and BCLK is greater than 2.5 MHz and continuous, the PLL takes BCLK as its input and generates the appropriate system clock for the selected system sample rate.

8.5.3 PLL in Sample Rate Matching Mode

Program the PLL to SRM mode when the DAI is in Slave mode and BCLK < 2.5 MHz or is not continuous, see Section 15.3.4. The SRM locks the PLL to the incoming DAI word clock.

The PLL initially locks to MCLK. Once PLL lock is achieved, it phase locks the PLL output to the DAI word clock. Lock time for the combined PLL and SRM is typically 35 ms.

The SRM constantly adjusts the feedback divider to maintain phase lock between the PLL output and the DAI word clock. The SRM detects, within 1 ms, if the SRM or PLL unlocks. In this case, it raises an interrupt, enables the internal oscillator, and switches the PLL into Bypass mode.

8.6 Clock Generator

The clock generator is responsible for generating all the required clocks. The input to the clock generator is the PLL output if the PLL is locked; otherwise the internal oscillator is used.

All outputs have independent clock gates to minimize power consumption when not in use.

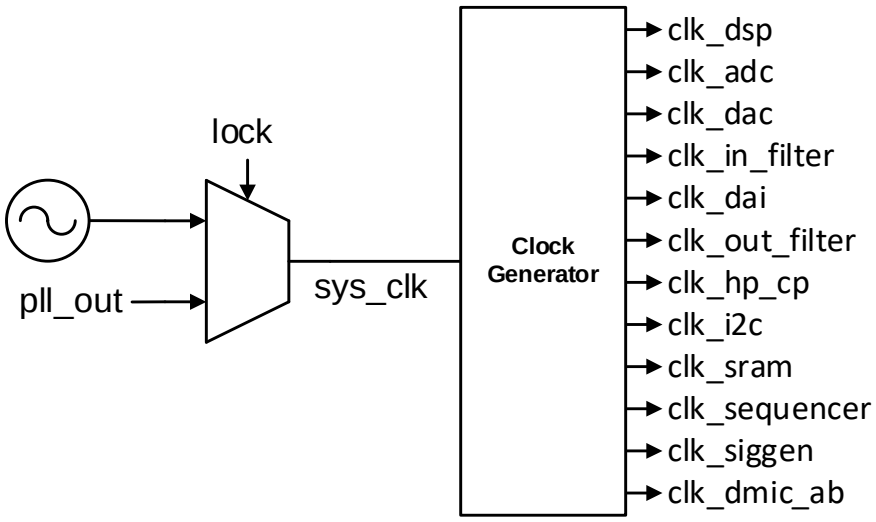


Figure 14: Clock Generator Block Diagram

9 Audio Processing Unit

9.1 Introduction

The DA7400 audio processing unit (APU) applies customizable routing and signal processing to the audio paths. This includes equalization, and sidetone. All audio paths are routed through the APU, see Section 15.4.

The signal processing algorithms run on a custom digital signal processor (DSP) core for optimal power consumption, latency, and audio performance. The algorithms are executed from either of the two banks of SRAM program memory, PROG-0 or PROG-1, see Section 15.4.2.

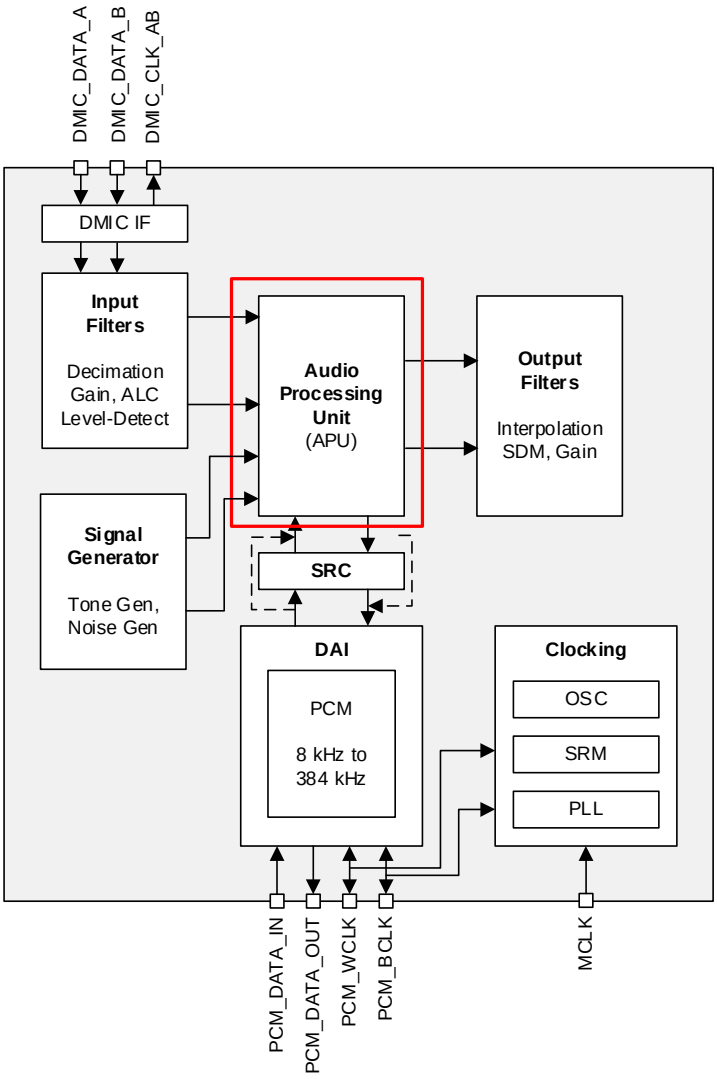


Figure 15: APU Block Dependencies

9.2 Features

- Custom DSP for routing and other effects
- Two banks of 2 kB SRAM program memory accessible via I^2C
- One bank of 2 kB SRAM data memory accessible via I^2C

9.3 Block Diagram

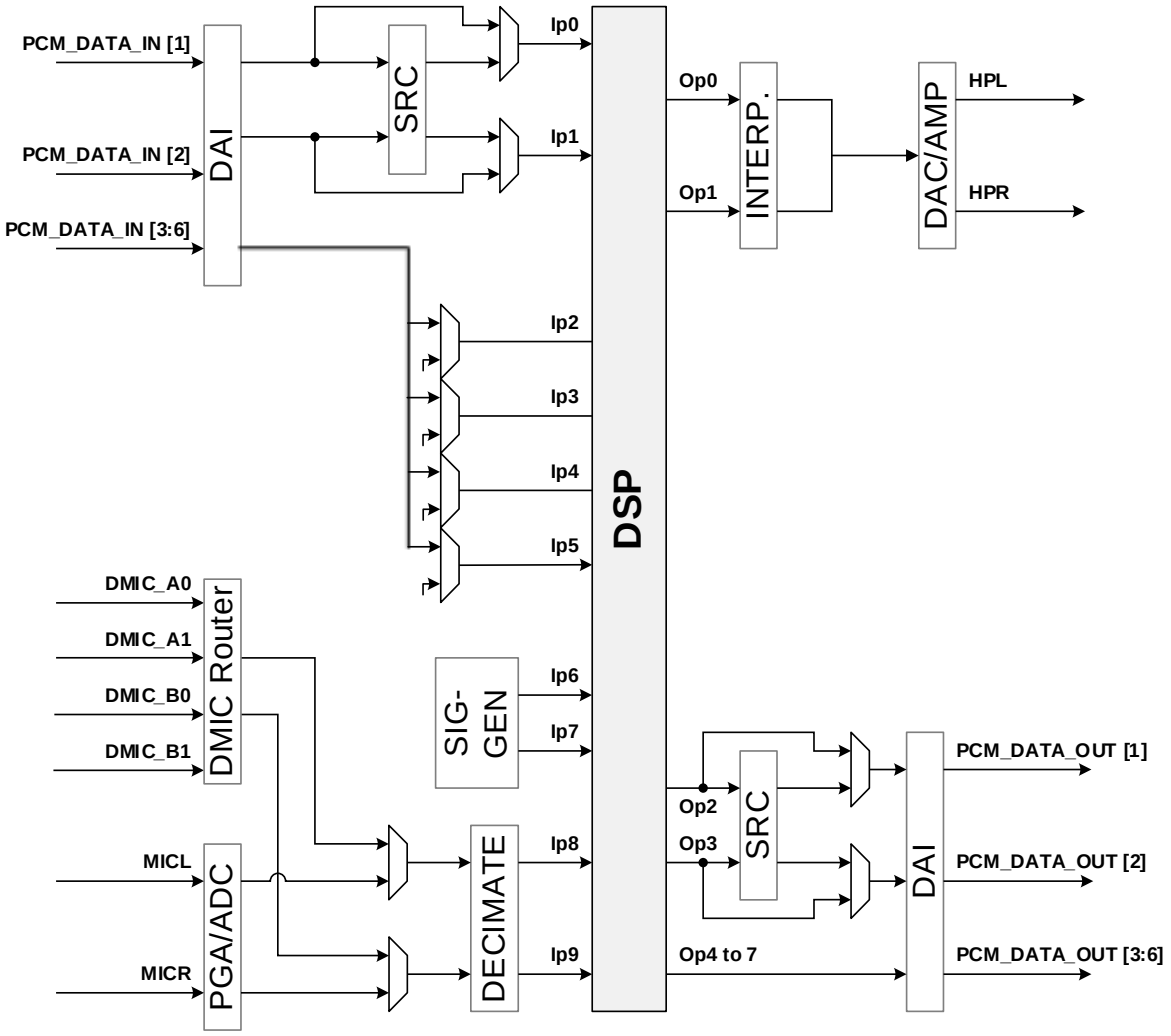


Figure 16: APU Signal Path Diagram

9.4 Block Architecture

The APU block contains the following sub-blocks:

- DSP, see Section 9.5
- SRAM, see Section 9.6

The APU contains two banks of SRAM program memory, PROG-0 and PROG-1, to support seamless switching between DSP programs. The active memory bank is selected using the system sequencer, see Section 7. The system sequencer automatically ramps up and down the audio paths to ensure switching between DSP programs is done in a pop-and-click free manner.

The DSP sub-block operates at the incoming DAI sample rate, or at 192 kHz to minimize latency if required.

9.4.1 Input Signals

The digital data inputs to the APU are as follows:

Connections from DAI:

- Six 24-bit PCM audio data, at 8 kHz to 192 kHz, to DSP

Connections from Signal Generator:

- Two 24-bit PCM audio data, at 8 kHz to 192 kHz, to DSP

Connections from Input Filters:

- Two 24-bit PCM audio data, at 8 kHz to 192 kHz, to DSP

Table 20: APU Inputs

APU Signal	Description
Ip0	DAI Channel 1
Ip1	DAI Channel 2
Ip2	DAI Channel 3
Ip3	DAI Channel 4
Ip4	DAI Channel 5
Ip5	DAI Channel 6
Ip6	Signal Generator Channel 0
Ip7	Signal Generator Channel 1
Ip8	Input Filters Channel 0
Ip9	Input Filters Channel 1

9.4.2 Output Signals

The digital data outputs from the APU are as follows:

Connections to Output Filters:

- Two 24-bit PCM audio data, at 8 kHz to 192 kHz, from DSP

Connections to DAI/SRC:

- Six 24-bit data, at 8 kHz to 192 kHz, from DSP

Table 21: APU Outputs

APU Signal	Description
Op0	Headphone Left Output
Op1	Headphone Right Output
Op2	DAI Channel 1
Op3	DAI Channel 2
Op4	DAI Channel 3
Op5	DAI Channel 4
Op6	DAI Channel 5
Op7	DAI Channel 6

9.5 DSP Subsystem

The programmable DSP core performs equalization, limiting, and sidetone from ADC to DAC.

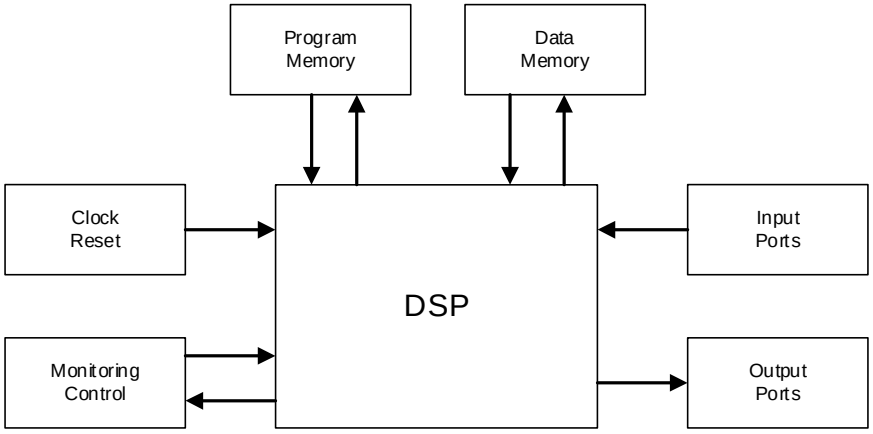


Figure 17: DSP Connections

The DSP core utilizes a ((24 * 32) + 64)-bit, single-cycle, multiply-accumulate operation with parallel load/store. The DSP does not have support for interrupts, stack, subroutines, and loops. A compiler/linker and an instruction set simulator are not available. The core is programmed using assembly language.

- When the system sample rate is 12, 16, 24, 32, 48, 96, or 192 kHz, the DSP core is clocked at 98.304 MHz.
- When the system sample rate is 11.025, 22.05, 44.1, 88.2, or 176.4 kHz, the DSP core is clocked at 90.3168 MHz.

9.5.1 DSP Program Switching

A program switch is initiated via the system sequencer. During a program switch the active SRAM bank is selected and the non-active SRAM is put in a low-power state and can be reprogrammed via I^2C. This allows multiple programs to be stored on the host device and uploaded to the DA7400 as required. To prevent audible artifacts, the program switch fades in and fades out of the active audio channels in the DSP.

9.6 SRAM Subsystem

The SRAM subsystem supports three banks of memory, one bank for temporary storage of data variables and two program memory banks for DSP programs, PROG-0 and PROG-1. Each SRAM cell contains 512 words, each word is made up of 4 bytes, resulting in 2 kB per cell and 6 kB in total.

Table 22: Memory Map

Register Address	Block Size	Description
0x4000	2 kB	Program memory PROG-0
0x4800	2 kB	Program memory PROG-1
0x5000	2 kB	DSP data memory

DA7400 provides direct byte-level, and indirect word-level, read and write access of the entire SRAM memory space to the I^2C slave.

Only the contents of one SRAM program memory bank is used for DSP processing at any one time. While a bank is not being used by the DSP it can be programmed with new information either directly or indirectly see Section 15.4.2.

10 Input Path

10.1 Introduction

The input path provides the analog input of the DA7400. Two analog microphones can be connected to the input path containing a microphone amplifier followed by the analog-to-digital converter (ADC) and digital filters. The record level can be controlled automatically. A microphone bias LDO (MICBIAS) output is provided to power electret condenser microphones.

10.2 Features

- Stereo microphone or line level input path
- 95 dB dynamic range
- -85 dB THD+N
- Automatic level control

10.3 Block Diagram

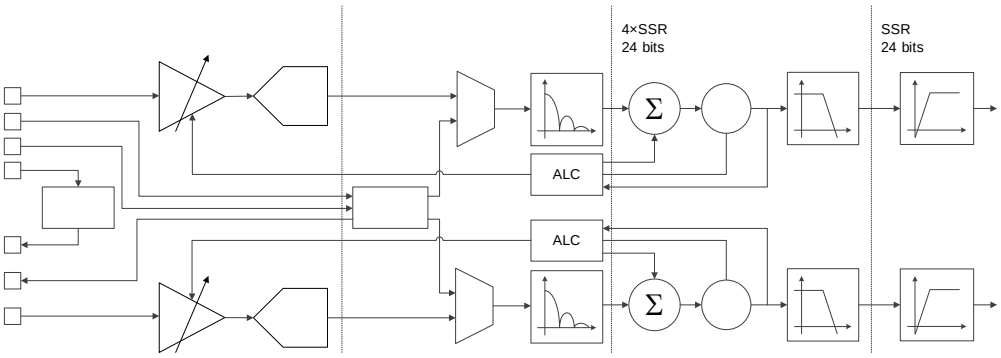


Figure 18: Input Path Block Diagram

10.4 Block Architecture

The input path consists of two single-ended microphone inputs and the following sub-blocks:

- MICBIAS, see Section 10.5
- Microphone Amplifier, see Section 10.6
- Analog-to-Digital Converter, see Section 10.7
- Input Filters, see Section 10.8
- Automatic Level Control, see Section 10.9
- High-Pass Filter, see Section 10.10

The output of the input path is 24-bit audio at system sample rate (SSR) connected to the APU.

10.4.1 Input Path Supplies

The MICBIAS is supplied by V_{DDMB}. The PGA and ADC are supplied by V_{DDA}. The digital filters are supplied by the internal digital supply V_{DDD} which is generated from V_{DDA}.

10.5 Microphone Bias

The MICBIAS circuit is supplied by an external supply V_{DDMB}. When enabled, the programmable low-dropout regulator (LDO) in the MICBIAS sets the bias voltage to a level according to the register setting. The MICBIAS LDO requires a dropout of at least 200 mV.

Biasing an analog microphone using the MICBIAS and connecting the microphone to MICL or MICR is illustrated in Figure 19. The value of the resistor R should match the impedance of the microphone. A decoupling capacitor is also required close to the MICBIAS and VDDMB pins.

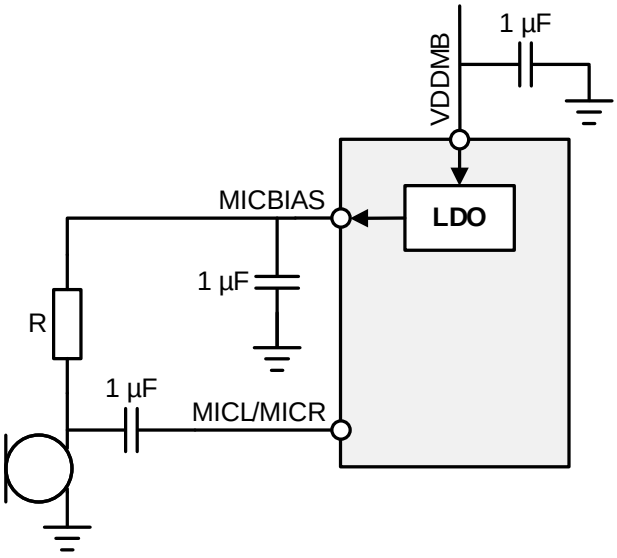


Figure 19: Analog Microphone Connection

10.6 Microphone Amplifier

The microphone amplifier is a Class-AB PGA with 0 to 30 dB programmable gain in 6 dB steps. The PGA gain is updated on a zero-cross to avoid audible artifacts when the gain is updated, see Section 15.5.

When the ALC functionality is enabled the PGA gain setting is automatically controlled and not user programmable.

10.7 Analog-to-Digital Converter

Stereo sigma-delta ADCs take the analog signal from the PGA through an anti-aliasing filter and converts it into digital data.

10.8 Input Filters

The input filters decimate the incoming data in multiple stages, downsampling the over-sampled ADC data to the system sample rate.

10.9 Automatic Level Control

For improved sound recordings of signals with a large volume range, the DA7400 offers a fully configurable ALC for microphone inputs. The ALC can be enabled independently on either of the input channels. The ALC monitors the digital signal within the ADC and adjusts the gains to maintain a constant recording level regardless of the signal level.

When analog microphones are used, the total gain is made up of analog gain in the PGA and digital gain in the input filters. In this case, the ALC can control both the analog and digital gains. When using digital microphones only the digital gain is adjusted.

Operation of the ALC is illustrated in Figure 20.

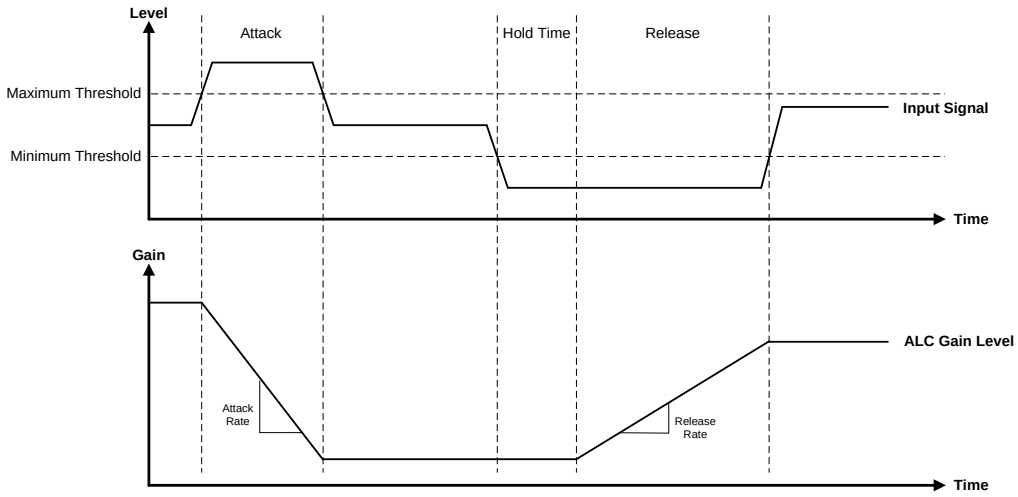


Figure 20: ALC Operation and Parameters

The ALC has a minimum and maximum threshold it intends to keep the signal level within. If the level exceeds the maximum threshold, the ALC decreases the gain at a specified attack rate until the level is within the limits. If the level falls below the minimum threshold, the ALC starts increasing the gain, after a programmable hold time, at a specified release rate. If the output signal is within the specified minimum and maximum levels, the ALC maintains the current gain.

To avoid clipping it is necessary to reduce rapidly increasing waveforms quickly. Therefore, typically the attack rate should be fast. The hold time and using a slower release time prevents unwanted pumping effect in the recording level due to changes in the signal level.

Limits for maximum gain and maximum attenuation for both analog and digital gains can be adjusted.

A recording noise-gate feature is provided to avoid increases in gain when there is no signal. Boosting a signal on which only noise is present may cause a pumping effect on noise and make noise audible. Whenever the level of the signal drops below the noise threshold the channel gain remains constant.

An anti-clip function automatically applies a very fast attack rate when the input signal is close to full-scale. This prevents clipping of the signal by reducing the signal gain at a faster rate than would normally be applied.

10.10 High-Pass Filter

A programmable digital high-pass filter is provided to filter out low-frequency content. At sample rates greater than 32 kHz these are designed to block DC, at sample rates less than or equal to 32 kHz the filter has higher corner frequencies to suit specific record path requirements, see Section 15.5.3.

11 Output Path

11.1 Introduction

The output path provides the analog audio output of the device. The output filters, DAC and headphone amplifiers have been designed to provide low latency for active noise cancellation applications whilst offering high performance and low power consumption.

11.2 Features

- 115 dB dynamic range
- -90 dB THD+N
- Configurable High-Performance and Low-Power modes
- Wide frequency response
- Stereo Class-G differential headphone driver

11.3 Block Diagram

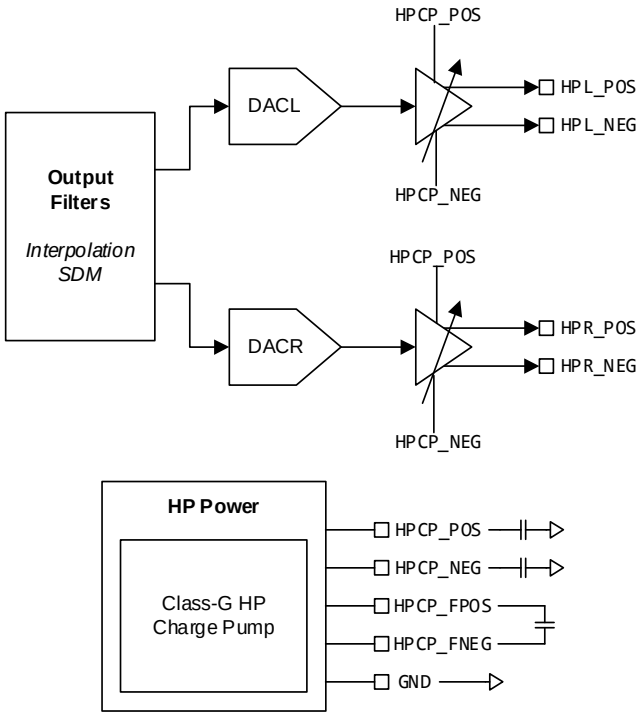


Figure 21: Output Path Block Diagram

11.4 Output Path Architecture

The output path consists of the following sub-blocks:

- Output Filters, see Section 11.5
- DACs, see Section 11.6
- Headphone Amplifiers, see Section 11.6
- Headphone Charge Pump, see Section 11.8

11.4.1 Output Path Power Supplies

V_{DDD} supplies the digital circuitry in the output filters. V_{DDA} supplies the DACs and headphone charge pump. The headphone charge pump generates positive (HPCP_P) and negative (HPCP_N) power supply rails for the headphone amplifiers.

The power supplies and clocks for disabled sub-blocks are gated to minimize power consumption.

11.5 Output Filters

The output filters are positioned between the APU and the DACs and convert the incoming signals from the system sample rate to the DAC sample rate.

Within the output filters there is an optional high-pass filter with a fixed cut-off at (SSR/12820) Hz. This filter is primarily to remove DC components from the output.

The output filters control the fixed gain of the output path; this is used to set the maximum level of the path. The gain can be set between -77.25 dB and +18 dB in 0.375 dB steps, see Section 15.6.1. The output filter gain control automatically balances the digital and analog gain to maximize the dynamic range. Variable gain control, for example volume up and down, is controlled via the APU, see Section 9.

11.6 Digital to Analog Converter

Each sigma-delta DAC takes the data from the output filters and converts it into an analog signal for the headphone amplifiers. Each DAC is only enabled when the respective headphone path is active.

11.7 Headphone Amplifiers

Each of the headphone amplifiers are differential-output drivers, capable of playing 30 mW into a 32 Ω load. The headphone amplifiers operate as Class-G with two-levels where the supply level tracks the output envelope to minimize the power consumption in the path.

The amplifiers are configured to operate differentially which offers excellent common mode noise rejection and vastly improved crosstalk performance compared to single-ended amplifiers.

The headphone loads are connected between HPL_POS and HPL_NEG for the left headphone and between HPR_POS and HPR_NEG for the right.

The headphone amplifier can be set to run in either a High-Performance mode or, a Low-Power mode via the audio sequencer, see Section 7.

11.8 Headphone Charge Pump

The headphone charge pump (HPCP) generates the positive and negative supplies for the headphone amplifier and is automatically enabled when a headphone path is active.

The headphone charge pump is a dual-rail switched capacitor DC-DC converter requiring one 1 µF flying capacitor (connected between HPCP_FPOS and HPCP_FNEG) and two 1 µF reservoir capacitors (connected respectively from HPCP_POS to GND and HPCP_NEG to GND).

The headphone charge pump generates the ±1.8 V or ±0.9 V supplies. The charge pump automatically switches between ±1.8 V and ±0.9 V depending on the signal level. This reduces power consumption when the signal level is small and prevents distortion when the signal level is high.

Inrush limiting circuitry prevents sudden supply spikes on V_{DDA} at startup and when transitioning between operating modes.

12 Digital Audio Interface

12.1 Introduction

The Digital Audio Interface (DAI) is the main synchronous audio interface between DA7400 and the host processor (host).

12.2 Features

- Bit clock rate up to 24.576 MHz
- PCM sample rate (PCM_WCLK frequency) from 8 kHz to 384 kHz
- Digital signal processing, left-justified, right-justified, and I²S formats
- Time division multiplexed mode
- Configurable frame and word lengths

12.3 Block Diagram

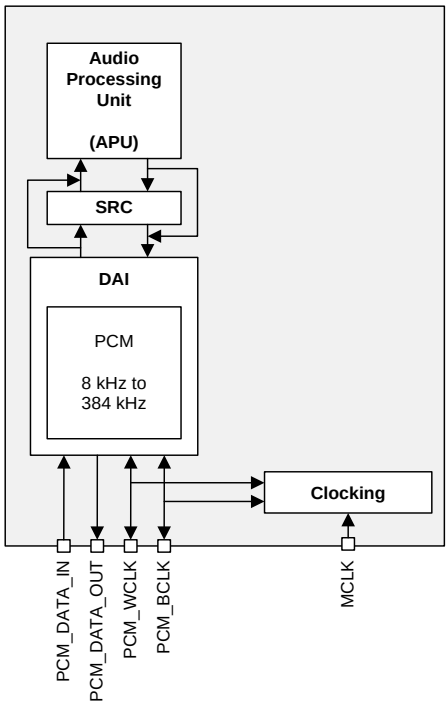


Figure 22: DAI Block Diagram

12.3.1 Block Architecture

The DAI is a four-wire serial interface. Configurable in either Master or Slave mode, it transmits data (such as analog or digital microphone data) from the APU to the host. It also receives digital audio data from the host for processing within the APU, usually for outputting to the headphone. The interface supports several formats and a time division multiplexed (TDM) mode is included to support multiple devices communicating simultaneously on the same bus.

12.3.1.1 Sample Rate Converter

A sample-rate converter (SRC) sits between the DAI and the APU. The APU operates either at a fixed sample rate of 192 kHz or at the DAI sample rate. When the APU is running at 192 kHz and the DAI sample rate is not 192 kHz the SRC converts the audio data to/from the DAI rate from/to 192 kHz.

12.4 DAI Functional Description

The DAI is a four-wire serial interface. The pins and signals are mapped as shown in Table 23.

Table 23: DAI Pins and Signals

Pin	Signal
PCM_BCLK	Bit clock (BCLK)
PCM_WCLK	Word clock (WCLK)
PCM_DATA_IN	Data in from host to DAI (DATA_IN)
PCM_DATA_OUT	Data out from DAI to host (DATA_OUT)

The DAI settings are programmed in conjunction with the master clock (MCLK) frequency and clocking registers.

The internal serialized DAI data is 24 bits wide. Serial data that is not 24 bits wide is either truncated or zero-padded at input to, or at output from, the DAI's internal 24-bit data width. The serial data word length can be programmed to be 16, 20, 24, or 32 bits wide.

In Slave mode DA7400 automatically detects the frame length (number of BCLKs per WCLK). In Master mode the frame length is configurable to be 32, 64, 128, 256, or 512 bits wide, see Section 15.7.1.4.

A configurable offset is available to determine the start of frame for Channel 1. The offset prevents conflict when two or more devices are on the bus.

12.4.1 Master or Slave Mode

The DAI operates in either master mode, see Figure 23, or slave mode, see Figure 24.

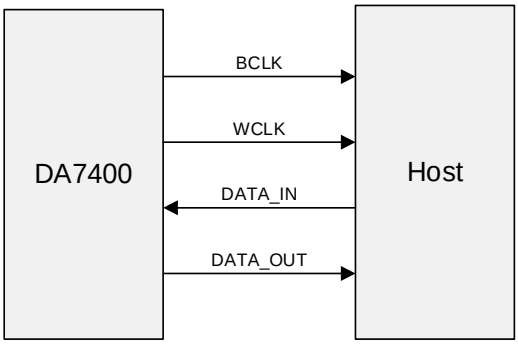


Figure 23: Master Mode

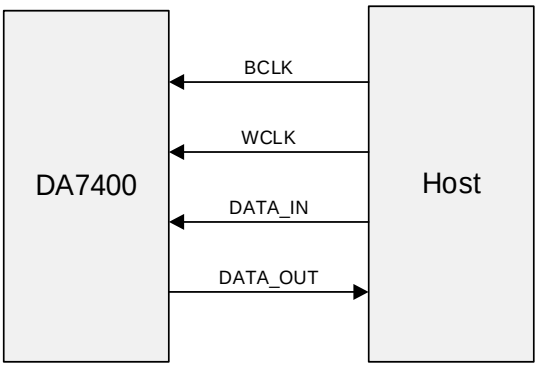


Figure 24: Slave Mode

The bit clock (BCLK) samples data coming from the host into the DAI via the PCM_DATA_IN pin and going to the host from the DAI via the PCM_DATA_OUT pin. The word clock (WCLK) is the DAI data sample clock, synchronizing the sample frames for the DAI data channels.

DA7400 provides synchronization clocks, BCLK and WCLK, in Master mode. In Slave mode, BLCK and WCLK must be provided externally.

12.4.2 DAI Channels

12.4.2.1 I²S Format

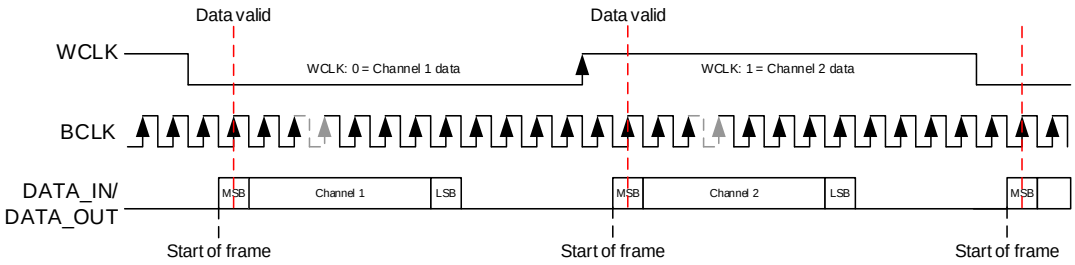


Figure 25: I²S Format

In I²S format, the start of frame for Channel 1 is on the second falling edge of BCLK after a falling edge of WCLK. The MSB of the Channel 1 is valid on the rising edge of BCLK after the start of frame condition.

The start of frame for Channel 2 is on the second falling edge of BCLK after a rising edge of WCLK. The MSB of Channel 2 is valid on the rising edge of BCLK after the start of frame condition.

12.4.2.2 DSP Format

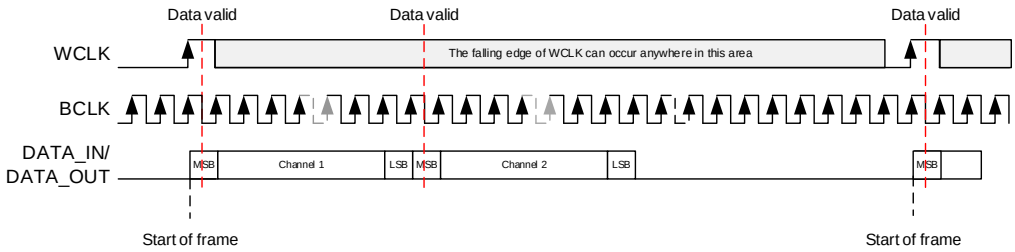


Figure 26: DSP Format

In DSP format, the rising edge of WCLK starts the data transfer (start of frame) with the Channel 1 data first, immediately followed by Channel 2 data and any subsequent channels. Each data bit is valid on the falling edge of BCLK.

12.4.2.3 Left Justified Format

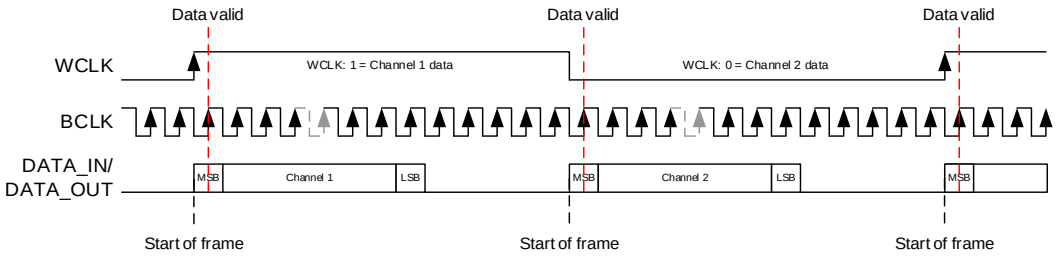


Figure 27: Left-Justified Format

In left-justified format (LJF), the MSB of Channel 1 is valid on the rising edge of BCLK following the rising edge of WCLK. The MSB of Channel 2 is valid on the rising edge of BCLK following the falling edge of WCLK.

12.4.2.4 Right Justified Format

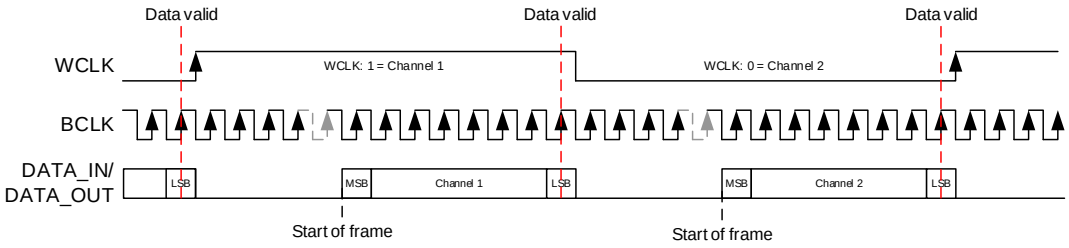


Figure 28: Right-Justified Format

In right-justified format (RJF), the LSB of the Channel 1 is valid on the rising edge of BCLK preceding the falling edge of WCLK. The LSB of Channel 2 is valid on the rising edge of BCLK preceding the rising edge of the WCLK.

12.4.3 Time Division Multiplexing Mode

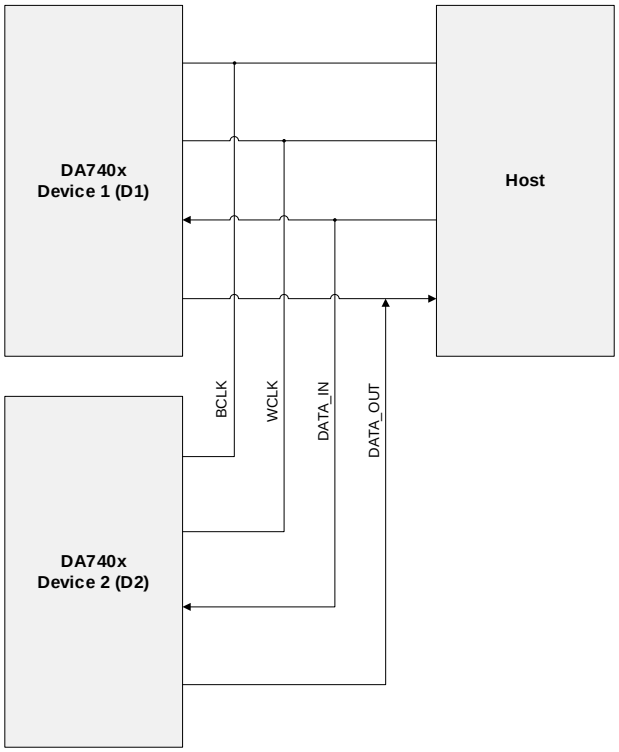


Figure 29: TDM Configuration

Time division multiplexing (TDM) mode allows multiple devices to communicate on the same bus without conflicting, see Figure 29. The serial data pin is tri-stated whenever the output is not valid to allow other devices on the bus to drive the data line.

TDM mode is available in both Master and Slave mode. TDM mode is an extension of LJF, see Figure 30 or DSP format, see Figure 31.

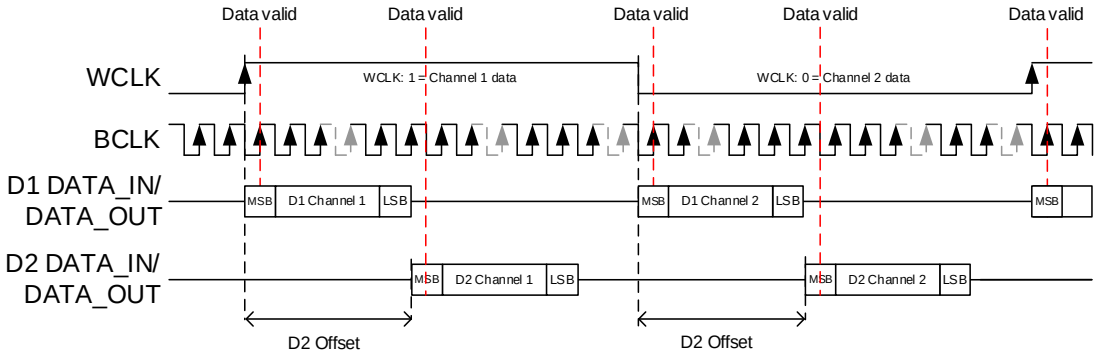


Figure 30: Two Devices in LJF with TDM Mode Active

In LJF with TDM mode active, the Device 2 (D2) Channel 1 data is offset by a configurable number of BCLK cycles (D2 Offset) after the rising edge of WCLK. The D2 Channel 2 data is valid the same number of BLCK cycles (D2 Offset) after the falling edge of WCLK.

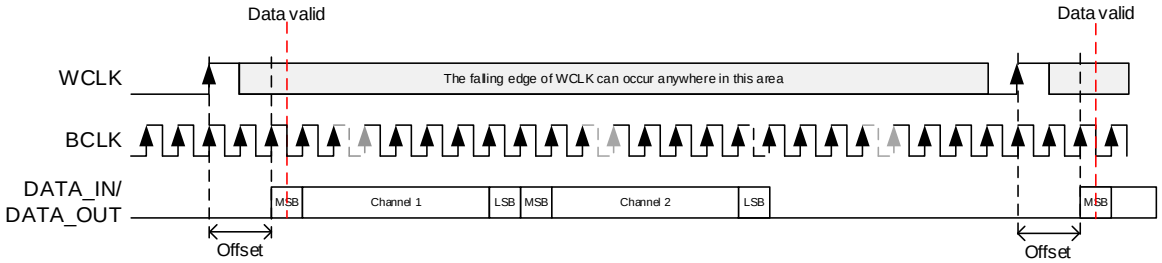


Figure 31: One Device in DSP Mode with Offset from TDM Mode

In DSP format with TDM mode active the start of frame is offset by a configurable number of BCLK cycles (Offset) from the rising edge of WCLK. The Channel 1 data is valid on the first falling edge of BCLK after the start of frame condition. Channel 2 data immediately follows Channel 1 data.

12.5 Sample Rate Converter

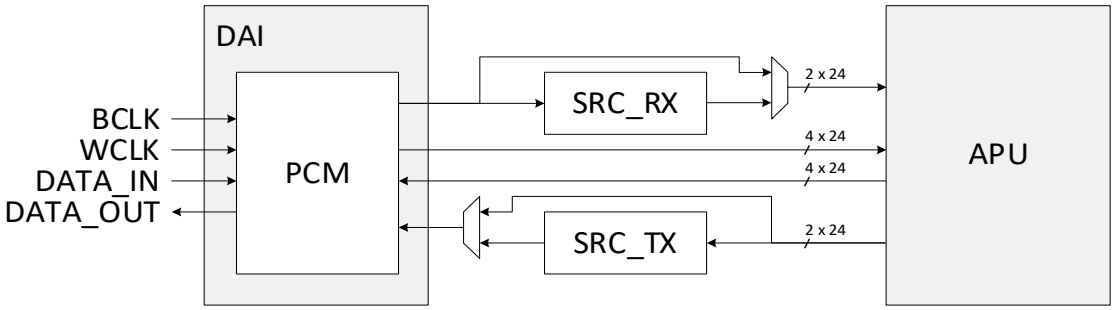


Figure 32: SRC Block Diagram

The SRC has a receiving (RX) converter (SRC_RX), a transmitting (TX) converter (SRC_TX), and bypass options. The RX and TX paths are automatically enabled or disabled, as required, to save power.

The SRC supports conversion to/from 192 kHz to/from (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 96, 88.2, 176.4, 352.8, 384) kHz, see Section 15.7.3.

NOTE
352.8 kHz and 384 kHz must always be down-sampled to 192 kHz via the SRC.

13 Digital Microphones Interface

13.1 Introduction

The Digital Microphone Interface (DMIC IF) supports two digital microphones for talk applications. It decodes and routes single-bit pulse-density modulated (PDM) data from external digital microphones (DMIC).

Two DMIC channels are routed to the ADC input filters.

13.2 Features

- Supports two digital microphones
- Master-only interface providing DMIC clock output

13.3 Block Diagram

The DMIC IF block diagram is shown in Figure 33. All signals marked as 0.7056 MHz to 6.144 MHz are PDM streams.

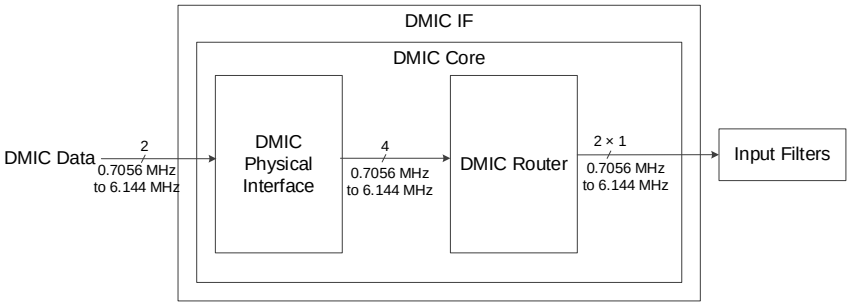


Figure 33: DMIC Interface Block Diagram

13.4 Block Architecture

The DMIC interface consists of the following:

- Physical Interface (data input and clock output pins)
- DMIC Router

13.5 Physical Interface

The DMIC IF consists of two data input pins, DMIC_DATA_A and DMIC_DATA_B, and a clock output pin, DMIC_CLK_AB, see Figure 2. The DMIC data inputs support dual data rate, resulting in four physical input streams, of which any two can be routed to the input filters, see Figure 16.

The clock is always an output as the DMIC interface operates in Master mode only. The clock output supports the following frequencies:

- 768.0 kHz, 1.5360, 2.45760, 3.0720, and 6.1440 MHz (when sys_clk = 98.304 MHz)
- 705.6 kHz, 1.4112, 2.25792, 2.8224, and 5.6448 MHz (when sys_clk = 90.3168 MHz)

The DMIC IF pins are supplied by V_{DDIO} and expect incoming DMIC data at V_{DDIO} level.

13.5.1 Sampling DMIC Data

The DMIC data inputs support dual data rate; therefore, two DMICs can be connected to the DMIC input. The data of one channel is valid on the rising edge of the DMIC clock and the data of the other channel is valid on the falling edge of the DMIC clock.

The sample point is adjusted using register settings and supports a range of digital microphones, setups, and data-valid periods ((ensure that this does not violate the DA7400 setup time or hold time requirements), see Figure 34. Sample point adjustments also compensate for delays due to physical separation of the DMICs.

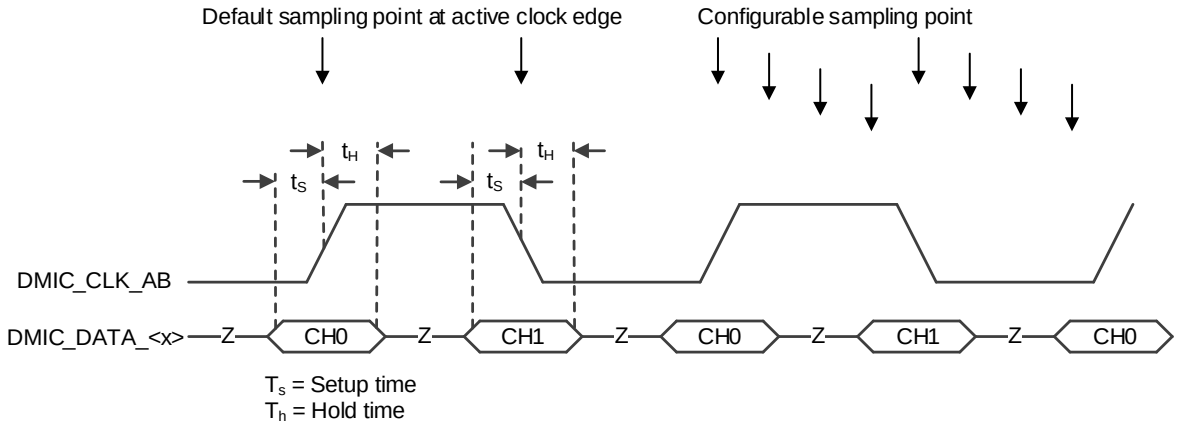


Figure 34: DMIC Interface Timing and Sampling Points

Setup (t_S) time defines the minimum time the data must be settled for prior to the sampling point. Hold time (t_H) is the minimum time after the sampling point that the data must be stable for. The exact timing depends on the DMIC used.

The DMIC sampling point is programmable, the default sampling point is at the active edge of the clock. The available phase shifts are 0º, 36º, 72º, and 108º when using a 2.25792 MHz or 2.4576 MHz clock, and 0º, 45º, 90º, and 135º when using any other DMIC clock frequency see Section 15.9.1.

13.6 DMIC Router

De-interleaved DMIC input data signals are routed through a register-configurable router, see Section 15.9.2. The router allows complete freedom in connecting DMIC input data to internal microphone talk (TK) signals, see Figure 35.The talk path is muxed with the ADC in the input filters of the input path block, see Section 10.

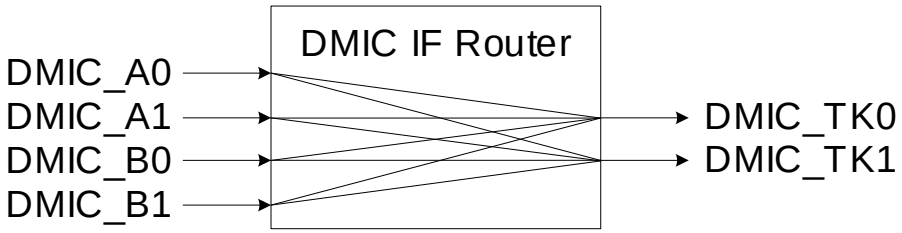


Figure 35: DA7400 DMIC Interface Router

14 Signal Generator

14.1 Introduction

DA7400 includes a signal generator to produce, for example, beeps for button presses and comfort noise. The signal generator consists of a tone generator and a noise generator.

14.2 Block Diagram

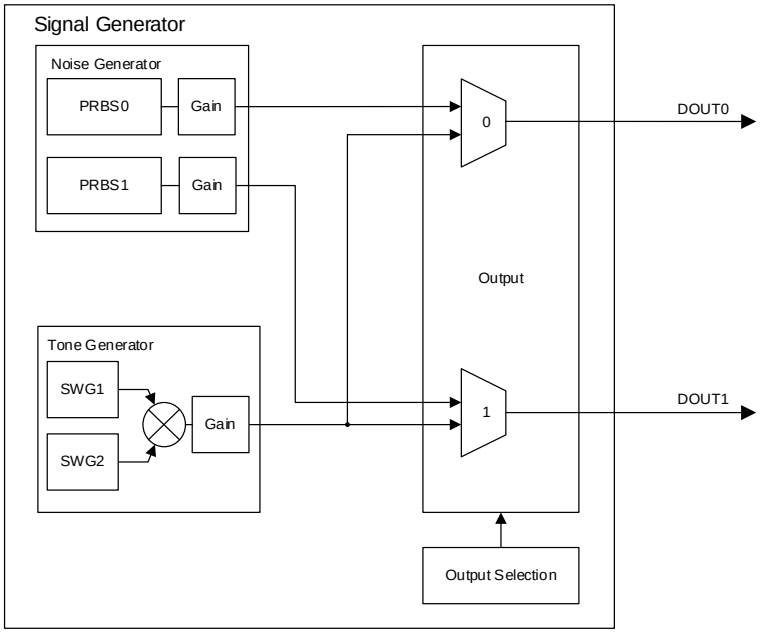


Figure 36: Signal Generator Block Diagram

14.3 Block Architecture

The tone generator generates two sine waves, with individually programmable frequencies, and mixes them together at the output. The noise generator generates pseudo-random binary sequences (PRBS) of noise. The output selection is programmable, see Section 15.10. Output paths can be configured as:

- both paths as tone
- both paths as noise
- a mixture of noise on one path and tone on the other

14.3.1 Tone Generator

The tone generator contains two sine wave generators (SWG), with independently programmable frequencies (20 Hz to 12 kHz). The configurable output level of the mixed SWG signals, ranges from 0 dBFS to -44.5 dBFS in 1.5 dB steps. Alternatively, the tone generator produces a programmable DC level. The signal generator routes the output from the tone generator to both DOUT0 and DOUT1 output paths.

14.3.2 Noise Generator

The noise generator contains two independent PRBS generators with adjustable gain. The output of PRBS0 is routed to the DOUT0 output path and the output of PRBS1 is routed to the DOUT1 output path. PRBS0 and PRBS1 generate noise based on individually programmable seed and polynomial settings.

15 Programming

15.1 Overview

This section provides a detailed description of the programming requirements for DA7400. There are important features of the device programming to understand before progressing with the detailed programming.

15.1.1 Set Switching

Sets are used to achieve seamless (pop-and-click free) operation when changes to multiple registers and bits are required; for example, when a call is answered while playing music. DA7400 uses two sets of duplicated registers (SET0 and SET1) to simultaneously switch audio path configuration, see Figure 37.

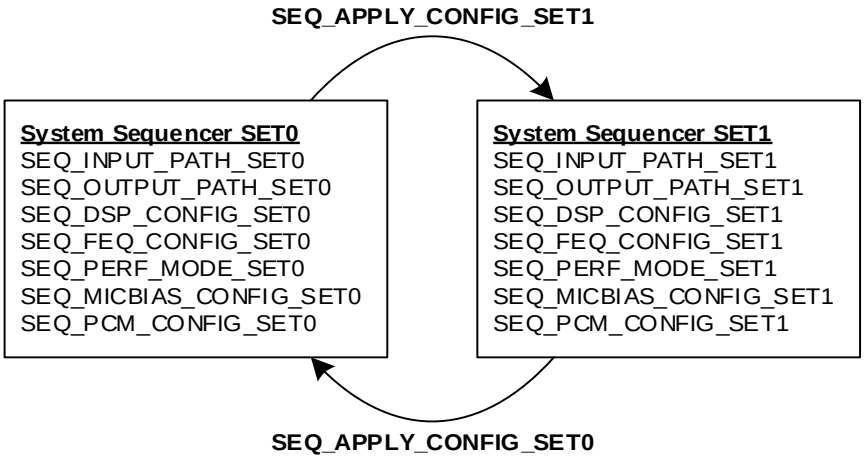


Figure 37: Set Switching

At any given time, only one set is actively controlling operation. Values in the other (inactive) set can be updated without immediately affecting operation. When all changes in the inactive set are complete it can be applied, causing all path configuration elements to be activated in unison, see Section 15.2.

NOTE
Audible artifacts may be produced if the path configuration is changed by writing to the registers in the active set. To prevent this, write to the registers in the inactive set then activate these registers simultaneously using a set switch operation.

15.1.1.1 Set Switch Operation

When a set switch operation is performed, all paths enabled in the currently active set are cleanly ramped down, then all paths in the next active set are cleanly ramped up. If the currently active set has no paths enabled, then the new active set paths are ramped up immediately. If the new active set has no paths enabled then the currently active set simply ramps down.

Two blocks of SRAM program memory are available, see Section 15.2.1.1, so that set switches with changes to the DSP program are possible (for example when answering a call while playing music). If the memory bank content does not change between set switches, then both sets can be configured to point to the same memory block, see Section 9.6.

NOTE
The sets only include some configuration registers. Updates to shared registers (those not included in the sets; for example, those which control the PLL or DAC settings) are achieved by switching to a set with no paths

NOTE
enabled, updating the set and shared registers required for the new configuration, then switching set again, see Section 15.2.2.

15.1.2 Programming Model

A device with no audio paths configured in its active set is in the low power STANDBY state. A device that has one or more audio paths configured in its active set is in the ACTIVE state. When the device is first enabled it will enter the STANDBY state with SET0 as the active set.

When a device is in the STANDBY state, it is safe to write to any registers that are not in the active set. The registers can be written to in any order, with a set switch operation being performed last.

When a device is in the ACTIVE state, **only** the registers in the inactive set can be written to safely.

It is recommended that one of the following two programming models are used:

15.1.2.1 Programming Model 1: SET0 for STANDBY and SET1 for ACTIVE

This programming model is the simplest approach. In this model, SET1 is always used for audio functionality, and SET0 is used to perform reconfiguration. SET0 registers are never updated from their default values. Switching to SET1 enables the path(s); and switching to SET0 disables the path(s).

15.1.2.2 Programming Model 2: Flexible

This programming model presents a more complex approach. It uses both SET0 and SET1 to quickly and dynamically move between different ACTIVE profiles and the STANDBY state. Example profile switches could be between music playback, voice call, or others.

To achieve this, the inactive set of registers is reconfigured (including any SRAM memory bank updates) during the ramp-down stage of the active set, see Figure 38.

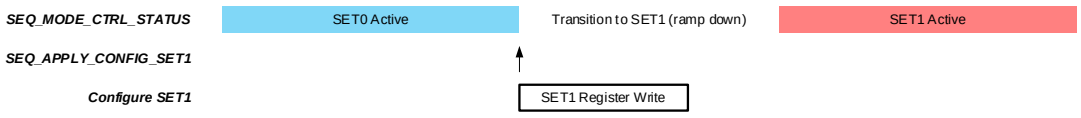


Figure 38: Configuring a New Set

15.1.3 Default Values

Default values have been assigned to registers to enable configuration with minimal I^2C accesses. For example, by default the PLL is configured to accept a 12.288 MHz reference on the MCLK pin. Typically, the blocks requiring the most configuration will be the DAI and DMIC (to assign channels), the PLL (if the reference is not 12.288 MHz), and the Sequencer (to configure sample rates and audio paths).

15.2 Sequencer

This section describes how to program the system sequencer, see Section 7. The sequencer consists of SET0 registers, SET1 registers, and shared (not in SET0 or SET1) registers.

15.2.1 Set Programming

SET0 and SET1 are referred to in this subsection as SET<x>. For example, when describing a register as REGISTER_SET<x>, when x = 0 the corresponding set is SET0 and when x = 1 the corresponding set is SET1.

A set switches when 0x1 is written to register SEQ_APPLY_CONFIG_SET<x>. The SEQ_MODE_CTRL_STATUS register identifies the currently active set, see Section 15.1.1.

NOTE
Audible artifacts may be produced if the path configuration is changed by writing to the registers in the active set. To prevent this, write to the registers in the inactive set then activate these registers simultaneously using a set switch operation.

15.2.1.1 Path Setup

The SEQ_INPUT_PATH_SET<x> registers enable or disable the left and right talk microphone paths. The paths include the microphones, the ADC, and the input filters. The path is activated only when the corresponding set is activated, see Section 15.5.

The SEQ_OUTPUT_PATH_SET<x> registers enable or disable the left and right headphone paths. The paths include the headphone amplifier, the DAC, and the output filters. The path is activated only when the corresponding set is activated, see Section 15.5. For details on other output configurations, for example the charge pump and the output gain, see Section 15.6.

The SRAM_SEL_SET<x> bit of the SEQ_DSP_CONFIG_SET <x> registers select which SRAM memory bank (PROG-0 or PROG-1) the APU runs from, see Section 9.4. The APU is only running when the device is in ACTIVE mode.

The SEQ_PERF_MODE_SET<x> registers control the power and performance of the headphone output path when the corresponding set is activated. Setting this register to 0x00 runs the output path in High-Performance mode, setting this register to 0x01 runs the output path in Low Power mode.

The SEQ_MICBIAS_CONFIG_SET<x> register enables or disables the microphone bias during audio bring up when the corresponding set is activated. The microphone bias voltage is selected in the shared register SEQ_MICBIAS_VOLTAGE, see Section 15.2.2.

The SEQ_PCM_CONFIG_SET<x> register enables or disables the PCM digital audio interface (DAI) when the corresponding set is activated. For details of other DAI configurations, for example the data format and channel selection, see Section 15.7.

15.2.2 Shared Sequencer Registers

The microphone bias voltage is configured by the shared register SEQ_MICBIAS_VOLTAGE and is enabled when the SEQ_MICBIAS_CONFIG_SET<x> register is activated on the corresponding set switch.

The SEQ_SR_CONFIG shared register selects the DAI sample rate and the system sample rate (SSR). The DAI sample rate is set via the PCM_SR bits.

The stereo sample rate converter (SRC) is automatically enabled when the DAI sample rate is either 352.4 kHz or 384 kHz. When the SRC is enabled, the system sample rate (SSR) is 192 kHz regardless of the DAI sample rate. The SRC can be programmed to force the SSR = 192 kHz via the SR192_EN bit in the SEQ_SR_CONFIG register.

The SEQ_MIC_MUTE_CTRL shared register individually mutes and unmutes the left and right analog microphone inputs if they are enabled in the active set, see Section 15.2.1.1

The CLKS_SW_RST generates a software reset, all registers (including those in an active set) are reset to their defaults.

NOTE
The software reset is instant and may cause audio artifacts. Return to the STANDBY state prior to writing to this register.

The CLKS_FSI_FREQ register controls the power and performance of the analog input path when the record path is active. Setting this register to 0x00 runs the ADC at 6 MHz in High-Performance mode, setting this register to 0x01 runs the ADC at 3 MHz in Low-Power mode with a small degradation in audio performance.

15.2.3 Sequencer Status Monitoring

Three read only registers are provided to monitor the sequencer:

- SEQ_MAIN_SM_STATE shows the current state of the device
- SEQ_MODE_CTRL_STATUS shows the current state of SET<x> including whether a switch is in progress
- SEQ_STATUS_RO returns information on the clocking setup
  - SRC_EN_RO bit indicates whether the SRC is enabled
  - ANC_EN_RO is not applicable to DA7400
  - DSP_SR_RO bits show the current SSR

15.3 Clocking

When DA7400 is in ACTIVE state, the PLL produces the system clock. When the device is in the STANDBY state the PLL is bypassed and the internal oscillator produces the system clock, see Section 8.5.

15.3.1 Selecting the PLL Input Clock

There are two inputs to the PLL: MCLK and BCLK. The inputs are selected by the CLK_SEL bits in the PLLD_CONFIG_2 register.

15.3.2 Configuring the Input Divider

The PLL expects a reference clock (ref_clk) of between 2.5 MHz and 5 MHz. The incoming clock (in_clk) is divided to within this range using the INDIV bits in the PLLD_CONFIG_2 register.

15.3.3 Programming the Feedback Divider

The feedback divider is programmed to enable the PLL to output the required system clock (sys_clk). DA7400 supports three system clocks depending on the DAI sample rate and SSR, see Section 8.5.1.3.

The feedback divider is a 20-bit value consisting of 13 fractional bits stored in the PLLD_FBDIV_FRAC_B0 and PLLD_FBDIV_FRAC_B1 registers and 7 integer bits stored in the PLLD_FBDIV_INTEG register. The value to be written to these registers is calculated as:

FBDIV = sys_clk * 2 / ref_clk

The fractional component of this value should be multiplied by 2^{13}, converted to binary and then written to the PLLD_FBDIV_FRAC_B0 and PLLD_FBDIV_FRAC_B1 registers. The integer component of the FBDIV is converted to binary and written directly to the PLLD_FBDIV_INTEG. For an example calculation of FBDIV and the corresponding register settings, see Section 15.3.6.

15.3.4 Enabling Sample Rate Matching

Enable SRM whenever the DAI is in Slave mode and the PLL input clock is MCLK. The SRM is enabled by setting the PLL_SRM_MODE bits in the PLLD_CONFIG_1 register.

15.3.5 PLL Status Monitoring

The PLL generates several interrupt events when the PLL and SRM lock or lose lock. The interrupts are read in the PLLD_STATUS register, cleared in the PLLD_EVENT register, and masked in the PLLD_IRQ_MASK register. By default, all the PLL events are masked and do not toggle the nIRQ pin.

15.3.6 PLL Calculation Example

Follow the steps outlined below to configure the PLL with the following setup:

- 35 MHz MCLK as input clock
- DAI in Master mode
- SSR = 192 kHz
- DAI sample rate = 48 kHz

Configuration steps

1. Set CLK_SEL = 0, to set the input clock as MCLK.
2. Set bits INDIV = 0x5, to divide the incoming clock by 8 to get a ref_clk in the range of 2.5 MHz to 5 MHz.
3. Set bits PLL_SRM_MODE = 0x0 to disable SRM (DAI in Master mode).
4. Calculate FBDIV (when DAI rate is 48 kHz, the required system clock is 98.304 MHz, see Section 15.3.3):

   FBDIV = (sys_clk * 2) ÷ ref_clk

   => FBDIV (98.304 MHz * 2) ÷ (35 MHz / 8)

   => FBDIV = 44.93897143

5. Multiply fractional part => 0.93897143 * 2^{13} = 7692 (decimal).
6. Convert fractional multiplication to binary => 0x1E0C.
7. Write fractional values to registers:
   PLLD_FBDIV_FRAC_B0 = 0x0C.
   PLLD_FBDIV_FRAC_B1 = 0x1E.
8. Write integer value to register
   PLLD_FBDIV_INTEG = 44 (decimal) = 0x2C.

15.4 Audio Processing Unit

The audio sequencer controls the enabling and disabling of the APU, see Section 9. Program the registers in the APU before switching the set.

15.4.1 APU Gain Control

The APU gain control is profile dependent and is typically used to control the output to the headphones. The APU_USER_GAIN_C0_DB and APU_USER_GAIN_C1_DB provide gain control in 1 dB steps for Channels 0 and 1. The APU_USER_GAIN_C0_FINE and APU_USER_GAIN_C1_FINE provide finer gain control in 0.0625 dB steps for Channels 0 and 1.

Changes to the APU gain are linearly ramped at the rate set in the APU_GAIN_RATE register.

15.4.2 Reading and Writing Memories

The two SRAM program memories, PROG-0 and PROG-1, and the data memory can be written to whenever the device is in the STANDBY or ACTIVE state, see Section 9.6. The memory can be read and written to directly a byte at a time or indirectly a word (4 bytes) at a time via the mailbox for atomic reads and writes.

To write to the SRAM memory banks via the mailbox:

1. Write the first address of the data into the APU_ADDR_B0 and APU_ADDR_B1 registers.
2. Write the data into the APU_WDATA_B0, APU_WDATA_B1, APU_WDATA_B2, and APU_WDATA_B3 registers.
3. Trigger the write by writing 0x1 to the APU_WT register.

To read from the SRAM memory bank via the mailbox:

1. Write the first address of the data into the APU_ADDR_B0 and APU_ADDR_B1 registers.
2. Trigger the read by writing 0x1 to the APU_RT register.
3. Read the data from the APU_RDATA_B0, APU_RDATA_B1, APU_RDATA_B2, and APU_RDATA_B3 registers.

15.4.3 DSP Input Selection

If channels three to six are required then the APU_FF_MXDSP_C0_SEL, APU_FF_MXDSP_C1_SEL, APU_FB_MXDSP_C0_SEL, APU_FB_MXDSP_C1_SEL registers are used to select these.

15.4.4 DSP Status Monitoring

The DSP can generate an interrupt event. The interrupt can be read in the APU_STATUS register, can be cleared in the APU_EVENT register, and masked in the APU_IRQ_MASK register. By default, the APU event is masked and does not toggle the nIRQ pin.

15.4.5 DSP Programs

Dialog Semiconductor will provide DSP programs. A DSP program is maximum 2 kB long. To load these programs, see Section 15.4.2.

15.5 Input Path

The audio sequencer enables and disables the input path, see Section 10. Program the input path registers before switching to an active set, see Section 15.2.

15.5.1 Input Filters Selection

The input path filters take either the ADC data from the analog microphone inputs or stereo data from a pair of digital microphone inputs. The input selection is made via the INPS_PATH_DATA_SEL register.

15.5.2 Gain Control

The input path contains two gain stages, analog gain in the microphone amplifier and digital gain in the input filters. The analog gain is controlled by the INPS_ANALOG_GAIN_CH0 and INPS_ANALOG_GAIN_CH1 registers from 0 dB to +30 dB in 6 dB steps. Analog gain is not available if the input path is using a digital microphone.

The digital gain is controlled by the INPS_DIGITAL_GAIN_CH0 and INPS_DIGITAL_GAIN_CH1 registers from -83.25 dB to +12 dB in 0.75 dB steps.

15.5.3 High-Pass Filter

An optional DC blocking high-pass filter (HPF) is available. The HPF is enabled by the HPF_EN bit in the INPS_HPF_FILTER_CONFIG register. Set the corner frequency of the filter based on the SSR:

- if SSR ≤ 32 kHz use the HPF_LOW_CORNER bits in the INPS_HPF_FILTER_CONFIG register
- if SSR > 32 kHz use the HPF_HIGH_CORNER bits in the INPS_HPF_FILTER_CONFIG register

15.5.4 Automatic Level Control Setup

The ALC is enabled for each channel in the INPS_ALC_ENABLE register.

For optimal dynamic range when using analog microphones, configure the ALC to automatically adjust both the analog and digital gains via the INPS_ALC_GAIN_MODE register. When using digital microphones set INPS_ALC_GAIN_MODE to digital only, see Section 10.9.

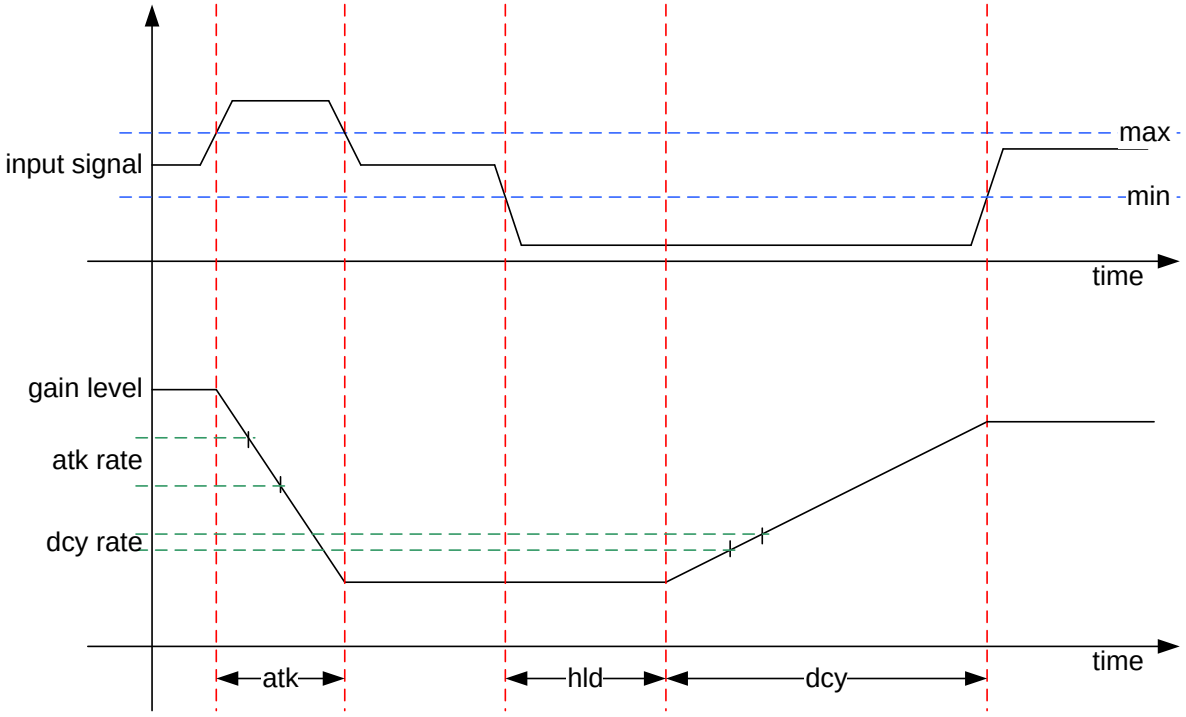


Figure 39: Gain Change Thresholds and Attack, Hold, and Decay Times

Set the minimum (min) and the maximum (max) input signal thresholds that trigger a gain change by the ALC in the INPS_ALC_MIN_THR and INPS_ALC_MAX_THR registers, see Figure 39.

Although the ALC is controlling the gain of the input path, it does not modify any of the gain registers. These registers are ignored while the ALC is in operation. The minimum and maximum levels of gain that can be applied by the ALC are controlled using the INPS_ALC_DIG_GAIN_LIMITS and INPS_ALC_ANA_GAIN_LIMITS registers.

The rates at which the gain is changed are defined by the attack (atk) and decay (dcy) rates in register INPS_ALC_ATTACK_RELEASE. When attacking, the gain decreases with ALC_ATTACK rate. When decaying, the gain increases with ALC_RELEASE rate.

The hold-time is defined by ALC_HOLD in the INPS_ALC_HOLD register. This controls the length of time that the system maintains the current gain level before starting to decay. This prevents unwanted changes in the recording level when there is a short-lived spike in input volume; for example, when recording speech.

Typically, the attack rate should be much faster than the decay rate. To avoid clipping it is necessary to reduce rapidly increasing waveforms as quickly as possible, whereas fast release times will result in the signal appearing to pump. The ALC also has an anti-clip function that applies a very fast attack rate when the input signal is close to full scale. This prevents clipping of the signal by reducing the signal gain at a faster rate than would normally be applied. The anti-clip function is enabled in the INPS_ALC_ANTICLIP_ENABLE register, and the trigger threshold is set in the INPS_ALC_ANTICLIP_THR register. This reduces the gain at a rate of 0.034 dB per sample to 0.272 dB per sample depending on the setting in the INPS_ALC_ANTICLIP_STEP register.

A recording noise-gate prevents the gain of the channel increasing when there is no signal, or when only a noise signal is present (noise pumping). When the level of the input signal drops below the noise threshold configured in the INPS_ALC_NOISE_THR register, the channel gain remains constant.

15.5.5 Level Detect

The level detect is enabled in the INPS_LVL_DET_EN register. The threshold uses the INPS_ALC_ANTICLIP_THR value as the trigger level.

When the threshold is exceeded the INPS_STATUS register will return 0x1 and an interrupt will be generated on the nIRQ pin. The interrupt is cleared by writing to the INPS_EVENT register, this can be masked by writing to the INPS_IRQ_MASK register.

When the level detect is enabled the ALC is automatically disabled, see Section 15.5.4.

15.6 Output Path

The audio sequencer enables and disables the output path, see Section 11. Program the registers in the output path in an inactive set. The new settings only take effect once the set is activated, see Section 15.2.

15.6.1 Fixed Gain

The fixed gain of the output path is controlled by the OUTS_FIXED_GAIN register, which applies gain to both the left and right output channels from -77.25 dB to +18 dB in 0.35 dB steps. Set this register to 0x00 to mute the audio output. DA7400 automatically selects the optimal balance of analog and digital gain to maximize dynamic range.

The fixed gain must be set to the desired value prior to activating the headphone outputs via the audio sequencer, see Section 7.6. Variable gain (volume control) of the individual left and right outputs is performed via the APU gain control registers, see Section 15.4.1.

15.6.2 High-Pass Filter

DC offset is optionally removed from the DAC by a first order HPF. This is enabled in the OUTS_HPF_EN register. The cut-off for this filter depends on the SSR with a frequency of $7.8 * 10^{-5} * SSR$; for example, at 48 kHz the filter cut off frequency is 3.744 Hz.

15.6.3 Headphone Charge Pump

The signal level where the headphone charge pump switches between ±1.8 V and ±0.9 V is controlled by the HPCP_V_THRESHOLD register, see Section 11.8. The switching threshold can be configured to be between -2 dBFS and -17 dBFS in 1 dB steps.

15.7 Digital Audio Interface

The audio sequencer enables and disables the DAI, see Section 12. Program the registers in the DAI before switching to an active set. The new settings only take effect once the set is activated, see Section 15.2.

15.7.1 Configuring the DAI

DA7400 has support for up to 16 slots on the DAI interface. DA7400 uses up to 6 slots, the total number of active slots on the bus is selected in the DAI_SLOT_CNT register.

15.7.1.1 Master/Slave Mode

The DAI operates in either Master or Slave clocking mode; set the mode in the DAI_MODE register.

15.7.1.2 Slot Count

The incoming and outgoing PCM data on the DAI is configured to transmit on 1 to 16 slots. The number of active slots on the bus is set in the DAI_SLOT_CNT register.

15.7.1.3 Data Format

The DAI supports I^2S, left-justified, right-justified and DSP data formats, these are selected by the FORMAT bits of the DAI_CONFIG register.

15.7.1.4 Frame Length

In Master mode the FRAME_LEN bits of the DAI_CONFIG register controls the frame length (number of BCLKs per WCLK). The DAI supports 32, 64,128, 256, or 512 BCLKs per WCLK in Master mode. These register bits are ignored in Slave mode.

15.7.1.5 Word Length

The DAI_W_LEN register sets the number of bits of valid audio data per channel per frame on the PCM_DATA_OUT and PCM_DATA_IN pins. The DAI supports 16, 20, 24, and 32 bits. Unused bits are zero filled.

15.7.1.6 Data Control

Data Sampling Point

Either edge of BCLK can be used to sample the data. Configure this via the BCLK_POL bit in the DAI_DATA_OUT_CTRL register. Setting BCLK_POL = 0x0 receives data on the rising edge of BCLK and transmits data on the falling edge. Setting BCLK_POL = 0x1 transmits data on the rising edge of BCLK and receives data on the falling edge.

PCM Frame Start

Either edge of WCLK can be used to define the start of the PCM frame. Configured this via the WCLK_POL bit in the DAI_DATA_OUT_CTRL register:

- for left-justified, right-justified and DSP data formats setting WCLK_POL = 0x0 indicates the start of the PCM frame is on the rising edge and setting WCLK_POL = 0x1 indicates the falling edge
- for I^2S data format setting WCLK_POL = 0x0 indicates the start of the PCM frame is on the falling edge and setting WCLK_POL = 0x1 indicates the rising edge

Multiple Devices on Data Output Line

The data out pin (PCM_DATA_OUT) can be set to a high-impedance state when not in use to allow multiple devices to share the same data line.

In the DAI_DATA_OUT_CTRL register:

- set DATA_OUT_EN = 0x0 or 0x1 to disable all the outputs and make the PCM_DATA_OUT pin high-impedance
- set DATA_OUT_EN = 0x2 to drive DATA_OUT continuously
- set DATA_OUT_EN = 0x3 to drive DATA_OUT during enabled slots only

15.7.1.7 Offset

The DAI offset can be configured to select where Channel 0, and subsequent channels, occur in the frame. The combined value of the DAI_OFFSET_MSB and DAI_OFFSET_LSB registers selects the number of bits after the default data formatting that Channel 0 data starts at, see Figure 30.

15.7.2 DAI Channel Selection

DA7400 can process up to six channels of audio data on the DAI. The inputs map to the corresponding DSP inputs Ip0 to Ip5, see Section 9.4.1. The outputs map to the corresponding DSP outputs Op2 to Op7, see Section 9.4.2.

The DAI_ADC<x>_CH registers select which slot on the DAI each corresponding channel is inserted on, selecting 0x0 disables the channel.

The DAI_DAC<x>_CH registers select which slot on the DAI each corresponding channel is received from, selecting 0x0 disables the channel.

DA7400 has support for up to 16 slots on the DAI that each channel can occupy.

15.7.3 Sample Rate Converter

When using the SRC the correct over-sampling ratio must be selected in the SRCRX_OSR_IN and SRCTX_OSR_OUT registers based on the DAI sample rate.

DAI Sample Rate (kHz)	SRCRX_OSR_IN and SRCTX_OSR_IN Settings
8 to 96	0x00
176.4 or 192	0x01
Reserved	0x02
352.8 or 384	0x03

15.8 Digital Microphone Interface Programming

The audio sequencer enables and disables the digital microphone paths. Program the registers in this section before switching to a new active set. The new settings only take effect once the set is activated, see Section 15.2.

15.8.1 DMIC Input Enable

Each of the two stereo DMIC interfaces are enabled when either of their channels are enabled using the DMIC_<x><n>_EN registers (where x = A or B and n = 0 or 1). When either channel of either DMIC_A or DMIC_B is enabled the DMIC_AB_CLK output will be enabled.

NOTE
The DMIC inputs are only enabled when the system is placed into ACTIVE state via the audio sequencer (see Section 7.6).

15.9 DMIC Clock Frequency Selection

The frequency of the DMIC clocks are controlled via the DMIC_AB_CLK_FREQ_SEL. DMIC_C_CLK_FREQ_SEL register is not applicable to DA7400.

15.9.1 DMIC Data Sampling Point

The DMIC_<x>_CLK_SAMP_PH registers control where the DMIC data is sampled relative to both DMIC clock edges. For most DMIC clock frequencies the sample point is a multiple of 45º, however for DMIC clock frequency of 2.25792 MHz or 2.4576 MHz, the sample point is a multiple of 36 º from the clock edge.

15.9.2 DMIC Router Configuration

Each of the four DMIC inputs can be routed to any of two different internal paths from the DMIC_<xxx>_SEL registers (where xxx = TK0, or TK1). The DMIC_<xxx>_SEL registers (where xxx = FF0, FF1, FB0, or FB1) are not applicable for DA7400.

DMIC_<xxx>_SEL Register Setting	Selected Input
0x0	No connections
0x1	A0
0x2	A1
0x3	B0
0x4	B1

The TK0 and TK1 signals are routed to the input path filters and may be further programmed, see Section 15.5.

15.10 Signal Generator

This chapter describes the programming for the signal generator, see Section 15.10.

15.10.1 Tone Generator

The output to the APU is selected by the SWG_SEL bits of the TONEG_CFG2 register.

15.10.1.1 Sine Wave Generator Frequency Selection

Each SWG can generate a sine wave at a frequency (FREQ[15:0]) from approximately 1 Hz to 12 kHz according to the programmed 16-bit value.

NOTE
The SWGs should not be programmed with a frequency greater than the Nyquist frequency (SSR/2).

For each SWG, the required generated frequency is set in two 8-bit registers TONEG_FREQ<n>_<x> where n= 1 or 2 (SWG1 and SWG2 respectively), and x = U and L (upper and lower bits).

- SWG1 is set in FREQ1_U = FREQ[15:8] and FREQ1_L = FREQ[7:0]
- SWG2 is set in FREQ2_U = FREQ[15:8] and FREQ2_L = FREQ[7:0]

15.10.1.2 DC Output

The tone generator DC output is programmed via the TONEG_DC_OUT register. Select the level in the DC_SEL bits and enable the DC output by setting DC_EN = 0x1.

If the SWG_SEL bits have been set to output DC with ramp then, when enabled, the tone generator will perform a ramp to the DC level at the SWG1 rate to avoid generating a DC pop. Disabling the tone generator with these settings will ramp the DC level down at the SWG1 rate.

15.10.1.3 Gain

The gain of the tone generator is configured in the TONEG_GAIN register from 0 dB to -44.5 dB. Gain is not applied if the tone generator is set to output a DC level.

15.10.1.4 Enabling and Disabling the Tone Generator

The tone generator is enabled by writing 0x1 and disabled by writing 0x0 to the START_STOPN bit of the TONEG_CFG2. When stopping the tone generator will continue until the next zero cross to avoid pops and clicks.

15.10.2 Noise Generator

The stereo PRBS noise generator has controllable gain, seed, and polynomial for each channel. The PRBS uses two 32-bit Galois format linear-feedback shift registers (LFSR).

15.10.2.1 Seed Programming

Each of the two LFSR seeds is programmed by writing to the PRBS_SEED<n>_B<n> registers. Each seed consists of four registers to form a 32-bit word. The seed value is loaded into the LFSR via the PRBS_CLEAR_CTRL register.

15.10.2.2 Polynomial Programming

An LFSR of any given size m (bits) can produce every possible state during the period $N = 2^m - 1$, but will do so only if proper feedback terms have been chosen. The polynomial registers' defaults contain a maximum length LFSR feedback term for a 32-bit word.

Each of the two LFSR polynomials can be programmed by writing to the PRBS_POLY<n>_B<n> registers. Each polynomial consists of four registers to form a 32-bit word.

15.10.2.3 Gain

The gain of each of the PRBS outputs is controlled from 0 dB to -144 dB in 6 dB steps via the PRBS_GAIN0_CTRL and PRBS_GAIN1_CTRL registers respectively.

15.10.2.4 Enable and Disable

The enabling and disabling of each of the PRBS outputs is controlled via the PRBS_CTRL register. Enabling the PRBS will disable the tone generator if it is enabled. Disabling the PRBS will re-enable the tone generator if it is enabled.

16 Register Definitions

16.1 Register Map

Table 24: Register Map

Addr	Register	7	6	5	4	3	2	1	0	Reset
Sequencer										
Chip IDs										
0x0200	SEQ_CHIP_ID_HI	CHIP_ID_HI<7:0>								0x26
0x0201	SEQ_CHIP_ID_LO	CHIP_ID_LO<7:0>								0x69
0x0202	SEQ_CHIP_VAR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHIP_VAR<1:0>		0x02
0x0203	SEQ_CHIP_REV	CHIP_REV_MAJOR<3:0>				CHIP_REV_MINOR<3:0>				0x00
System Sequencer - SET0										
0x0206	SEQ_INPUT_PATH_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MICR_EN_SET0	MICL_EN_SET0	0x00
0x0207	SEQ_OUTPUT_PATH_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPR_EN_SET0	HPL_EN_SET0	0x00
0x0208	SEQ_DSP_CONFIG_SET0	Reserved	Reserved	Reserved	SRAM_SEL_SET0	FFR_EN_SET0	FBR_EN_SET0	FFL_EN_SET0	FBL_EN_SET0	0x60
0x0209	SEQ_FEQ_CONFIG_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FEQ_MODE_SET0<1:0>		0x00
0x020A	SEQ_PERF_MODE_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LP_MODE_SET0	0x00
0x020B	SEQ_MICBIAS_CONFIG_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MICBIAS_EN_SET0	0x00
0x020C	SEQ_PCM_CONFIG_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCM_EN_SET0	0x00
0x020D	SEQ_APPLY_CONFIG_SET0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	APPLY_CONFIG_SET0	0x01

Addr	Register	7	6	5	4	3	2	1	0	Reset
System Sequencer - SET1										
0x020E	SEQ_INPUT_PATH_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MICR_EN_SET1	MICL_EN_SET1	0x00
0x020F	SEQ_OUTPUT_PATH_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPR_EN_SET1	HPL_EN_SET1	0x00
0x0210	SEQ_DSP_CONFIG_SET1	Reserved	Reserved	Reserved	SRAM_SEL_SET1	FFR_EN_SET1	FBR_EN_SET1	FFL_EN_SET1	FBL_EN_SET1	0x70
0x0211	SEQ_FEQ_CONFIG_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FEQ_MODE_SET1<1:0>		0x00
0x0212	SEQ_PERF_MODE_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LP_MODE_SET1	0x00
0x0213	SEQ_MICBIAS_CONFIG_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MICBIAS_EN_SET1	0x00
0x0214	SEQ_PCM_CONFIG_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCM_EN_SET1	0x00
0x0215	SEQ_APPLY_CONFIG_SET1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	APPLY_CONFIG_SET1	0x00
Mode Control Status										
0x0216	SEQ_MODE_CTRL_STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MODE_CTRL_STATUS<1:0>		0x00
Microphone Bias Configuration										
0x0217	SEQ_MICBIAS_VOLTAGE	Reserved	Reserved	Reserved	Reserved	Reserved	MICBIAS_VOLT<2:0>			0x00
DAI/PCM Interface Sample Rate Configuration										
0x0218	SEQ_SR_CONFIG	Reserved	Reserved	PCM_SR<4:0>					SR192_EN	0x26
Device Status										
0x0219	SEQ_STATUS_RO	Reserved	DSP_SR_RO<4:0>					ANC_EN_RO	SRC_EN_RO	0x4C
Main FSM Status										
0x021B	SEQ_MAIN_SM_STATE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MAIN_SM_STATE<1:0>		0x00
Audio Sequencer Configuration										
0x021	SEQ_MIC_MUTE_CTRL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MICR_MUTE	MICL_MUTE	0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
C										
DAI										
DAI Configuration										
0x0301	DAI_MODE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MODE	0x00
0x0302	DAI_SLOT_CNT	Reserved	Reserved	Reserved	SLOT_CNT<4:0>					0x00
0x0305	DAI_CONFIG	Reserved	Reserved	Reserved	FRAME_LEN<2:0>			FORMAT<1:0>		0x00
0x0306	DAI_W_LEN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	W_LEN<1:0>		0x03
0x0307	DAI_DATA_OUT_CTRL	Reserved	Reserved	TDM_EARLY_RLS	DATA_OUT_EN<1:0>		Reserved	WCLK_POL	BCLK_POL	0x10
0x0309	DAI_OFFSET_MSB	Reserved	Reserved	Reserved	Reserved	OFFSET_MSB<3:0>				0x00
0x030A	DAI_OFFSET_LSB	OFFSET_LSB<7:0>								0x00
DAI ADC Channel Configuration										
0x030B	DAI_ADC1_CH	Reserved	Reserved	Reserved	ADC1_CH<4:0>					0x00
0x030C	DAI_ADC2_CH	Reserved	Reserved	Reserved	ADC2_CH<4:0>					0x00
0x030D	DAI_ADC3_CH	Reserved	Reserved	Reserved	ADC3_CH<4:0>					0x00
0x030E	DAI_ADC4_CH	Reserved	Reserved	Reserved	ADC4_CH<4:0>					0x00
0x030F	DAI_ADC5_CH	Reserved	Reserved	Reserved	ADC5_CH<4:0>					0x00
0x0310	DAI_ADC6_CH	Reserved	Reserved	Reserved	ADC6_CH<4:0>					0x00
DAI DAC Channel Configuration										
0x031B	DAI_DAC1_CH	Reserved	Reserved	Reserved	DAC1_CH<4:0>					0x00
0x031C	DAI_DAC2_CH	Reserved	Reserved	Reserved	DAC2_CH<4:0>					0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x031D	DAI_DAC3_CH	Reserved	Reserved	Reserved	DAC3_CH<4:0>					0x00
0x031E	DAI_DAC4_CH	Reserved	Reserved	Reserved	DAC4_CH<4:0>					0x00
0x031F	DAI_DAC5_CH	Reserved	Reserved	Reserved	DAC5_CH<4:0>					0x00
0x0320	DAI_DAC6_CH	Reserved	Reserved	Reserved	DAC6_CH<4:0>					0x00
SRC - RX										
SRC Configuration										
0x0416	SRCRX_OSR_IN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OSR_IN<1:0>		0x00
SRC - TX										
SRC Configuration										
0x0518	SRCTX_OSR_OUT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OSR_OUT<1:0>		0x00
DMIC Interface										
DMIC Channel Enables										
0x0600	DMIC_A0_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	A0_EN	0x00
0x0601	DMIC_A1_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	A1_EN	0x00
0x0602	DMIC_B0_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	B0_EN	0x00
0x0603	DMIC_B1_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	B1_EN	0x00
0x0604	DMIC_C0_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	C0_EN	0x00
0x0605	DMIC_C1_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	C1_EN	0x00
DMIC Clock Frequency Configuration										
0x0606	DMIC_AB_CLK_FREQ_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	AB_CLK_FREQ_SEL<2:0>			0x00
0x060	DMIC_C_CLK_FREQ_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	C_CLK_FREQ_SEL<2:0>			0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
7										
DMIC Clock Sampling Phase Configuration										
0x0608	DMIC_A_CLK_SAMP_PH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	A_CLK_SAMP_PH<1:0>		0x00
0x0609	DMIC_B_CLK_SAMP_PH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	B_CLK_SAMP_PH<1:0>		0x00
0x060A	DMIC_C_CLK_SAMP_PH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	C_CLK_SAMP_PH<1:0>		0x00
DMIC Router Configuration										
0x060B	DMIC_FF0_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	FF0_SEL<2:0>			0x00
0x060C	DMIC_FF1_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	FF1_SEL<2:0>			0x00
0x060D	DMIC_FB0_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	FB0_SEL<2:0>			0x00
0x060E	DMIC_FB1_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	FB1_SEL<2:0>			0x00
0x060F	DMIC_TK0_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	TK0_SEL<2:0>			0x00
0x0610	DMIC_TK1_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	TK1_SEL<2:0>			0x00
Input Filters										
Input Filter Configuration										
0x0700	INPS_PATH_DATA_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PATH_DATA_SEL	0x00
0x0701	INPS_HPF_FILTER_CONFIG	Reserved	HPF_EN	HPF_LOW_CORNER<2:0>			HPF_HIGH_CORNER<1:0>		Reserved	0x40
0x0702	INPS_ANALOG_GAIN_CH0	Reserved	Reserved	Reserved	Reserved	Reserved	A_GAIN0<2:0>			0x00
0x0703	INPS_ANALOG_GAIN_CH1	Reserved	Reserved	Reserved	Reserved	Reserved	A_GAIN1<2:0>			0x00
0x0704	INPS_DIGITAL_GAIN_CH0	Reserved	D_GAIN0<6:0>							0x6F
0x0705	INPS_DIGITAL_GAIN_CH1	Reserved	D_GAIN1<6:0>							0x6F

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x0706	INPS_DIGITAL_GAIN_RAMP_RATE	Reserved	Reserved	D_GAIN1_RMP_RATE<1:0>		Reserved	Reserved	D_GAIN0_RMP_RATE<1:0>		0x11
ALC Configuration										
0x070D	INPS_ALC_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ALC1_EN	ALC0_EN	0x00
0x070E	INPS_ALC_GAIN_MODE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ALC1_GAIN_MODE	ALC0_GAIN_MODE	0x00
0x070F	INPS_ALC_ATTACK_RELEASE	ALC_RELEASE<3:0>				ALC_ATTACK<3:0>				0x20
0x0710	INPS_ALC_HOLD	Reserved	Reserved	Reserved	Reserved	ALC_HOLD<3:0>				0x00
0x0711	INPS_ALC_NOISE_THR	Reserved	Reserved	ALC_NOISE_THR<5:0>						0x3F
0x0712	INPS_ALC_MIN_THR	Reserved	Reserved	ALC_MIN_THR<5:0>						0x3F
0x0713	INPS_ALC_MAX_THR	Reserved	Reserved	ALC_MAX_THR<5:0>						0x00
0x0714	INPS_ALC_DIG_GAIN_LIMITS	ALC_D_GAIN_MAX<3:0>				ALC_D_GAIN_MIN<3:0>				0xCD
0x0715	INPS_ALC_ANA_GAIN_LIMITS	Reserved	ALC_A_GAIN_MAX<2:0>			Reserved	ALC_A_GAIN_MIN<2:0>			0x50
0x0716	INPS_ALC_ANTICLIP_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ALC_ANTICLIP_EN	0x01
0x0717	INPS_ALC_ANTICLIP_THR	Reserved	ALC_ANTICLIP_THR<6:0>							0x73
0x0718	INPS_ALC_ANTICLIP_STEP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ALC_ANTICLIP_STEP<1:0>		0x00
Level Detection										
0x071F	INPS_LVL_DET_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LVL_DET1_EN	LVL_DET0_EN	0x00
Level Detection Interrupt Handling										
0x0720	INPS_EVENT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EVT_LVL_DET	0x00
0x0721	INPS_STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STA_LVL_DET	0x00
0x072	INPS_IRQ_MASK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IRQ_LVL_DET	0x01

Addr	Register	7	6	5	4	3	2	1	0	Reset
2										
Output Filters										
Output Filter Configuration										
0x0800	OUTS_HPF_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPF_EN	0x00
0x0801	OUTS_FIXED_GAIN	FIXED_GAIN<7:0>								0xCF
0x0804	OUTS_FEQ_CFG	Reserved	Reserved	Reserved	FEQ_MODE	Reserved	Reserved	FEQ1_SEL_N	FEQ0_SEL_N	0x03
Headphone Charge Pump										
HPCP Configuration										
0x0900	HPCP_V_THRESHOLD	Reserved	Reserved	Reserved	Reserved	V_THRESHOLD<3:0>				0x06
Clocking and Reset										
Clocking Configuration										
0x0A00	CLKS_FSI_FREQ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FSI	0x00
Software Reset										
0x0A01	CLKS_SW_RST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SW_RST	0x00
PLL/SRM										
PLL/SRM Configuration										
0x0B00	PLLD_FBDIV_FRAC_B0	FBDIV_FRAC_B0<7:0>								0x00
0x0B01	PLLD_FBDIV_FRAC_B1	Reserved	Reserved	Reserved	FBDIV_FRAC_B1<4:0>					0x00
0x0B02	PLLD_FBDIV_INTEG	Reserved	FBDIV_INTEG<6:0>							0x40
0x0B03	PLLD_CONFIG_1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLL_SRM_MODE<1:0>		0x00
0x0B04	PLLD_CONFIG_2	INDIV<2:0>			Reserved	Reserved	CLK_SEL<1:0>		OSC_SEL	0x60

Addr	Register	7	6	5	4	3	2	1	0	Reset
PLL/SRM Interrupt Handling										
0x0B05	PLLD_EVENT	Reserved	Reserved	Reserved	EVT_REFCLK_LOSS	EVT_PLL_LOCK	EVT_PLL_LOST_LOCK	EVT_SRM_LOCK	EVT_SRM_LOST_LOCK	0x00
0x0B06	PLLD_STATUS	Reserved	Reserved	Reserved	STA_REFCLK_LOSS	STA_PLL_LOCK	STA_PLL_LOST_LOCK	STA_SRM_LOCK	STA_SRM_LOST_LOCK	0x00
0x0B07	PLLD_IRQ_MASK	Reserved	Reserved	Reserved	IRQ_REFCLK_LOSS	IRQ_PLL_LOCK	IRQ_PLL_LOST_LOCK	IRQ_SRM_LOCK	IRQ_SRM_LOST_LOCK	0x3F
PRBS Signal Generator										
PRBS0 Configuration										
0x0C00	PRBS_SEED0_B0	SEED0_B0<7:0>								0xFF
0x0C01	PRBS_SEED0_B1	SEED0_B1<7:0>								0xFF
0x0C02	PRBS_SEED0_B2	SEED0_B2<7:0>								0xFF
0x0C03	PRBS_SEED0_B3	SEED0_B3<7:0>								0xFF
0x0C04	PRBS_POLY0_B0	POLY0_B0<7:0>								0x57
0x0C05	PRBS_POLY0_B1	POLY0_B1<7:0>								0x00
0x0C06	PRBS_POLY0_B2	POLY0_B2<7:0>								0x00
0x0C07	PRBS_POLY0_B3	POLY0_B3<7:0>								0x80
PRBS1 Configuration										
0x0C08	PRBS_SEED1_B0	SEED1_B0<7:0>								0xFF
0x0C09	PRBS_SEED1_B1	SEED1_B1<7:0>								0xFF
0x0C0A	PRBS_SEED1_B2	SEED1_B2<7:0>								0xFF
0x0C0B	PRBS_SEED1_B3	SEED1_B3<7:0>								0xFF
0x0C0	PRBS_POLY1_B0	POLY1_B0<7:0>								0xCC

Addr	Register	7	6	5	4	3	2	1	0	Reset
C										
0x0C0D	PRBS_POLY1_B1	POLY1_B1<7:0>								0x02
0x0C0E	PRBS_POLY1_B2	POLY1_B2<7:0>								0x00
0x0C0F	PRBS_POLY1_B3	POLY1_B3<7:0>								0x80
PRBS Gain										
0x0C10	PRBS_GAIN0_CTRL	Reserved	Reserved	Reserved	GAIN0<4:0>					0x00
0x0C11	PRBS_GAIN1_CTRL	Reserved	Reserved	Reserved	GAIN1<4:0>					0x00
PRBS Enable										
0x0C12	PRBS_CLEAR_CTRL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLEAR0	CLEAR1	0x00
0x0C13	PRBS_CTRL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN0	EN1	0x00
Sine Wave Signal Generator										
Tone Generator Configuration										
0x0C81	TONEG_CFG2	START_STOPN	Reserved	Reserved	Reserved	Reserved	Reserved	SWG_SEL<1:0>		0x00
0x0C82	TONEG_FREQ1_L	FREQ1_L<7:0>								0x55
0x0C83	TONEG_FREQ1_U	FREQ1_U<7:0>								0x15
0x0C84	TONEG_FREQ2_L	FREQ2_L<7:0>								0x00
0x0C85	TONEG_FREQ2_U	FREQ2_U<7:0>								0x40
0x0C89	TONEG_DC_OUT	Reserved	Reserved	DC_SEL<1:0>		Reserved	Reserved	Reserved	DC_EN	0x00
0x0C8A	TONEG_GAIN	Reserved	Reserved	Reserved	Reserved	GAIN<3:0>				0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
Analog Peripherals										
Temperature Interrupt Handling										
0x0D00	ANAR_EVENT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EVT_TEMP_SHUTD	EVT_TEMP_WARN	0x00
0x0D01	ANAR_STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STA_TEMP_SHUTD	STA_TEMP_WARN	0x00
0x0D02	ANAR_IRQ_MASK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IRQ_TEMP_SHUTD	IRQ_TEMP_WARN	0x03
Pad Configuration										
0x0D58	ANAR_NIRQ_CFG	NIRQ_OD_CFG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x99
APU										
PROG-0 SRAM										
0x4000	APU_PROG_RAM0_START	PROG_RAM0_START<7:0>								0x00
0x47FF	APU_PROG_RAM0_END	PROG_RAM0_END<7:0>								0x00
PROG-1 SRAM										
0x4800	APU_PROG_RAM1_START	PROG_RAM1_START<7:0>								0x00
0x4FFF	APU_PROG_RAM1_END	PROG_RAM1_END<7:0>								0x00
DATA SRAM										
0x5000	APU_DATA_RAM_START	DATA_RAM_START<7:0>								0x00
0x57FF	APU_DATA_RAM_END	DATA_RAM_END<7:0>								0x00
Mailbox SRAM Access										
0x6000	APU_ADDR_B0	ADDR_B0<7:0>								0x00
0x6001	APU_ADDR_B1	Reserved	Reserved	Reserved	Reserved	Reserved	ADDR_B1<2:0>			0x00
0x6002	APU_WDATA_B0	WDATA_B0<7:0>								0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x6003	APU_WDATA_B1	WDATA_B1<7:0>								0x00
0x6004	APU_WDATA_B2	WDATA_B2<7:0>								0x00
0x6005	APU_WDATA_B3	WDATA_B3<7:0>								0x00
0x6006	APU_RDATA_B0	RDATA_B0<7:0>								0x00
0x6007	APU_RDATA_B1	RDATA_B1<7:0>								0x00
0x6008	APU_RDATA_B2	RDATA_B2<7:0>								0x00
0x6009	APU_RDATA_B3	RDATA_B3<7:0>								0x00
0x600A	APU_RT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RT	0x00
0x600B	APU_WT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WT	0x00
FEQ HPF Offset Coefficients										
0x6010	APU_HPF_OFFSET_FF0_IN_B0	HPF_OFFSET_FF0_IN_B0<7:0>								0x00
0x6011	APU_HPF_OFFSET_FF0_IN_B1	HPF_OFFSET_FF0_IN_B1<7:0>								0x00
0x6012	APU_HPF_OFFSET_FF0_IN_VALID	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPF_OFFSET_FF0_IN_VALID	0x00
0x6013	APU_HPF_OFFSET_FF1_IN_B0	HPF_OFFSET_FF1_IN_B0<7:0>								0x00
0x6014	APU_HPF_OFFSET_FF1_IN_B1	HPF_OFFSET_FF1_IN_B1<7:0>								0x00
0x6015	APU_HPF_OFFSET_FF1_IN_VALID	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPF_OFFSET_FF1_IN_VALID	0x00
0x6016	APU_HPF_OFFSET_FB0_IN_B0	HPF_OFFSET_FB0_IN_B0<7:0>								0x00
0x6017	APU_HPF_OFFSET_FB0_IN_B1	HPF_OFFSET_FB0_IN_B1<7:0>								0x00
0x6018	APU_HPF_OFFSET_FB0_IN_VALID	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPF_OFFSET_FB0_IN_VALID	0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x6019	APU_HPF_OFFSET_FB1_IN_B0	HPF_OFFSET_FB1_IN_B0<7:0>								0x00
0x601A	APU_HPF_OFFSET_FB1_IN_B1	HPF_OFFSET_FB1_IN_B1<7:0>								0x00
0x601B	APU_HPF_OFFSET_FB1_IN_VALID	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HPF_OFFSET_FB1_IN_VALID	0x00
FEQ HPF Offset Coefficients Status										
0x601C	APU_HPF_OFFSET_FF0_OUT_B0	HPF_OFFSET_FF0_OUT_B0<7:0>								0x00
0x601D	APU_HPF_OFFSET_FF0_OUT_B1	HPF_OFFSET_FF0_OUT_B1<7:0>								0x00
0x601E	APU_HPF_OFFSET_FF1_OUT_B0	HPF_OFFSET_FF1_OUT_B0<7:0>								0x00
0x601F	APU_HPF_OFFSET_FF1_OUT_B1	HPF_OFFSET_FF1_OUT_B1<7:0>								0x00
0x6020	APU_HPF_OFFSET_FB0_OUT_B0	HPF_OFFSET_FB0_OUT_B0<7:0>								0x00
0x6021	APU_HPF_OFFSET_FB0_OUT_B1	HPF_OFFSET_FB0_OUT_B1<7:0>								0x00
0x6022	APU_HPF_OFFSET_FB1_OUT_B0	HPF_OFFSET_FB1_OUT_B0<7:0>								0x00
0x6023	APU_HPF_OFFSET_FB1_OUT_B1	HPF_OFFSET_FB1_OUT_B1<7:0>								0x00
DSP Input Source Selection										
0x6024	APU_FF_MXDSP_C0_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FF_MXDSP_C0_SEL	0x00
0x6025	APU_FF_MXDSP_C1_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FF_MXDSP_C1_SEL	0x00
0x6026	APU_FB_MXDSP_C0_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FB_MXDSP_C0_SEL	0x00
0x6027	APU_FB_MXDSP_C1_SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FB_MXDSP_C1_SEL	0x00
DSP Gain										
0x6028	APU_USER_GAIN_C0_DB	USER_GAIN_C0_DB<7:0>								0x79
0x602	APU_USER_GAIN_C0_FIN	Reserved	Reserved	Reserved	Reserved	USER_GAIN_C0_FINE<3:0>				0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
9	E									
0x602A	APU_USER_GAIN_C1_DB	USER_GAIN_C1_DB<7:0>								0x79
0x602B	APU_USER_GAIN_C1_FINE	Reserved	Reserved	Reserved	Reserved	USER_GAIN_C1_FINE<3:0>				0x00
0x602C	APU_GAIN_RATE	GAIN_RATE<7:0>								0x20

16.2 Register Descriptions

16.2.1 Sequencer

16.2.1.1 Chip IDs

Table 25: SEQ_CHIP_ID_HI (0x0200)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	CHIP_ID_HI	Device identifier (most significant byte).	0x26

Table 26: SEQ_CHIP_ID_LO (0x0201)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	CHIP_ID_LO	Device identifier (least significant byte).	0x69

Table 27: SEQ_CHIP_VAR (0x0202)

Bit	Mode	Symbol	Description	Reset
[1:0]	RWT	CHIP_VAR	Device variant code **Value** **Description** 0x0 DA7400 (Stereo Codec) 0x1 DA7401 (Mono Hybrid ANC) 0x2 DA7402 (Stereo Hybrid ANC) 0x3 Reserved	0x0

Table 28: SEQ_CHIP_REV (0x0203)

Bit	Mode	Symbol	Description	Reset
[7:4]	RO	CHIP_REV_MAJOR	Device revision code (major).	0x0
[3:0]	RO	CHIP_REV_MINOR	Device revision code (minor).	0x0

16.2.1.2 System Sequencer - SET0

Table 29: SEQ_INPUT_PATH_SET0 (0x0206)

Bit	Mode	Symbol	Description	Reset
[1]	RW	MICR_EN_SET0	Right microphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	MICL_EN_SET0	Left microphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 30: SEQ_OUTPUT_PATH_SET0 (0x0207)

Bit	Mode	Symbol	Description	Reset
[1]	RW	HPR_EN_SET0	Right headphone enable . **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	HPL_EN_SET0	Left headphone enable **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 31: SEQ_DSP_CONFIG_SET0 (0x0208)

Bit	Mode	Symbol	Description	Reset
[4]	RW	SRAM_SEL_SET0	DSP program memory (PRAM) profile selection. **Value** **Description** 0x0 PROG-0 0x1 PROG-1	0x0
[3]	RW	FFR_EN_SET0	ANC right feedforward microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[2]	RW	FBR_EN_SET0	ANC right feedback microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[1]	RW	FFL_EN_SET0	ANC left feedforward microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	FBL_EN_SET0	ANC left feedback microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 32: SEQ_PERF_MODE_SET0 (0x020A)

Bit	Mode	Symbol	Description	Reset
[0]	RW	LP_MODE_SET0	Power versus performance selection.	0x0

Bit	Mode	Symbol	Description	Reset
			Value **Description** 0x0 High performance 0x1 Low power	

Table 33: SEQ_MICBIAS_CONFIG_SET0 (0x020B)

Bit	Mode	Symbol	Description	Reset
[0]	RW	MICBIAS_EN_SET0	Microphone bias (MICBIAS) enabled during audio bring up when input path enabled. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 34: SEQ_PCM_CONFIG_SET0 (0x020C)

Bit	Mode	Symbol	Description	Reset
[0]	RW	PCM_EN_SET0	DAI PCM interface enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 35: SEQ_APPLY_CONFIG_SET0 (0x020D)

Bit	Mode	Symbol	Description	Reset
[0]	RW	APPLY_CONFIG_SET0	Write 0x1 to switch from SET1 to SET0. Writing 0x0 has no effect. **Value** **Description** 0x0 Inactive 0x1 Active	0x1

16.2.1.3 System Sequencer - SET1

Table 36: SEQ_INPUT_PATH_SET1 (0x020E)

Bit	Mode	Symbol	Description	Reset
[1]	RW	MICR_EN_SET1	Right microphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	MICL_EN_SET1	Left microphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 37: SEQ_OUTPUT_PATH_SET1 (0x020F)

Bit	Mode	Symbol	Description	Reset
[1]	RW	HPR_EN_SET1	Right headphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	HPL_EN_SET1	Left headphone enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 38: SEQ_DSP_CONFIG_SET1 (0x0210)

Bit	Mode	Symbol	Description	Reset
[4]	RW	SRAM_SEL_SET1	DSP program memory (PRAM) profile selection. **Value** **Description** 0x0 PROG-0 0x1 PROG-1	0x1
[3]	RW	FFR_EN_SET1	ANC right feedforward microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[2]	RW	FBR_EN_SET1	ANC right feedback microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[1]	RW	FFL_EN_SET1	ANC left feedforward microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	FBL_EN_SET1	ANC left feedback microphones enable. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 39: SEQ_PERF_MODE_SET1 (0x0212)

Bit	Mode	Symbol	Description	Reset
[0]	RW	LP_MODE_SET1	Power versus performance selection. **Value** **Description** 0x0 High performance 0x1 Low power	0x0

Table 40: SEQ_MICBIAS_CONFIG_SET1 (0x0213)

Bit	Mode	Symbol	Description	Reset
[0]	RW	MICBIAS_EN_SET1	Microphone bias (MICBIAS) enabled during audio bring up when input path enabled. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 41: SEQ_PCM_CONFIG_SET1 (0x0214)

Bit	Mode	Symbol	Description	Reset
[0]	RW	PCM_EN_SET1	DAI PCM interface enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 42: SEQ_APPLY_CONFIG_SET1 (0x0215)

Bit	Mode	Symbol	Description	Reset
[0]	RW	APPLY_CONFIG_SET1	Write 0x1 to switch from SET0 to SET1. Writing 0x0 has no effect. **Value** **Description** 0x0 Inactive 0x1 Active	0x0

16.2.1.4 Mode Control Status

Table 43: SEQ_MODE_CTRL_STATUS (0x0216)

Bit	Mode	Symbol	Description	Reset
[1:0]	RO	MODE_CTRL_STATUS	Sequencer SET switching status. **Value** **Description** 0x0 SET0 active 0x1 Switching to SET1 0x2 Switching to SET0	0x0

Bit	Mode	Symbol	Description	Reset
			0x3 SET1 active	

16.2.1.5 Microphone Bias Configuration

Table 44: SEQ_MICBIAS_VOLTAGE (0x0217)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	MICBIAS_VOLT	Microphone bias (MICBIAS) voltage (V). **Value** **Description** 0x0 1.2 0x1 1.4 0x2 1.6 0x3 1.8 0x4 2.16 0x5 2.4 0x6 2.7 0x7 2.98	0x0

16.2.1.6 DAI/PCM Interface Sample Rate Configuration

Table 45: SEQ_SR_CONFIG (0x0218)

Bit	Mode	Symbol	Description	Reset
[5:1]	RW	PCM_SR	DAI PCM sample rate (kHz). **Value** **Description** 0x0 Reserved 0x1 8 0x2 11.025 0x3 12 0x4 Reserved 0x5 16 0x6 22.05 0x7 24 0x8 Reserved 0x9 32 0xA 44.1 0xB 48 0xC Reserved 0xD Reserved 0xE 88.2 0xF 96	0x13

Bit	Mode	Symbol	Description	Reset
			0x10 Reserved 0x11 Reserved 0x12 176.4 0x13 192 0x14 Reserved 0x15 Reserved 0x16 352.8 0x17 384 0x18 Reserved 0x19 Reserved 0x1A Reserved 0x1B Reserved 0x1C Reserved 0x1D Reserved 0x1E Reserved 0x1F Reserved	
[0]	RW	SR192_EN	Force system sample rate (SSR) to 192 kHz. When disabled, SSR = PCM_SR. **Value Description** 0x0 SSR = PCM_SR 0x1 SSR = 192 kHz	0x0

16.2.1.7 Device Status

Table 46: SEQ_STATUS_RO (0x0219)

Bit	Mode	Symbol	Description	Reset
[6:2]	RO	DSP_SR_RO	System sample rate (SSR). **Value Description** 0x0 Reserved 0x1 8 0x2 11.025 0x3 12 0x4 Reserved 0x5 16 0x6 22.05 0x7 24 0x8 Reserved 0x9 32 0xA 44.1	0x13

Bit	Mode	Symbol	Description	Reset
			0xB 48 0xC Reserved 0xD Reserved 0xE 88.2 0xF 96 0x10 Reserved 0x11 Reserved 0x12 176.4 0x13 192 0x14 Reserved 0x15 Reserved 0x16 Reserved 0x17 Reserved 0x18 Reserved 0x19 Reserved 0x1A Reserved 0x1B Reserved 0x1C Reserved 0x1D Reserved 0x1E Reserved 0x1F Reserved	
[1]	RO	ANC_EN_RO	ANC is enabled (reads 1 when any of the feedforward or feedback registers are set). Not applicable to DA7400. **Value Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RO	SRC_EN_RO	SRC status. **Value Description** 0x0 Disabled 0x1 Enabled	0x0

16.2.1.8 Main FSM Status

Table 47: SEQ_MAIN_SM_STATE (0x021B)

Bit	Mode	Symbol	Description	Reset
[1:0]	RO	MAIN_SM_STATE	Current device state. **Value Description** 0x0 OFF	0x0

Bit	Mode	Symbol	Description	Reset
			0x1 BOOT 0x2 STANDBY 0x3 ACTIVE	

16.2.1.9 Audio Sequencer Configuration

Table 48: SEQ_MIC_MUTE_CTRL (0x021C)

Bit	Mode	Symbol	Description	Reset
[1]	RW	MICR_MUTE	Right microphone mute. **Value Description** 0x0 Unmuted 0x1 Muted	0x0
[0]	RW	MICL_MUTE	Left microphone mute. **Value Description** 0x0 Unmuted 0x1 Muted	0x0

16.2.2 DAI

16.2.2.1 DAI Configuration

Table 49: DAI_MODE (0x0301)

Bit	Mode	Symbol	Description	Reset
[0]	RW	MODE	Selects between Master and Slave clock generation mode for the digital audio interface (DAI). **Value Description** 0x0 DAI receives clocks (Slave mode) 0x1 DAI generates clocks (Master mode)	0x0

Table 50: DAI_SLOT_CNT (0x0302)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	SLOT_CNT	The total number of slots on the bus. 0x0 = no slots enabled, 0x10 = 16 slots (maximum) enabled. Slots 17 to 31 are reserved.	0x0

Table 51: DAI_CONFIG (0x0305)

Bit	Mode	Symbol	Description	Reset
[4:2]	RW	FRAME_LEN	Master clock generator frame length. The DAI word clock is generated with a 50 % duty cycle according to the applied frame length. This register is ignored when the DAI is in slave mode. **Value Description**	0x0

Bit	Mode	Symbol	Description	Reset
			0x0 32-bit 0x1 64-bit 0x2 128-bit 0x3 256-bit 0x4 512-bit	
[1:0]	RW	FORMAT	DAI frame format. **Value** **Description** 0x0 I²S 0x1 Left-justified format (LJF) 0x2 Right-justified format (RJF) 0x3 DSP	0x0

Table 52: DAI_W_LEN (0x0306)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	W_LEN	The width of the audio data sent and received over the DAI per channel. **Value** **Description** 0x0 16-bits per slot 0x1 20-bits per slot 0x2 24-bits per slot 0x3 32-bits per slot	0x3

Table 53: DAI_DATA_OUT_CTRL (0x0307)

Bit	Mode	Symbol	Description	Reset
[5]	RW	TDM_EARLY_RLS	Configures the timing of the DAI data output in TDM mode. **Value** **Description** 0x0 Data is driven until the end of the slot 0x1 Data is driven until half of BCLK before the end of the slot	0x0
[4:3]	RW	DATA_OUT_EN	DAI output enable. **Value** **Description** 0x0 Data output is tristate 0x1 Data output is tristate 0x2 Data driven on all slots 0x3 Data driven only during enabled slots	0x2
[1]	RW	WCLK_POL	The WCLK edge defining the start of the PCM frame. Note: The edge is dependent on the DAI format. **Value** **Description** 0x0 Rising (LJF, RJF, DSP), Falling (I2S)	0x0

Bit	Mode	Symbol	Description	Reset
			0x1 Falling (LJF, RJF, DSP), Rising (I2S)	
[0]	RW	BCLK_POL	The BCLK edge used to sample incoming data (DATA_IN). Outgoing data (DATA_OUT) is driven on the opposite edge. **Value** **Description** 0x0 Rising 0x1 Falling	0x0

Table 54: DAI_OFFSET_MSB (0x0309)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	OFFSET_MSB	Most significant 4 bits of the 12-bit OFFSET, which is the number of BCLK cycles offset relative to the normal data formatting. The minimum offset value is 0x0, the maximum is equal to the applied frame length.	0x0

Table 55: DAI_OFFSET_LSB (0x030A)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	OFFSET_LSB	Least significant 8 bits of the 12-bit OFFSET, which is the number of BCLK cycles offset relative to the normal data formatting. The minimum offset value is 0x0, the maximum is equal to the applied frame length.	0x0

16.2.3 DAI ADC Channel Configuration

Table 56: DAI_ADC1_CH (0x030B)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC1_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 57: DAI_ADC2_CH (0x030C)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC2_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 58: DAI_ADC3_CH (0x030D)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC3_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are	0x0

Bit	Mode	Symbol	Description	Reset
			reserved).	

Table 59: DAI_ADC4_CH (0x030E)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC4_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 60: DAI_ADC5_CH (0x030F)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC5_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 61: DAI_ADC6_CH (0x0310)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	ADC6_CH	ADC input channel control. Set to 0x0 to disable this channel, any other value allocates this ADC channel to the corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

16.2.3.1 DAI DAC Channel Configuration

Table 62: DAI_DAC1_CH (0x031B)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC1_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 63: DAI_DAC2_CH (0x031C)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC2_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 64: DAI_DAC3_CH (0x031D)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC3_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are	0x0

Bit	Mode	Symbol	Description	Reset
			reserved).	

Table 65: DAI_DAC4_CH (0x031E)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC4_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 66: DAI_DAC5_CH (0x031F)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC5_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

Table 67: DAI_DAC6_CH (0x0320)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	DAC6_CH	DAC input channel control. Set to 0x0 to disable this DAC channel, any other value allocates this DAC channel to corresponding frame slot. 0x10 (16 slots) is the maximum applicable value (slots 17 to 31 are reserved).	0x0

16.2.4 SRC - RX

16.2.4.1 SRC Configuration

Table 68: SRCRX_OSR_IN (0x0416)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	OSR_IN	Select SRC input oversampling factor. **Value** **Description** 0x0 1x (8 kHz <= PCM SR <= 96 kHz) 0x1 2x (96 kHz < PCM_SR <= 192 kHz) 0x2 Reserved 0x3 4x (192 kHz < PCM_SR <= 384 kHz)	0x0

16.2.5 SRC - TX

16.2.5.1 SRC Configuration

Table 69: SRCTX_OSR_OUT (0x0518)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	OSR_OUT	Select output oversampling factor. **Value** **Description** 0x0 1x (8 kHz <= PCM SR <= 96 kHz) 0x1 2x (96 kHz < PCM_SR <= 192 kHz) 0x2 Reserved 0x3 4x (192 kHz < PCM_SR <= 384 kHz)	0x0

16.2.6 DMIC Interface

16.2.6.1 DMIC Channel Enables

Table 70: DMIC_A0_EN (0x0600)

Bit	Mode	Symbol	Description	Reset
[0]	RW	A0_EN	Enable sampling of DMIC A data on the rising edge of the DMIC clock. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 71: DMIC_A1_EN (0x0601)

Bit	Mode	Symbol	Description	Reset
[0]	RW	A1_EN	Enable sampling of DMIC A data on the falling edge of the DMIC clock. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 72: DMIC_B0_EN (0x0602)

Bit	Mode	Symbol	Description	Reset
[0]	RW	B0_EN	Enable sampling of DMIC B data on the rising edge of the DMIC clock. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 73: DMIC_B1_EN (0x0603)

Bit	Mode	Symbol	Description	Reset
[0]	RW	B1_EN	Enable sampling of DMIC B data on the falling edge of the DMIC clock. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 74: DMIC_C0_EN (0x0604)

Bit	Mode	Symbol	Description	Reset
[0]	RW	C0_EN	Enable sampling of DMIC C data on the rising edge of the DMIC clock. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 75: DMIC_C1_EN (0x0605)

Bit	Mode	Symbol	Description	Reset
[0]	RW	C1_EN	Enable sampling of DMIC C data on the falling edge of the DMIC clock. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

16.2.6.2 DMIC Clock Frequency Configuration

Table 76: DMIC_AB_CLK_FREQ_SEL (0x0606)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	AB_CLK_FREQ_SEL	Select a clock frequency (MHz) to drive on DMIC_CLK_AB. **Value** **Description** 0x0 6.144 0x1 3.072 0x2 2.4576 0x3 1.536 0x4 0.768 0x5 Reserved 0x6 Reserved 0x7 Reserved	0x0

Table 77: DMIC_C_CLK_FREQ_SEL (0x0607)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	C_CLK_FREQ_SEL	Select a clock frequency (MHz) to drive on DMIC_CLK_C. Not applicable to DA7400. **Value** **Description** 0x0 6.144 0x1 3.072 0x2 2.4576 0x3 1.536 0x4 0.768 0x5 Reserved 0x6 Reserved 0x7 Reserved	0x0

16.2.6.3 DMIC Clock Sampling Phase Configuration

Table 78: DMIC_A_CLK_SAMP_PH (0x0608)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	A_CLK_SAMP_PH	Selects the sampling phase shift (degrees) relative to DMIC A master clock. The phase shift is defined as the multiple of 45 degrees that the sampling clock is delayed relative to the DMIC master clock. In the case of the 2.4576 MHz clock, the phase shift is the multiple of 36 degrees that the sampling clock is delayed relative to the DMIC master clock. **Value** **Description** 0x0 None 0x1 36 or 45 0x2 72 or 90 0x3 108 or 135	0x0

Table 79: DMIC_B_CLK_SAMP_PH (0x0609)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	B_CLK_SAMP_PH	Selects the sampling phase shift (degrees) relative to DMIC B master clock. The phase shift is defined as the multiple of 45 degrees that the sampling clock is delayed relative to the DMIC master clock. In the case of the 2.4576 MHz clock, the phase shift is the multiple of 36 degrees that the sampling clock is delayed relative to the DMIC master clock. **Value** **Description** 0x0 None 0x1 36 or 45 0x2 72 or 90	0x0

Bit	Mode	Symbol	Description	Reset
			0x3 108 or 135	

Table 80: DMIC_C_CLK_SAMP_PH (0x060A)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	C_CLK_SAMP_PH	Not applicable to DA7400. Selects the sampling phase shift (degrees) relative to DMIC C master clock. The phase shift is defined as the multiple of 45 degrees that the sampling clock is delayed relative to the DMIC master clock. In the case of the 2.4576 MHz clock, the phase shift is the multiple of 36 degrees that the sampling clock is delayed relative to the DMIC master clock. **Value** **Description** 0x0 None 0x1 36 or 45 0x2 72 or 90 0x3 108 or 135	0x0

16.2.6.4 DMIC Router Configuration

Table 81: DMIC_FF0_SEL (0x060B)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	FF0_SEL	Selects which DMIC input is routed to Channel 0 of the feedforward filter. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 DMIC A0 0x2 DMIC A1 0x3 DMIC B0 0x4 DMIC B1 0x5 DMIC C0 0x6 DMIC C1 0x7 Reserved	0x0

Table 82: DMIC_FF1_SEL (0x060C)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	FF1_SEL	Selects which DMIC input is routed to Channel 1 of the feedforward filter. Not applicable to DA7400. **Value** **Description** 0x0 Disabled 0x1 DMIC A0 0x2 DMIC A1	0x0

Bit	Mode	Symbol	Description	Reset
			0x3 DMIC B0 0x4 DMIC B1 0x5 DMIC C0 0x6 DMIC C1 0x7 Reserved	

Table 83: DMIC_FB0_SEL (0x060D)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	FB0_SEL	Selects which DMIC input is routed to Channel 0 of the feedback filter. Not applicable to DA7400. **Value Description** 0x0 Disabled 0x1 DMIC A0 0x2 DMIC A1 0x3 DMIC B0 0x4 DMIC B1 0x5 DMIC C0 0x6 DMIC C1 0x7 Reserved	0x0

Table 84: DMIC_FB1_SEL (0x060E)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	FB1_SEL	Selects which DMIC input is routed to Channel 1 of the feedback filter. Not applicable to DA7400. **Value Description** 0x0 Disabled 0x1 DMIC A0 0x2 DMIC A1 0x3 DMIC B0 0x4 DMIC B1 0x5 DMIC C0 0x6 DMIC C1 0x7 Reserved	0x0

Table 85: DMIC_TK0_SEL (0x060F)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	TK0_SEL	Selects which DMIC input is routed to Channel 0 of the talk filter. **Value Description**	0x0

Bit	Mode	Symbol	Description		Reset
			0x0	Disabled	
			0x1	DMIC A0	
			0x2	DMIC A1	
			0x3	DMIC B0	
			0x4	DMIC B1	
			0x5	DMIC C0 (Reserved for DA7400)	
			0x6	DMIC C1 (Reserved for DA7400)	
			0x7	Reserved	

Table 86: DMIC_TK1_SEL (0x0610)

Bit	Mode	Symbol	Description		Reset
[2:0]	RW	TK1_SEL	Selects which DMIC input is routed to Channel 1 of the talk filter.		0x0
			Value	**Description**	
			0x0	Disabled	
			0x1	DMIC A0	
			0x2	DMIC A1	
			0x3	DMIC B0	
			0x4	DMIC B1	
			0x5	DMIC C0 (Reserved for DA7400)	
			0x6	DMIC C1 (Reserved for DA7400)	
			0x7	Reserved	

16.2.7 Input Filters

16.2.7.1 Input Filter Configuration

Table 87: INPS_PATH_DATA_SEL (0x0700)

Bit	Mode	Symbol	Description	Reset
[0]	RW	PATH_DATA_SEL	Selects the data source of the input filters. **Value** **Description** 0x0 ADC 0x1 DMIC TK	0x0

Table 88: INPS_HPF_FILTER_CONFIG (0x0701)

Bit	Mode	Symbol	Description	Reset
[6]	RW	HPF_EN	High-pass filter enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x1
[5:3]	RW	HPF_LOW_CORNER	High pass filter 3 dB cut-off (only applies to system sample rates <= 32 kHz). **Value** **Description** 0x0 SSR / 3200 0x1 SSR / 320 0x2 SSR / 160 0x3 SSR / 80 0x4 SSR / 53.3 0x5 SSR / 40 0x6 SSR / 26.7 0x7 SSR / 20	0x0
[2:1]	RW	HPF_HIGH_CORNER	High-pass filter 3 dB cut-off (only applies to system sample rates > 32 kHz). **Value** **Description** 0x0 SSR / 26667 0x1 SSR / 12800 0x2 SSR / 6400 0x3 SSR / 3200	0x0

Table 89: INPS_ANALOG_GAIN_CH0 (0x0702)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	A_GAIN0	Channel 0 analog gain (dB). **Value** **Description** 0x0 0	0x0

Bit	Mode	Symbol	Description	Reset
			0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 30 0x7 30	

Table 90: INPS_ANALOG_GAIN_CH1 (0x0703)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	A_GAIN1	Channel 1 analog gain (dB). **Value Description** 0x0 0 0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 30 0x7 30	0x0

Table 91: INPS_DIGITAL_GAIN_CH0 (0x0704)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	D_GAIN0	Channel 0 digital gain (dB). Note: this only applies when ALC (ALC0_EN) is disabled. **Value Description** 0x0 -83.25 0x1 -82.5 ... (0.75 * D_GAIN0) - 83.25 dB 0x6F 0 ... (0.75 * D_GAIN0) - 83.25 dB 0x7E 11.25 0x7F 12	0x6F

Table 92: INPS_DIGITAL_GAIN_CH1 (0x0705)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	D_GAIN1	Channel 1 digital gain (dB). Note: this only applies when ALC (ALC1_EN) is disabled.	0x6F

Bit	Mode	Symbol	Description	Reset
			Value **Description** 0x0 -83.25 0x1 -82.5 ... (0.75 * D_GAIN1) - 83.25 dB 0x6F 0 ... (0.75 * D_GAIN1) - 83.25 dB 0x7E 11.25 0x7F 12	

Table 93: INPS_DIGITAL_GAIN_RAMP_RATE (0x0706)

Bit	Mode	Symbol	Description	Reset
[5:4]	RW	D_GAIN1_RMP_RATE	Channel 1 digital gain ramp rate. **Value** **Description** 0x0 Very fast (0.11 ms / dB) 0x1 Fast (0.88 ms / dB) 0x2 Slow (7.04 ms / dB) 0x3 Very slow (14.08 ms / dB)	0x1
[1:0]	RW	D_GAIN0_RMP_RATE	Channel 0 digital gain ramp rate. **Value** **Description** 0x0 Very fast (0.11 ms / dB) 0x1 Fast (0.88 ms / dB) 0x2 Slow (7.04 ms / dB) 0x3 Very slow (14.08 ms / dB)	0x1

16.2.7.2 ALC Configuration

Table 94: INPS_ALC_ENABLE (0x070D)

Bit	Mode	Symbol	Description	Reset
[1]	RW	ALC1_EN	Channel 1 ALC enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	ALC0_EN	Channel 0 ALC enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 95: INPS_ALC_GAIN_MODE (0x070E)

Bit	Mode	Symbol	Description	Reset
[1]	RW	ALC1_GAIN_MODE	Channel 1 ALC gain mode. **Value** **Description** 0x0 Digital only 0x1 Digital and analog	0x0
[0]	RW	ALC0_GAIN_MODE	Channel 0 ALC gain mode. **Value** **Description** 0x0 Digital only 0x1 Digital and analog	0x0

Table 96: INPS_ALC_ATTACK_RELEASE (0x070F)

Bit	Mode	Symbol	Description	Reset
[7:4]	RW	ALC_RELEASE	Sets the ALC release rate. This is the rate in s/dB at which the ALC increases the gain. **Value** **Description** 0x0 29.49 / SSR 0x1 58.49 / SSR 0x2 117.96 / SSR 0x3 235.92 / SSR 0x4 471.84 / SSR 0x5 943.68 / SSR 0x6 1887 / SSR 0x7 3774 / SSR 0x8 7549 / SSR 0x9 15098 / SSR 0xA 30197 / SSR 0xB 30197 / SSR 0xC 30197 / SSR 0xD 30197 / SSR 0xE 30197 / SSR 0xF 30197 / SSR	0x2
[3:0]	RW	ALC_ATTACK	Sets the ALC attack rate. This is the rate in s/dB at which the ALC decreases the gain. **Value** **Description** 0x0 7.37 / SSR 0x1 14.745 / SSR 0x2 29.49 / SSR 0x3 58.49 / SSR	0x0

Bit	Mode	Symbol	Description	Reset
			0x4 117.96 / SSR 0x5 235.92 / SSR 0x6 471.84 / SSR 0x7 943.68 / SSR 0x8 1887 / SSR 0x9 3774 / SSR 0xA 7549 / SSR 0xB 15098 / SSR 0xC 30197 / SSR 0xD 30197 / SSR 0xE 30197 / SSR 0xF 30197 / SSR	

Table 97: INPS_ALC_HOLD (0x0710)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	ALC_HOLD	Sets the ALC hold time (s). This is the length of time that the ALC waits before releasing. **Value Description** 0x0 62 / SSR 0x1 124 / SSR 0x2 248 / SSR 0x3 496 / SSR 0x4 992 / SSR 0x5 1984 / SSR 0x6 3968 / SSR 0x7 7936 / SSR 0x8 15872 / SSR 0x9 31744 / SSR 0xA 63488 / SSR 0xB 126976 / SSR 0xC 253952 / SSR 0xD 507904 / SSR 0xE 1015808 / SSR 0xF 2031616 / SSR	0x0

Table 98: INPS_ALC_NOISE_THR (0x0711)

Bit	Mode	Symbol	Description	Reset
[5:0]	RW	ALC_NOISE_THR	Threshold below which input signals will not cause the ALC to change gain (dBFS).	0x3F

Bit	Mode	Symbol	Description		Reset
			Value	**Description**	
			0x0	0	
			0x1	-1.5	
			...	-1.5 * ALC_NOISE_THR dBFS	
			0x1F	-46.5	
			...	-1.5 * ALC_NOISE_THR dBFS	
			0x3E	-93	
			0x3F	-94.5	

Table 99: INPS_ALC_MIN_THR (0x0712)

Bit	Mode	Symbol	Description		Reset
[5:0]	RW	ALC_MIN_THR	Sets the minimum target amplitude of the ALC output signal (dBFS). If the output signal drops below this level, the ALC will increase the gain until the output signal rises above this level.		0x3F
			Value	**Description**	
			0x0	0	
			0x1	-1.5	
			...	-1.5 * ALC_MIN_THR dBFS	
			0x1F	-46.5	
			...	-1.5 * ALC_MIN_THR dBFS	
			0x3E	-93	
			0x3F	-94.5	

Table 100: INPS_ALC_MAX_THR (0x0713)

Bit	Mode	Symbol	Description		Reset
[5:0]	RW	ALC_MAX_THR	Sets the maximum target amplitude of the ALC output signal (dBFS). If the output signal exceeds this level, the ALC will decrease the gain until the output signal drops below this level.		0x0
			Value	**Description**	
			0x0	0	
			0x1	-1.5	
			...	-1.5 * ALC_MAX_THR dBFS	
			0x1F	-46.5	
			...	-1.5 * ALC_MAX_THR dBFS	
			0x34	-78	
			0x35	Reserved	
			...	Reserved	
			0x3F	Reserved	

Table 101: INPS_ALC_DIG_GAIN_LIMITS (0x0714)

Bit	Mode	Symbol	Description	Reset
[7:4]	RW	ALC_D_GAIN_MAX	Sets the maximum amount of gain (dB) applied by the ALC. Note: When in digital only mode (ALC_GAIN_MODE = 0x0), ALC_A_GAIN_MAX = 0x0. In this case, the maximum available gain is 42 dB. **Value** **Description** 0x0 0 0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 36 0x7 42 0x8 MIN (48, 42 + ALC_A_GAIN_MAX) 0x9 MIN (54, 42 + ALC_A_GAIN_MAX) 0xA MIN (60, 42 + ALC_A_GAIN_MAX) 0xB MIN (66, 42 + ALC_A_GAIN_MAX) 0xC MIN (72, 42 + ALC_A_GAIN_MAX) 0xD Reserved 0xE Reserved 0xF Reserved	0xC
[3:0]	RW	ALC_D_GAIN_MIN	Sets the maximum amount of attenuation (dB) applied by the ALC. **Value** **Description** 0x0 0 0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 36 0x7 42 0x8 48 0x9 54 0xA 60 0xB 66 0xC 72	0xD

Bit	Mode	Symbol	Description	Reset
			0xD 78 0xE Reserved 0xF Reserved	

Table 102: INPS_ALC_ANA_GAIN_LIMITS (0x0715)

Bit	Mode	Symbol	Description	Reset
[6:4]	RW	ALC_A_GAIN_MAX	Sets the maximum amount of analog gain (dB) applied by the ALC (mixed analog and digital gain mode only). **Value Description** 0x0 0 0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 Reserved 0x7 Reserved	0x5
[2:0]	RW	ALC_A_GAIN_MIN	Sets the minimum amount of analog gain (dB) applied by the ALC (mixed analog and digital gain mode only). **Value Description** 0x0 0 0x1 6 0x2 12 0x3 18 0x4 24 0x5 30 0x6 Reserved 0x7 Reserved	0x0

Table 103: INPS_ALC_ANTICLIP_ENABLE (0x0716)

Bit	Mode	Symbol	Description	Reset
[0]	RW	ALC_ANTICLIP_EN	Enable the ALC signal anti-clip. **Value Description** 0x0 Disabled 0x1 Enabled	0x1

Table 104: INPS_ALC_ANTICLIP_THR (0x0717)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	ALC_ANTICLIP_THR	Sets the threshold relative to full-scale (FS) above which the ALC activates anti-clip. The threshold represented by this field setting, where x is the value of the bit-field, is x = ((x+1)/128) FS. This register is also used for the level detect threshold for the RMS level detector. **Value** **Description** 0x0 0.0078 0x1 0.0156 0x2 0.0234 ... 0.0078*ALC_ANTICLIP_THR FS 0x3F 0.4992 ... 0.0078*ALC_ANTICLIP_THR FS 0x7D 0.9844 0x7E 0.9922 0x7F 1	0x73

Table 105: INPS_ALC_ANTICLIP_STEP (0x0718)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	ALC_ANTICLIP_STEP	Sets the ALC step size (dB) when the output signal exceeds the anticlip threshold level specified in ALC_ANTICLIP_THR. The step size is updated at 4*SSR. **Value** **Description** 0x0 0.034 0x1 0.068 0x2 0.136 0x3 0.272	0x0

16.2.7.3 Level Detection

Table 106: INPS_LVL_DET_EN (0x071F)

Bit	Mode	Symbol	Description	Reset
[1]	RW	LVL_DET1_EN	Channel 1 level-detect enable, when set ALC is disabled. The threshold is set by ALC_ANTICLIP_THR register. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	LVL_DET0_EN	Channel 0 level-detect enable, when set ALC is disabled. The threshold is set by ALC_ANTICLIP_THR	0x0

Bit	Mode	Symbol	Description	Reset
			register. **Value** **Description** 0x0 Disabled 0x1 Enabled	

16.2.7.4 Level Detection Interrupt Handling

Table 107: INPS_EVENT (0x0720)

Bit	Mode	Symbol	Description	Reset
[0]	EVENT	EVT_LVL_DET	Indicates a level-detect event. **Value** **Description** 0x0 No level-detect event 0x1 Level-detect event	0x0

Table 108: INPS_STATUS (0x0721)

Bit	Mode	Symbol	Description	Reset
[0]	RO	STA_LVL_DET	Status of level-detect. **Value** **Description** 0x0 Level-detect inactive 0x1 Level-detect active	0x0

Table 109: INPS_IRQ_MASK (0x0722)

Bit	Mode	Symbol	Description	Reset
[0]	IRQ_MASK	IRQ_LVL_DET	Mask for level-detect event. **Value** **Description** 0x0 Unmasked 0x1 Masked	0x1

16.2.8 Output Filters

16.2.8.1 Output Filter Configuration

Table 110: OUTS_HPF_EN (0x0800)

Bit	Mode	Symbol	Description	Reset
[0]	RW	HPF_EN	Output path high-pass filter enable. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0

Table 111: OUTS_FIXED_GAIN (0x0801)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FIXED_GAIN	Output path user-programmed fixed gain (dB). **Value** **Description** 0x0 Muted 0x1 -77.25 0x2 -76.875 ... (0.375 * FIXED_GAIN) - 77.625 dB 0xCF 0 ... (0.375 * FIXED_GAIN) - 77.625 dB 0xFE 17.625 0xFF 18	0xCF

16.2.9 Headphone Charge Pump

16.2.9.1 HPCP Configuration

Table 112: HPCP_V_THRESHOLD (0x0900)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	V_THRESHOLD	Sets volume threshold at which HPCP switches from VDD/2 output to VDD (dBFS). **Value** **Description** 0x0 -2.0 0x1 -3.0 0x2 -4.0 0x3 -5.0 0x4 -6.0 0x5 -7.0 0x6 -8.0 0x7 -9.0 0x8 -10.0 0x9 -11.0 0xA -12.0 0xB -13.0 0xC -14.0 0xD -15.0 0xE -16.0 0xF -17.0	0x6

16.2.10 Clocking and Reset

16.2.10.1 Clocking Configuration

Table 113: CLKS_FSI_FREQ (0x0A00)

Bit	Mode	Symbol	Description	Reset
[0]	RW	FSI	ADC sample rate (MHz). Setting 0x0 (6 MHz) will result in higher audio performance; setting 0x1 (3 MHz) will result in lower power consumption. **Value** **Description** 0x0 6 (High-Performance mode) 0x1 3 (Low-Power mode)	0x0

16.2.10.2 Software Reset

Table 114: CLKS_SW_RST (0x0A01)

Bit	Mode	Symbol	Description	Reset
[0]	RW	SW_RST	Writing 0x1 will cause a full reset of digital logic and registers. **Value** **Description** 0x0 - 0x1 Reset	0x0

16.2.11 PLL/SRM

16.2.11.1 PLL/SRM Configuration

Table 115: PLLD_FBDIV_FRAC_B0 (0x0B00)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FBDIV_FRAC_B0	Lower fractional bits of the feedback divider value FBDIV[7:0]. The combination of {FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0} forms a 20-bit fixed point PLL multiplier in 7.13 format, with the binary point lying between FBDIV_INTEG and FBDIV_FRAC_B1. The PLL feedback divide ratio = (FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0) / 2^13. Write to all three registers from LSB to MSB (FBDIV_FRAC_B0, FBDIV_FRAC_B1, FBDIV_INTEG) to update the PLL state.	0x0

Table 116: PLLD_FBDIV_FRAC_B1 (0x0B01)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	FBDIV_FRAC_B1	Upper fractional bits of the feedback divider value FBDIV[12:8]. The combination of {FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0} forms a 20-bit fixed point PLL multiplier in 7.13 format, with the binary point lying between FBDIV_INTEG and FBDIV_FRAC_B1. The PLL feedback divide ratio = (FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0) / 2^13. Write to all three registers from LSB to MSB (FBDIV_FRAC_B0, FBDIV_FRAC_B1, FBDIV_INTEG) to update the PLL state.	0x0

Table 117: PLLD_FBDIV_INTEG (0x0B02)

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	FBDIV_INTEG	Integer value of the feedback divider value FBDIV[19:13]. The combination of {FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0} forms a 20-bit fixed point PLL multiplier in 7.13 format, with the binary point lying between FBDIV_INTEG and FBDIV_FRAC_B1. The PLL feedback divide ratio = (FBDIV_INTEG, FBDIV_FRAC_B1, FBDIV_FRAC_B0) / 2^13. Write to all three registers from LSB to MSB (FBDIV_FRAC_B0, FBDIV_FRAC_B1, FBDIV_INTEG) to update the PLL state.	0x40

Table 118: PLLD_CONFIG_1 (0x0B03)

Bit	Mode	Symbol	Description	Reset
[1:0]	RW	PLL_SRM_MODE	Sample rate matching (SRM) enable. **Value** **Description** 0x0 Disabled 0x1 Reserved 0x2 Enabled 0x3 Reserved	0x0

Table 119: PLLD_CONFIG_2 (0x0B04)

Bit	Mode	Symbol	Description	Reset
[7:5]	RW	INDIV	Frequency range of PLL reference clock (MHz). **Value** **Description** 0x0 2.5 to 5 0x1 5 to 10	0x3

Bit	Mode	Symbol	Description	Reset
			0x2 Reserved 0x3 10 to 20 0x4 Reserved 0x5 20 to 40 0x6 Reserved 0x7 40 to 54	
[2:1]	RW	CLK_SEL	PLL reference clock selection. **Value** **Description** 0x0 MCLK 0x1 PCM_BLCK 0x2 Reserved 0x3 Reserved	0x0
[0]	RW	OSC_SEL	Force internal oscillator as PLL reference clock (priority over CLK_SEL bits). **Value** **Description** 0x0 PLL reference is MCLK or BCLK 0x1 PLL reference is internal oscillator	0x0

16.2.12 PLL/SRM Interrupt Handling

Table 120: PLLD_EVENT (0x0B05)

Bit	Mode	Symbol	Description	Reset
[4]	EVENT	EVT_REFCLK_LOSS	Interrupt when reference clock to PLL is lost. **Value** **Description** 0x0 Reference clock is active 0x1 Reference clock is stopped or out of range	0x0
[3]	EVENT	EVT_PLL_LOCK	Interrupt when PLL locked to reference clock. **Value** **Description** 0x0 PLL not in lock 0x1 PLL acquired lock	0x0
[2]	EVENT	EVT_PLL_LOST_LOCK	Interrupt when PLL loses lock to reference clock. **Value** **Description** 0x0 PLL not in lock 0x1 PLL acquired lock	0x0
[1]	EVENT	EVT_SRM_LOCK	Interrupt when SRM locked to reference frequency. **Value** **Description** 0x0 SRM not in lock 0x1 SRM achieved lock	0x0

Bit	Mode	Symbol	Description	Reset
[0]	EVENT	EVT_SRM_LOST_LOCK	Interrupt when SRM loses lock. **Value** **Description** 0x0 Normal operation 0x1 SRM lost lock	0x0

Table 121: PLLD_STATUS (0x0B06)

Bit	Mode	Symbol	Description	Reset
[4]	RO	STA_REFCLK_LOSS	PLL reference clock status. **Value** **Description** 0x0 Reference clock is stopped or out of range 0x1 Reference clock is active	0x0
[3]	RO	STA_PLL_LOCK	PLL lock status. **Value** **Description** 0x0 PLL not in lock 0x1 PLL acquired lock	0x0
[2]	RO	STA_PLL_LOST_LOCK	PLL lost lock status. **Value** **Description** 0x0 PLL not in lock 0x1 PLL acquired lock	0x0
[1]	RO	STA_SRM_LOCK	SRM lock status. **Value** **Description** 0x0 SRM not in lock 0x1 SRM in lock	0x0
[0]	RO	STA_SRM_LOST_LOCK	SRM lock status. **Value** **Description** 0x0 SRM not in lock 0x1 SRM in lock	0x0

Table 122: PLLD_IRQ_MASK (0x0B07)

Bit	Mode	Symbol	Description	Reset
[4]	IRQ_MASK	IRQ_REFCLK_LOSS	Mask for lost reference interrupt. **Value** **Description** 0x0 EVT_REFCLK_LOSS interrupt not masked 0x1 EVT_REFCLK_LOSS interrupt masked	0x1
[3]	IRQ_MASK	IRQ_PLL_LOCK	Mask for PLL lock interrupt. **Value** **Description** 0x0 EVT_PLL_LOCK interrupt not masked	0x1

Bit	Mode	Symbol	Description	Reset
			0x1 EVT_PLL_LOCK interrupt masked	
[2]	IRQ_MASK	IRQ_PLL_LOST_LOCK	Mask for PLL lost lock interrupt. **Value** **Description** 0x0 EVT_PLL_LOST_LOCK interrupt not masked 0x1 EVT_PLL_LOST_LOCK interrupt masked	0x1
[1]	IRQ_MASK	IRQ_SRM_LOCK	Mask for SRM lock interrupt. **Value** **Description** 0x0 EVT_SRM_LOCK interrupt not masked 0x1 EVT_SRM_LOCK interrupt masked	0x1
[0]	IRQ_MASK	IRQ_SRM_LOST_LOCK	Mask for SRM lost lock interrupt. **Value** **Description** 0x0 EVT_SRM_LOST_LOCK interrupt not masked 0x1 EVT_SRM_LOST_LOCK interrupt masked	0x1

16.2.13 PRBS Signal Generator

16.2.13.1 PRBS0 Configuration

Table 123: PRBS_SEED0_B0 (0x0C00)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED0_B0	Bit [7:0] of PRBS0 seed.	0xFF

Table 124: PRBS_SEED0_B1 (0x0C01)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED0_B1	Bit [15:8] of PRBS0 seed.	0xFF

Table 125: PRBS_SEED0_B2 (0x0C02)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED0_B2	Bit [23:16] of PRBS0 seed.	0xFF

Table 126: PRBS_SEED0_B3 (0x0C03)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED0_B3	Bit [31:24] of PRBS0 seed.	0xFF

Table 127: PRBS_POLY0_B0 (0x0C04)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY0_B0	Bit [7:0] of PRBS0 polynomial.	0x57

Table 128: PRBS_POLY0_B1 (0x0C05)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY0_B1	Bit [15:8] of PRBS0 polynomial.	0x0

Table 129: PRBS_POLY0_B2 (0x0C06)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY0_B2	Bit [23:16] of PRBS0 polynomial.	0x0

Table 130: PRBS_POLY0_B3 (0x0C07)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY0_B3	Bit [31:24] of PRBS0 polynomial.	0x80

16.2.13.2 PRBS1 Configuration

Table 131: PRBS_SEED1_B0 (0x0C08)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED1_B0	Bit [7:0] of PRBS1 seed.	0xFF

Table 132: PRBS_SEED1_B1 (0x0C09)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED1_B1	Bit [15:8] of PRBS1 seed.	0xFF

Table 133: PRBS_SEED1_B2 (0x0C0A)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED1_B2	Bit [23:16] of PRBS1 seed.	0xFF

Table 134: PRBS_SEED1_B3 (0x0C0B)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SEED1_B3	Bit [31:24] of PRBS1 seed.	0xFF

Table 135: PRBS_POLY1_B0 (0x0C0C)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY1_B0	Bit [7:0] of PRBS1 polynomial.	0xCC

Table 136: PRBS_POLY1_B1 (0x0C0D)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY1_B1	Bit [15:8] of PRBS1 polynomial.	0x2

Table 137: PRBS_POLY1_B2 (0x0C0E)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY1_B2	Bit [23:16] of PRBS1 polynomial.	0x0

Table 138: PRBS_POLY1_B3 (0x0C0F)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	POLY1_B3	Bit [31:24] of PRBS1 polynomial.	0x80

16.2.13.3 PRBS Gain

Table 139: PRBS_GAIN0_CTRL (0x0C10)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	GAIN0	PRBS0 gain (dB). **Value** **Description** 0x0 0 0x1 -6 0x2 -12 0x3 -18 0x4 -24 0x5 -30 0x6 -36 0x7 -42 0x8 -48 0x9 -54 0xA -60 0xB -66 0xC -72 0xD -78 0xE -84 0xF -90 0x10 -96 0x11 -102 0x12 -108 0x13 -114 0x14 -120 0x15 -126 0x16 -132 0x17 -138 0x18 -144 0x19 Reserved 0x1A Reserved 0x1B Reserved 0x1C Reserved	0x0

Bit	Mode	Symbol	Description	Reset
			0x1D Reserved 0x1E Reserved 0x1F Reserved	

Table 140: PRBS_GAIN1_CTRL (0x0C11)

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	GAIN1	PRBS1 Gain (dB). **Value** **Description** 0x0 0 0x1 -6 0x2 -12 0x3 -18 0x4 -24 0x5 -30 0x6 -36 0x7 -42 0x8 -48 0x9 -54 0xA -60 0xB -66 0xC -72 0xD -78 0xE -84 0xF -90 0x10 -96 0x11 -102 0x12 -108 0x13 -114 0x14 -120 0x15 -126 0x16 -132 0x17 -138 0x18 -144 0x19 Reserved 0x1A Reserved 0x1B Reserved 0x1C Reserved	0x0

Bit	Mode	Symbol	Description	Reset
			0x1D Reserved 0x1E Reserved 0x1F Reserved	

16.2.13.4 PRBS Enable

Table 141: PRBS_CLEAR_CTRL (0x0C12)

Bit	Mode	Symbol	Description	Reset
[1]	RW	CLEAR0	Load PRBS0 with PRBS0_SEED[31:0]. **Value Description** 0x0 - 0x1 Load	0x0
[0]	RW	CLEAR1	Load PRBS1 with PRBS0_SEED[31:0]. **Value Description** 0x0 - 0x1 Load	0x0

Table 142: PRBS_CTRL (0x0C13)

Bit	Mode	Symbol	Description	Reset
[1]	RW	EN0	Enable PRBS0. Note: Enabling PRBS0 will take priority over the tone generator. **Value Description** 0x0 Disabled 0x1 Enabled	0x0
[0]	RW	EN1	Enable PRBS1. Note: Enabling PRBS1 will take priority over the tone generator. **Value Description** 0x0 Disabled 0x1 Enabled	0x0

16.2.14 Sine Wave Signal Generator

16.2.14.1 Tone Generator Configuration

Table 143: TONEG_CFG2 (0x0C81)

Bit	Mode	Symbol	Description	Reset
[7]	RW	START_STOPN	Tone generator start and stop. **Value Description** 0x0 STOP	0x0

Bit	Mode	Symbol	Description	Reset
			0x1 START	
[1:0]	RW	SWG_SEL	Sine wave configuration. **Value** **Description** 0x0 SWG1+SWG2 0x1 SWG1 0x2 SWG2 0x3 SWG1 DC with inverted cosine ramp	0x0

Table 144: TONEG_FREQ1_L (0x0C82)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FREQ1_L	SWG1 frequency, lower byte. {FREQ1_U, FREQ1_L} = (2^24*(fout / CLK_TG)	0x55

Table 145: TONEG_FREQ1_U (0x0C83)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FREQ1_U	SWG1 frequency, upper byte. {FREQ1_U, FREQ1_L} = (2^24*(fout / CLK_TG)	0x15

Table 146: TONEG_FREQ2_L (0x0C84)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FREQ2_L	SWG2 frequency, lower byte. {FREQ1_U, FREQ1_L} = (2^24*(fout / CLK_TG)	0x0

Table 147: TONEG_FREQ2_U (0x0C85)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FREQ2_U	SWG2 frequency, upper byte. {FREQ1_U, FREQ1_L} = (2^24*(fout / CLK_TG)	0x40

Table 148: TONEG_DC_OUT (0x0C89)

Bit	Mode	Symbol	Description	Reset
[5:4]	RW	DC_SEL	DC output level. **Value** **Description** 0x0 0x000000 (Zero) 0x1 0x400000 (+half-scale) 0x2 0x800000 (-full-scale) 0x3 0xC00000 (-half-scale)	0x0
[0]	RW	DC_EN	Force DC output enable. Note: Gain does not apply to DC values. **Value** **Description**	0x0

Bit	Mode	Symbol	Description	Reset
			0x0 Sine 0x1 DC	

Table 149: TONEG_GAIN (0x0C8A)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	GAIN	Gain applied to output (dBFS). Note: Gain does not apply to DC values. **Value** **Description** 0x0 0 0x1 -2.5 0x2 -6 0x3 -8.5 0x4 -12 0x5 -14.5 0x6 -18 0x7 -20.5 0x8 -24 0x9 -26.5 0xA -30 0xB -32.5 0xC -36 0xD -38.5 0xE -42 0xF -44.5	0x0

16.2.15 Analog Peripherals

16.2.15.1 Temperature Interrupt Handling

Table 150: ANAR_EVENT (0x0D00)

Bit	Mode	Symbol	Description	Reset
[1]	EVENT	EVT_TEMP_SHUTD	Over-temperature shutdown warning. **Value** **Description** 0x0 Not triggered 0x1 Triggered	0x0
[0]	EVENT	EVT_TEMP_WARN	High temperature warning. Note: shut down device if triggered. **Value** **Description** 0x0 Not triggered	0x0

Bit	Mode	Symbol	Description	Reset
			0x1 Triggered	

Table 151: ANAR_STATUS (0x0D01)

Bit	Mode	Symbol	Description	Reset
[1]	RO	STA_TEMP_SHUTD	Status of over-temperature shutdown warning. **Value** **Description** 0x0 Temperature < 125 °C 0x1 Temperature > 125 °C	0x0
[0]	RO	STA_TEMP_WARN	Status of high temperature warning. **Value** **Description** 0x0 Temperature < 85 °C 0x1 Temperature > 85 °C	0x0

Table 152: ANAR_IRQ_MASK (0x0D02)

Bit	Mode	Symbol	Description	Reset
[1]	IRQ_MASK	IRQ_TEMP_SHUTD	Mask for over-temperature shutdown warning interrupt. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[0]	IRQ_MASK	IRQ_TEMP_WARN	Mask for high temperature warning interrupt. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1

16.2.15.2 Pad Configuration

Table 153: ANAR_NIRQ_CFG (0x0D58)

Bit	Mode	Symbol	Description	Reset
[7]	RW	NIRQ_OD_CFG	Pad drive control. **Value** **Description** 0x0 Push-pull 0x1 Open drain	0x1

16.2.16 APU

16.2.16.1 PROG-0 SRAM

Table 154: APU_PROG_RAM0_START (0x4000)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	PROG_RAM0_START	Start byte of PROG-0 SRAM (least significant byte).	0x0

Table 155: APU_PROG_RAM0_END (0x47FF)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	PROG_RAM0_END	End byte of PROG-0 SRAM (most significant byte).	0x0

16.2.16.2 PROG-1 SRAM

Table 156: APU_PROG_RAM1_START (0x4800)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	PROG_RAM1_START	Start byte of PROG-1 SRAM (least significant byte).	0x0

Table 157: APU_PROG_RAM1_END (0x4FFF)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	PROG_RAM1_END	End byte of PROG-1 SRAM (most significant byte).	0x0

16.2.16.3 DATA SRAM

Table 158: APU_DATA_RAM_START (0x5000)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	DATA_RAM_START	Start byte of Data SRAM (least significant byte).	0x0

Table 159: APU_DATA_RAM_END (0x57FF)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	DATA_RAM_END	End byte of Data SRAM (most significant byte).	0x0

16.2.16.4 Mailbox SRAM Access

Table 160: APU_ADDR_B0 (0x6000)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	ADDR_B0	Lower byte of address for mailbox access of SRAM.	0x0

Table 161: APU_ADDR_B1 (0x6001)

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	ADDR_B1	Upper byte of address for mailbox access of SRAM.	0x0

Table 162: APU_WDATA_B0 (0x6002)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	WDATA_B0	Byte 0 of data for mailbox write to SRAM.	0x0

Table 163: APU_WDATA_B1 (0x6003)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	WDATA_B1	Byte 1 of data for mailbox write to SRAM.	0x0

Table 164: APU_WDATA_B2 (0x6004)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	WDATA_B2	Byte 2 of data for mailbox write to SRAM.	0x0

Table 165: APU_WDATA_B3 (0x6005)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	WDATA_B3	Byte 3 of data for mailbox write to SRAM.	0x0

Table 166: APU_RDATA_B0 (0x6006)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	RDATA_B0	Byte 0 of data for mailbox read from SRAM.	0x0

Table 167: APU_RDATA_B1 (0x6007)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	RDATA_B1	Byte 1 of data for mailbox read from SRAM.	0x0

Table 168: APU_RDATA_B2 (0x6008)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	RDATA_B2	Byte 2 of data for mailbox read from SRAM.	0x0

Table 169: APU_RDATA_B3 (0x6009)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	RDATA_B3	Byte 3 of data for mailbox read from SRAM.	0x0

Table 170: APU_RT (0x600A)

Bit	Mode	Symbol	Description	Reset
[0]	RW	RT	Trigger a read access to SRAM. **Value** **Description** 0x0 - 0x1 Trigger	0x0

Table 171: APU_WT (0x600B)

Bit	Mode	Symbol	Description	Reset
[0]	RW	WT	Trigger a write access to SRAM. **Value** **Description** 0x0 - 0x1 Trigger	0x0

16.2.16.5
16.2.16.5 DSP Input Source Selection

Table 172: APU_FF_MXDSP_C0_SEL (0x6024)

Bit	Mode	Symbol	Description	Reset
[0]	RW	FF_MXDSP_C0_SEL	Select source for DSP input FF_MXDSP_C0. **Value** **Description** 0x0 Feedforward DMIC Channel 0 (Not applicable for DA7400) 0x1 DAI Channel 2	0x0

Table 173: APU_FF_MXDSP_C1_SEL (0x6025)

Bit	Mode	Symbol	Description	Reset
[0]	RW	FF_MXDSP_C1_SEL	Select source for DSP input FF_MXDSP_C1. **Value** **Description** 0x0 Feedforward DMIC Channel 1 (Not applicable for DA7400) 0x1 DAI Channel 3	0x0

Table 174: APU_FB_MXDSP_C0_SEL (0x6026)

Bit	Mode	Symbol	Description	Reset
[0]	RW	FB_MXDSP_C0_SEL	Select source for DSP input FB_MXDSP_C0. **Value** **Description** 0x0 Feedback DMIC Channel 0 (Not applicable for DA7400) 0x1 DAI Channel 4	0x0

Table 175: APU_FB_MXDSP_C1_SEL (0x6027)

Bit	Mode	Symbol	Description	Reset
[0]	RW	FB_MXDSP_C1_SEL	Select source for DSP input FB_MXDSP_C1. **Value** **Description** 0x0 Feedback DMIC Channel 1 (Not applicable for DA7400) 0x1 DAI Channel 5	0x0

16.2.16.6 DSP Gain

Table 176: APU_USER_GAIN_C0_DB (0x6028)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	USER_GAIN_C0_DB	DSP Channel 0 user gain level in +1 dB steps (dB). **Value** **Description** 0x0 Mute 0x1 -120 ... -121 + USER_GAIN_C0_DB dB 0x8A +17 0x8B +18 (max) ... +18 (max) 0xFF +18 (max)	0x79

Table 177: APU_USER_GAIN_C0_FINE (0x6029)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	USER_GAIN_C0_FINE	DSP Channel 0 user gain level fine grain control (dB). The values shown below are added to the value in USER_GAIN_C0_DB to control the volume in finer steps. If USER_GAIN_C0_DB is set to mute or +18 dB (max), this register has no effect. **Value** **Description** 0x0 + 0 0x1 + 0.0625 ... USER_GAIN_C0_FINE * 0.0625 dB 0xF + 0.9375	0x0

Table 178: APU_USER_GAIN_C1_DB (0x602A)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	USER_GAIN_C1_DB	DSP Channel 1 user gain level in +1 dB steps (dB). **Value** **Description** 0x0 Mute 0x1 -120 ... -121 + USER_GAIN_C1_DB dB 0x8A +17 0x8B +18 (max) ... +18 (max) 0xFF +18 (max)	0x79

Table 179: APU_USER_GAIN_C1_FINE (0x602B)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	USER_GAIN_C1_FINE	DSP Channel 1 user gain level fine grain control	0x0

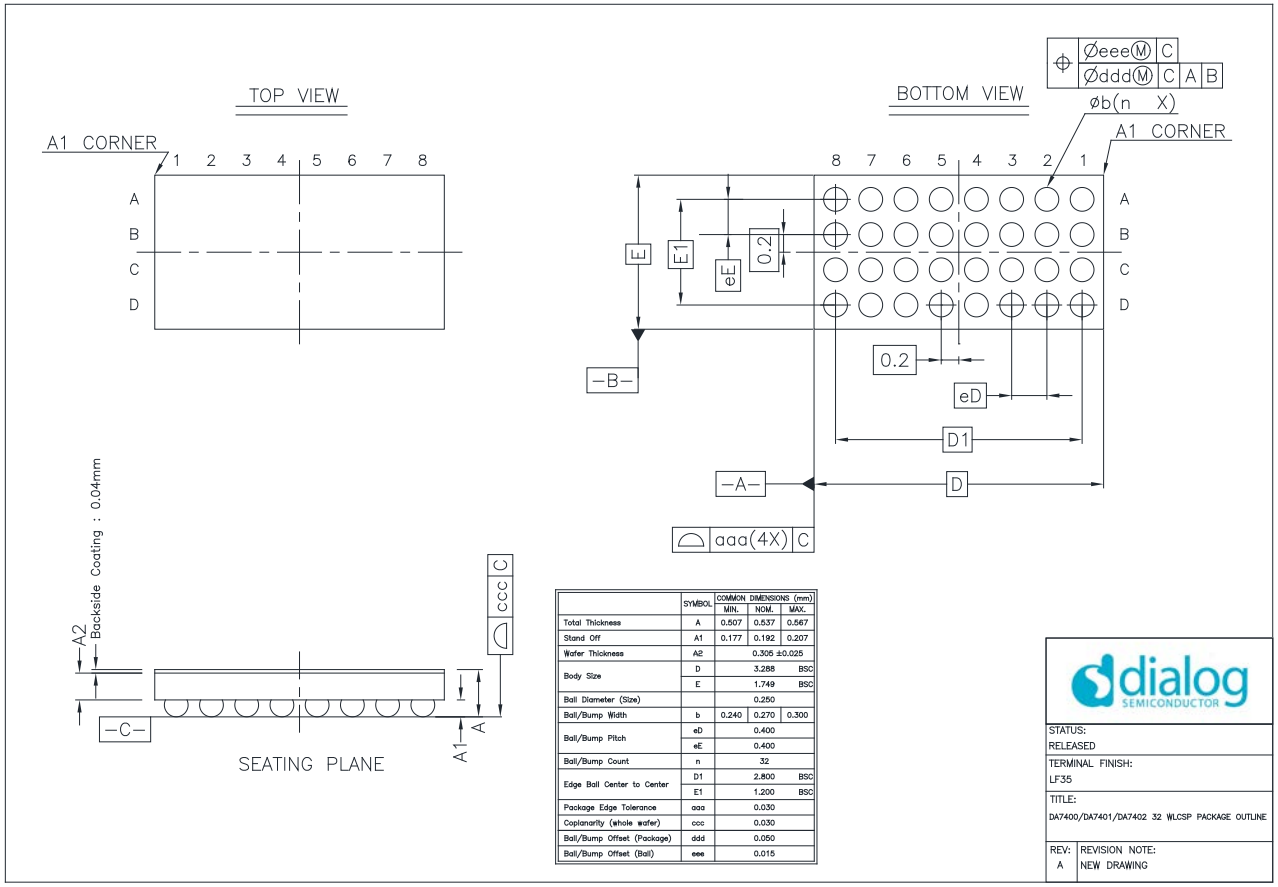
Bit	Mode	Symbol	Description	Reset
			(dB). The values shown below are added to the value in USER_GAIN_C1_DB to control the volume in finer steps. If USER_GAIN_C1_DB is set to mute or +18 dB (max), this register has no effect. **Value** **Description** 0x0 + 0 0x1 + 0.0625 ... USER_GAIN_C1_FINE * 0.0625 dB 0xF + 0.9375	

Table 180: APU_GAIN_RATE (0x602C)

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	GAIN_RATE	DSP gain rate. This determines the linear increase or decrease, relative to full scale (FS), in USER_GAIN_* per DSP sample frame. **Value** **Description** 0x0 0 0x1 (1/SSR)*10^(-120/20) ... (1/SSR)*10^((-120 + (GAIN_RATE - 1))/20) FS 0x8A (1/SSR)*10^(17/20) 0x8B (1/SSR)*10^(18/20) (max) ... (1/SSR)*10^(18/20) (max) 0xFF (1/SSR)*10^(18/20) (max)	0x8

17 Package Information

17.1 WLCSP32 Package Outline



	SYMBOL	COMMON DIMENSIONS (mm) MIN.	NOM.	MAX.
Total Thickness	A	0.507	0.537	0.567
Stand Off	A1	0.177	0.192	0.207
Wafer Thickness	A2		0.305 ±0.025	
Body Size	D		3.288	BSC
	E		1.749	BSC
Ball Diameter (Size)			0.250	
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD		0.400	
	eE		0.400	
Ball/Bump Count	n		32	
Edge Ball Center to Center	D1		2.800	BSC
	E1		1.200	BSC
Package Edge Tolerance	aaa		0.030	
Coplanarity (whole wafer)	ccc		0.030	
Ball/Bump Offset (Package)	ddd		0.050	
Ball/Bump Offset (Ball)	eee		0.015	

Figure 40: WLCSP32 Package Outline Diagram

17.2 Moisture Sensitivity Level (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60 % RH. before the solder reflow process.

WLCSP packages are qualified for MSL 1

MSL Level	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C / 85 % RH

17.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal will cause damage to the solder balls and therefore a removed sample cannot be reused.

WLCSP is sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

17.4 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

18 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Dialog Semiconductor local sales representative.

Table 181: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity Samples	Pack Quantity Production
DA7400-01 000OJ2	WLCSP	3.29 x 1.75 x 0.54	Tape and Reel	100/1000	8000

19 Application Information

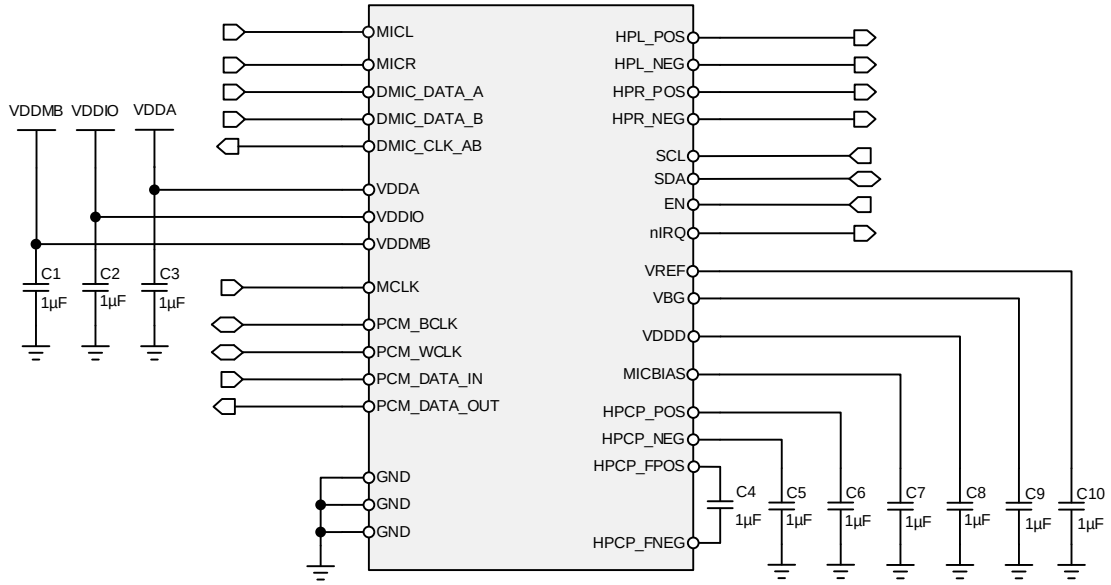


Figure 41: DA7400 External Components Diagram

Notes:

- Murata GRM155R61A105KE15D capacitor or similar recommended
- DC blocking capacitors required if analog MICL and MICR inputs are used
- C1 and C7 only required if MICBIAS is to be used
- nIRQ is open drain and must be pulled up to VDDIO
- SCL and SDA require pull-up resistors, typical value 2.2 kΩ

20 Layout Guidelines

For optimal layout, place all 1 µF decoupling capacitors as close to their respective pins as possible. If optimal placing is not possible, headphone charge pump capacitors, C4, C5, and C6 in Figure 41, carry higher currents and should be given priority. Capacitors at VBG pin (C9) and VREF pin (C10) are important and should be protected from noise coupling.

Headphone outputs are differential and should be routed as differential pairs. It is also recommended to have clearance between traces from digital pins ● and analog pins ●. GND pins and decoupling capacitors should be tied to a solid ground plane using low-impedance connections.

The WLCSP can be routed out on two layers and use capacitor size 0201, see Figure 42.

20.1 WLCSP

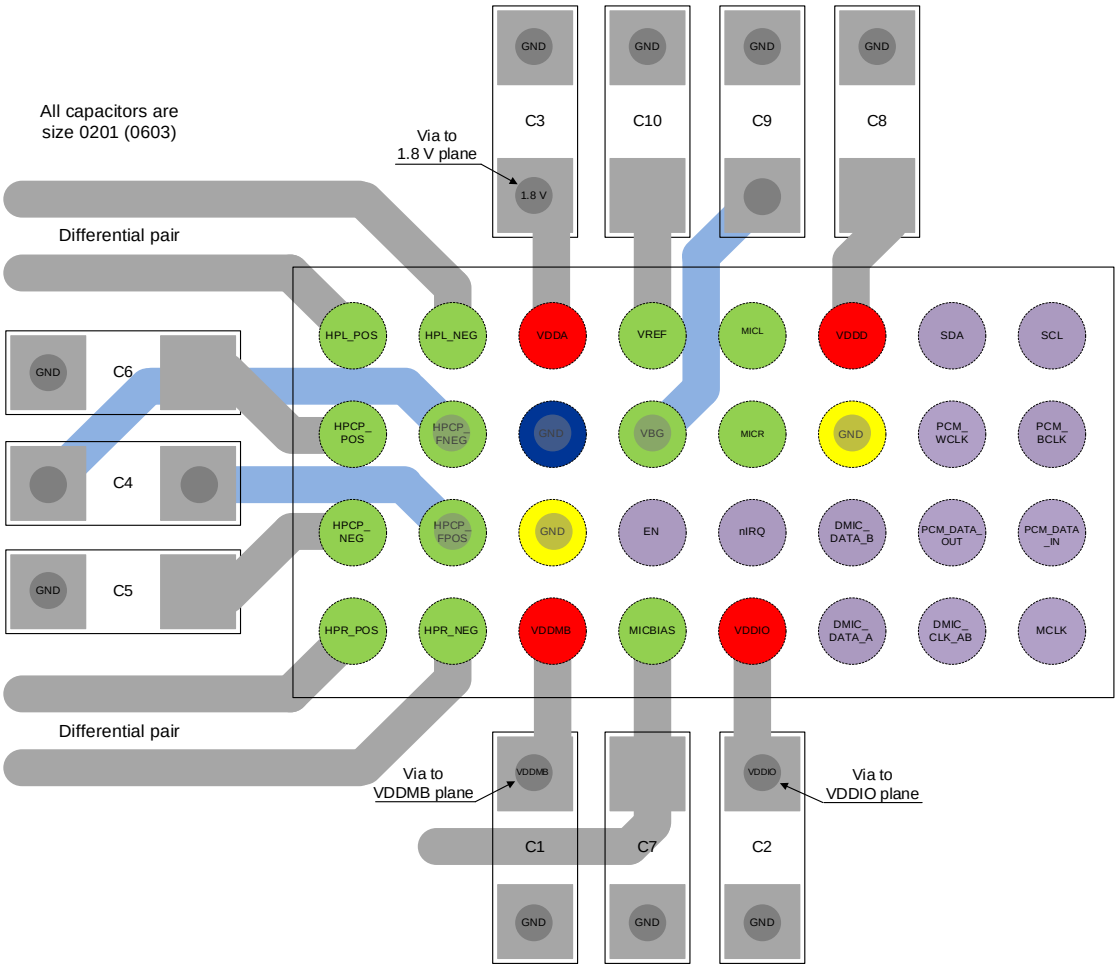


Figure 42: DA7400 WLCSP PCB Layout

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

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