

General Configuration

| Parameter | Value |
|--------------------------------------|---------------------------------|
| Device Version | XP version (150fs phase jitter) |
| Package | 7.0mm × 5.0mm |
| Output Frequency | 625.000000MHz |
| Frequency Stability | ±25ppm |
| VDD Voltage | 3.3V |
| Output Type | LVPECL |
| Output Enable/Disable (E/D) Position | Pin 1 |
| Temperature Grade | -40°C to +85°C |

Pin Assignments

| Number | Name | Description |
|--------|-----------------|-------------------------------------|
| 1 | OE | Output Enable. |
| 2 | NC | No connect. |
| 3 | GND | Connect to ground. |
| 4 | OUT0 | Output. |
| 5 | OUT0b | Complementary output. |
| 6 | V _{DD} | Supply voltage. |
| 7 | SDA | Serial data. Not used for XO mode. |
| 8 | SCL | Serial clock. Not used for XO mode. |

Revision History

| Revision Date | Description of Change |
|-------------------|-----------------------|
| February 21, 2019 | Initial release. |

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