RENESAS

PCIE RTD3

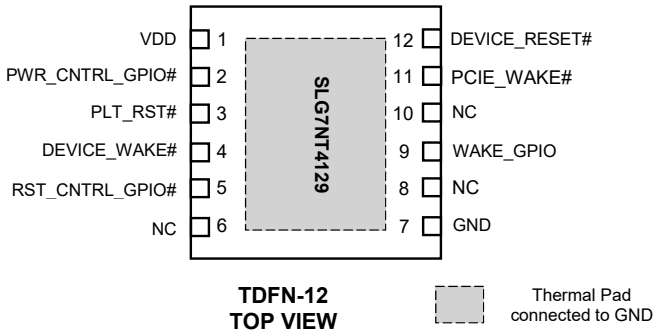
General Description

Renesas SLG7NT4129 is a low power and small form device. The SoC is housed in a 2.5mm x 2.5mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Dynamic Supply Voltage
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 Package

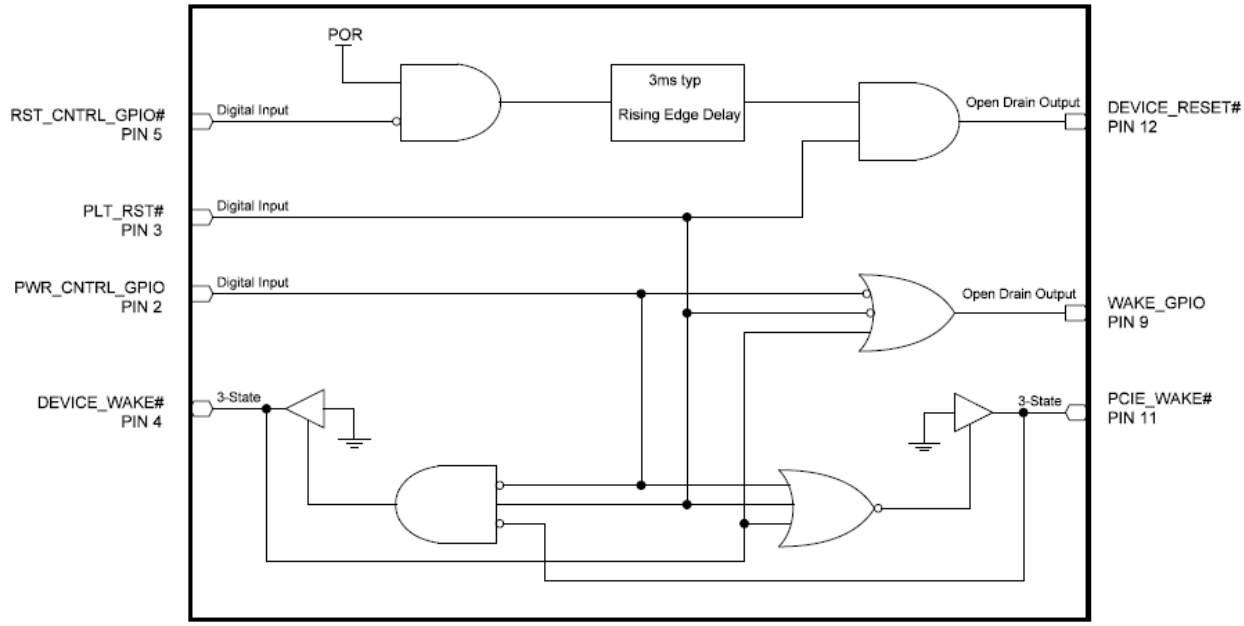
Pin Configuration



Output Summary

- 2 Outputs – Open Drain
- 2 Outputs – 3-State

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PWR_CNTRL_GPIO#	Input	Digital Input
3	PLT_RST#	Input	Digital Input
4	DEVICE_WAKE#	Input/Output	3-State
5	RST_CNTRL_GPIO#	Input	Digital Input
6	NC	--	Keep floating or connect to GND
7	GND	GND	Ground
8	NC	--	Keep floating or connect to GND
9	WAKE_GPIO	Output	Open Drain
10	NC	--	Keep floating or connect to GND
11	PCIE_WAKE#	Input/Output	3-State
12	DEVICE_RESET#	Output	Open Drain
Exposed Bottom Pad	Exposed Bottom Pad	GND	Ground

Ordering Information

Part Number	Package Type
SLG7NT4129V	V = TDFN-12
SLG7NT4129VTR	VTR = TDFN-12 - Tape and Reel (3k units)

Absolute Maximum Conditions

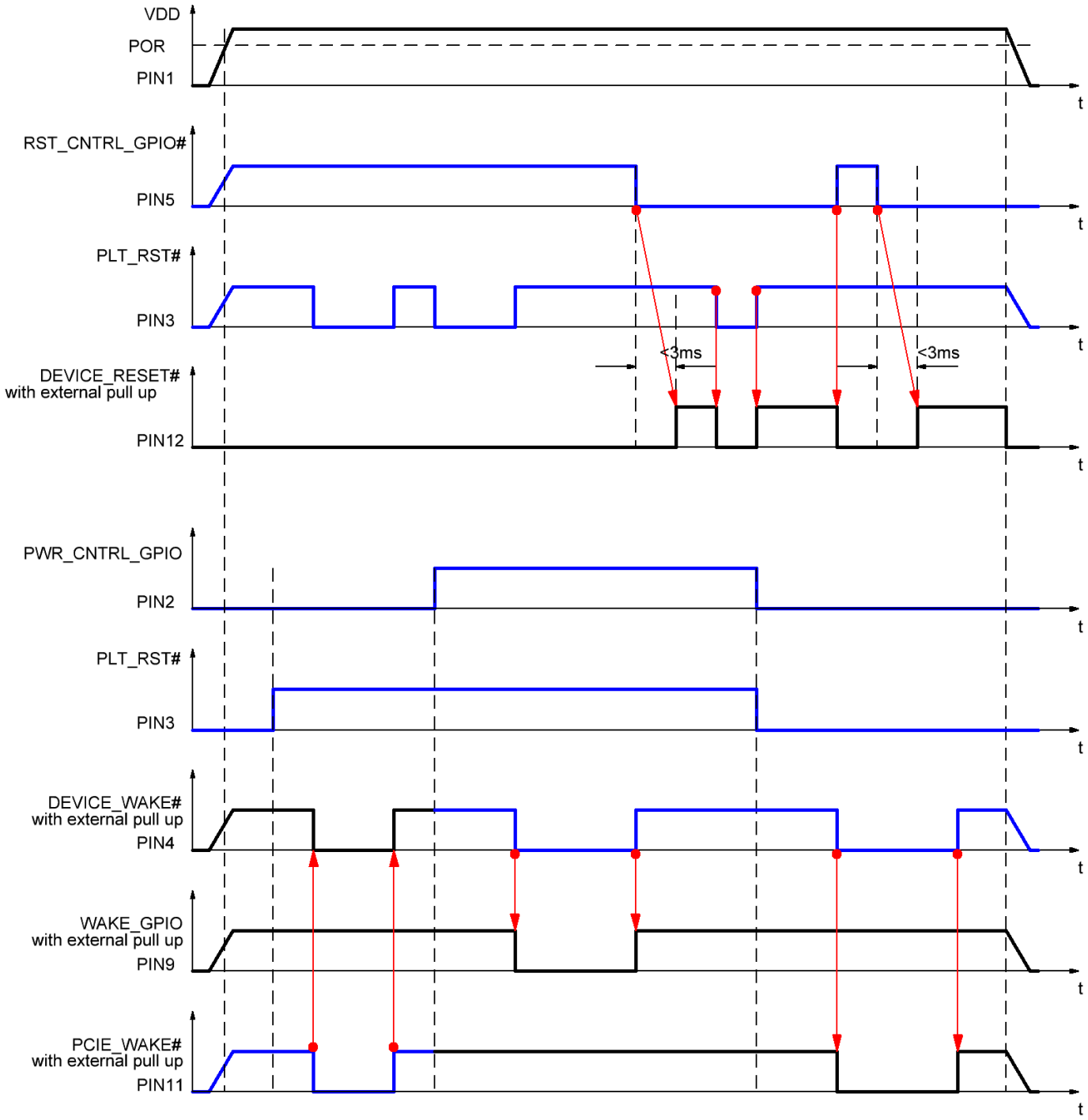
Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

Electrical Characteristics

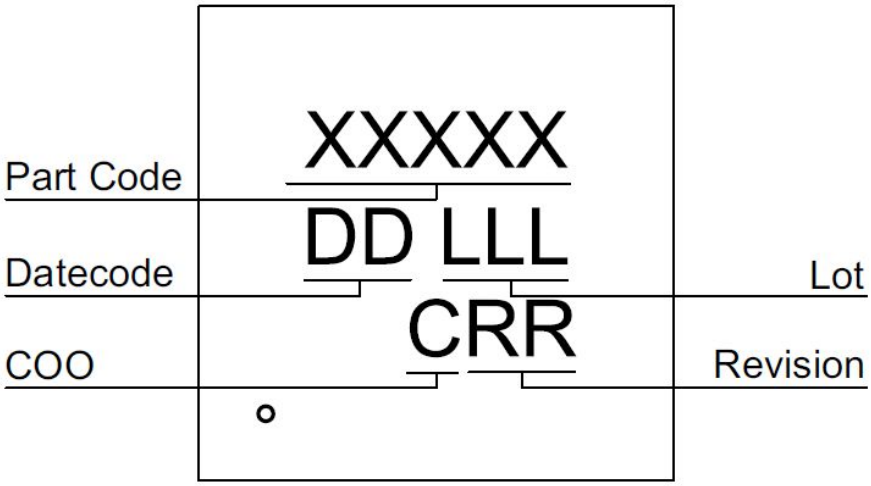
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	--	3.6	V
I_Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
T_A	Operating Temperature		-40	25	85	°C
I_L	Input Leakage Current	Leakage Current for Digital Inputs or outputs in High impedance state	-100	--	100	nA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.1	--	--	V
		Logic Input, at VDD=3.3V	1.8			
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.65	V
		Logic Input, at VDD=3.3V			1.1	
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN}=VDD	-1		1	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN}=0V	-1		1	µA
T_{DLY0}	Delay0 Time		2.1	3	3.9	ms
V_{OH}	Output Voltage High	3-State, OE=1, I_{OH} = 100µA at VDD=1.8V	1.66	--	--	V
		3-State, OE=1, I_{OH} = 3mA at VDD=3.3V	2.1	--	--	
V_{OL}	Output Voltage Low	3-State, OE=1, I_{OL} = 100µA at VDD=1.8V	--	--	0.04	V
		3-State, OE=1, I_{OL} = 3mA at VDD=3.3V	--	--	0.81	
		Open Drain, I_{OL} = 5mA, at VDD=1.8V	--	--	0.340	
		Open Drain, I_{OL} = 20mA at VDD=3.3V	--	--	0.605	
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{OL}	LOW-Level Output Current	3-State, OE=1, V_{OL} =0.15V, at VDD=1.8V	0.34	--	--	mA
		3-State, OE=1, V_{OL} = 0.4V, at VDD=3.3V	1.836	--	--	
		Open Drain, V_{OL} =0.15V, at VDD=1.8V	2.7	--	--	
		Open Drain, V_{OL} = 0.4V, at VDD=3.3V	14.6	--	--	
T_{SU}	Start up Time	After VDD reaches 1.6V level	--	7	--	ms

Timing diagram



Package Top Marking

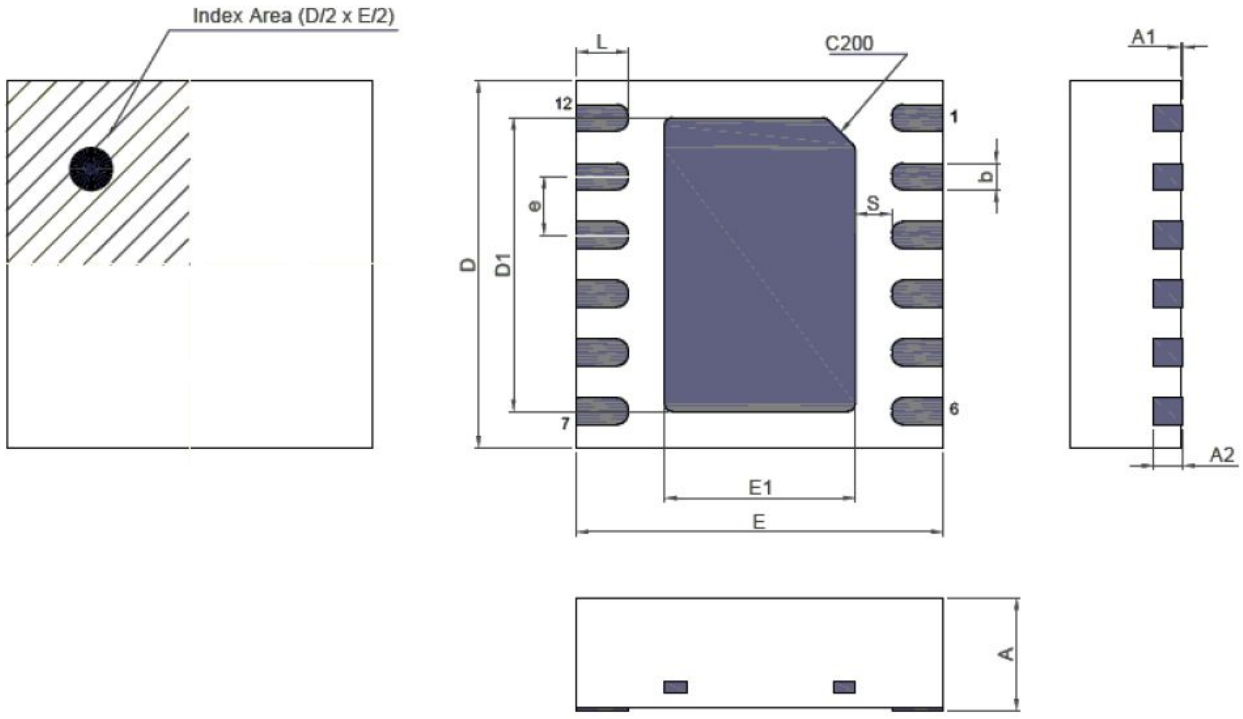


XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – COO: Specifies Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.02	04	4129V	AA	02/25/2022

Package Drawing and Dimensions

12 Lead TDFN Package
JEDEC MO-252, Variation 2525E



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				

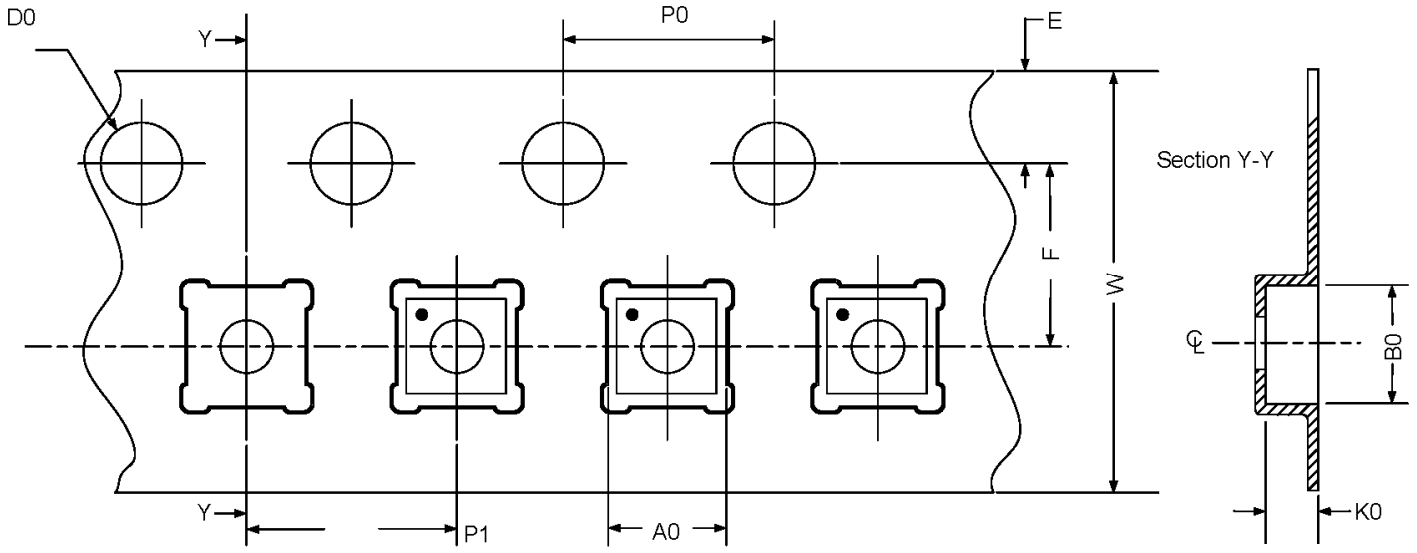
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 12L 2.5x2.5mm 0.4P Green	12	2.5x2.5x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L 2.5x2.5mm 0.4P Green	2.75	2.75	1.05	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm^3 (nominal). More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
11/08/2012	0.1	New design
11/22/2012	0.11	Changed PIN12 type to Open Drain
11/26/2012	0.20	Changed DEVICE_WAKE# and PCIE_WAKE# functionality to bi-directional
01/18/2013	0.21	Some typos in PIN out table are fixed
01/23/2013	1.0	Production Release
06/11/2013	1.01	Housekeeping (fixed block diagram)
02/25/2022	1.02	Updated Company name and logo

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(Rev.1.0 Mar 2020)

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