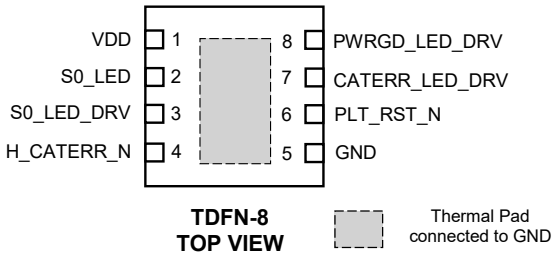
LED CONTROL

General Description

Renesas SLG7NT4084 is a low power and small form device. The SoC is housed in a 2mm x 2mm TDFN package which is optimal for using with small devices.



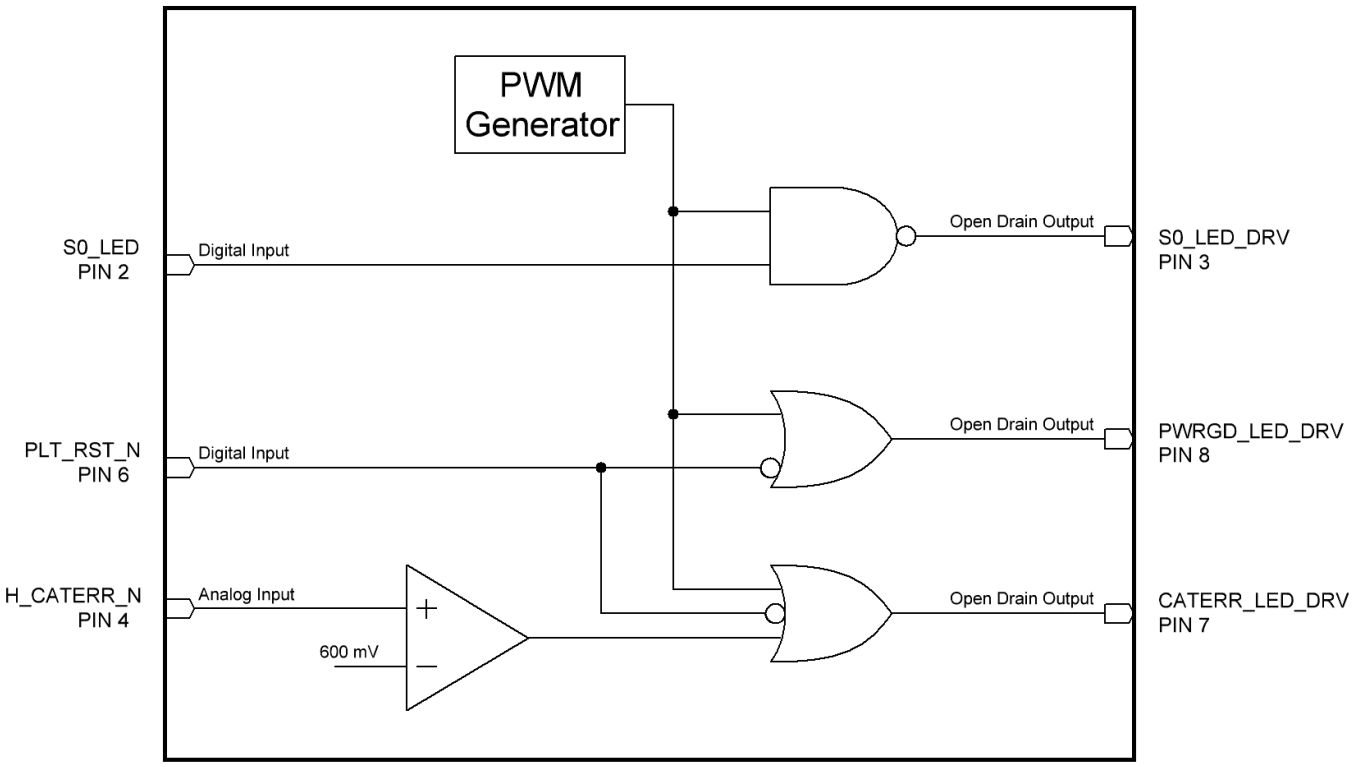
Features

- Low Power Consumption
- 3.3V Supply
- Pb-Free / RoHS Compliant
- Halogen-Free
- TDFN-8 Package

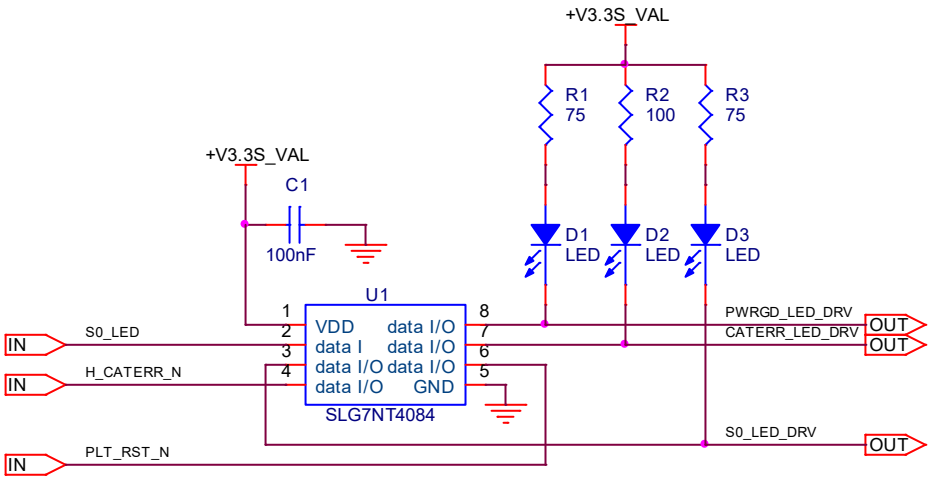
Output Summary

- 3 Outputs – Open Drain

Block Diagram



Typical Application Circuit



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	3.3V Supply Voltage
2	S0_LED	Input	Digital input
3	S0_LED_DRV	Output	Open Drain
4	H_CATERR_N	Input	Analog input
5	GND	GND	Ground
6	PLT_RST_N	Input	Digital input
7	CATERR_LED_DRV	Output	Open Drain
8	PWRGD_LED_DRV	Output	Open Drain
Exposed Bottom Pad	GND	GND	Ground

Ordering Options & Configuration

Part Number	Package Type
SLG7NT4084V	V = TDFN-8
SLG7NT4084VTR	VTR = TDFN-8 – Tape and Reel (3k units)

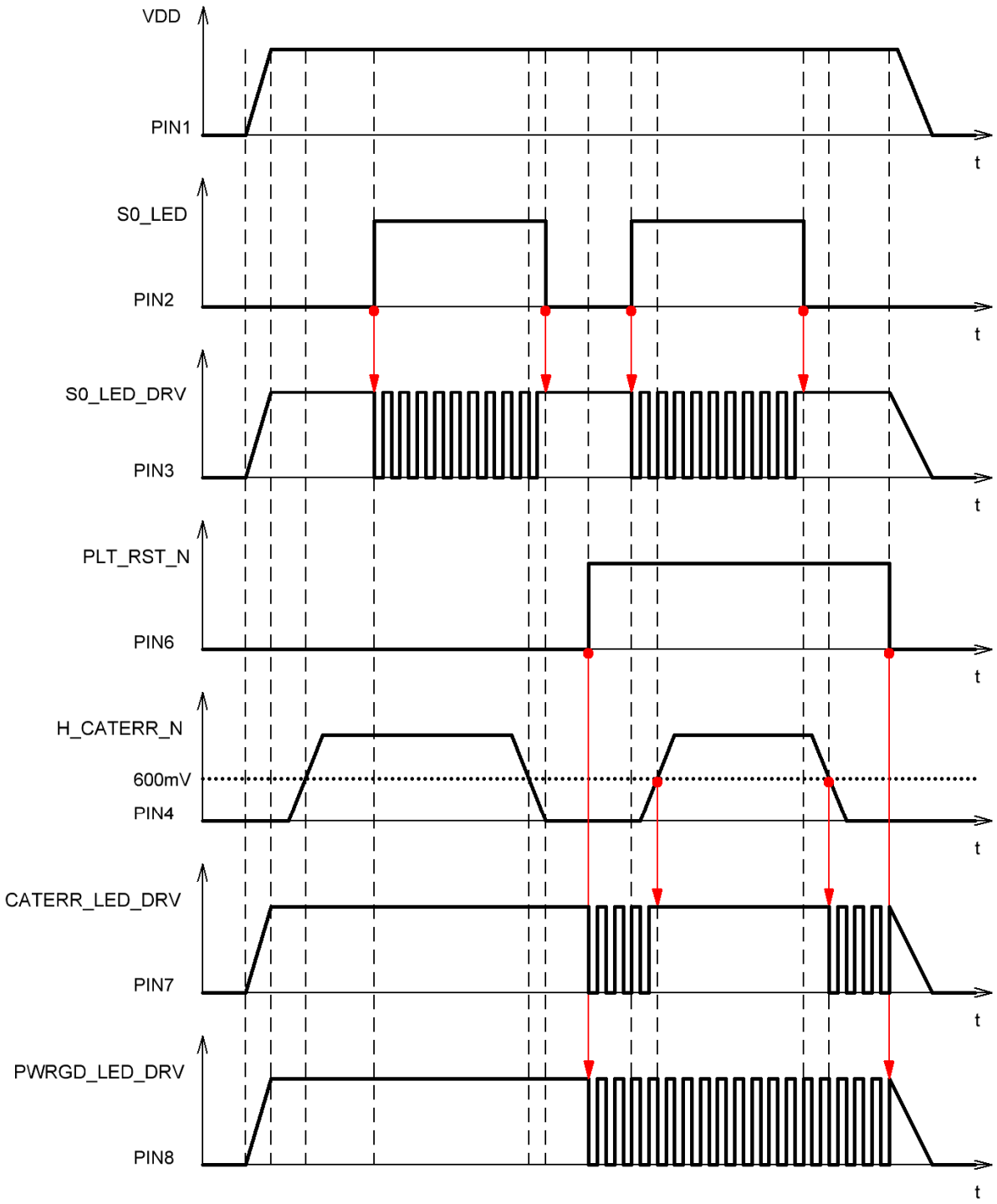
Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{DD} to GND	-0.3	4.6	V
Voltage at input pins	-0.3	4.6	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

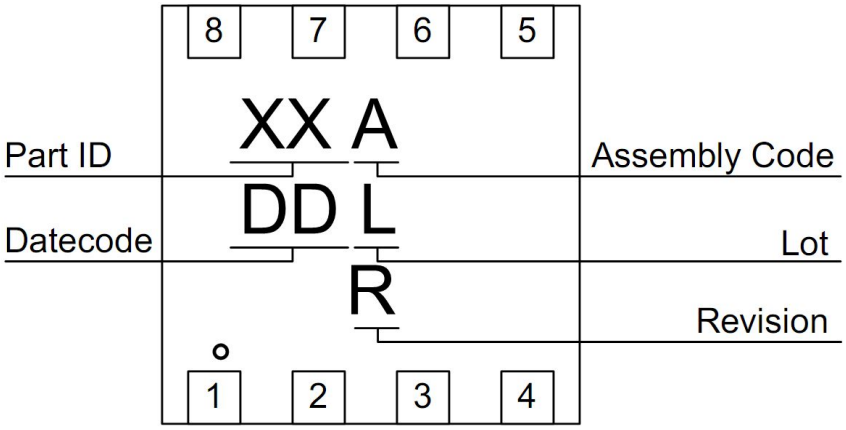
Electrical Characteristics

Symbol	Parameter	Condition / Note	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	**3.3**	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	35	--	µA
T_A	Operating temperature		-40	25	85	°C
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.8	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.95	V
V_{ACMP}	Analog Comparator Input Voltage	Analog Comparator Threshold Variation Including Hysteresis	515	--	685	mV
I_{IH}	HIGH-Level Input Leakage Current	Logic Input Pins; VIN=3.3V	-100	--	100	nA
I_{IL}	LOW-Level Input Leakage Current	Logic Input Pins; VIN=0V	-100	--	100	nA
V_{OL}	LOW-Level Output Voltage	Open Drain Logic Level Outputs	--	--	0.4	V
I_{OL}	LOW-Level Output Current	Open Drain	--	20	--	mA
T_{StUp}	Start Up Time	After VDD reaches 1.4V level	--	7	--	ms

Timing Diagram



Package Top Marking



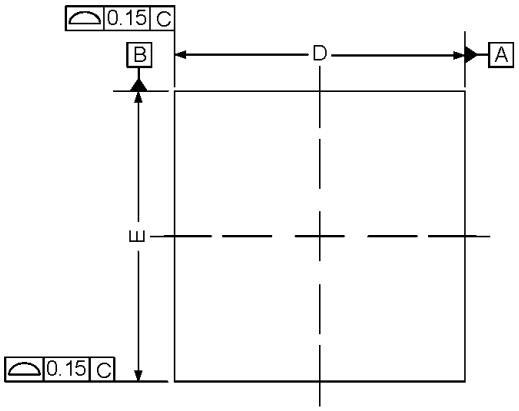
XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.03	06	JU	F	02/25/2022

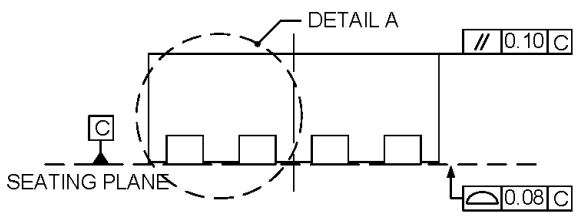
Package Drawing and Dimensions

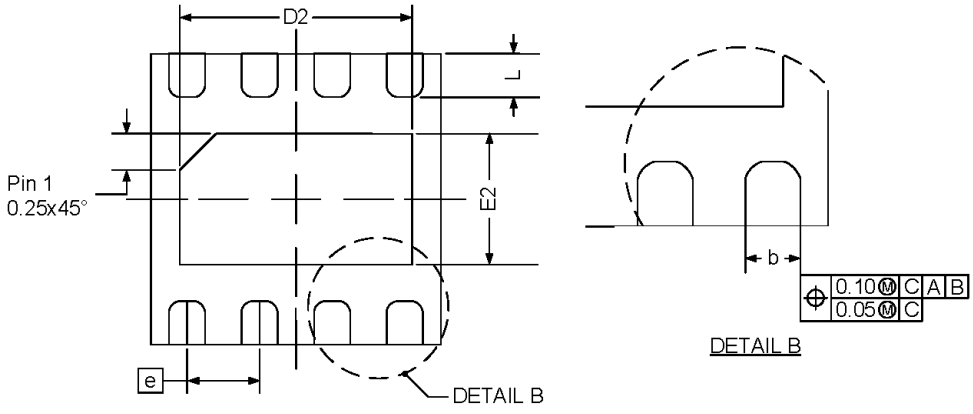
TDFN-8 Package

JEDEC MO-229, Variation WCCD



Symbol	Min (mm)	NOM (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	--	0.05
A2	--	0.55	--
A3	--	0.20	--
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.50 BSC		
L	0.20	0.30	0.40



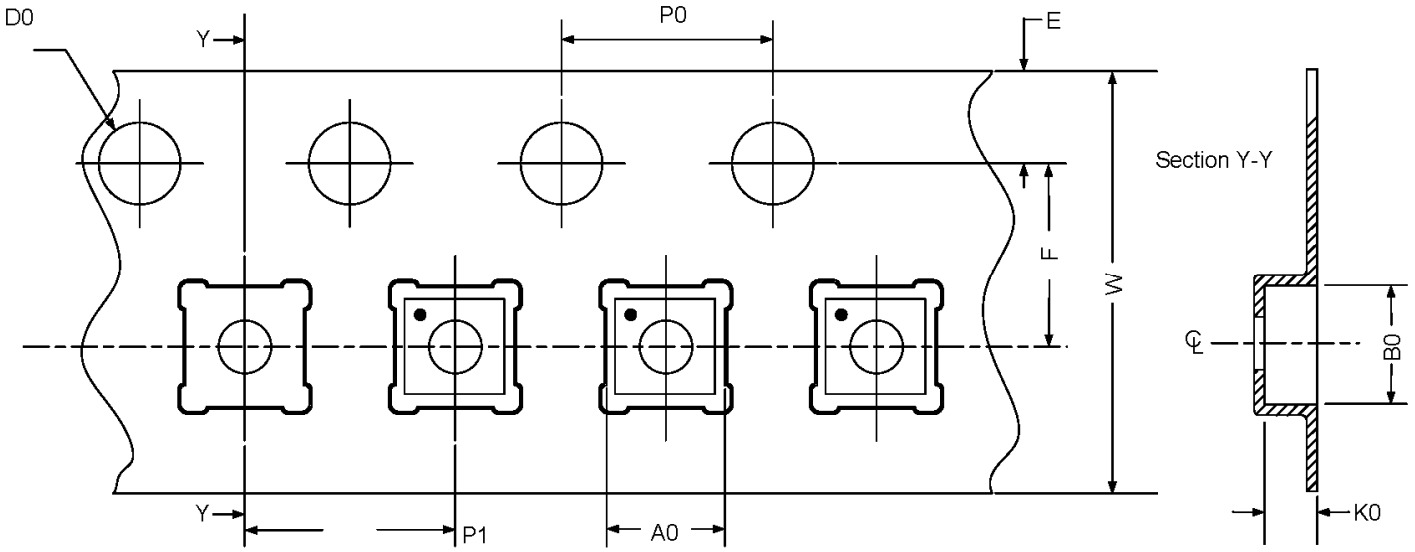


Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 8L 2x2mm Green	8	2x2x0.75	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L 2x2mm Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.