

## An Ultra-small, 17 mΩ, 2.5 A Load Switch with Discharge

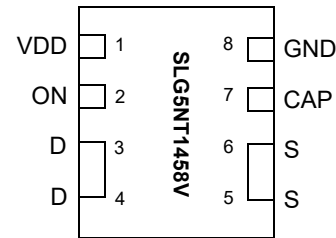
## General Description

The SLG5NT1458V is a 17 mΩ 2.5 A single-channel load switch that is able to switch 0.85 V to 5.5 V power rails. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

## Features

- 1.0 x 1.6 x 0.55 mm STDFN package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 17 mΩ RDS<sub>ON</sub> while supporting 2.5 A
- Discharges load when off
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -20 °C to 70 °C
- Operating Voltage: 2.5 V to 5.5 V

## Pin Configuration

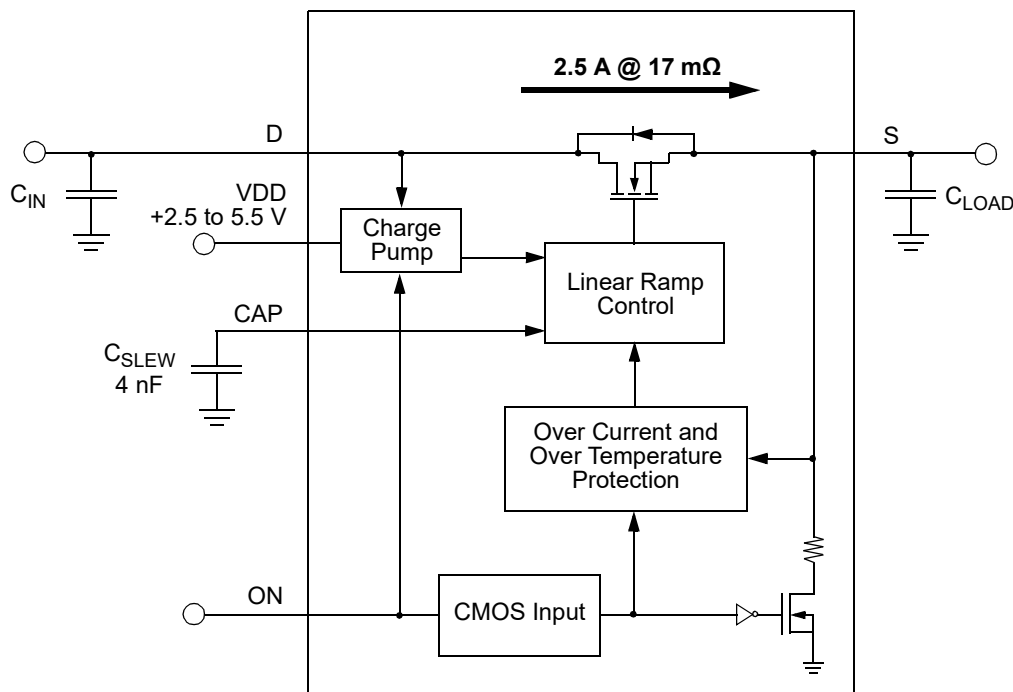


### 8-pin STDFN (Top View)

## Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

## Block Diagram



## SLG5NT1458V

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### Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG5NT1458V's state machine. ON is a CMOS input with $ON\_V_{IL} < 0.3\text{ V}$ and $ON\_V_{IH} > 0.85\text{ V}$ thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for D). Connect at least a low-ESR 0.1 μF capacitor from this pin to ground. Capacitors used at D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended $C_{LOAD}$ range. Capacitors used at S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the $V_S$ slew rate and overall turn-on time of the SLG5NT1458V. For best performance $C_{SLEW}$ value should be $\geq 1.5\text{ nF}$ and voltage level should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

### Ordering Information

Part Number	Type	Production Flow
SLG5NT1458V	STDFN 8L	Commercial, -20 °C to 70 °C
SLG5NT1458VTR	STDFN 8L (Tape and Reel)	Commercial, -20 °C to 70 °C

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## Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Power Supply		--	--	7	V
$T_S$	Storage Temperature		-65	--	150	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	--	--	V
MSL	Moisture Sensitivity Level		1			
$W_{DIS}$	Package Power Dissipation		--	--	0.4	W
MOSFET IDS <sub>PK</sub>	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	3.5	A
$\theta_{JA}$	Junction to Ambient Thermal Resistance	2-layer FR4 PCB. D and S power plane area = 1" x 1". 1 oz copper min.	--	--	72	°C/W
$\theta_{JC}$	Junction to Case Thermal Resistance	2-layer FR4 PCB. D and S power plane area = 1" x 1". 1 oz copper min.	--	--	70	°C/W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A = -20\text{ °C}$  to  $70\text{ °C}$  unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Power Supply Voltage	-20 °C to 70 °C	2.5	--	5.5	V
$I_{DD}$	Power Supply Current (PIN 1)	when OFF	--	--	1	μA
		when ON, No load	--	70	100	μA
$R_{DS(ON)}$	ON Resistance	$T_A = 25\text{ °C}$ , $I_{DS} = 100\text{ mA}$	--	17	19	mΩ
		$T_A = 70\text{ °C}$ , $I_{DS} = 100\text{ mA}$	--	18.5	20	mΩ
MOSFET IDS	Current from D to S	Continuous	--	--	2.5	A
$V_D$	Drain Voltage		0.85	--	$V_{DD}$	V
$T_{ON\_Delay}$	ON Delay Time	50% ON to $V_S$ Ramp Start; $C_{LOAD} = 10\text{ μF}$ , $R_{LOAD} = 20\text{ Ω}$	--	300	500	μs
$T_{Total\_ON}$	Total Turn On Time	50% ON to 90% $V_S$	Set by External $C_{SLEW}^1$			ms
		Example: $C_{SLEW} = 4\text{ nF}$ , $V_{DD} = V_D = 5\text{ V}$ , $C_{LOAD} = 10\text{ μF}$ , $R_{LOAD} = 20\text{ Ω}$	--	1.96	--	ms
$V_{S(SR)}$	Slew Rate	10% $V_S$ to 90% $V_S$	Set by External $C_{SLEW}^1$			V/ms
		Example: $C_{SLEW} = 4\text{ nF}$ , $V_{DD} = V_D = 5\text{ V}$ , $C_{LOAD} = 10\text{ μF}$ , $R_{LOAD} = 20\text{ Ω}$	--	3.0	--	V/ms
$C_{LOAD}$	Output Load Capacitance	$C_{LOAD}$ connected from S to GND	--	--	500	μF
$R_{DISCHARGE}$	Discharge Resistance		100	150	300	Ω
ON_ $V_{IH}$	High Input Voltage on ON pin		0.85	--	$V_{DD}$	V
ON_ $V_{IL}$	Low Input Voltage on ON pin		-0.3	0	0.3	V
$I_{LIMIT}$	Active Current Limit, $I_{ACL}$	MOSFET will automatically limit current when $V_S > 250\text{ mV}$	--	3.7	--	A
	Short Circuit Current Limit, $I_{SCL}$	MOSFET will automatically limit current when $V_S < 250\text{ mV}$	--	0.9	--	A
THERM <sub>ON</sub>	Thermal shutoff turn-on temperature		--	125	--	°C

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## Electrical Characteristics (continued)

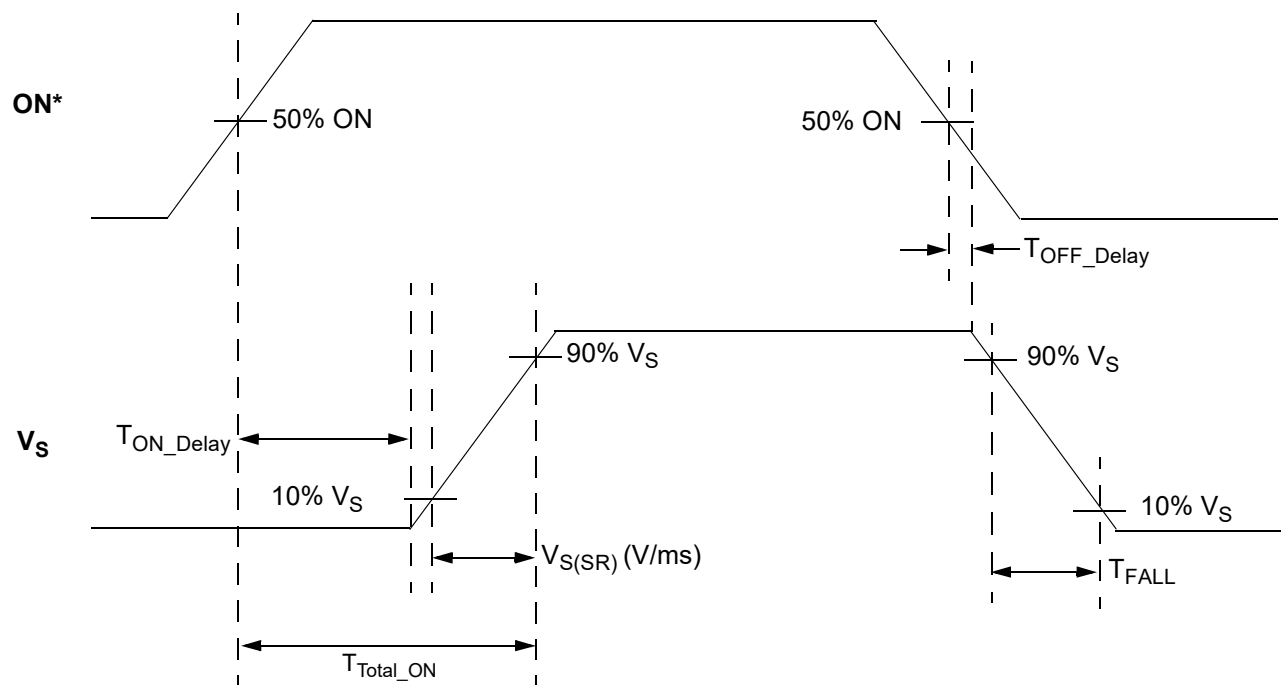
$T_A = -20\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$  unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
THERM <sub>OFF</sub>	Thermal shutoff turn-off temperature		--	100	--	$^{\circ}\text{C}$
THERM <sub>TIME</sub>	Thermal shutoff time		--	--	1	ms
T <sub>OFF_Delay</sub>	OFF Delay Time	50% ON to $V_S$ Fall Start; $V_{DD} = V_D = 5\text{ V}$ ; $R_{LOAD} = 20\text{ }\Omega$ , no $C_{LOAD}$	--	8	--	$\mu\text{s}$

Notes:

1. Refer to typical timing parameter vs.  $C_{SLEW}$  performance charts for additional information when available.

## $T_{ON\_Delay}$ , $V_{S(SR)}$ , and $T_{Total\_ON}$ Timing Details



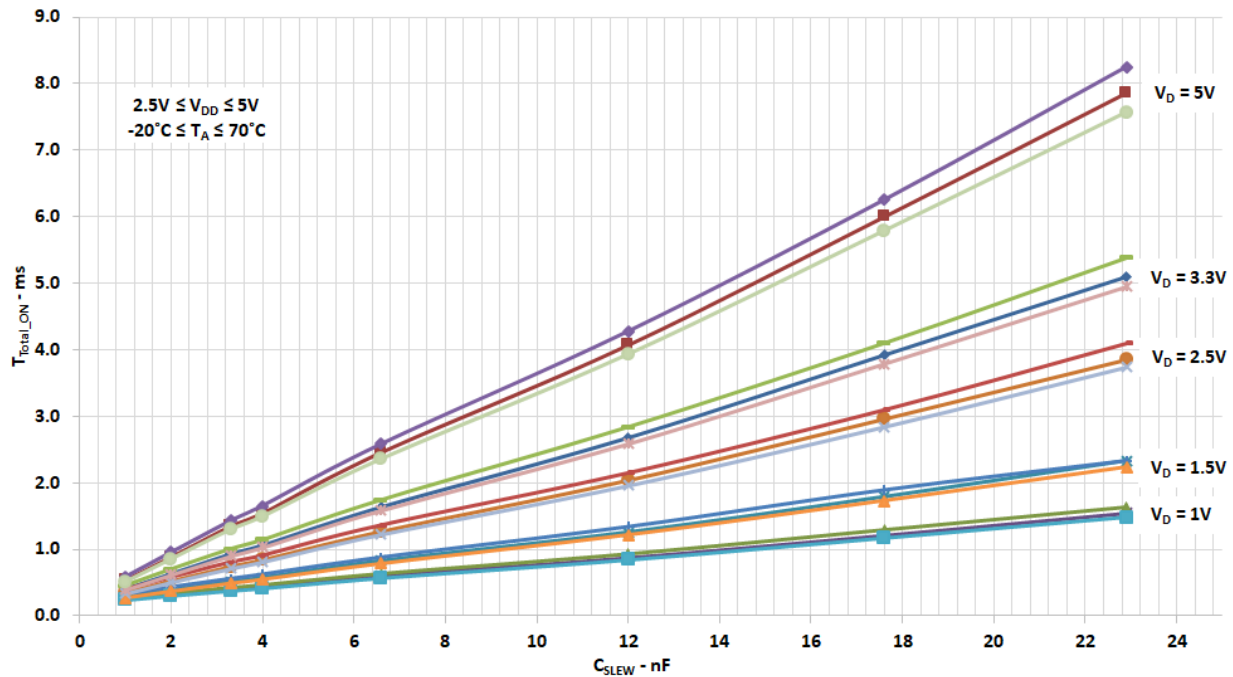
Note: \* Rise and Fall times of the ON signal are 100 ns

## SLG5NT1458V

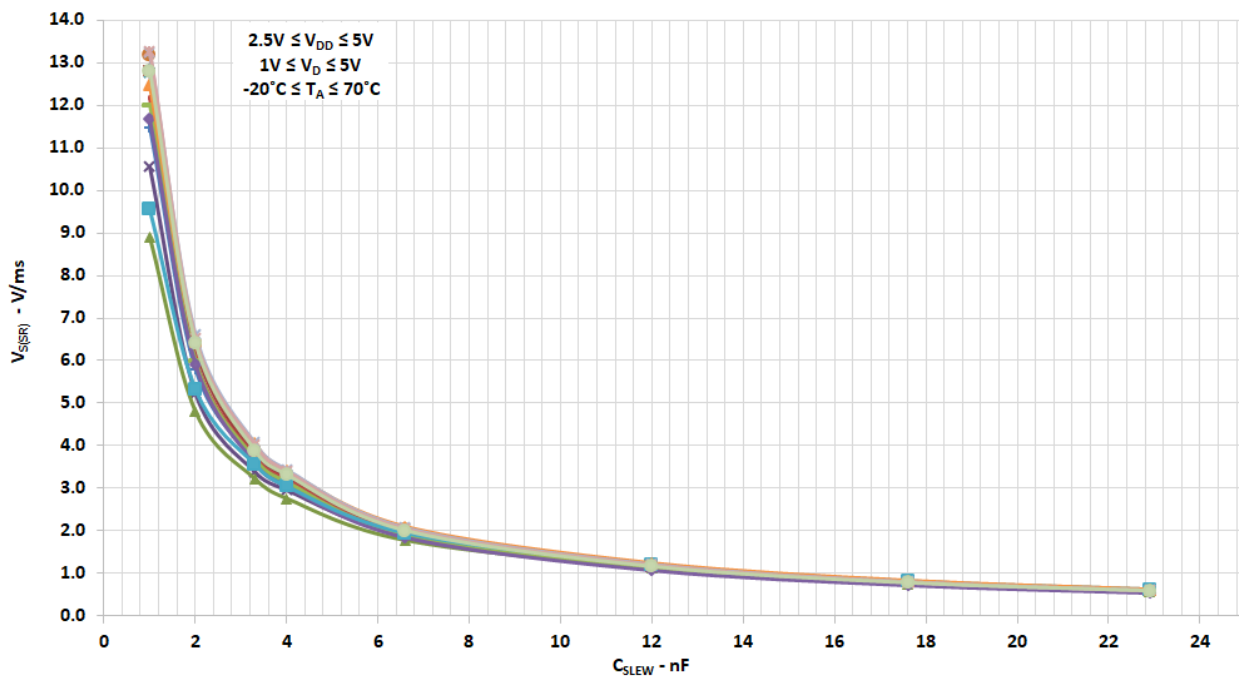
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### Typical Performance Characteristics

#### $T_{\text{Total\_ON}}$ vs $C_{\text{SLEW}}$ , $V_D$ , $V_{DD}$ , and Temperature



#### $V_S$ Slew Rate vs. $C_{\text{SLEW}}$ , $V_{DD}$ , and Temperature



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### SLG5NT1458V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply  $V_{DD}$  first, followed by  $V_D$  after  $V_{DD}$  exceeds 1 V. Then allow  $V_D$  to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If  $V_{DD}$  and  $V_D$  need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10  $\mu$ F  $C_{LOAD}$  will prevent glitches for rise times of  $V_{DD}$  and  $V_D$  less than 2 ms.

If the ON pin is toggled HIGH before  $V_{DD}$  and  $V_D$  have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output  $V_S$  follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

### SLG5NT1458V Current Limiting Operation

The SLG5NT1458V has two types of current limiting triggered by the output S pin voltage.

#### 1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the  $V_S$  voltage > 250 mV, the output current is initially limited to the Active Current Limit ( $I_{ACL}$ ) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's  $I_{ACL}$  threshold.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed  $THERM_{ON}$  specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed  $THERM_{OFF}$  temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

#### 2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the  $V_S$  voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the load switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 900 mA (the  $I_{SCL}$  threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the  $I_{SCL}$  threshold is much lower than the  $I_{ACL}$  threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

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#### Power Dissipation

The junction temperature of the SLG5NT1458V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG5NT1458V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = R_{DS(ON)} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

$R_{DS(ON)}$  = Power MOSFET ON resistance, in Ohms ( $\Omega$ )

$I_{DS}$  = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

$T_J$  = Junction temperature, in Celsius degrees ( $^{\circ}\text{C}$ )

$\theta_{JA}$  = Package thermal resistance, in Celsius degrees per Watt ( $^{\circ}\text{C}/\text{W}$ )

$T_A$  = Ambient temperature, in Celsius degrees ( $^{\circ}\text{C}$ )

During active current-limit operation, the SLG5NT1458V's power dissipation can be calculated by taking into account the voltage drop across the load switch ( $V_D - V_S$ ) and the magnitude of the output current in active current-limit operation ( $I_{ACL}$ ):

$$PD = (V_D - V_S) \times I_{ACL} \text{ or}$$

$$PD = (V_D - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

$V_D$  = Input Voltage, in Volts (V)

$R_{LOAD}$  = Load Resistance, in Ohms ( $\Omega$ )

$I_{ACL}$  = Output limited current, in Amps (A)

$V_S = R_{LOAD} \times I_{ACL}$

For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics"

## SLG5NT1458V

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### Layout Guidelines:

1. The VDD pin needs a 0.1 μF and 10 μF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG5NT1458V's PIN1.
2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 1](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C<sub>IN</sub> and output C<sub>LOAD</sub> low-ESR capacitors as close as possible to the SLG5NT1458V's D and S pins;
4. The GND pin should be connected to system analog or power ground plane.
5. 2 oz. copper is recommended for high current operation.

### SLG5NT1458V Evaluation Board:

A GreenFET Evaluation Board for SLG5NT1458V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D\_Sense and S\_Sense pads. They cannot carry high currents and dedicated only for RDS<sub>ON</sub> evaluation.

Please solder your SLG5NT1458V here

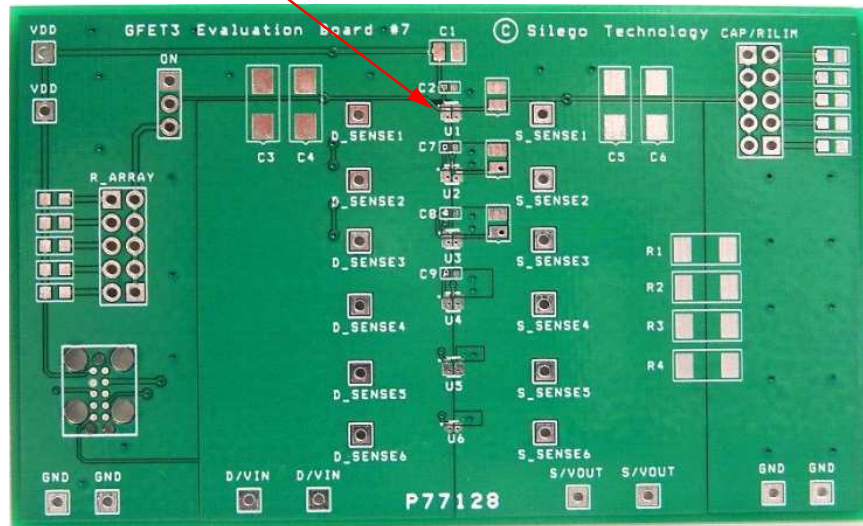
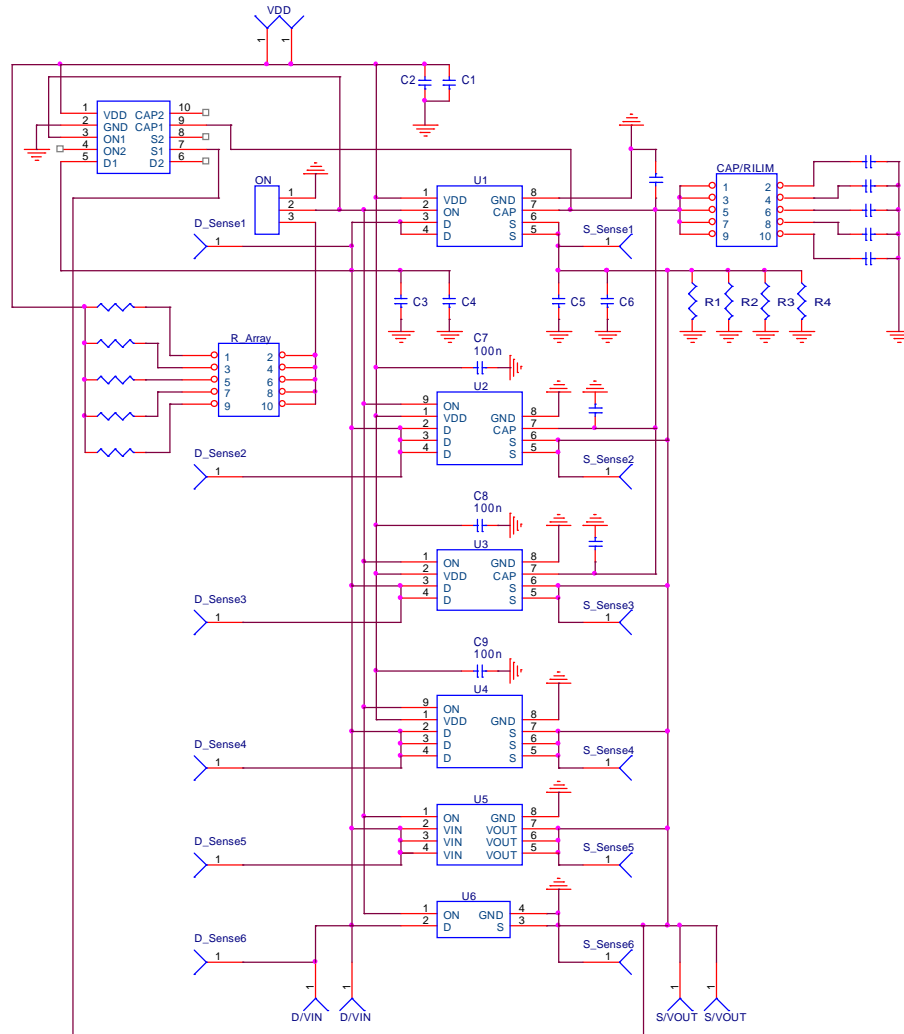


Figure 1. SLG5NT1458V Evaluation Board.



## An Ultra-small, 17 mΩ, 2.5 A Load Switch with Discharge



**Figure 2. SLG5NT1458V Evaluation Board Connection Circuit.**

# SLG5NT1458V

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## Basic Test Setup and Connections

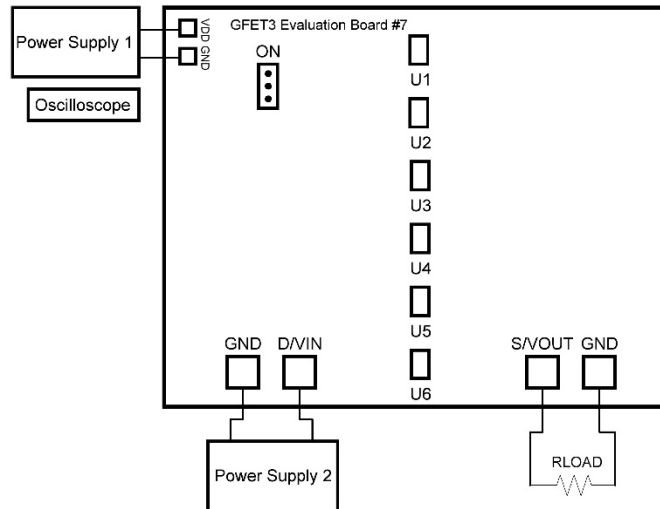


Figure 3. Typical connections for GreenFET Evaluation.

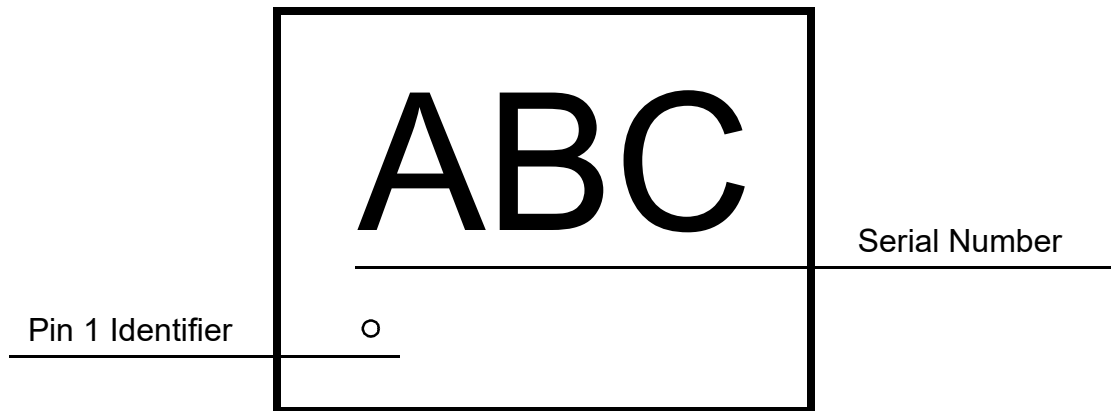
### EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
2. Turn on Power Supply 1 and set desired  $V_{DD}$  from 2.5 V...5.5 V range;
3. Turn on Power Supply 2 and set desired  $V_D$  from 0.85 V...5.5 V range;
4. Toggle the ON signal High or Low to observe SLG5NT1458V operation.

## SLG5NT1458V

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### Package Top Marking System Definition



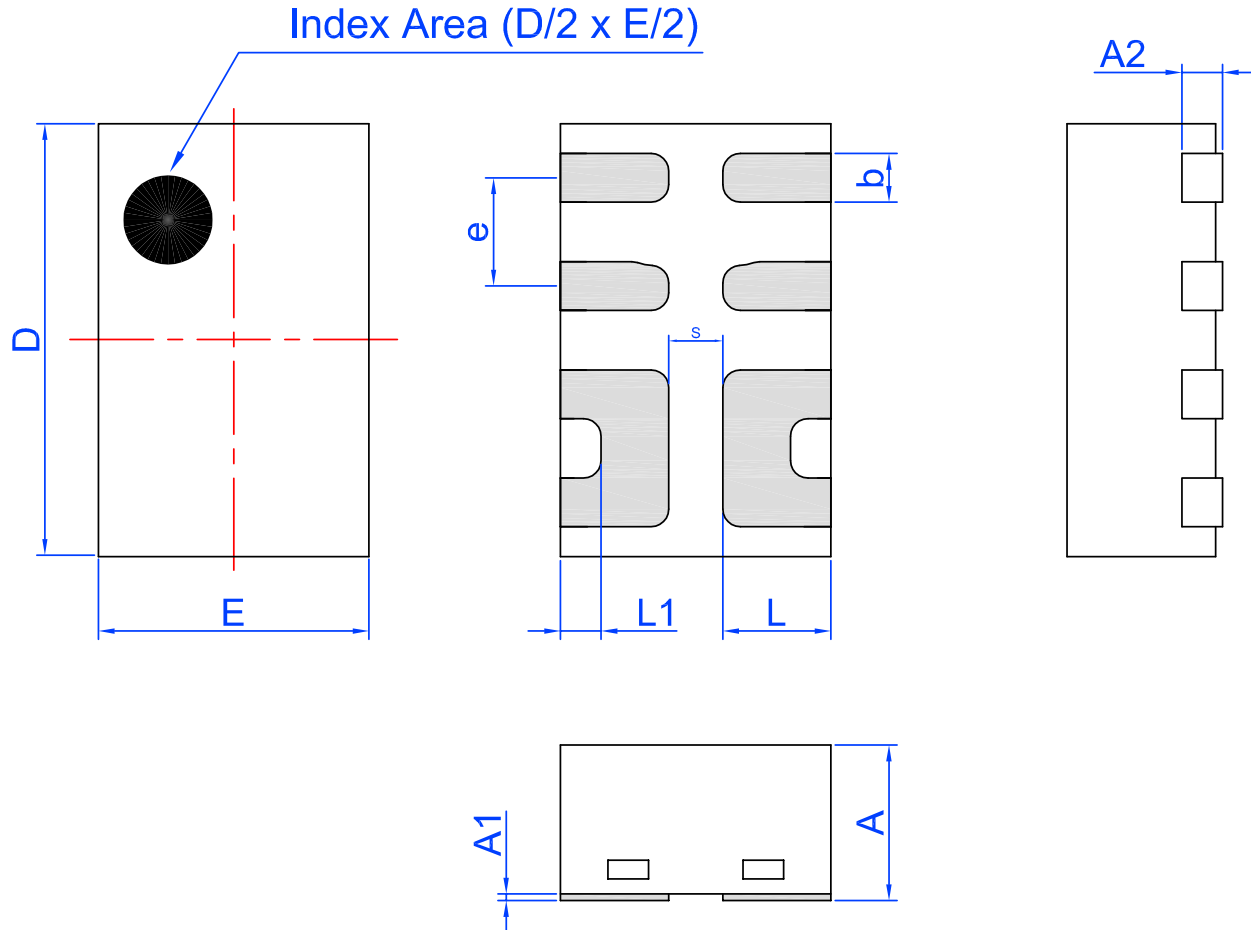
ABC - 3 alphanumeric Part Serial Number  
where A, B, or C can be A-Z and 0-9

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## Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.10	0.15	0.20
e	0.40 BSC			S	0.2 REF		

# SLG5NT1458V

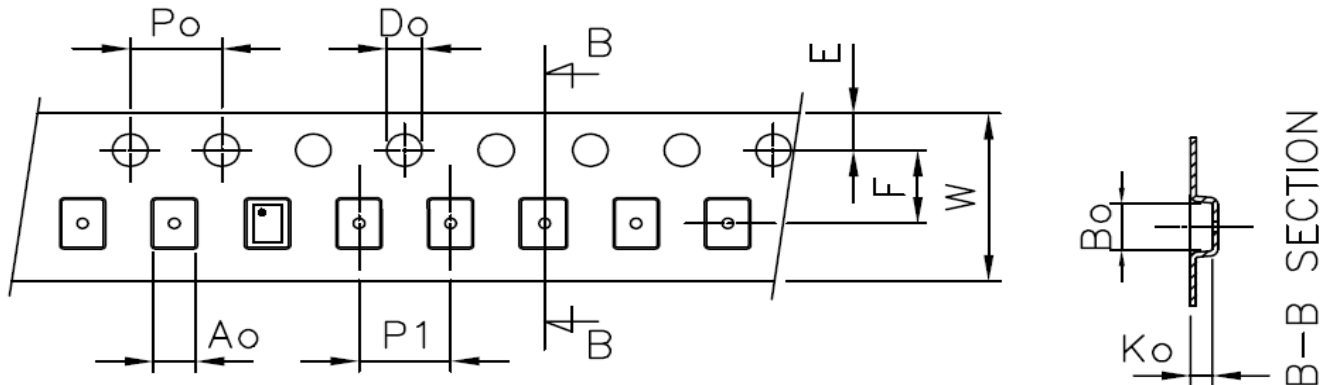
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## Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FC Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

## Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FC Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

## SLG5NT1458V

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### Revision History

Date	Version	Change
2/7/2022	1.07	Renesas rebranding Fixed typos
3/30/2020	1.06	Updated Style and Formatting Updated Pin Discription Updated Charts Added Power Dissipation Section Added Layout Guidelines Fixed typos
9/5/2016	1.05	Updated Power Up/Down Sequencing Considerations Updated Current Limiting Description Updated text and parameter names for clarity
5/25/2016	1.04	Added MSL
11/9/2015	1.03	Updated VD min to 0.85 V

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(Rev.1.0 Mar 2020)

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