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DATASHEET

AT25SL321

32-Mbit, 1.7 V Minimum SPI Serial Flash Memory with Dual I/O, Quad I/O and QPI Support

Features

- Single 1.7 V - 2.0 V Supply
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual Output Read and Quad I/O Program and Read
  - Supports QPI Program and Read
  - 104 MHz Maximum Operating Frequency
  - Clock-to-Output (t_{V1}) of 6 ns
  - Up tp 65 Mbytes/s continuous data transfer rate
- Full Chip Erase
- Flexible, Optimized Erase Architecture for Code and Data Storage Applications
  - 0.6 ms Typical Page Program (256 bytes) Time
  - 60 ms Typical 4 kbyte Block Erase Time
  - 200 ms Typical 32 kbyte Block Erase Time
  - 300 ms Typical 64 kbyte Block Erase Time
- Hardware Controlled Locking of Protected Blocks via $\overline{WP}$ Pin
- 4 kbit secured One-Time Programmable Security Register
- Hardware Write Protection
- Serial Flash Discoverable Parameters (SFDP) Register
- Flexible Programming
  - Byte/Page Program (1 to 256 bytes)
  - Dual or Quad Input Byte/Page Program (1 to 256 bytes)
  - Accelerated programming mode via 9V ACC pin
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 2 µA Deep Power-Down Current (Typical)
  - 10 µA Standby current (Typical)
  - 5 mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4, 32, or 64 kbyte blocks)
- Data Retention: 20 Years
- Industrial Temperature Range: -40 °C to +85 °C
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8S4, 8-lead SOIC (208-mil)
  - 8MA1, 8-pad UDFN (6 x 5 x 0.6 mm)
  - 8MA2, 8-pad USON(3 x 4 x 0.55 mm)
  - 8S1, 8-lead SOIC (150 mil)
  - 8-ball WLCSP, die Ball Grid Array (dBGA)

Adesto™

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1. Introduction

The Adesto® AT25SL321 is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25SL321 is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the AT25SL321 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

SPI clock frequencies of up to 104 MHz* are supported, allowing equivalent clock rates of 266 MHz for Dual Output and 532 MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O instructions.The AT25SL321 array is organized into 65,536 programmable pages of 256 bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased 4 kB Block, 32 kB Block, 64 kB Block or the entire chip.

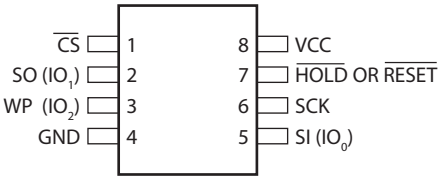
The devices operate on a single 1.7V to 1.95V power supply with current consumption as low as 5 mA active and 2 µA for Deep Power Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4-kbit Secured OTP.

*Contact Adesto for availability of 133 MHz operating frequency.

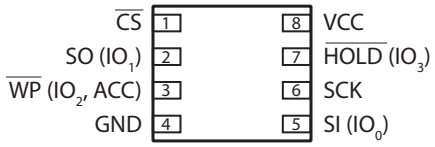
2. Pinouts and Pin Descriptions

The following figures show the available package types.

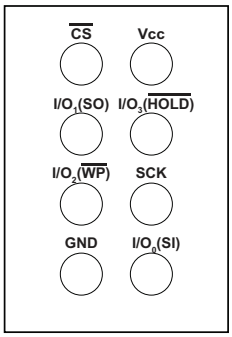
Wide and Narrrow 8-SOIC (Top View)



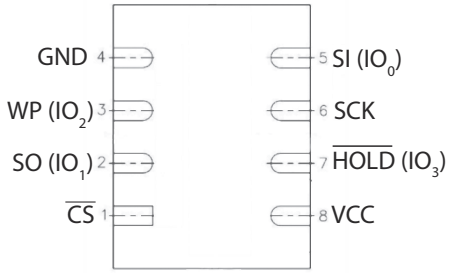
8-UDFN (Top View)



8-WLCSP (Bottom View)



8-pad USON (Bottom View)



*Final package outline drawing to be confirmed.

Figure 2-1. Package Types

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC} (min) to V_{CC} (max). All of the input and output signals must be held high or low (according to voltages of VIH, VOH, VIL or VOL.

Table 2-1. Pin Descriptions

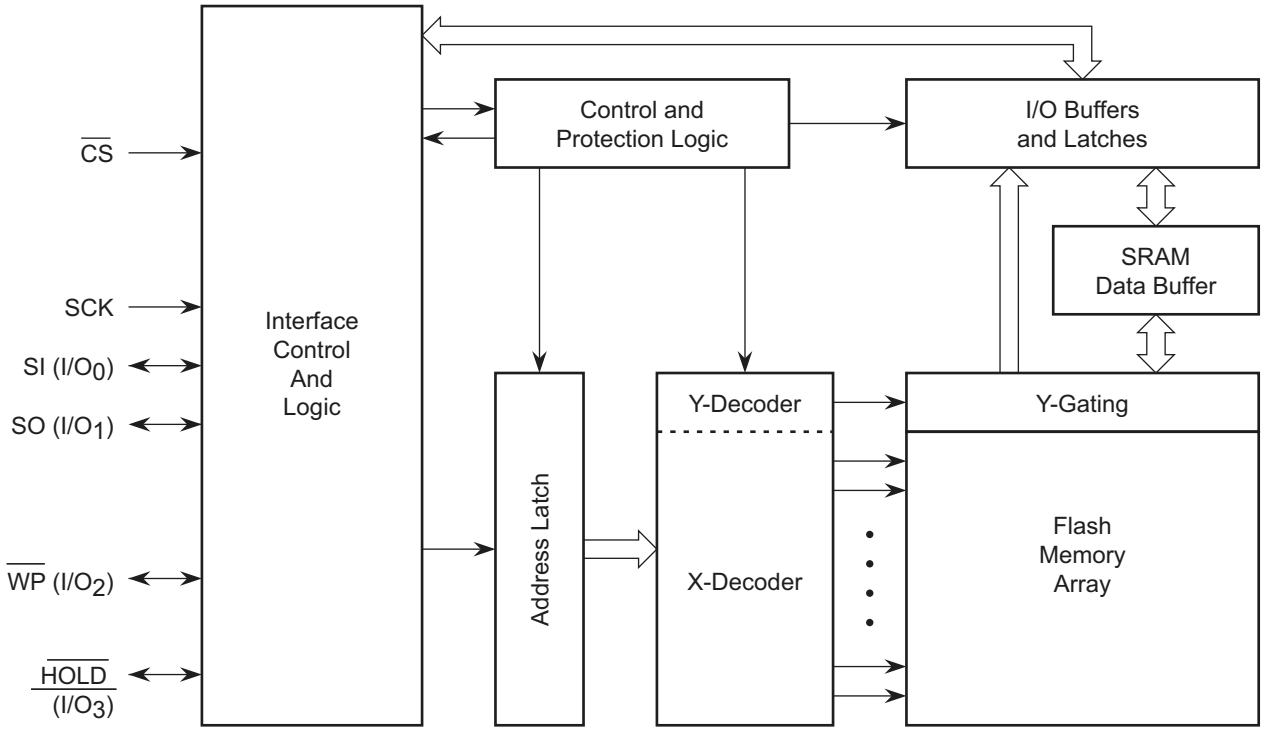
Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT** When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device needs to be in the standby power mode (this is not the deep power down mode). Driving Chip Select ($\overline{CS}$) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select ($\overline{CS}$) is required prior to the start of any instruction.	Low	Input
SCK	**SERIAL CLOCK** This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK).	-	Input
SI (I/O_0)	**SERIAL INPUT** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin (I/O_0) in conjunction with other pins to allow two or four bits of data on (I/O_{3-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes in which case it is referenced as I/O_0. Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
SO (I/O_1)	**SERIAL OUTPUT** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O0) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it is referenced as I/O_1. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
$\overline{WP}$ (I/O_2)	**WRITE PROTECT** The Write Protect ($\overline{WP}$) pin can be used to protect the Status Register against data modification. The $\overline{WP}$ pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the $\overline{WP}$ pin (Hardware Write Protect) function is not available since this pin is used for IO_2. See figures 1-1, 1-2, and 1-3 for the pin configuration of Quad I/O and QPI operation.	-	Input/Output
ACC	**ACCELERATED PROGRAMMING** The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{HH} on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing V_{HH} from the ACC pin returns the device to normal operation. Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device result. The ACC function is only available during standard SPI Mode.		

Table 2-1. Pin Descriptions *(continued)*

Symbol	Name and Function	Asserted State	Type
$\overline{HOLD}$ (I/O_3)	**$\overline{HOLD}$** The $\overline{HOLD}$ pin is used to pause a serial sequence of the SPI flash memory without resetting the clocking sequence. To enable the $\overline{HOLD}$ mode, the $\overline{CS}$ must be in low state. The $\overline{HOLD}$ mode effects on with the falling edge of the $\overline{HOLD}$ signal with CLK being low. The $\overline{HOLD}$ mode ends on the rising edge of $\overline{HOLD}$ signal with SCK being low. In other words, $\overline{HOLD}$ mode can't be entered unless SCK is low at the falling edge of the $\overline{HOLD}$ signal. And $\overline{HOLD}$ mode can't be exited unless SCK is low at the rising edge of the $\overline{HOLD}$ signal. If $\overline{CS}$ is driven high during a $\overline{HOLD}$ condition, it resets the internal logic of the device. As long as $\overline{HOLD}$ signal is low, the memory remains in the $\overline{HOLD}$ condition. To re-work communication with the device, $\overline{HOLD}$ must go high, and $\overline{CS}$ must go low. See Figure 9.11 for $\overline{HOLD}$ timing.	-	Input/Output
V_{CC}	**DEVICE POWER SUPPLY:** V_{CC} is the supply voltage. It is the single voltage used for all device functions including read, program, and erase. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages produce spurious results; do not attempt them.	-	Power
GND	**GROUND:** V_{SS} is the reference for the V_{CC} supply voltage. The ground reference for the power supply. Connect GND to the system ground.	-	Power

3. Block Diagram

Figure 3-1 shows a block diagram of the AT25SL321 serial Flash.



Note: I/O_{3-0} pin naming convention is used for Dual-I/O and Quad-I/O commands.

Figure 3-1. AT25SL321 Block Diagram

4. Memory Array

To provide the greatest flexibility, the memory array of the AT25SL321 can be erased in four levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram illustrates the breakdown of each erase level.

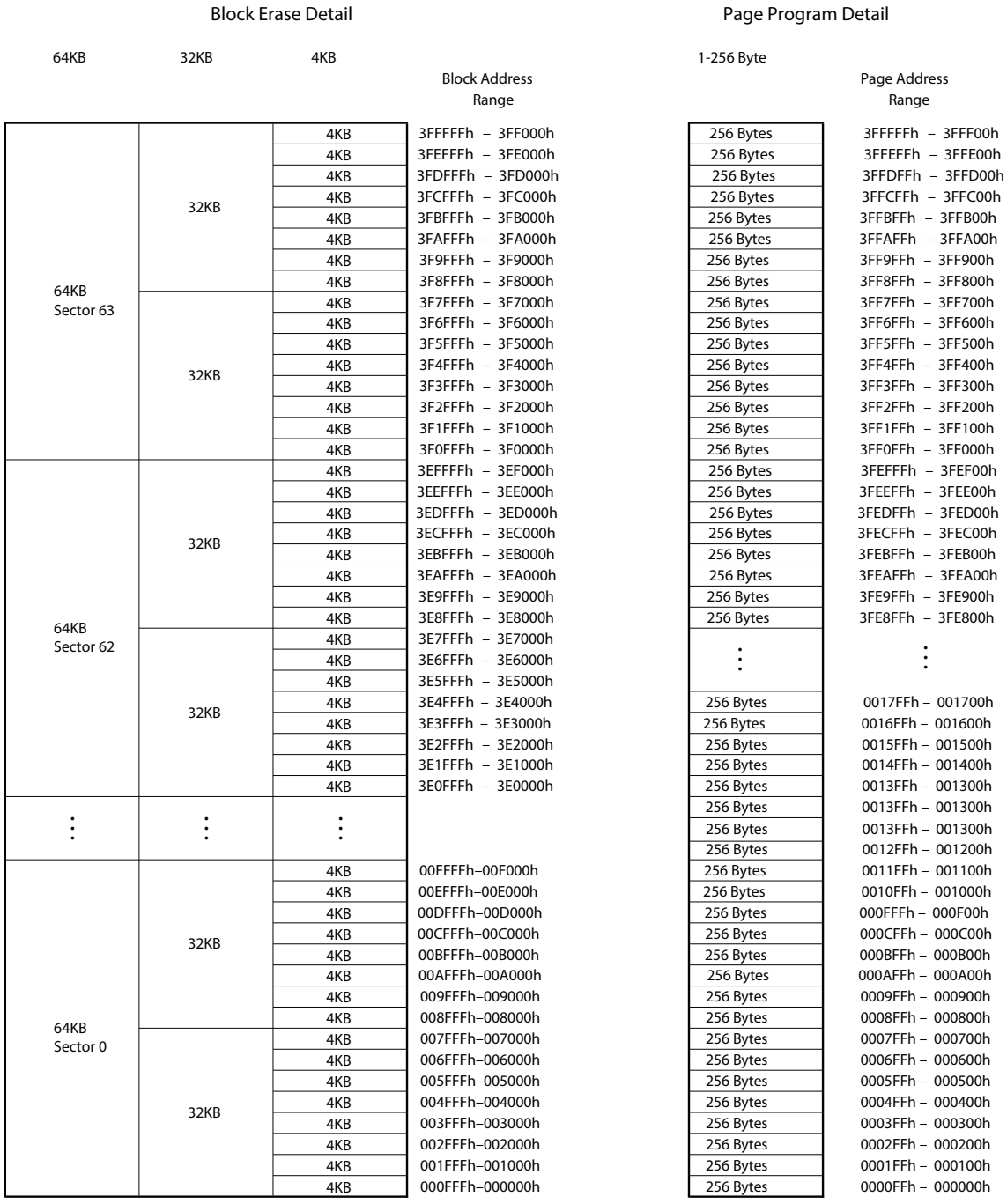


Figure 4-1. Memory Architecture Diagram

5. Device Operation

5.1 Standard SPI Operation

The AT25SL321 features a serial peripheral interface on four signals: Serial Clock (SCK). Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of $\overline{CS}$. For Mode 3 the SCK signal is normally high on the falling and rising edges of $\overline{CS}$.

5.2 Dual SPI Operation

The AT25SL321 supports Dual SPI operation. This instruction allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions the SI and SO pins become bidirectional I/0 pins; IO_0 and IO_1.

5.3 Quad SPI Operation

The AT25SL321 supports Quad SPI operation. This instruction allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code- shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the SI and SO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

5.4 QPI Operation

The AT25SL321 supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/Dual/ Quad SPI mode to QPI mode. To switch to QPI mode, the following two events must occur in order:

1. Set the non-volatile Quad Enable bit (QE) in Status Register-2.
2. Execute the Enable QPI (38h) instruction.

When using QPI instructions, the SI and SO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively.

The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/ Dual/ Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time, The Enable QPI (38h) and Disable QPI (FFh) instructions are used to switch between these two modes. Upon power-up or after software reset using the Reset (99h) instruction, the default state of the device is Standard/Dual/Quad SPI mode.

6. Write Protection

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory.

6.1 Write Protect Features

- While Power-on reset, all operations are disabled and no instruction is recognized.
- An internal time delay of t_{PUW} can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register and the Write Status Register instructions.
- For data changes, Write Enable instruction must be issued to set the Write Enable Latch (WEL) bit to “0”. Power-up, Completion of Write Disable, Write Status Register, Page program, Block Erase and Chip Erase are subjected to this condition.
- Write Protect ($\overline{WP}$) pin can control to change the Status Register under hardware control.
- The Deep Power Down mode provides extra protection from unexpected data changes as all instructions are ignored under this status except for Release Deep Power Down instruction.

7. Status Register

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the $\overline{WP}$ pin.

Table 7-1. Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
SRP	(R)	(R)	(R)	(R)	(R)0	WEL	BUSY
Status Register Protect 0 (Non-Volatile)	Reserved	Reserved	Reserved	Reserved	Reserved	Write Enable Latch	Erase or Write in Progress

Table 7-2. Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS	(R)	(R)	(R)	(R)	(R)	QE	SRP1
Suspend Status	Reserved	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non- Volatile)	Status Register Protect 1 (Non-Volatile)

7.1 Busy

BUSY is a read-only bit in the Status register (S0) that hardware sets to 1 whenever the device is executing a Page Program, Erase, Write Status Register or Write Security Register instruction. During this time the device ignores further instructions, except for the Read Status Register and Erase / Program Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE1}, t_{BE2}, and t_{CE} in AC Characteristics). When the Program, Erase, Write Status Register or Write Security Register instruction has completed, hardware clears the BUSY bit to 0, indicating the device is ready for further instructions.

7.2 Write Enable Latch (WEL)

The Write Enable Latch (WEL) is a read-only bit in the Status register (S1) that hardware sets to 1 after executing a Write Enable (06h) instruction. Hardware clears the WEL bit when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Erase, and Write Status Register.

7.3 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the Status register (S8 and S7). The SRP bits control the method of write protection. These include software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 7-3. Encoding of the SRP[1:0] Bits in the Status Register

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	0	X	Software Protected	The register can be written to after a Write Enable instruction, WEL = 1. [Factory Default]
0	1	0	Hardware Protected	When $\overline{WP}$ pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When $\overline{WP}$ pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power down, power-up cycle(1)
1	1	X	One-Time Program	Status Register is permanently protected and cannot be written to.

Note 1. When SRP1, SRP0 = (1,0), a power down, power-up cycle changes SRP1, SRP0 = (0,0).

7.4 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the $\overline{WP}$ pin and $\overline{HOLD}$ are enabled. When the QE pin is set to a 1 the Quad IO_2 and IO_3 pins are enabled. **WARNING: Never set The QE bit to a 1 during standard SPI or Dual SPI operation if the $\overline{WP}$ or $\overline{HOLD}$ pins are tied directly to the power supply or ground.**

7.5 Erase/Program Suspend Status (SUS)

The Suspend Status bit (SUS) is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power down, power-up cycle.

8. Instructions

The SPI instruction set of the AT25SL321 consists of thirty eight basic instructions and the QPI instruction set of the AT25SL321 consists of thirty-one basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 8-1 and Table 8-2). Instructions are initiated with the falling edge of Chip Select ($\overline{CS}$). The first byte of data clocked into the input pins (SI or IO [3:0]) provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions are completed with the rising edge of edge $\overline{CS}$. Clock relative timing diagrams for each instruction are included in Figure 8-1 through Figure 8-63. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte ($\overline{CS}$ driven high after a full 8-bit have been clocked) otherwise the instruction needs to be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Register are ignored until the program or erase cycle has completed.

Table 8-1. Manufacturer and Device Identification

		ID code	Instruction
Manufacturer ID	Adesto	1Fh	90h, 92h, 94h, 9Fh
Device ID	AT25SL321	15h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	42h	9Fh
Capacity Type ID	32M	16h	9Fh

8.1 Instruction Set Tables

Table 8-2. Instruction Set Table 1 (SPI instruction)(1)

Instruction Name	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
(Clock Number)	**(0 – 7)**	**(8 - 15)**	**(16 - 23)**	**(24 - 31)**	**(32 - 39)**	**(40 - 47)**
Write Enable	06h					
Write Enable For Volatile Status Register	50h					
Write Disable	04h					
Read Status Register-1	05h	(SR7-SR0)(2)				
Read Status Register-2	35h	(SR15-SR8)(2)				
Write Status Register-1	01h	(SR7-SR0)	(SR15-SR8)			
Write Status Register-2	31h	(SR15-SR8)				
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read Data	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	
Enable QPI	38h					
Block Erase (4 kB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32 kB)	52h	A23-A16	A15-A8	A7-A0		

Table 8-2. Instruction Set Table 1 (SPI instruction)[1] *(continued)*

Instruction Name	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
(Clock Number)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Block Erase(64 kB)	D8h	A23-A16	A15-A8	A7-A0		
Chip Erase	60h/C7h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Deep Power Down	B9h					
Release Deep Power down/ Device ID[4]	ABh	dummy	dummy	dummy	(ID7-ID0)[2]	
Read Manufacturer/ Device ID[4]	90h	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)
Read JEDEC ID	9Fh	(MID7-MID0) Manufacturer	(D7-D0) Memory Type	(D7-D0) Capacity Type		
Reset Enable	66h					
Reset	99h					
Enter Secured OTP	B1h					
Exit Secured OTP	C1h					
ReadSecurity Register	2Bh	(SC7-SC0) [10]				
WriteSecurity Register	2Fh					
Read Serial Flash Discovery Parameter	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)

Table 8-3. Instruction Set Table 2 (Dual SPI Instruction)

Instruction Name	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
(Clock Number)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[6]
Fast Read Dual I/O	BBh	A23-A8[5]	A7-A0, M7-M0[3]	(D7-D0, …)[6]		
Read Dual Manufacturer/ Device ID[4]	92h	0000h	(00h, xxxx) or (01h, xxxx)	(MID7-MID0) (DID7-DID0)[6]		

Table 8-4. Instruction Set Table 3 (Quad SPI Instruction)

Instruction Name	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
(Clock Number)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) [8]
Fast Read Quad I/O	EBh	A23-A0, M7-M0[7]	(xxx, D7-D0,…)[9]	(D7-D0, …)[8]		
Quad Page Program	33h	A23-A0 (D7-D0, …)[8]				
Read Quad Manufacturer /Device ID[4]	94h	(00_0000h, xx) or (00_0001h, xx)	(xxxx,MID7-MID0) (xxxx,DID7-DID0)[9]			
Word Read Quad I/O	E7h	A23-A0, M7-M0[7]	(xx, D7-D0..)	(D7-D0)[8]		
Set Burst with Wrap	77h	xxxxxx, W6-W4[7]				

Table 8-5. Instruction Set Table 4 (QPI instruction)

Instruction Name		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
(Clock Number)		(0 – 1)	(2 - 3)	(4 - 5)	(6 - 7)	(8 - 9)	(10 - 11)	(12 - 13)	(14 - 15)	(16 - 17)
Write Enable		06h								
Write Enable for Volatile Status Register		50h								
Write Disable		04h								
Read Status Register-1		05h	(SR7-SR0) [2]							
Read Status Register-2		35h	(SR15-SR8)[2]							
Write Status Register-1[5]		01h	(SR7-SR0)	(SR15-SR8)						
Write Status Register-2		31h	(SR15-SR8)							
Fast Read Data	>80 MHz	0Bh	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
Page Program		02h	A23-A16	A15-A8	A7-A0	(D7-D0)[3]				
Block Erase(4 kB)		20h	A23-A16	A15-A8	A7-A0					
Block Erase(32 kB)		52h	A23-A16	A15-A8	A7-A0					
Block Erase(64 kB)		D8h	A23-A16	A15-A8	A7-A0					
Chip Erase		60h/C7h								
Erase/Program Suspend		75h								
Erase/Program Resume		7Ah								
Deep Power Down		B9h								
Release Deep Power Down		ABh								

Table 8-5. Instruction Set Table 4 (QPI instruction) *(continued)*

Instruction Name		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
(Clock Number)		(0 – 1)	(2 - 3)	(4 - 5)	(6 - 7)	(8 - 9)	(10 - 11)	(12 - 13)	(14 - 15)	(16 - 17)
Read Manufacturer/Device ID(4)		90h	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)			
Read JEDEC ID(4)		9Fh	(MID7-MID0) Manufacturer	(D7-D0) Memory Type	(D7-D0) Capacity Type					
Enter Security		B1h								
Exit Security		C1h								
Read Security Register		2Bh	(SC7-SC0) (10)							
Write Security Register		2Fh								
Fast Read Quad I/O	>80 MHz	EBh	A23-A16	A15-A8	A7-A0	(M7-M0)	dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	(M7-M0)	dummy	dummy	(D7-D0)	
Reset Enable		66h								
Reset		99h								
Disable QPI		FFh								
Burst Read with Wrap	>80 MHz	0Ch	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
Set Read Parameter		C0h	P7-P0							
Quad Page Program		33h	A23-A16	A15-A8	A7-A0	(D7-D0)				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the IO pin.
2. SR = status register, The Status Register contents and Device ID are repeated continuously until $\overline{CS}$ terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrite previously sent data.
4. See Manufacturer and Device Identification table for Device ID information.
5. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
6. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap Input
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x x
8. Quad Input/ Output Data
   IO0 = (D4, D0…)
   IO1 = (D5, D1…)
   IO2 = (D6, D2…)
   IO3 = (D7, D3…)
9. Fast Read Quad I/O Data Output
   IO0 = (x, x, x, x, D4, D0…)
   IO1 = (x, x, x, x, D5, D1…)
   IO2 = (x, x, x, x, D6, D2…)
   IO3 = (x, x, x, x, D7, D3…)
10. SC = security register

8.2 Write Enable (06h)

Write Enable instruction is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set prior to every Program, Erase and Write Status Register instruction. To enter the Write Enable instruction, drive $\overline{CS}$ low prior to driving the instruction 06h onto the SI pin on the rising edge of SCK, and then driving $\overline{CS}$ high to terminate the operation.

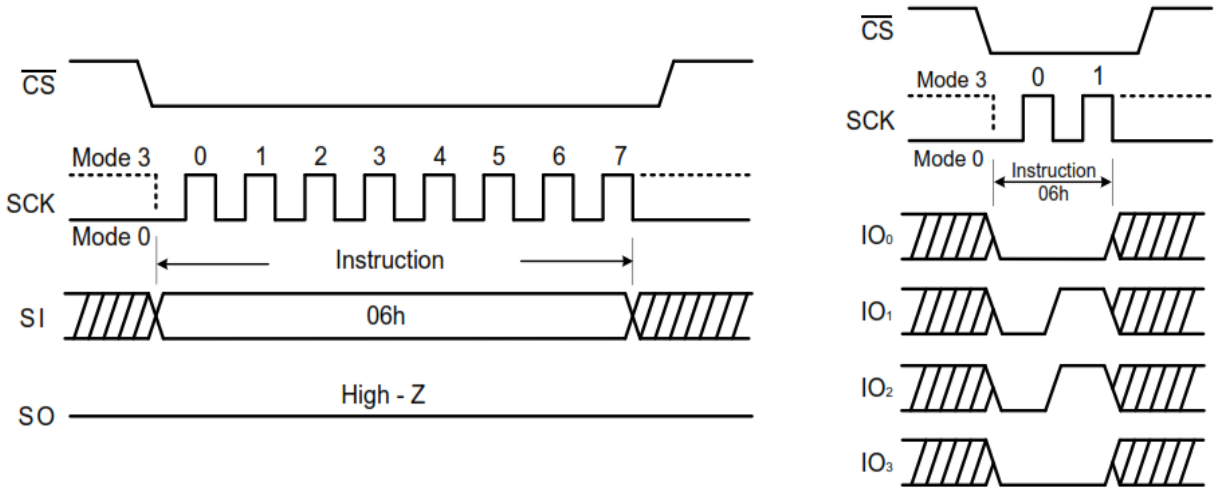


Figure 8-1. Write Enable Instruction for SPI Mode (left) and QPI Mode (right)

8.3 Write Enable for Volatile Status Register (50h)

This instruction provides additional flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Execution of the Write Enable for Volatile Status Register instruction (Figure 8-2) does not set the Write Enable Latch (WEL) bit.

Once the Write Enable for Volatile Status Register instruction is executed, a Write Enable instruction can not have been issued prior to setting Write Status Register instruction (01h or 31h). When the Write Enable for Volatile Status Register (50h) is set in QPI Mode, the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 must be driven to high after a Write Status Register instruction (01h). Once a Read Status Register (05h or 31h) is issued, the read values of SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 are ignored.

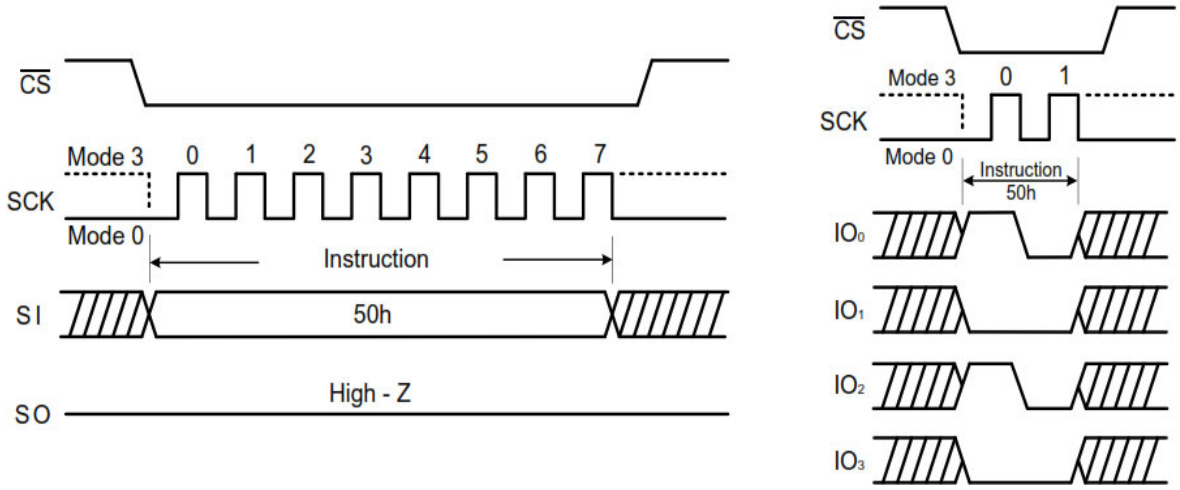


Figure 8-2. Write Enable for Volatile Status Register Instruction for SPI Mode (left) and QPI Mode (right)

8.4 Write Disable (04h)

The Write Disable instruction is used to reset the Write Enable Latch (WEL) bit in the Status Register. To enter the Write Disable instruction, assert $\overline{CS}$ low prior to driving the instruction 04h onto the SI on the rising edge of SCK, and then driving $\overline{CS}$ high to terminate the operation. The WEL bit is automatically reset write- disable status of “0” after Power-up and upon completion of the every Program, Erase and Write Status Register instructions.

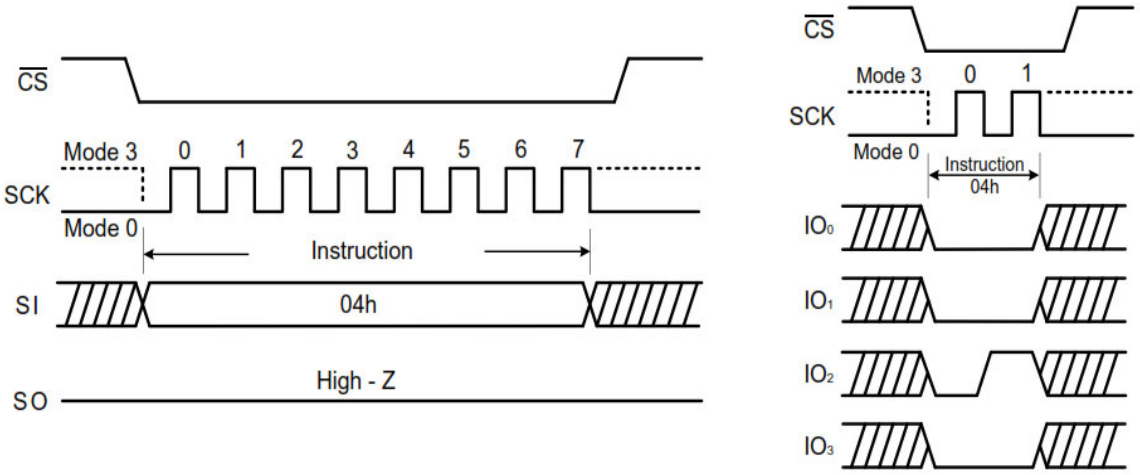


Figure 8-3. Write Disable Instruction for SPI Mode (left) and QPI Mode (right)

8.5 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions are to read the Status Registers. The Read Status Register can be executed at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the BUSY bit before sending a new instruction when a Program, Erase, Write Status Register or Write Status Register operation is in progress.

The instruction is entered by driving $\overline{CS}$ low and sending the instruction code 05h for Status Register-1 or 35h for Status Register-2 onto the SI pin on the rising edge of SCK. The Status register bits are then shifted out on the SO pin at the falling edge of SCK with the most significant bit (MSB) first as shown in (Figure 8-4 and Figure 8-5). The Status Register can be read continuously. The instruction is completed by driving $\overline{CS}$ high.

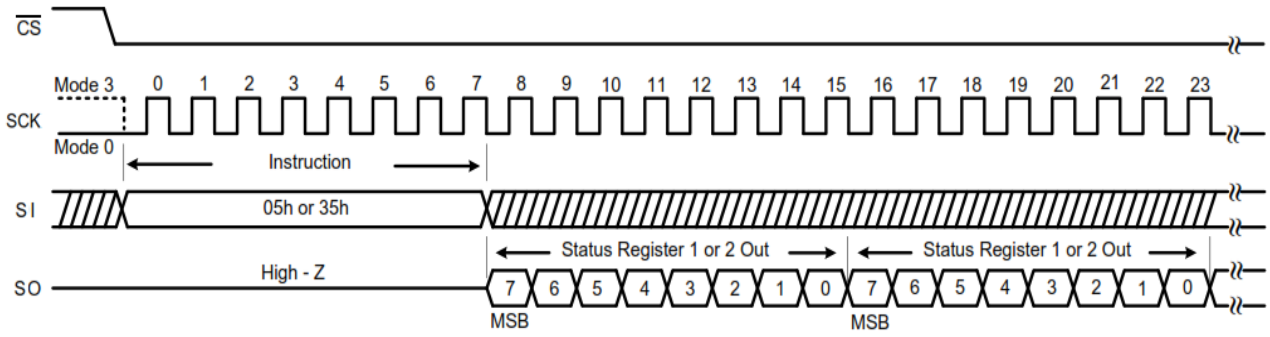


Figure 8-4. Read Status Register Instruction (SPI Mode)

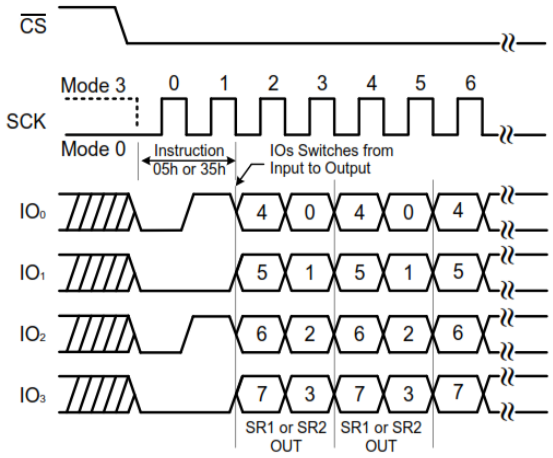


Figure 8-5. Read Status Register Instruction (QPI Mode)

8.6 Write Status Register (01h)

The Write Status Register instruction is to write the non-volatile Status Register-1 bit (SRP0) and Status Register-2 bits (QE and SRP1). All other Status Register bit locations are read-only and are not affected by the Write Status Register instruction.

A Write Enable (06h) instruction must have been previously issued prior to setting Write Status Register Instruction (Status Register bit WEL = 1). Once the write is enabled, the instruction is entered by driving $\overline{CS}$ low, sending the instruction code, and then writing the status register data byte as illustrated in Figure 8-6 and Figure 8-7.

The $\overline{CS}$ pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction can not be executed. If $\overline{CS}$ is driven high after the eighth clock, hardware clears the CMP, QE and SRP1 bits to 0. After $\overline{CS}$ is driven high, the self- timed Write Status Register cycle commences for a time duration of t_w (See AC Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is set during the Write Status Register cycle and cleared when the cycle is finished to indicate the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in Status Register is cleared to 0.

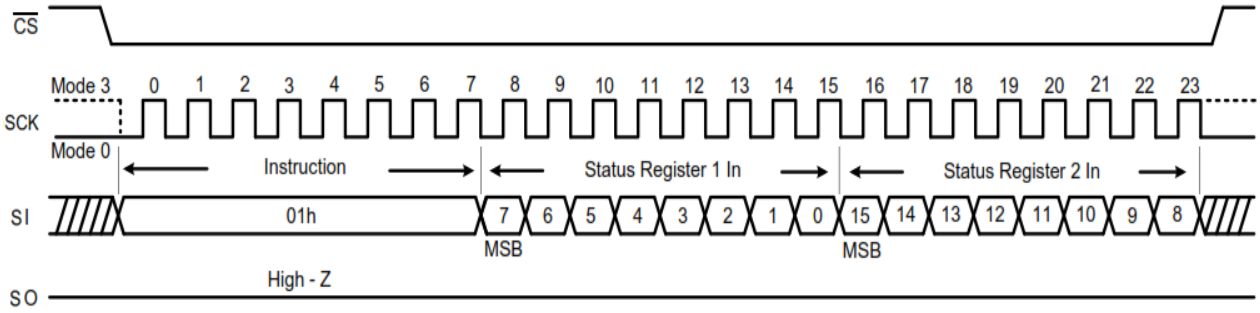


Figure 8-6. Write Status Register Instruction (SPI Mode)

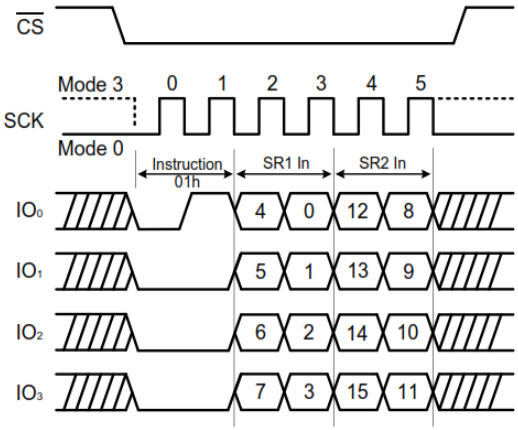


Figure 8-7. Write Status Register Instruction (QPI Mode

8.7 Write Status Register-2 (31h)

The Write Status Register-2 instruction is to write only non-volatile Status Register-2 bits (CMP, QE, and SRP1).

A Write Enable instruction must have previously been issued prior to setting Write Status Register Instruction (Status Register bit WEL = 1). Once the write enable occurs, the Write Status Register 2 instruction is entered by driving $\overline{CS}$ low, sending the instruction code (31h), and then writing the Status Register 2 data byte as illustrated in Figure 8-8 and Figure 8-9.

Using the Write Status Register-2 (31h) instruction, software can individually access each one-byte status registers via different instructions.

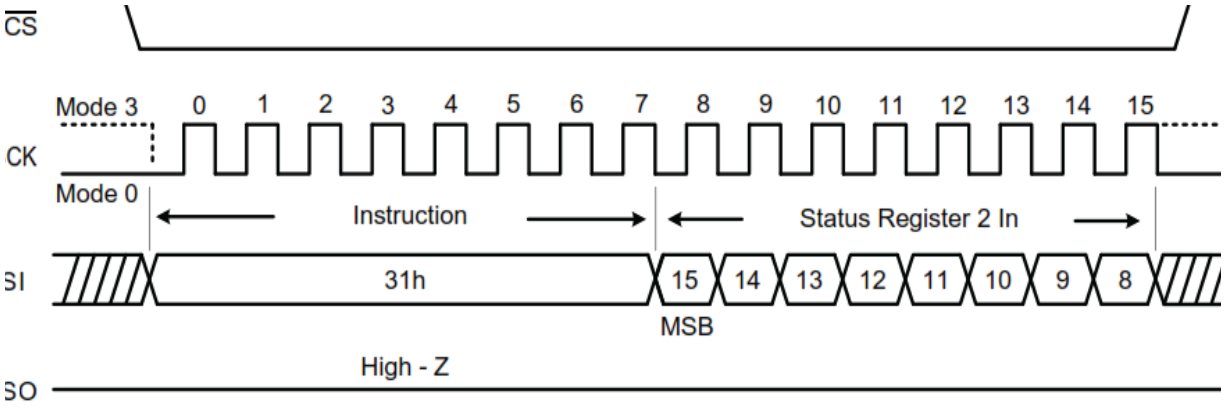


Figure 8-8. Write Status Register-2 Instruction (SPI Mode)

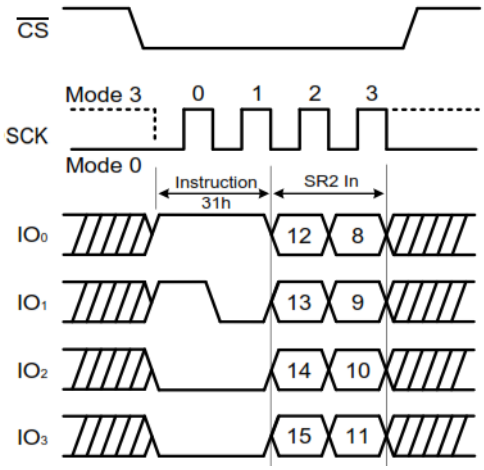


Figure 8-9. Write Status Register-2 Instruction (QPI Mode)

8.8 Read Data (03h)

The Read Data instruction is used to read data out from the memory. The instruction is initiated by driving the $\overline{CS}$ pin low and then sending the instruction code 03h, followed by a 24-bit address (A23- A0), onto the SI pin. After the address is received, the data byte of the addressed memory location is shifted out on the SO pin at the falling edge of SCK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues.

The instruction is completed by driving $\overline{CS}$ high. The Read Data instruction sequence is shown in Figure 8-10. If a Read Data instruction is issued while an Erase, Program or Write Status Register cycle is in process (BUSY = 1) the instruction is ignored and does not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f**R** (see AC Electrical Characteristics).

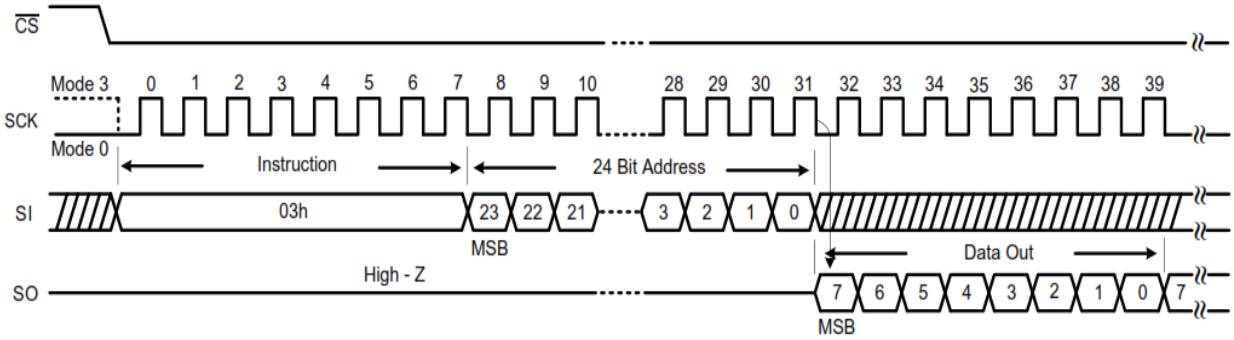


Figure 8-10. Read Data Instruction

8.9 Fast Read (0Bh)

The Fast Read instruction can operate at the highest possible frequency of FR. The OBh instruction is driven onto the SI pin, followed by the 24-bit address, and is latched on the rising edge of SCK. The address is then followed by 8 dummy clocks as shown in Figure 8-11. The dummy clocks allows the internal circuits time to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. Data of each bit shifts out on the falling edge of SCK.

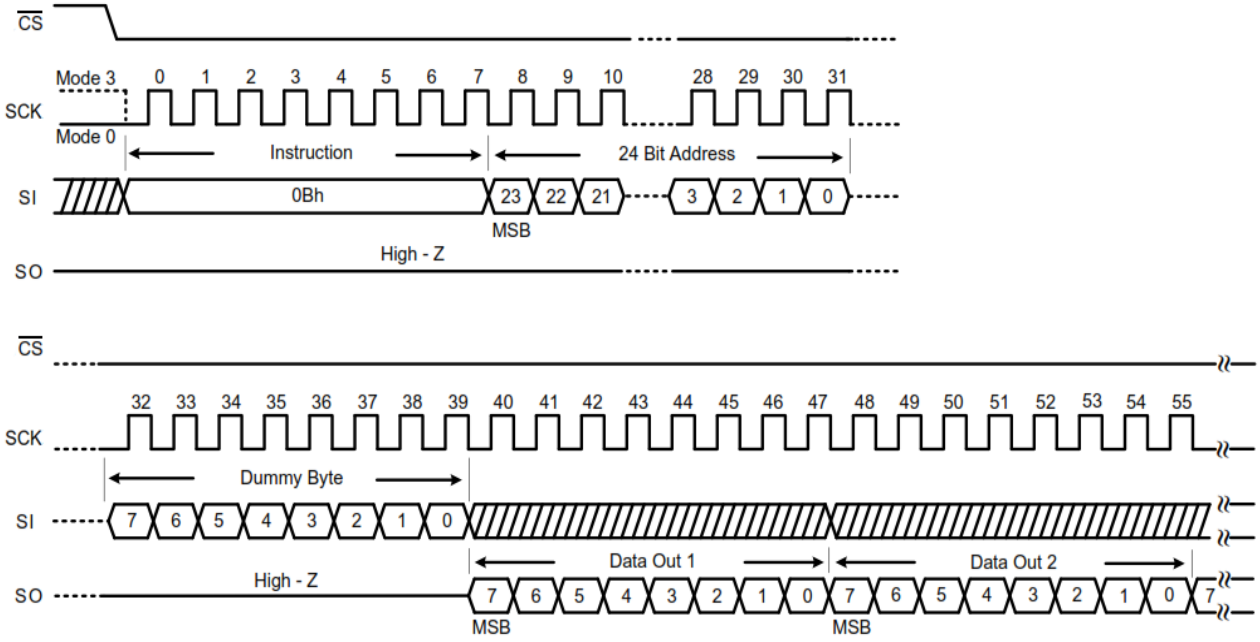


Figure 8-11. Fast Read Instruction (SPI Mode)

8.10 Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the Set Read Parameters (C0h) instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the state of the Read Parameter bits P[4] and P[5], the number of dummy clocks can be configured as either 4, or 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4. See Figure 8-12 and Figure 8-13.

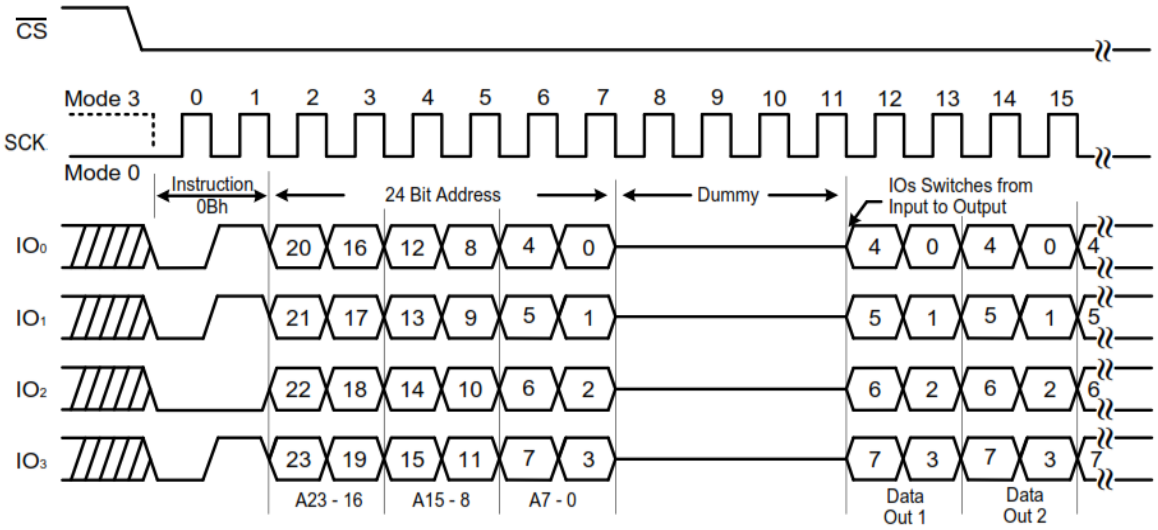


Figure 8-12. Fast Read instruction (QPI Mode, 80 MHz)

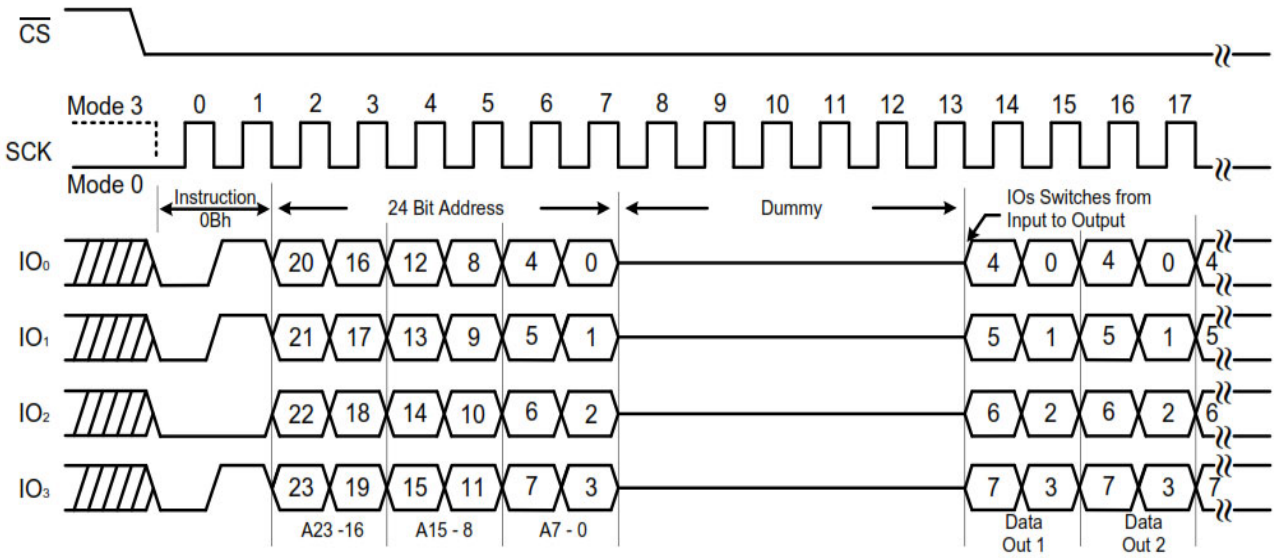


Figure 8-13. Fast Read instruction (QPI Mode, 104 MHz)

8.11 Fast Read Dual Output (3Bh)

By using two pins (IO_0 and IO_1, instead of just IO_0), the Fast Read Dual Output instruction allows data to be transferred from the AT25SL321 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to the RAM for execution.

The Fast Read Dual Output instruction can operate at the highest possible frequency of F**R** (see AC Electrical Characteristics). After the 24-bit address, eight “dummy” clocks are inserted to allow the internal circuits time set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, the IO**0** pin is going to be high-impedance prior to the falling edge of the first data out clock. This is shown in Figure 8-14.

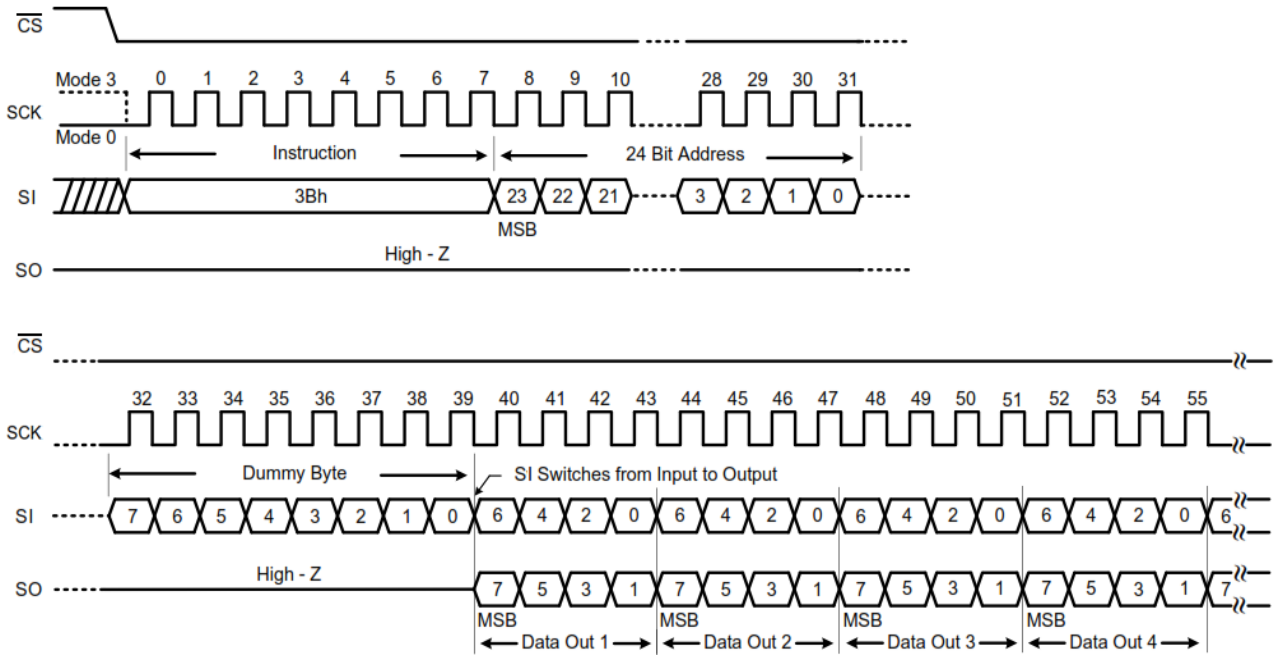


Figure 8-14. Fast Read Dual Output Instruction (SPI Mode)

8.12 Fast Read Quad Output (6Bh)

By using four pins (IO_0, IO_1, IO_2, and IO_3), The Fast Read Quad Output instruction allows data to be transferred from the AT25SL321 at four times the rate of standard SPI devices. A Quad Enable bit of Status Register-2 must be set before the device accepts the Fast Read Quad Output instruction (Status Register bit QE must equal 1).

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24- bit address as shown in Figure 8-15. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, the IO_0 pin is going to be high-impedance prior to the falling edge of the first data out clock.

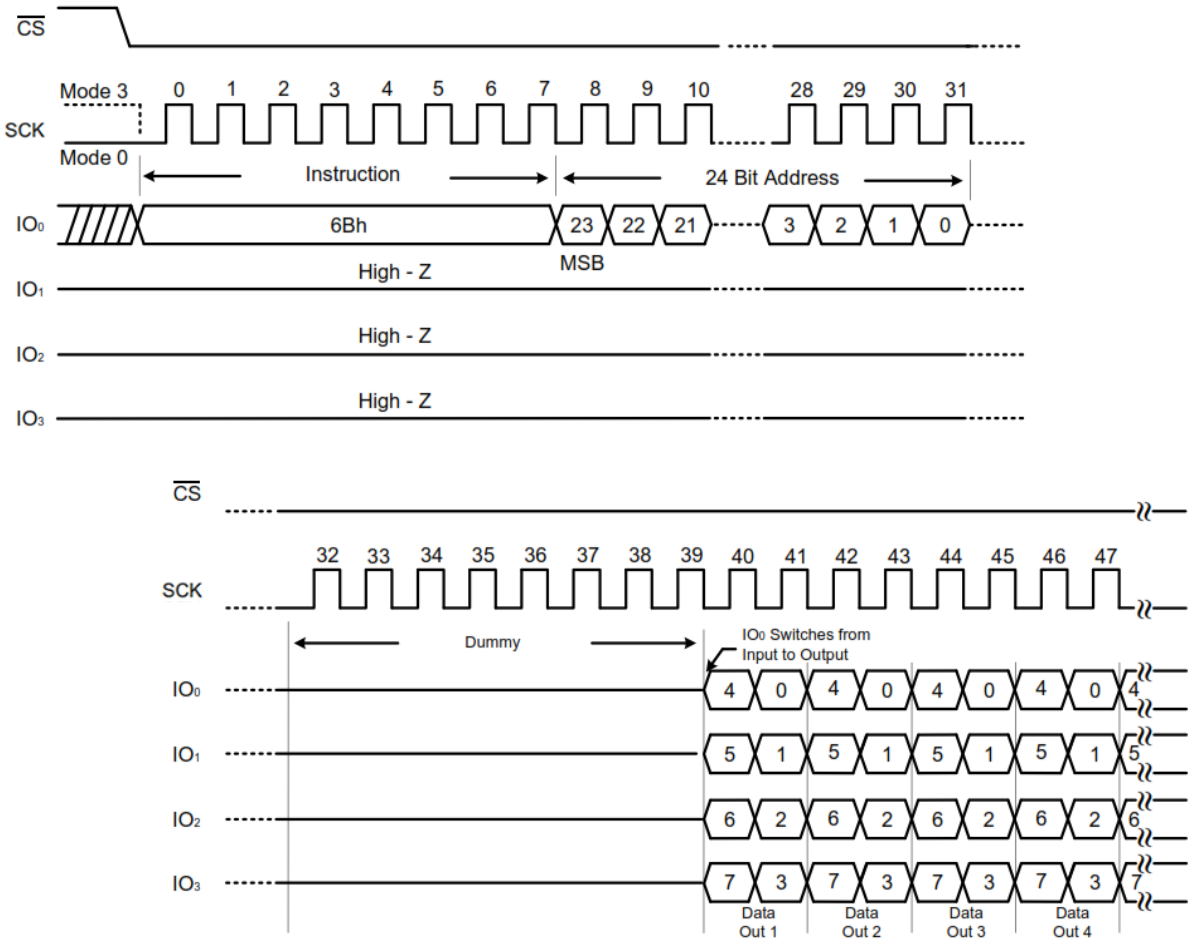


Figure 8-15. Fast Read Quad Output Instruction (SPI Mode)

8.13 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O instruction reduces cycle overhead through double access using two IO pins: IO_0 and IO_1.

Continuous Read Mode

This instruction can further reduce cycle overhead by setting the Mode bits (M7-0) after the input address bits (A23-0). The upper nibble of the Mode field (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode field (M3-0) are don’t care (“X”); however, the I/O pins are high-impedance before the falling edge of the first data out clock.

If the Mode bits (M7-0) equal “Ax” hex, then the next Fast Dual I/O instruction (after $\overline{CS}$ is raised and then lowered) does not require the instruction (BBh) code, as shown in Figure 8-16 and Figure 8-17. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low.

If Mode bits (M7-0) are any value other “Ax” hex, the next instruction (after $\overline{CS}$ is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0) before issuing normal instructions.

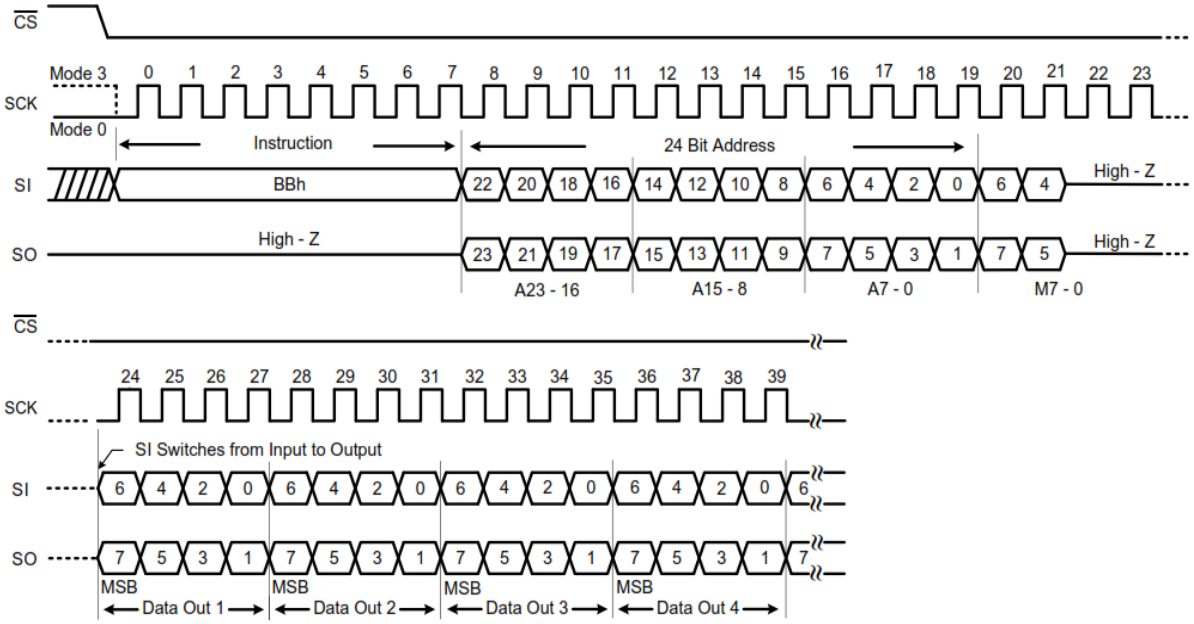


Figure 8-16. Fast Read Dual I/O Instruction (initial instruction or previous M7-0 ≠ Axh)

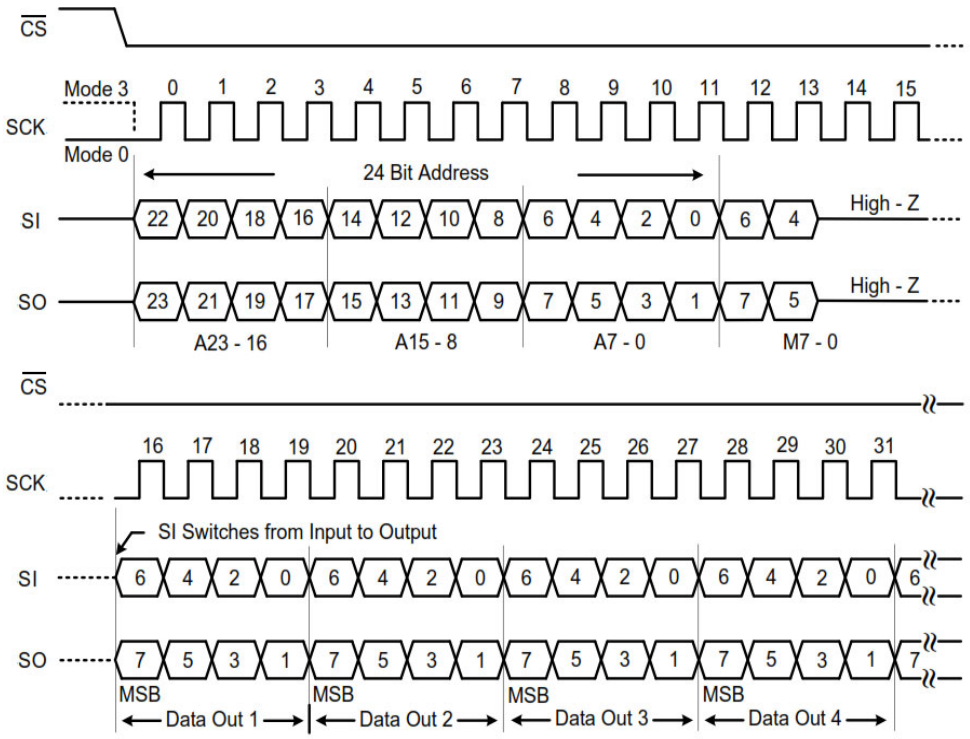


Figure 8-17. Fast Read Dual I/O Instruction (previous M7-0 = Axh)

8.14 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O instruction reduces cycle overhead through quad access using four IO pins: IO**0**, IO**1**, IO**2,** and IO**3.** The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Instruction.

Continuous Read Mode

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) with following the input Address bits (A23-0), as shown in Figure 8-18. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("X"). However, the IO pins are going to be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0) equal "Ax" hex, then the next Fast Read Quad I/O instruction (after $\overline{CS}$ is raised and then lowered) does not require the EBh instruction code, as shown in Figure 8-19. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next instruction (after $\overline{CS}$ is raised and then lowered) requires the first byte instruction code, thus retuning normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0) before issuing normal instructions.

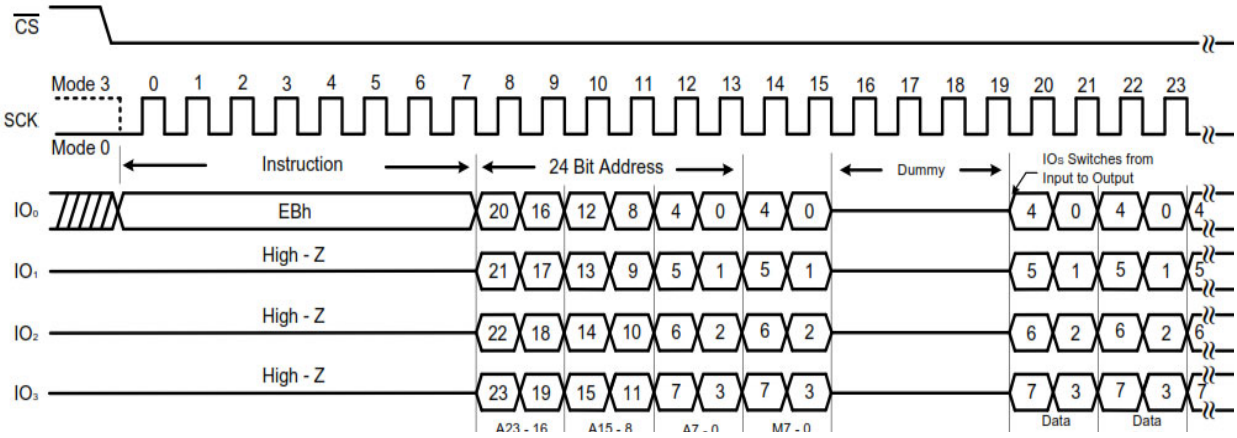


Figure 8-18. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ Axh, SPI mode)

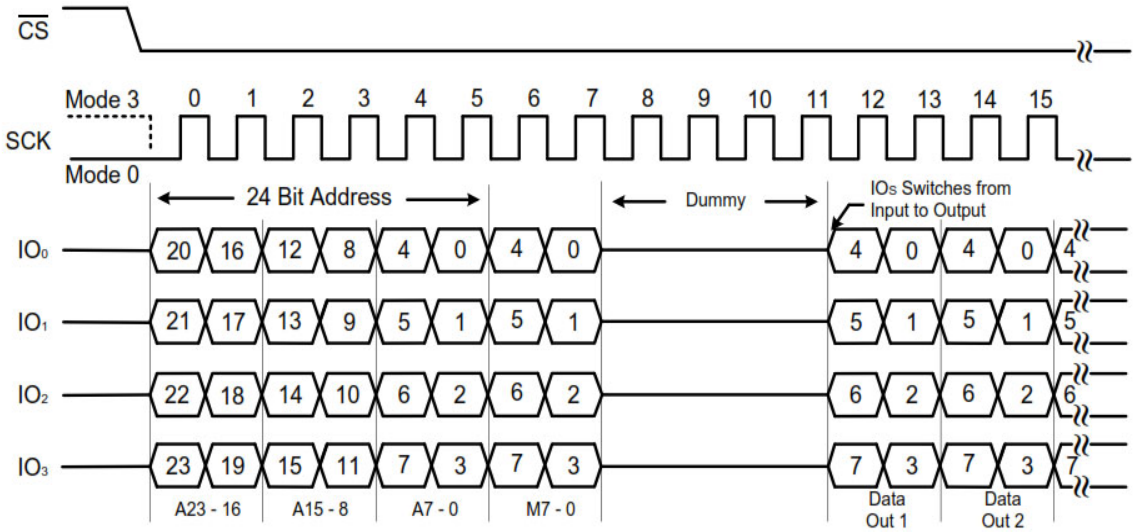


Figure 8-19. Fast Read Quad I/O Instruction (previous M7-0 = Axh, SPI mode)

Wrap Around in SPI mode

The Fast Read Quad I/O instruction can also be used to access specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior Fast Read Quad I/O (EBh) instruction. The Set Burst with Wrap (77h) instruction can either enable or disable the Wrap Around feature for the following Fast Read Quad I/O instruction.

When Wrap Around is enabled, the data being accessed can be limited to an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions. (See Section 8.32 Set Burst with Wrap).

Fast Read Quad I/O in QPI mode

When QPI mode in enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) instruction to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[4] and P[5] setting, the number of dummy clocks can be configured as either 4 or 6 or 8. The default number of dummy clocks upon power up or after a Reset (99h) instruction is 4.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O instruction. In QPI mode, the Continuous Read Mode bits M7-0 are also considered as dummy clocks. In the default setting, the data output needs to follow the Continuous Read Mode bits immediately.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a Burst Read with Wrap (0Ch) instruction must be used. For more information, see Section 8.33, Burst Read with Wrap.

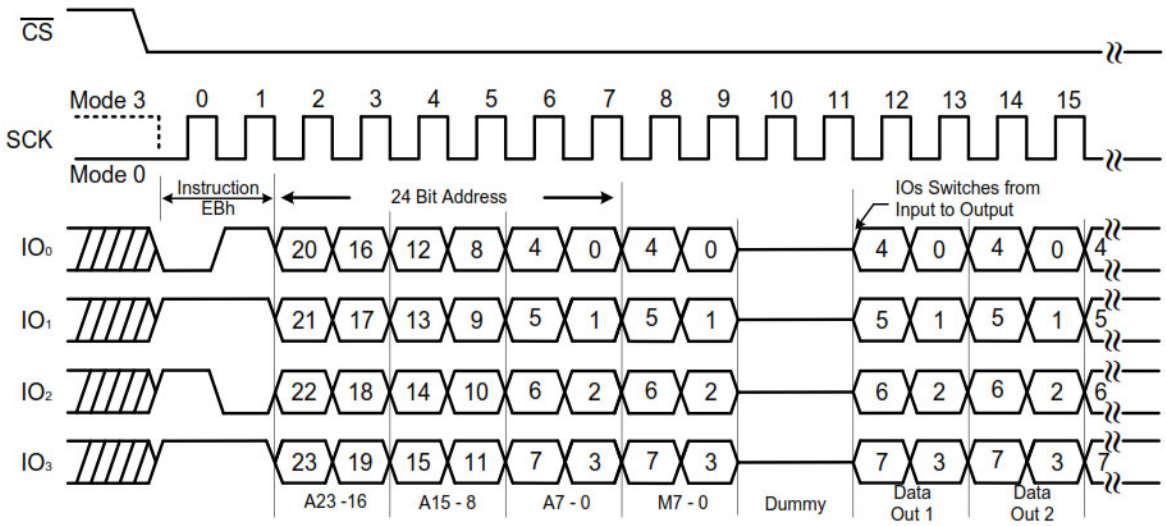


Figure 8-20. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ Axh, QPI mode, 80 MHz)

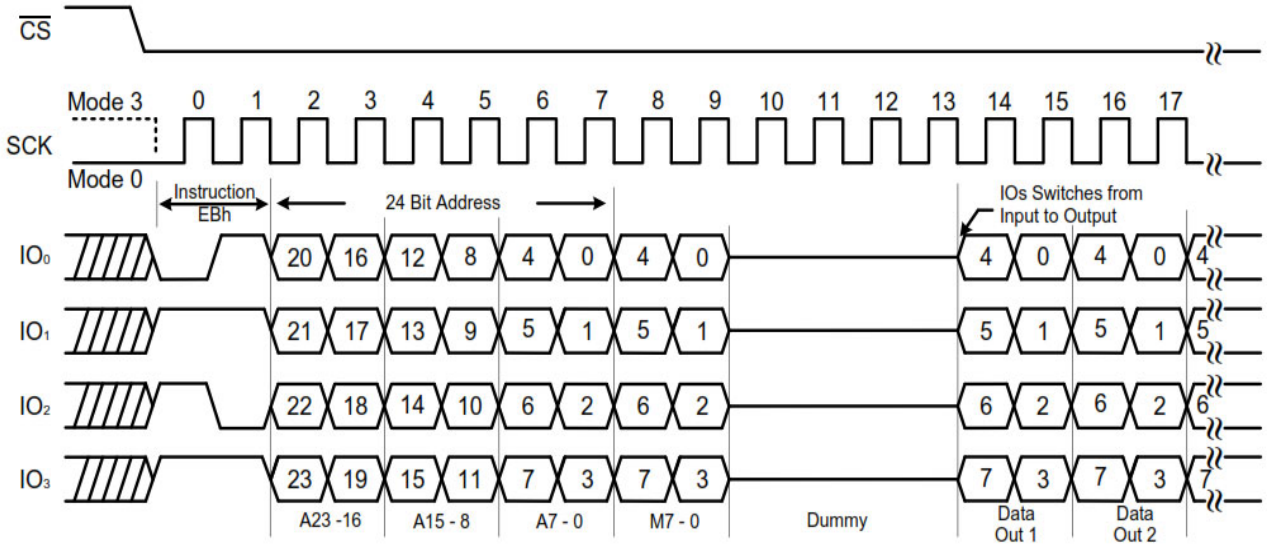


Figure 8-21. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ Axh, QPI mode, 104 MHz)

8.15 Page Program (02h)

This instruction programs the memory to 0. A Write Enable instruction must be issued before the device accepts this instruction (Status Register bit WEL = 1). After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL). The instruction is entered by driving the $\overline{CS}$ pin low, then sending the instruction code 02h with a 24-bits address (A23-A0) and at least one data byte, into the SI pin. The $\overline{CS}$ pin must be driven low for the entire time of the instruction while data is being sent to the device. (See Figure 8-22 and Figure 8-23).

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) is set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing must wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device, the addressing must wrap to the beginning of the page and overwrite previously sent data.

The $\overline{CS}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, this instruction cannot be executed. After $\overline{CS}$ is driven high, the self-timed Page Program instruction commences for a time duration of t_{PP} (see Section 9.8, AC Electrical Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction can still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

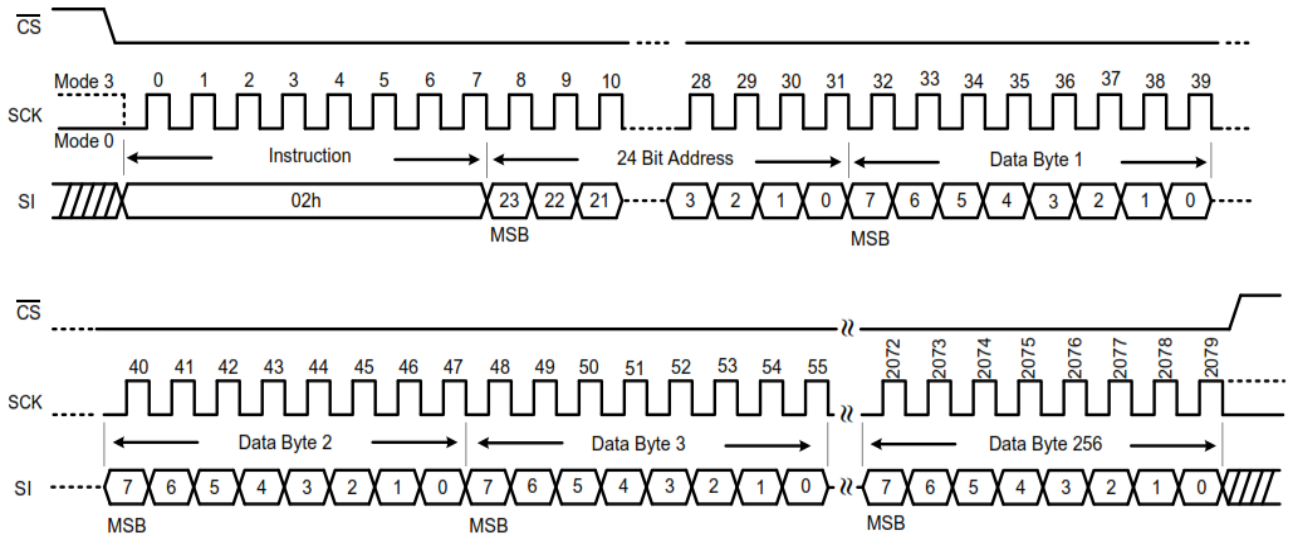


Figure 8-22. Page Program Instruction (SPI Mode)

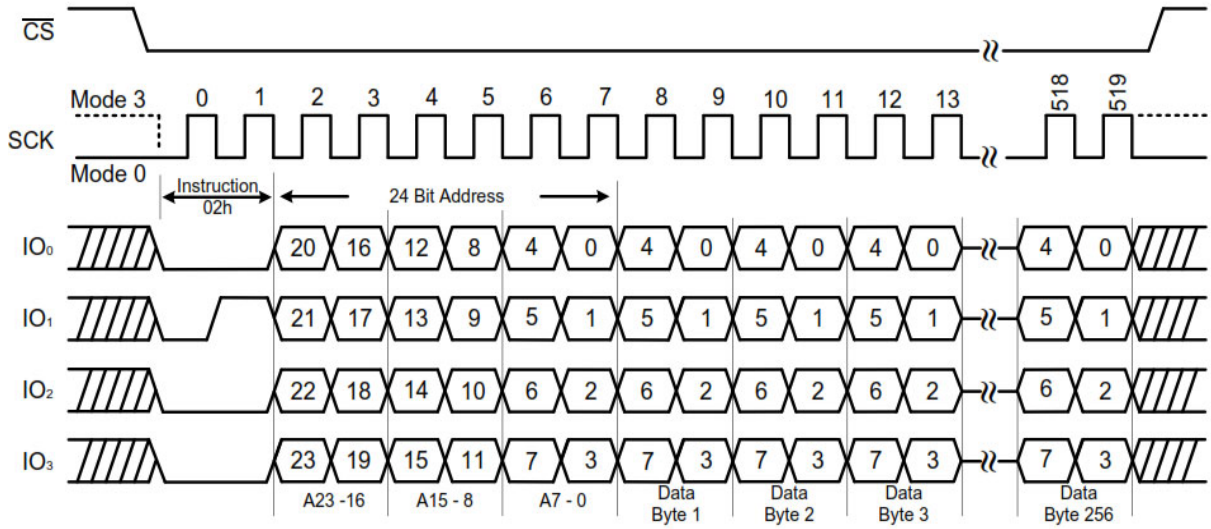


Figure 8-23. Page Program Instruction (QPI Mode)

8.16 Quad Page Program (33h)

The Quad Page Program instruction is to program the memory as being ‘0’ at previously erased memory areas. The Quad Page Program takes four pins: IO**0**, IO**1**, IO**2** and IO**3** as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 5 MHz. System using faster clock speed does not get more benefit for the Quad Page Program as the required internal page program time is far more than the time data clock-in.

To use Quad Page Program, the Quad Enable bit must be set, A Write Enable instruction must be executed before the device accepts the Quad Page Program instruction (Status Register-1, WEL = 1). The instruction is initiated by driving the $\overline{CS}$ pin low then sending the instruction code 33h with following a 24-bit address (A23-A0) and at least one data, into the IO pins. The $\overline{CS}$ pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are perfectly same as standard Page Program. (See Figure 8-24 and Figure 8-25).

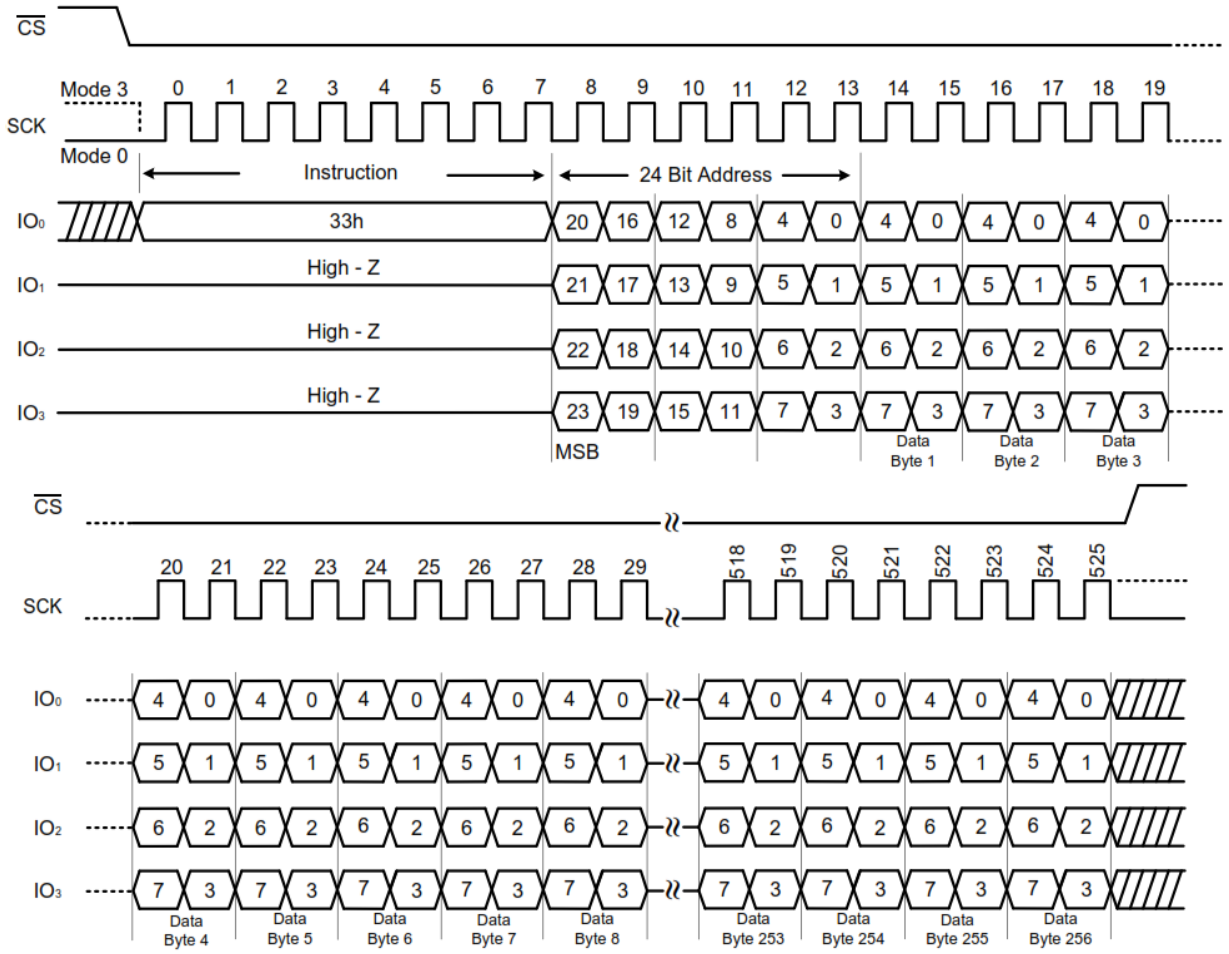


Figure 8-24. Quad Page Program Instruction (SPI mode)

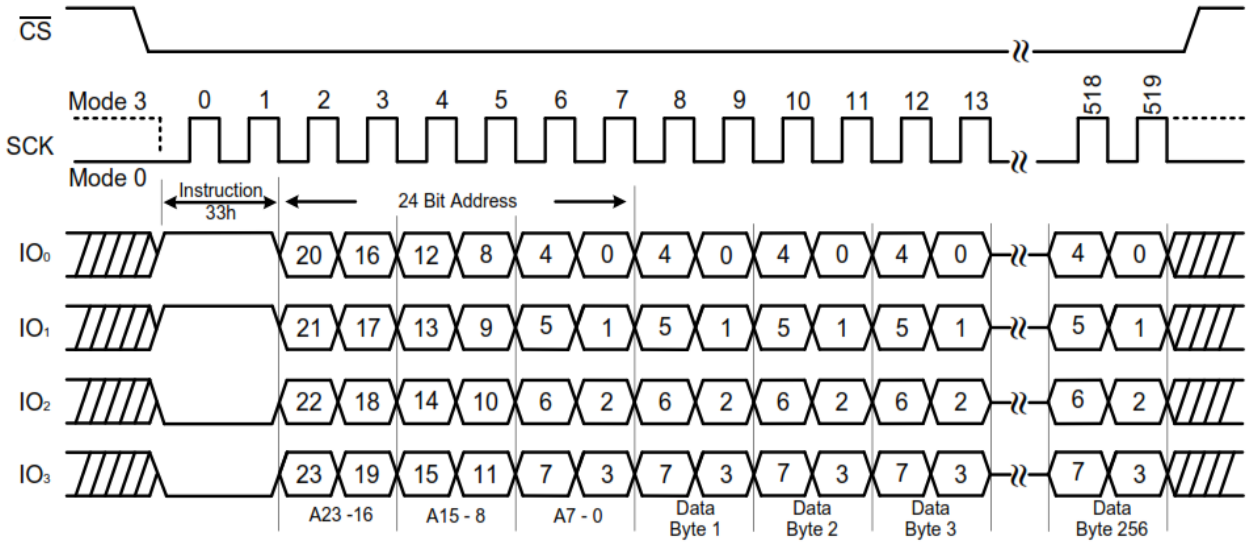


Figure 8-25. Quad Page Program Instruction (QPI mode)

8.17 Block Erase (20h)

The Block Erase instruction is to erase the data of the selected sector as being '1'. The instruction is used for 4K-byte Block. Prior to the Block Erase Instruction, the Write Enable instruction must be issued. The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 20h followed a 24-bit Block address (A23-A0). See Figure 8-26 and Figure 8-27. The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction can not be executed. After $\overline{CS}$ goes high, the self-timed Block Erase instruction commences for a time duration of t_{SE}. See Section 9.8, AC Electrical Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction can still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

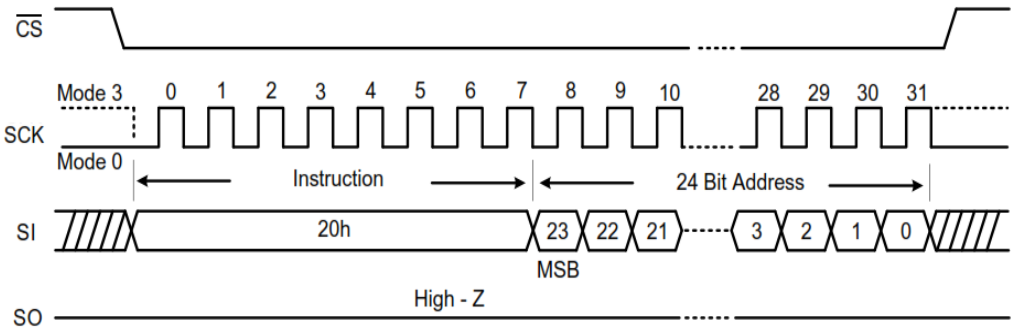


Figure 8-26. Block Erase Instruction (SPI Mode)

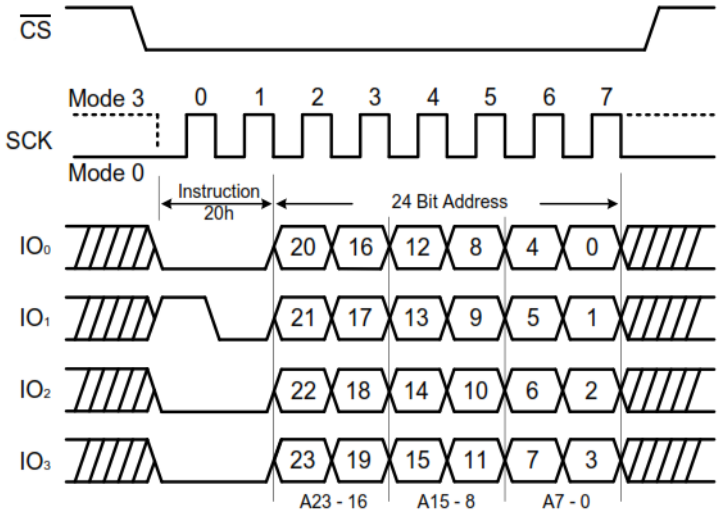


Figure 8-27. Block Erase Instruction (QPI Mode)

8.18 32 kB Block Erase (52h)

The Block Erase instruction is to erase the data of the selected block as being '1'. The instruction is used for 32K-byte Block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 52h followed a 24-bit block address (A23-A0). See Figure 8-28 and Figure 8-29.

The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction can not be executed. After $\overline{CS}$ is driven high, the self-timed Block Erase instruction commences for a time duration of t_{BE1}. See Section 9.8, AC Electrical Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction can still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

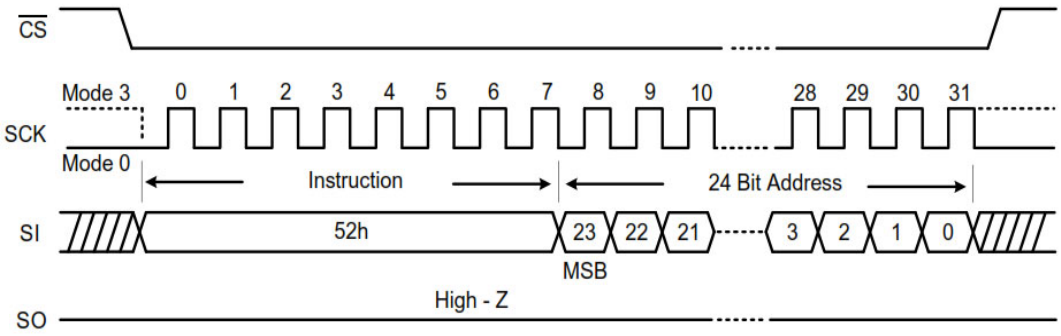


Figure 8-28. 32 kB Block Erase Instruction (SPI Mode)

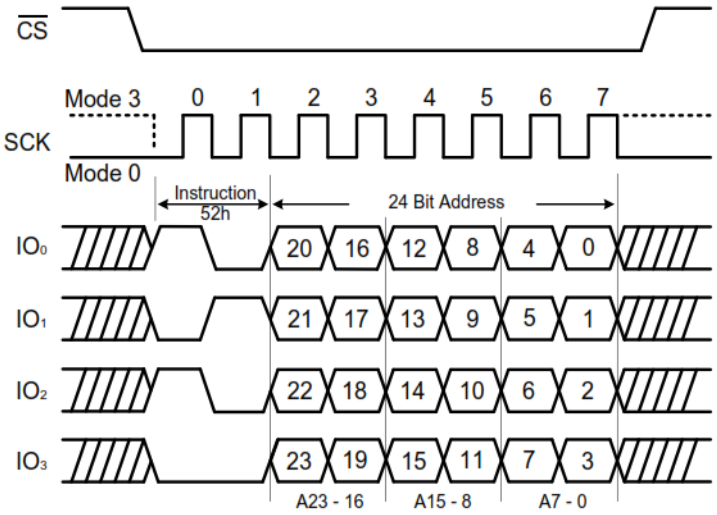


Figure 8-29. 32 kB Block Erase Instruction (QPI Mode)

8.19 64 kB Block Erase (D8h)

The Block Erase instruction is to erase the data of the selected block as being '1'. The instruction is used for 64K-byte Block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code D8h followed a 24-bit block address (A23-A0). (See Figure 8-30 and Figure 8-31). The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction can not be executed. After $\overline{CS}$ is driven high, the self-timed Block Erase instruction commences for a time duration of t_{BE2}. See Section 9.8, AC Electrical Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction can still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

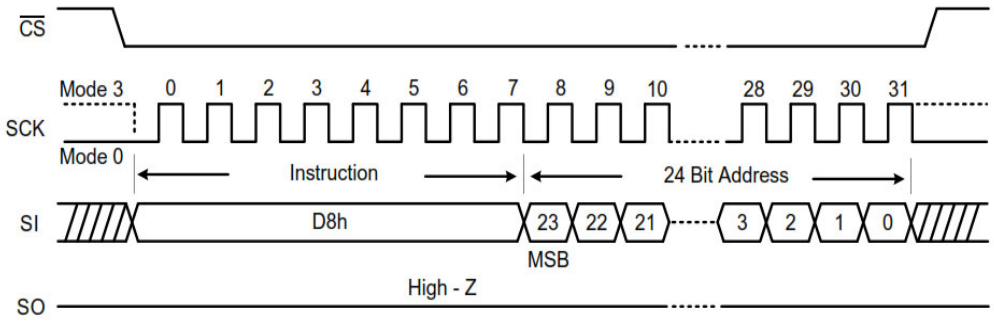


Figure 8-30. 64 kB Block Erase Instruction (SPI Mode)

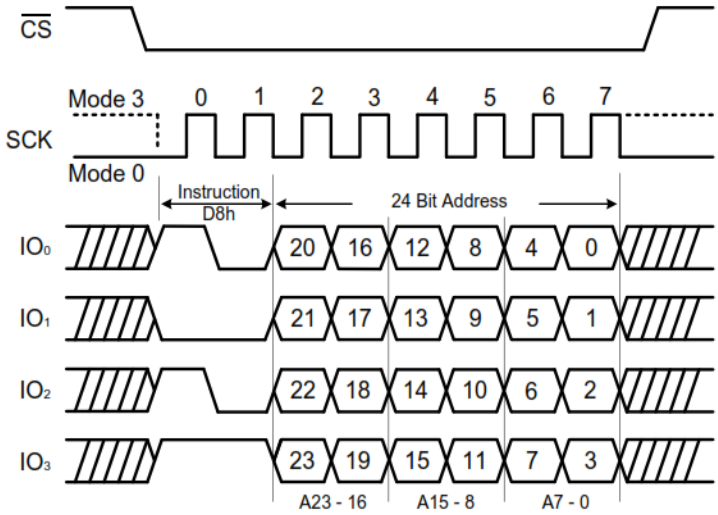


Figure 8-31. 64 kB Block Erase Instruction (QPI Mode)

8.20 Chip Erase (C7h / 60h)

The Chip Erase instruction clears all bits in the device to be FFh (all 1s). Prior to the Chip Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code C7h or 60h. (See Figure 8-32). The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Chip Erase instruction can not be executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase instruction commences for a duration of t_{CE}. See Section 9.8, AC Electrical Characteristics.

While the Chip Erase cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

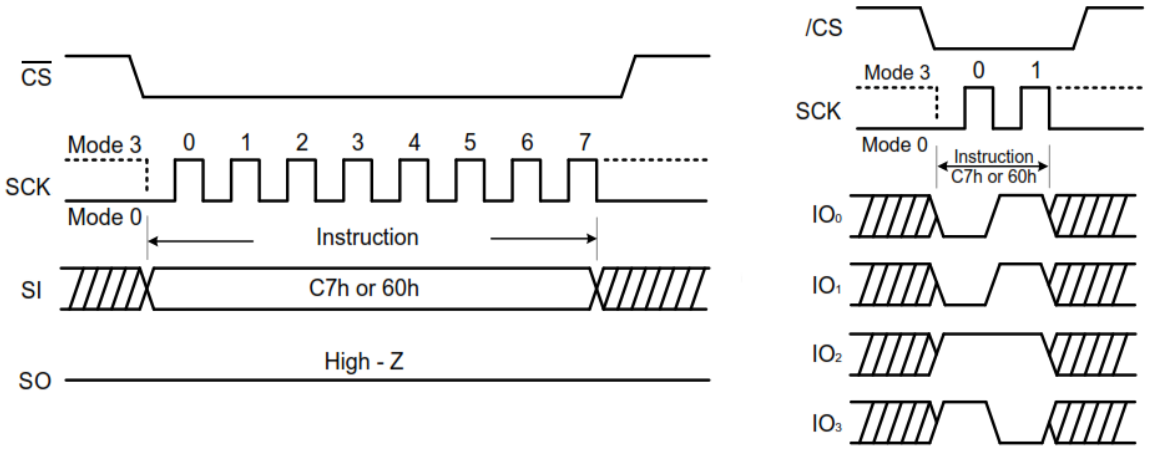


Figure 8-32. Chip Erase Instruction for SPI Mode (left) and QPI Mode (right)

8.21 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction allows the system to interrupt a Block Erase operation or a Page Program, Quad Data Input Page Program, Quad Page Program operation.

Erase Suspend is valid only during the Block erase operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) instruction and Erase instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Erase Suspend. During the Chip Erase operation, the Erase Suspend instruction is ignored.

Program Suspend is valid only during the Page Program, Quad Data Input Page Program or Quad Page Program operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) instruction, Program instructions (02h and 33h) and Erase Instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Program Suspend.

The Erase/Program Suspend instruction “75h” is accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction is ignored by the device. A maximum of time of t_{SUS} (see Section 9.8) is required to suspend the erase or program operation. After Erase/Program Suspend, the SUS bit in the Status Register is set from 0 to 1 immediately and the BUSY bit in the Status Register is cleared from 1 to 0 within t_{SUS}. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume instruction 7Ah.

Unexpected power off during the Erase/Program suspend state resets the device and releases the suspend state. SUS bit in the Status Register is also reset to 0. The data within the page or block that was being suspended might become corrupted. It is recommended for the user to implement system design techniques against the

accidental power interruption and preserve data integrity during erase/program suspend state. See Figure 8-33 and Figure 8-34.

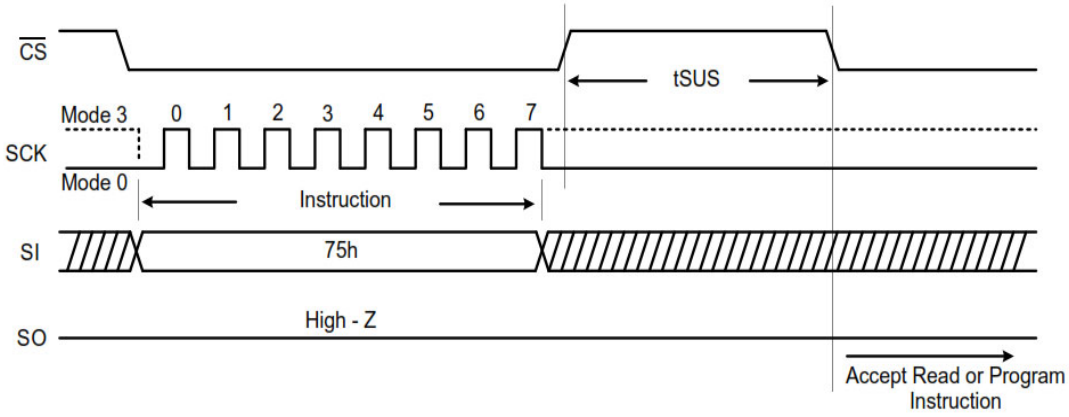


Figure 8-33. Erase Suspend Instruction (SPI Mode)

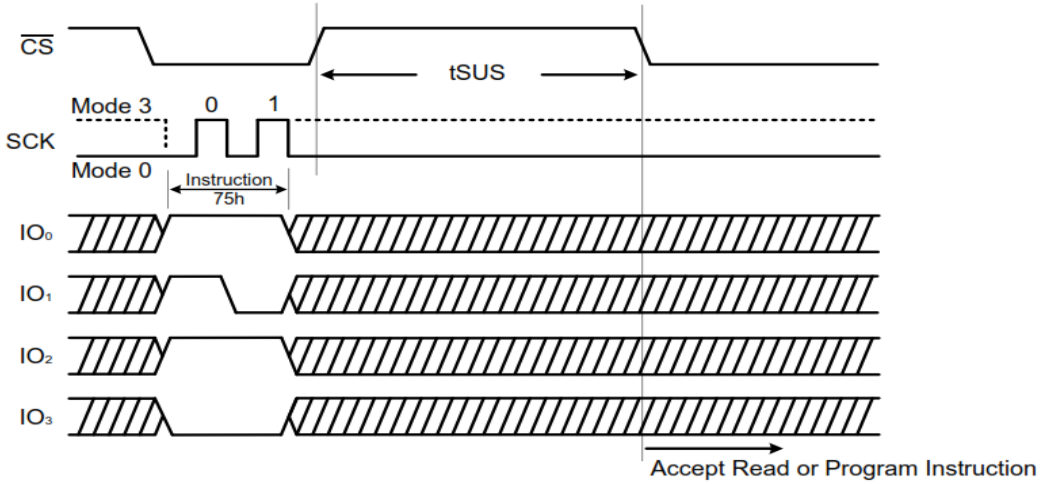


Figure 8-34. Erase Suspend Instruction (QPI Mode)

8.22 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction 7Ah is to restart the Block Erase operation or the Page Program operation upon an Erase/Program Suspend. The Resume instruction 7Ah is accepted by the device only if the SUS bit in the Status Register equals 1 and the BUSY bit equals 0. After issue, the SUS bit is cleared from 1 to 0 immediately, the BUSY bit is set from 0 to 1 within 200 ns and the Block completes the erase operation or the page completes the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction 7Ah is ignored by the device.

Resume instruction cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of t_{SUS} following a previous Resume instruction. See Figure 8-35 and Figure 8-36.

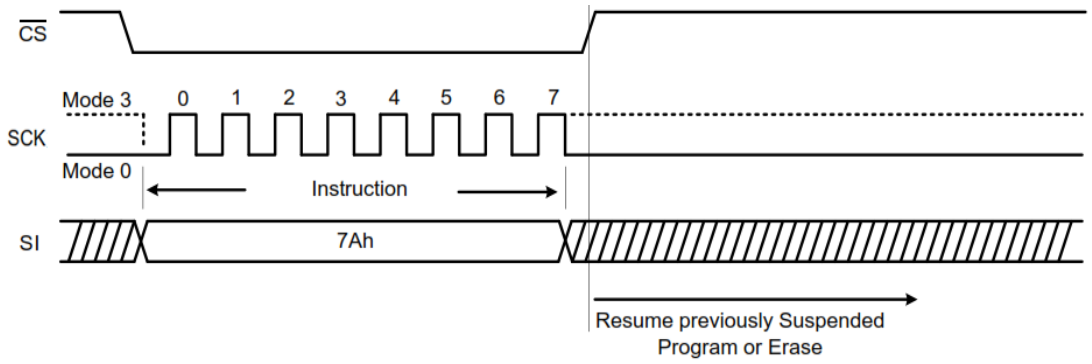


Figure 8-35. Erase / Program Resume Instruction (SPI Mode)

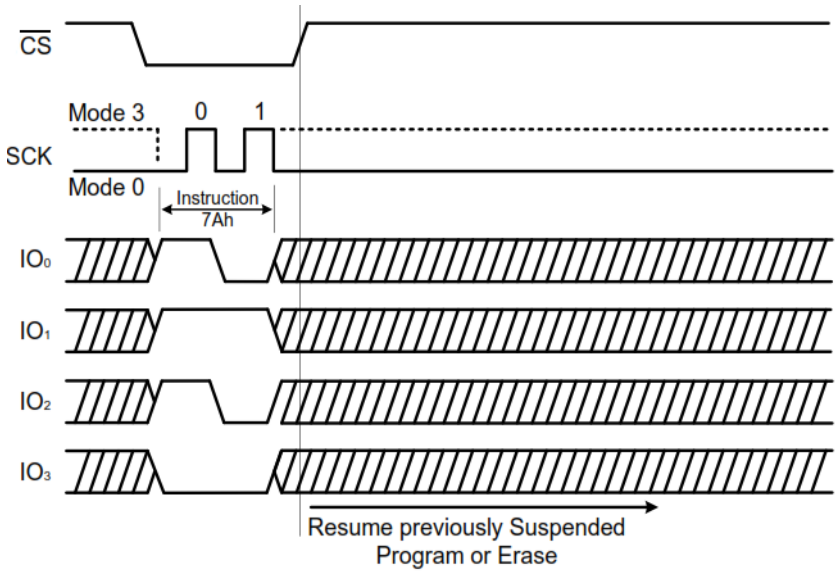


Figure 8-36. Erase / Program Resume Instruction (QPI Mode)

8.23 Deep Power Down (B9h)

Executing the Deep Power Down (DPD) instruction is the best way to put the device in the lowest power consumption. The Deep Power Down instruction reduces the standby current (from ICC1 to ICC2, as specified in Section 9.8, AC Electrical Characteristics). The instruction is entered by driving the $\overline{CS}$ pin low with following the instruction code B9h. See Figure 8-37 and Figure 8-38.

The $\overline{CS}$ pin must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the Deep Power Down instruction is not executed. After $\overline{CS}$ goes high, it requires a delay of t_{DP} before Deep Power Down mode is entered. While in DPD mode, only the Release Deep Power Down / Device ID instruction, which restores the device to normal operation, is recognized. All other instructions are ignored, including the Read Status Register instruction, which is always available during normal operation. Deep Power Down Mode automatically stops at power-down, and the device always power-ups in the standby mode.

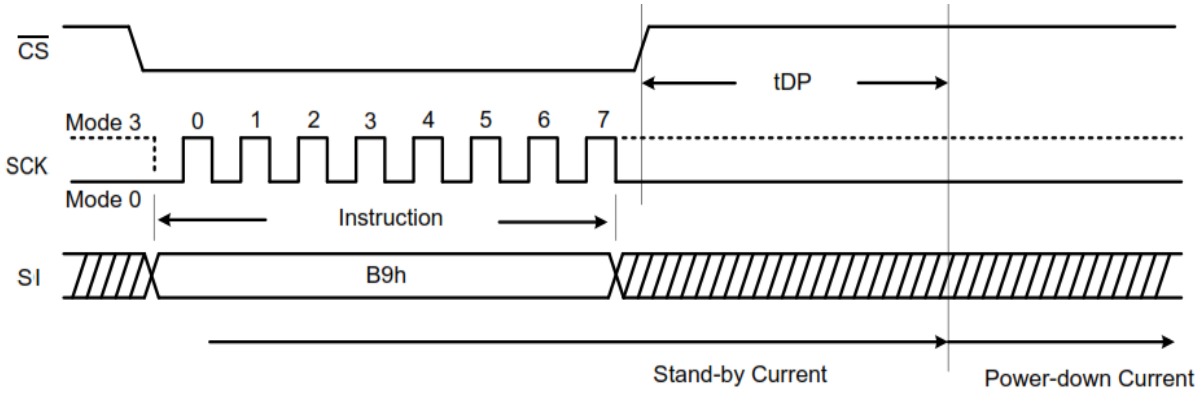


Figure 8-37. Deep Power Down Instruction (SPI Mode)

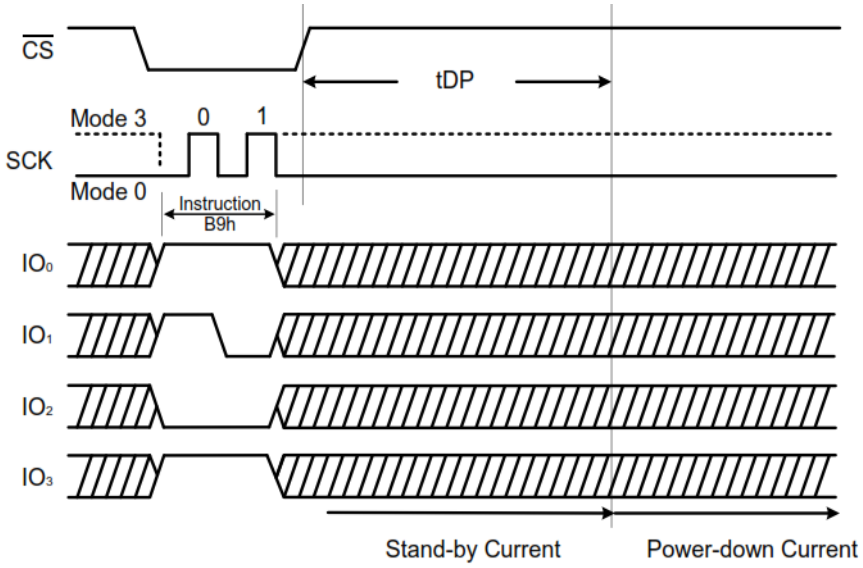


Figure 8-38. Deep Power Down Instruction (QPI Mode)

8.24 Release Deep Power Down / Device ID (ABh)

The Release Deep Power Down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Deep Power Down state or obtain the device identification (ID).

The instruction is issued by driving the $\overline{CS}$ pin low, sending the instruction code ABh and driving $\overline{CS}$ high as shown in figure Figure 8-39 and Figure 8-40. The Release from Deep Power Down operation requires the time duration of $t_{RES1.}$ The $\overline{CS}$ pin must keep high during the t_{RES1} time duration.

The Device ID can be read during SPI mode only. In other words, Device ID feature is not available in QPI mode for Release Deep Power Down/Device ID instruction. To obtain the Device ID in SPI mode, instruction is initiated by driving the $\overline{CS}$ pin low and sending the instruction code ABh with following 3-dummy bytes. The Device ID bits are then shifted on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 8-41. After $\overline{CS}$ is driven high it must keep high for a time duration of t_{RES2}. See Section 9.8, AC Electrical Characteristics. The Device ID can be read continuously. The instruction is completed by driving $\overline{CS}$ high.

If the Release from Deep Power Down /Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and does not have any effects on the current cycle.

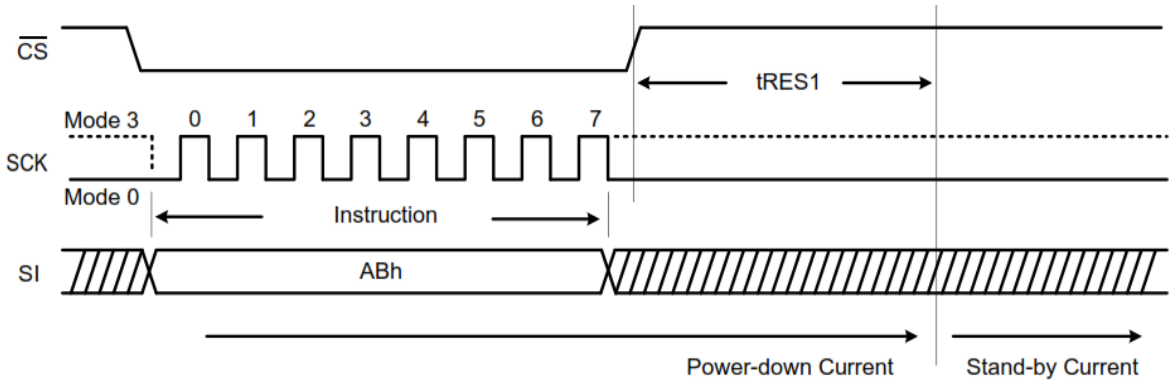


Figure 8-39. Release Power Down Instruction (SPI Mode)

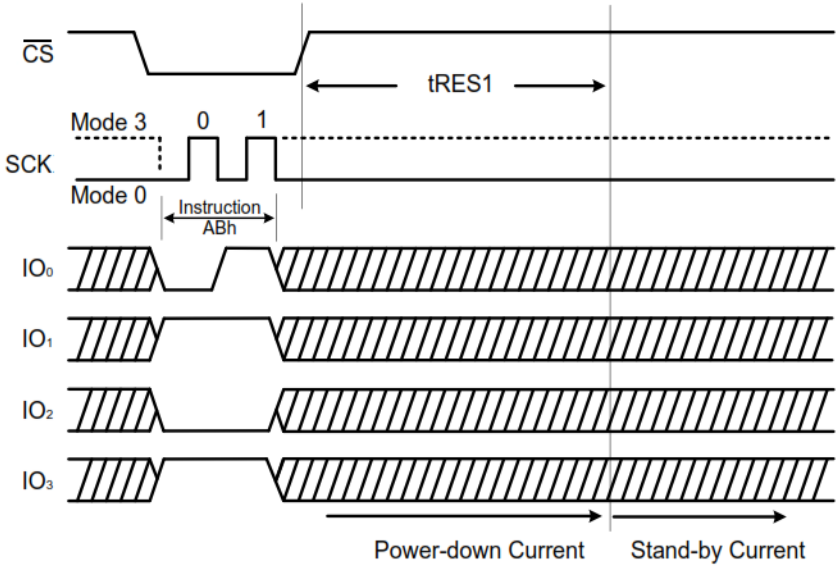


Figure 8-40. Release Power Down Instruction (QPI Mode)

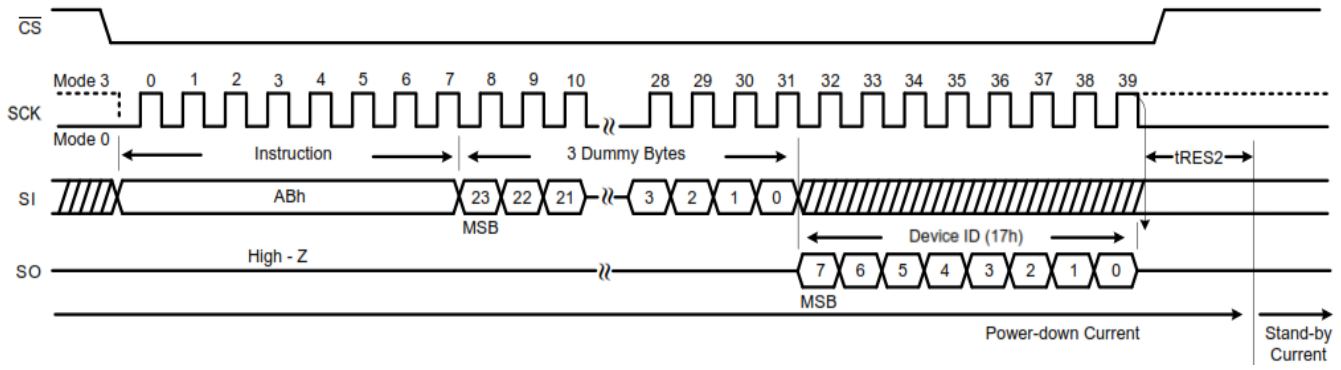


Figure 8-41. Release Power Down / Device ID Instruction (SPI Mode)

8.25 Read Manufacturer / Device ID (90h)

The Read Manufacturer/ Device ID instruction provides both the JEDEC assigned manufacturer ID and the specific device ID. This instruction can be issued in both SPI mode and QPI mode. In SPI mode, the 90h instruction is called a 1-1-1 transfer, where the instruction, address, and data are all driven on a single pin (SI for instruction and address, and SO for data). In QPI mode, the 90h instruction is called a 4-4-4 transfer, where the instruction, address, and data are driven on the IO_0 - IO_3 pins.

Note that in QPI mode, the following events must occur in the order shown.

1. Set the QE bit in Status Register-2.
2. Execute the QPI Enable (38h) instruction.
3. Execute the 90h instruction.

In SPI mode, the operation is initiated by driving the $\overline{CS}$ pin low and then driving the instruction code 90h onto the SI pin, followed by a 24-bit address (A23-A0) of 000000h. The 90h instruction requires 8 clocks to transfer, and the 24-bit address requires 24 clocks to transfer. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the SO pin on the falling edge of SCK with most significant bit (MSB) first. A minimum or 16 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CS}$ high.

In QPI mode, the SI, SO, $\overline{WP}$, and $\overline{HOLD}$ pins are configured as bidirectional pins IO_0, IO_1, IO_2, and IO_3 respectively. The 90h operation the operation is initiated by driving the $\overline{CS}$ pin low and then driving the instruction code 90h onto the IO_0 - IO_3 pins, followed by a 24-bit address (A23-A0) of 000000h. The 90h instruction requires 2 clocks to transfer, and the 24-bit address requires 6 clocks to transfer. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the bidirectional IO_0 - IO_3 pins on the falling edge of SCK, with most significant bit (MSB) first. A minimum or 4 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CS}$ high.

Figure 8-42 shows the 90h command as executed in SPI mode. In this mode the instruction and address are driven on the SI pin. Figure 8-43 shows the 90h command as executed in QPI mode. In this mode the instruction and address are driven on all four I/O pins.

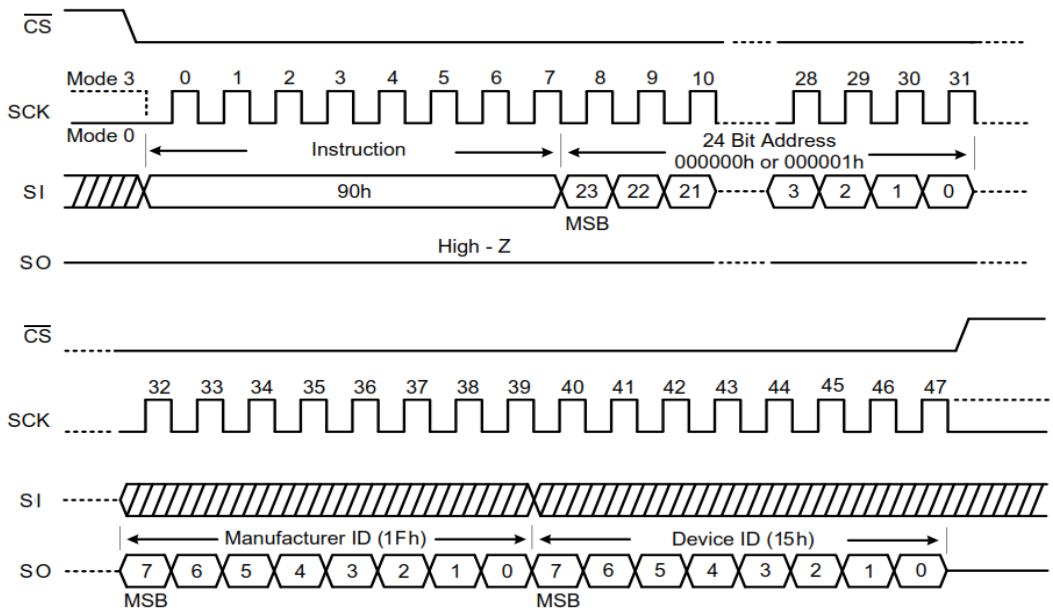


Figure 8-42. Read Manufacturer/ Device ID Instruction (SPI Mode)

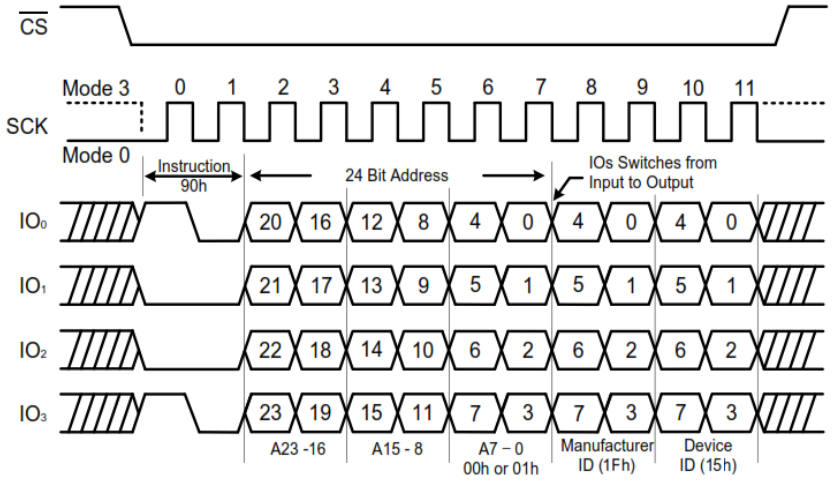


Figure 8-43. Read Manufacturer/ Device ID Instruction (QPI Mode)

8.26 Read Manufacturer / Device ID (92h) — Dual I/O

The Read Manufacturer/ Device ID Dual I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID. This command allows the address and manufacturer/device ID information to be driven on both the SI and SO pins. During the address transfer, the SI and SO pins are inputs, allowing the 24-bit address to be transferred in only 12 clocks. Device hardware then switches the SI and SO pins to outputs and drives the manufacturer/device ID information on these two pins, again requiring only half the number of clocks as required by the 90h instruction. The 92h instruction is called a 1-2-2 transfer, where the instruction is transferred on a single pin (SI), and the address and data are driven on two pins (SI and SO).

The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 92h followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 8-44. A minimum of eight clock cycles are required to transfer the information.

If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CS}$ high.

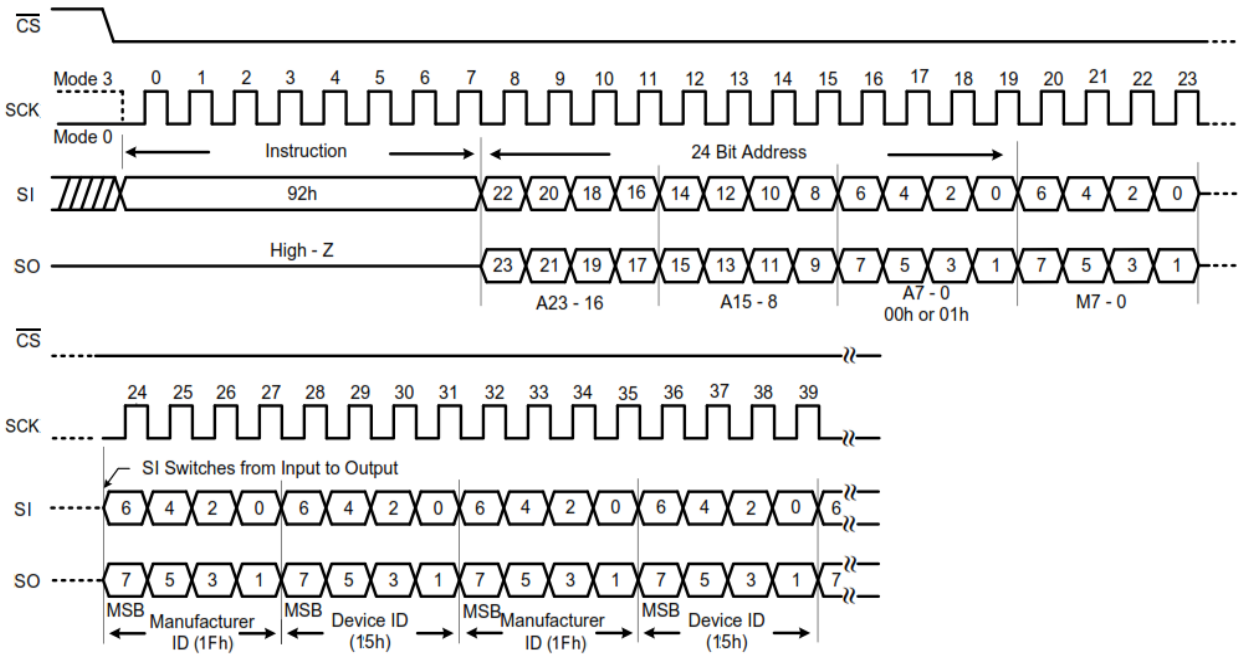


Figure 8-44. Read Dual Manufacturer/ Device ID Dual I/O Instruction (SPI Mode)

8.27 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/Device ID Quad I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID. This command allows both address and manufacturer/device ID information to be driven on the SI (IO_0), SO (IO_1), $\overline{WP}$ (IO_2), and $\overline{HOLD}$ (IO_3) pins. During the address transfer, the IO_0, IO_1, IO_2, and IO_3 pins are inputs, allowing the 24-bit address to be transferred in only 6 clocks. Device hardware then switches these pins to outputs and drives the manufacturer/device ID information on these pins, transferring the information in one-fourth the number of clocks required by the 90h instruction. The 94h instruction is called a 1-4-4 transfer, where the instruction in transferred on a single pin (IO_0), and the address and data are driven on four pins (IO_0 - IO_3).

The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 94h followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 8-45. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CS}$ high.

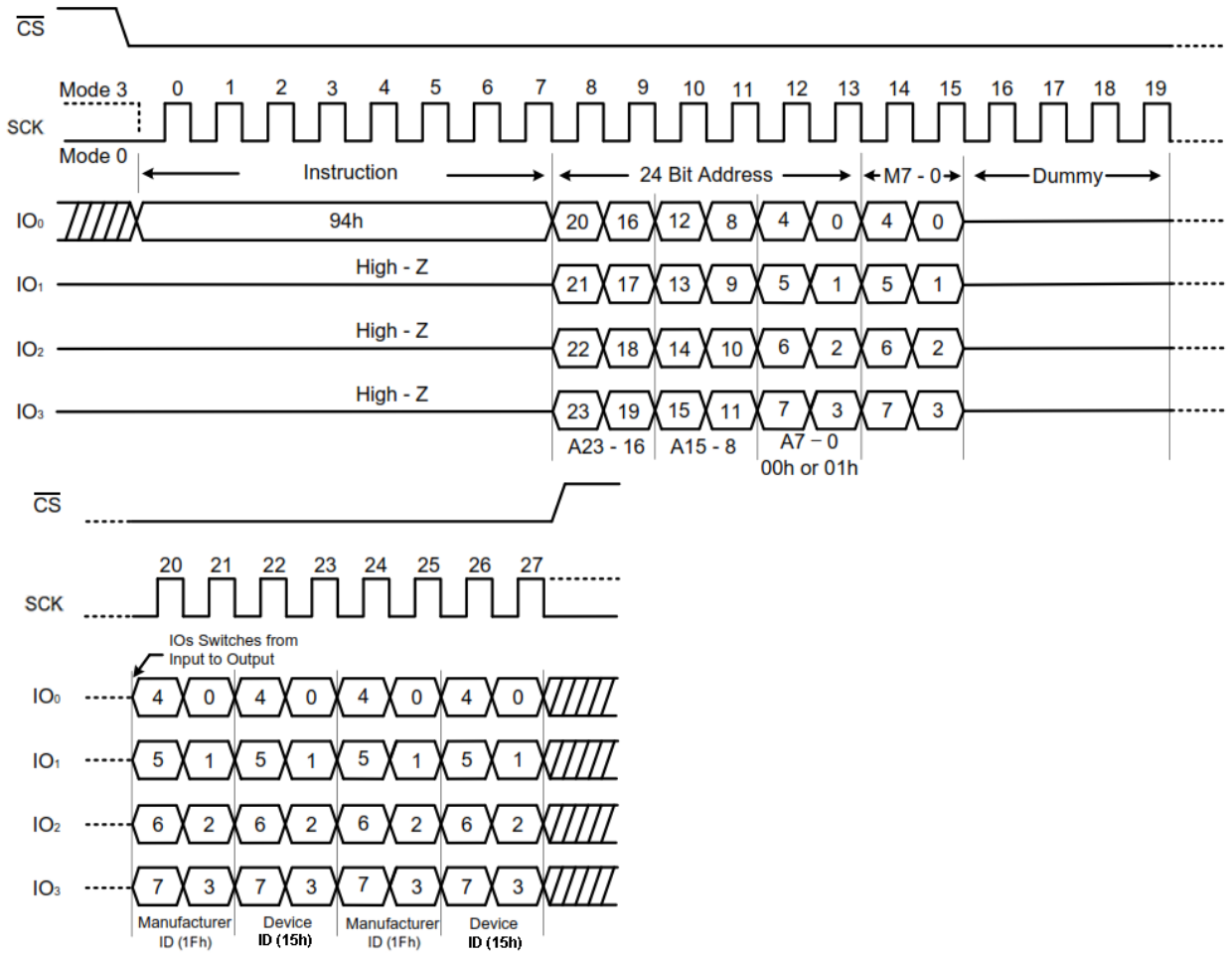


Figure 8-45. Read Quad Manufacturer/ Device ID Quad I/O instruction (SPI Mode)

8.28 JEDEC ID (9Fh)

For compatibility reasons, the AT25SL321 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is congruous with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The instruction is entered by driving the $\overline{CS}$ pin low with following the instruction code 9Fh. JEDEC assigned Manufacturer ID byte for Adesto (1Fh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCK with most significant bit (MSB) first shown in Figure 8-46 and Figure 8-47. For memory type and capacity values, see Manufacturer and Device Identification Table 8-1. The JEDEC ID can be read continuously. The instruction is terminated by driving $\overline{CS}$ high.

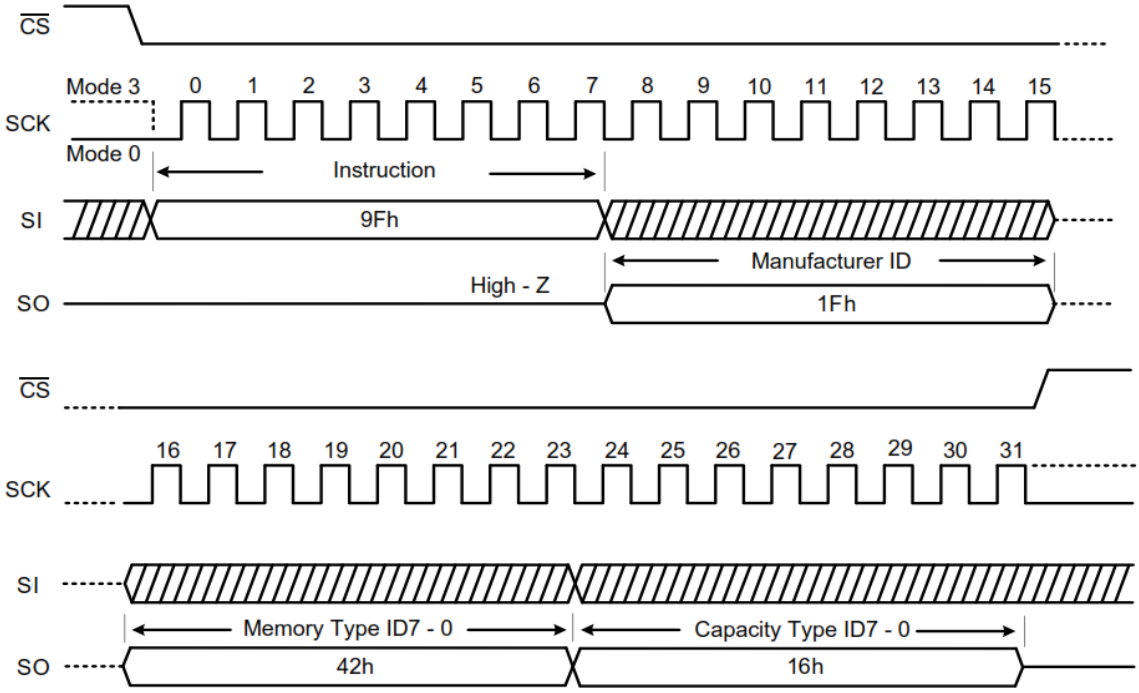


Figure 8-46. Read JEDEC ID Instruction (SPI Mode)

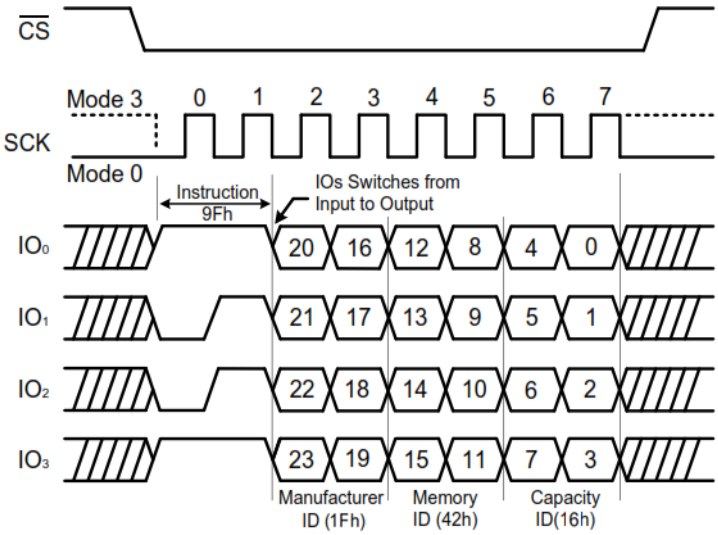


Figure 8-47. Read JEDEC ID Instruction (QPI Mode)

8.29 Enable QPI (38h)

The AT25SL321 support both Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. Enable QPI instruction is the only way to switch the device from SPI mode to QPI mode.

In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an Enable QPI instruction must be issued. If the Quad Enable (QE) bit is 0, the Enable QPI instruction is ignored and the device remains in SPI mode.

After power-up, the default state of the device is SPI mode. See the Instruction Set Table 8-2 for all the commands supported in SPI mode and the Instruction Set Table 8-5 for all the instructions supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

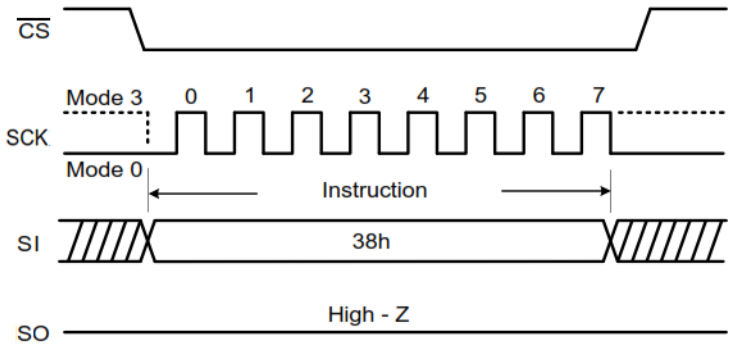


Figure 8-48. Enable QPI Instruction (SPI Mode only)

8.30 Disable QPI (FFh)

By issuing Disable QPI (FFh) instruction, the device switches back to SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting remain unchanged.

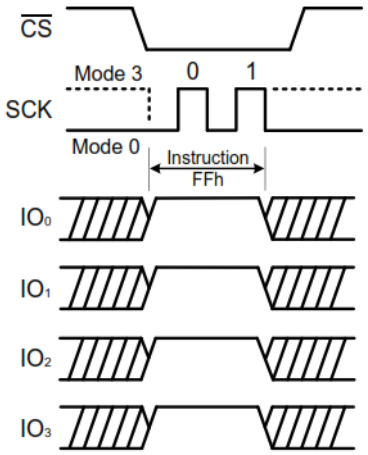


Figure 8-49. Disable QPI Instruction for QPI Mode

8.31 Word Read Quad I/O (E7h)

The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O instruction. The lowest Address bit (A0) must equal 0 and only two dummy clocks are required prior to the data output.

Continuous Read Mode

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 8-50. The upper nibble of the (M7-4) controls the length of the next Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M[3:0]) are don't care ('X'). However, the IO pins are going to be high-impedance prior to the falling edge of the first data out clock.

If the Continuous Read Mode bits M[7-4] = Ah, then the next Fast Read Quad I/O instruction (after $\overline{CS}$ is raised and then lowered) does not require the E7h instruction code, as shown in Figure 8-51. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M[7:4] do not equal to Ah (1,0,1,0) the next instruction (after $\overline{CS}$ is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

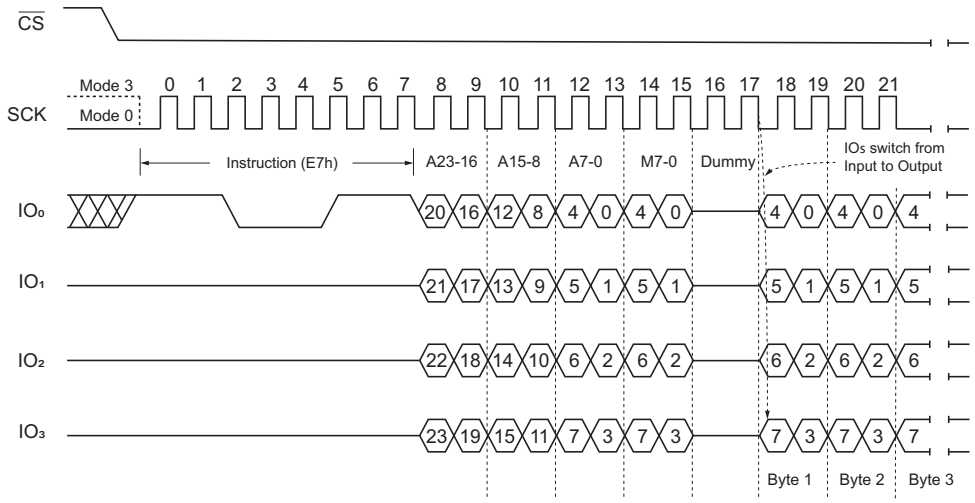


Figure 8-50. Word Read Quad I/O Instruction (Initial instruction or previous set M7-0 ≠ Axh, SPI Mode)

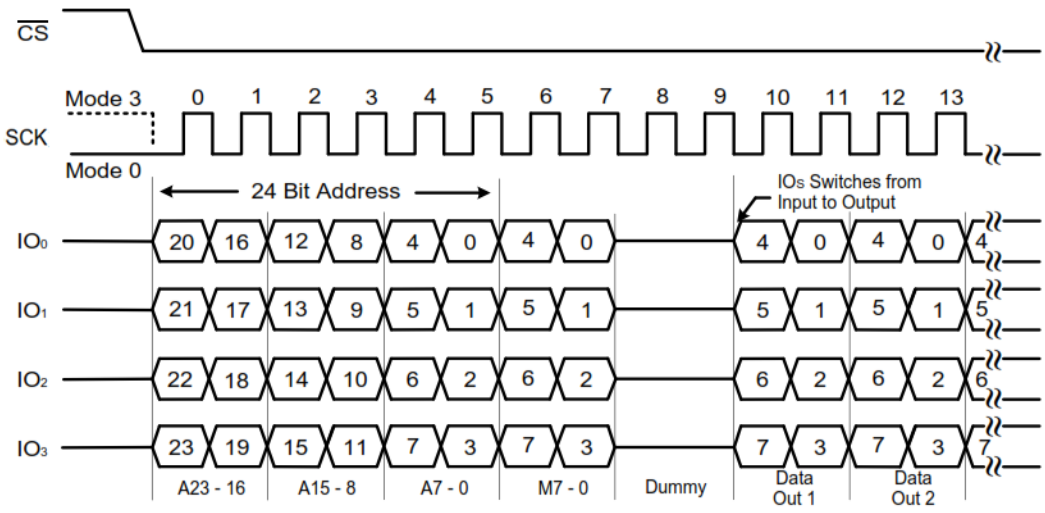


Figure 8-51. Word Read Quad I/O instruction (Previous Instruction set M7-0= Axh, SPI Mode)

Wrap Around in SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior to E7h. The Set Burst with Wrap (77h) instruction can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing read instructions.

The Set Burst with Wrap instruction allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 is used to specify the length of the wrap around section within a page. See

8.32 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with Fast Read Quad I/O and Word Read Quad I/O instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance. Before the device accepts the Set Burst with Wrap instruction, a Quad enable of Status Register-2 must be set (Status Register bit QE must equal 1).

The Set Burst with Wrap instruction is initiated by driving the $\overline{CS}$ pin low and then shifting the instruction code 77h followed by 24 dummy bits and 8 Wrap Bits, W7-0. The instruction sequence is shown in Set Burst with Wrap Instruction Sequence. Wrap bit W7 and W3-0 are not used.

Table 8-6. Set Burst with Wrap W6:W4 Encoding

W6, W5	W4 = 0		W4 = 1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
00	Yes	8-byte	No	N/A
01	Yes	16-byte	No	N/A
10	Yes	32-byte	No	N/A
11	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following Fast Read Quad I/O and Word Read Quad I/O instructions use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, issue to set W4=1, another Set Burst with Wrap instruction. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction or Reset (99h) instruction to reset W4 = 1 prior to any normal Read instructions since AT25SL321 does not have a hardware Reset Pin.

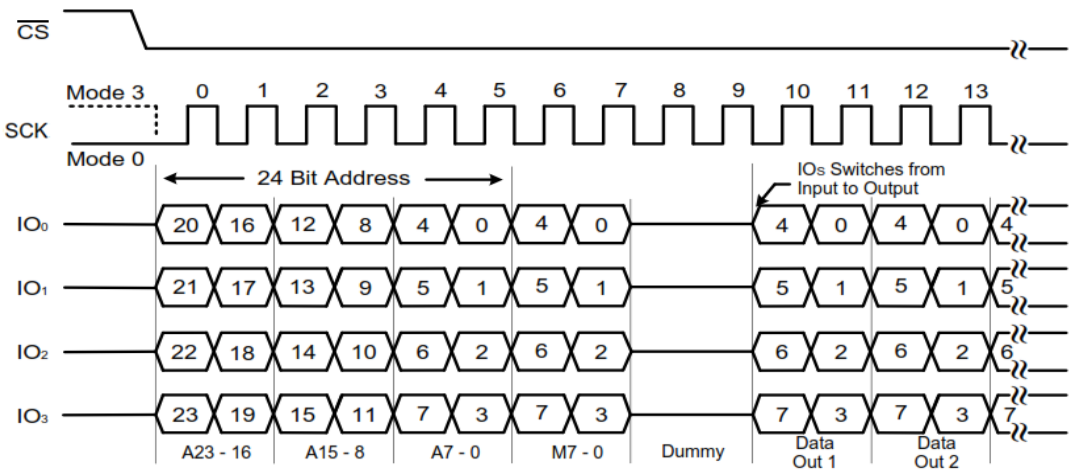


Figure 8-52. Set Burst with Wrap Instruction Sequence

8.33 Burst Read with Wrap (0Ch)

The Burst Read with Wrap (0Ch) instruction provides an alternative way to perform the read operation with Wrap Around in QPI mode. The instruction is similar to the Fast Read (0Bh) instruction in QPI mode, except the addressing of the read operation needs to Wrap Around to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The Wrap Length and the number of dummy of clocks can be configured by the Set Read Parameters (C0h) instruction.

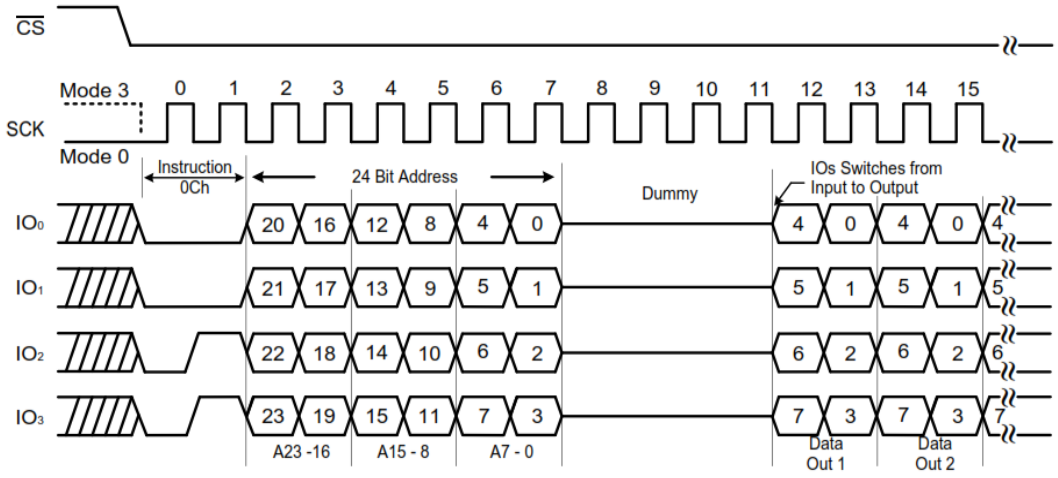


Figure 8-53. Burst Read with Wrap instruction (QPI Mode, 80 MHz)

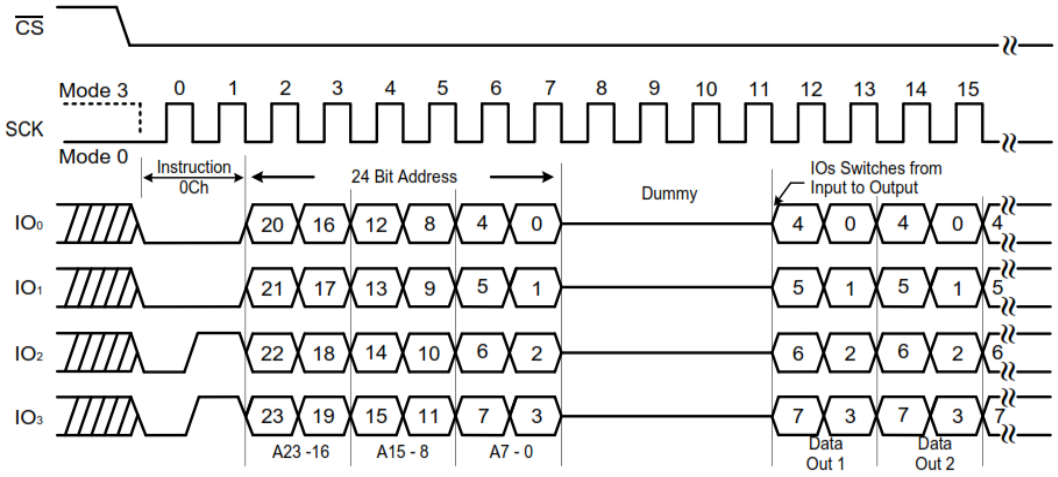


Figure 8-54. Burst Read with Wrap instruction (QPI Mode, 104 MHz)

8.34 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) instruction can be used to configure the number of dummy clocks for the Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) instructions, and also configure the number of bytes of 'Wrap Length' for the Burst Read with Wrap (0Ch) instruction.

In Standard SPI mode, the Set Read Parameters (C0h) instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed. See the corresponding instruction. The encoding for the number of dummy clocks and wrap length are shown in the following tables. The default 'Wrap Length' after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4.

Table 8-7. Dummy Clock Encoding

P5, P4	Dummy Clocks	Maximum Read Frequency
00	4	80 MHz
01	4	80 MHz
10	6	104 MHz

Table 8-8. Wrap Length Encoding

P1, P0	Wrap Length
00	8-bytes
01	16-bytes
10	32-bytes
11	64-bytes

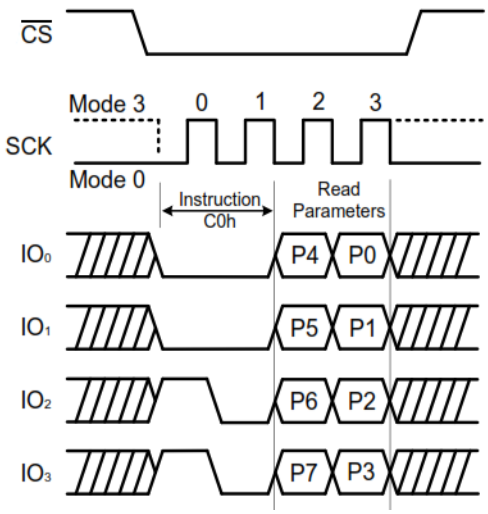


Figure 8-55. Set Read Parameters instruction (QPI Mode)

8.35 Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the AT25SL321 provides a software reset instruction instead of a dedicated RESET pin.

Once the Reset instruction is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

The Enable Reset (66h) and Reset (99h) instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any instruction other than Reset (99h) after the Enable (66h) instruction disables the Reset Enable state. A new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset instruction is accepted by the device takes approximately t_{RST} = 30 µs to reset. During this period, no instructions are accepted.

Data corruption can happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

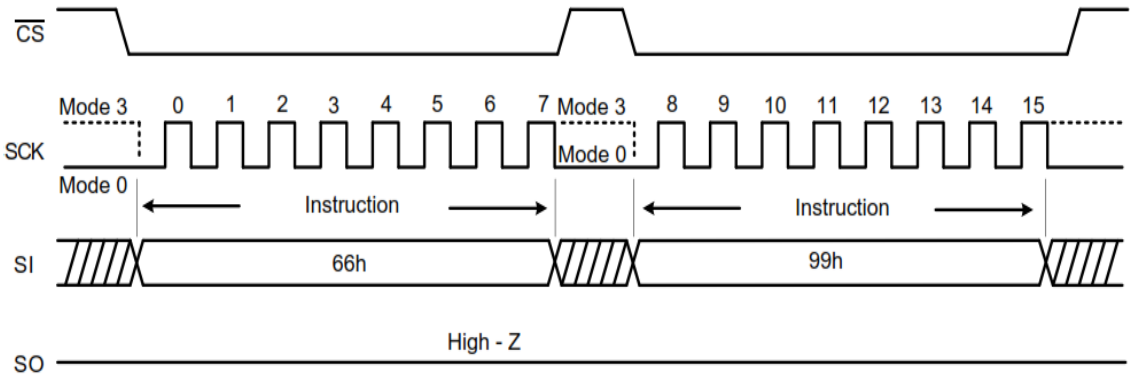


Figure 8-56. Enable Reset and Reset Instruction (SPI Mode)

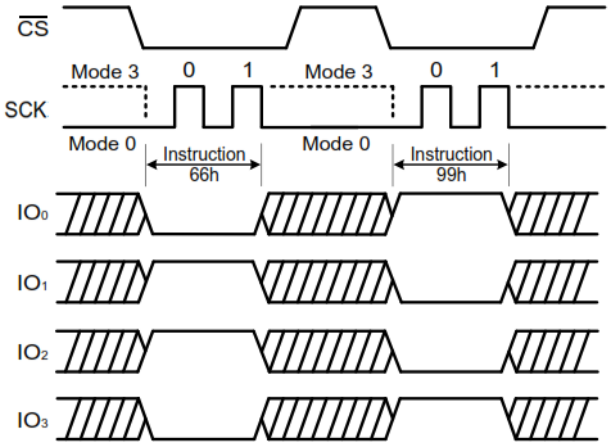


Figure 8-57. Enable Reset and Reset Instruction (QPI Mode)

8.36 Read Serial Flash Discovery Parameter (5Ah)

The Read Serial Flash Discovery Parameter (SFDP) instruction allows reading the Serial Flash Discovery Parameter area (SFDP). This SFDP area is composed of 2048 read-only bytes containing operating characteristics and vendor specific information. The SFDP area is factory programmed. If the SFDP area is blank, the device is shipped with all the SFDP bytes at FFh. If only a portion of the SFDP area is written to, the portion not used is shipped with bytes in erased state (FFh).

The instruction sequence for the read SFDP has the same structure as that of a Fast Read instruction. First, the device is selected by driving Chip Select ($\overline{CS}$) low. Next, the 8-bit instruction code (5Ah) and the 24-bit address are shifted in, followed by 8 dummy clock cycles. The bytes of SFDP content are shifted out on the Serial Data Output (SO) starting from the specified address. Each bit is shifted out during the falling edge of Serial Clock (SCK). The instruction sequence is shown here. The Read SFDP instruction is terminated by driving Chip Select ($\overline{CS}$) High at any time during data output.

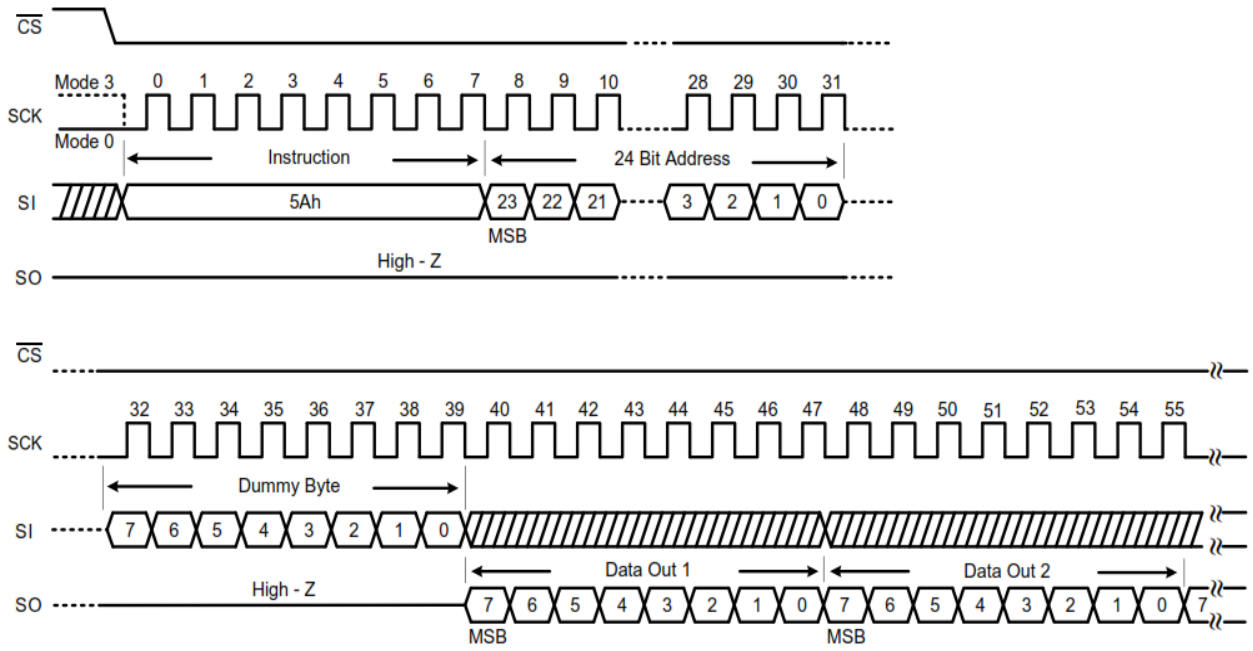


Figure 8-58. Read SFDP Register Instruction

Table 8-9. SFDP Signature and Headers

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
SFDP Signature		00h	07:00	0101 0011	53h
		01h	15:08	0100 0110	46h
		02h	23:16	0100 0100	44h
		03h	31:24	0101 0110	50h
SFDP Minor Revision	Start from 00h	04h	07:00	0000 0110	06h
SFDP Major Revision	Start from 01h	05h	15:08	0000 0001	01h

Table 8-9. SFDP Signature and Headers *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Number of Parameters Headers	Start from 00h	06h	23:16	0000 0001	01h
Reserved	FFh	07h	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	JEDEC Parameter ID (LSB) = 00h	08h	07:00	0000 0000	00h
Parameter Table Minor Revision	Start from 00h	09h	15:08	0000 0110	06h
Parameter Table Major Revision	Start from 01h	0Ah	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	0Bh	31:24	0001 0000	10h
Parameter Table Pointer	Address of Adesto Parameter Table	0Ch	07:00	0011 0000	30h
		0Dh	15:08	0000 0000	00h
		0Eh	23:16	0000 0000	00h
JEDEC Parameter ID (MSB)	JEDEC Parameter ID (MSB):FFh	0Fh	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	Adesto Manufacturer ID	10h	07:00	0001 1111	1Fh
Parameter Table Minor Revision	Start from 00h	11h	15:08	0000 0000	00h
Parameter Table Major Revision	Start from 01h	12h	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	13h	31:24	0000 0010	02h
Parameter Table Pointer (PTP)	Address of Adesto Parameter Table	14h	07:00	1000 0000	80h
		15h	15:08	0000 0000	00h
		16h	23:16	0000 0000	00h
Reserved	FFh	17h	31:24	0000 0001	01h

Table 8-10. SFDP Parameters Table 1

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Erase Granularity	01:4 kB available 11:4 kB not available	30h	01:00	01	E5h
Write Granularity	0:1Byte, 1:64 bytes or larger		02	1	
Volatile Status Register Block Protect Bits	0: Nonvolatile status bit 1: Volatile status bit		03	0	
Volatile Status Register Write Enable Opcode	0:50H Opcode to enable, if bit-3 = 1		04	0	
Reserved			07:05	111	
4 kB Erase Opccde	Opcode or FFh	31h	15:08	0010 0000	20h
Fast Dual Read Output (1 -1 -2)	0 = Not supported 1 = Supported	32h	16	1	F1h
Number of Address Bytes	00: 3 Byte only 01: 3 or 4 Byte 10: 4 Byte only 11: Reserved		18:17	00	
Double Transfer Rate (DTR) Clocking	0 = Not supported 1 = Supported		19	0	
Fast Dual I/O Read (1-2- 2)	0 = Not supported 1 = Supported		20	1	
Fast Quad I/O Read (1-4-4)	0 = Not supported 1 = Supported		21	1	
Fast Quad Output Read (1-1-4)	0 = Not supported 1 = Supported		22	1	
Reserved	FFh		23	1	
Reserved	FFh	33h	31:24	1111 1111	FFh
Flash Memory Density		34h	07:00	1111 1111	FFh
		35h	15:08	1111 1111	FFh
		36h	23:16	1111 1111	FFh
		37h	31:24	0000 0001	01h
Fast Quad I/O (1-4-4) Number of dummy clocks	Number of dummy clocks	38h	04:00	00100	44h
Fast Quad I/O (1-4-4) Number of mode bits	Number of mode bits		07:05	010	
Fast Quad I/O (1-4-4) Read Opcode	Opcode or FFh	39h	15:08	1110 1011	EBh

Table 8-10. SFDP Parameters Table 1 *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Fast Quad Output (1-1-4) Number of dummy clocks	Number of dummy clocks	3Ah	20:16	01000	08h
Fast Quad Output (1-1-4) Number of mode bits	Number of mode bits		23:21	000	
Fast Quad Output (1-1-4) Read Opcode	Opcode or FFh	3Bh	31:24	0110 1011	6Bh
Fast Dual Output (1-1-2) Number of dummy clocks	Number of dummy clocks	3Ch	04:00	01000	08h
Fast Dual Output (1-1-2) Number of mode bits	Number of mode bits		07:05	000	
Fast Dual Output (1-1-2) Read Opcode	Opcode or FFh	3Dh	15:08	0011 1011	3Bh
Fast Dual I/O (1-2-2) Number of dummy clocks	Number of dummy clocks	3Eh	20:16	00000	80h
Fast Dual I/O (1-2-2) Number of mode bits	Number of mode bits		23:21	100	
Fast Dual I/O (1-2-2) Read Opcode	Opcode or FFh	3Fh	31:24	1011 1011	BBh
Fast Dual DPI (2-2-2)	0 = Not supported 1 = Supported	40h	0	0	FEh
Reserved	FFh		03:01	111	
Fast Quad QPI (4-4-4)	0 = Not supported 1 = Supported		04	1	
Reserved	FFh		07:05	111	
Reserved	FFh	41h	15:08	1111 1111	FFh
Reserved	FFh	42h	23:16	1111 1111	FFh
Reserved	FFh	43h	31:24	1111 1111	FFh
Reserved	FFh	44h	07:00	1111 1111	FFh
Reserved	FFh	45h	15:08	1111 1111	FFh
Fast Dual DPI (2-2-2) Number of dummy clocks	Number of dummy clocks	46h	20:16	0 0000	00h
Fast Dual DPI (2-2-2) Number of mode bits	Number of mode bits		23:21	000	
Fast Dual DPI(2-2-2) Read Opcode	Opcode or FFh	47h	31:24	1111 1111	FFh
Reserved	FFh	48h	07:00	1111 1111	FFh
Reserved	FFh	49h	15:08	1111 1111	FFh

Table 8-10. SFDP Parameters Table 1 *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Fast Quad QPI (4-4-4) Number of dummy clocks	Number of dummy clocks	4Ah	20:16	00010	42h
Fast Quadl QPI (4-4-4) Number of mode bits	Number of mode bits		23:21	010	
Fast Quad QPI (4-4-4) Read Opcode	Opcode or FFh	4Bh	31:24	1110 1011	EBh
Erase type-1 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	4Ch	07:00	0000 1100	0Ch
Erase type-1 Opcode	Opcode or FFh	4Dh	15:08	0010 0000	20h
Erase type-2 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	4Eh	23:16	0000 1111	0Fh
Erase type-2 Opcode	Opcode or FFh	4Fh	31:24	0101 0010	52h
Erase Type-3 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	50h	07:00	0001 0000	10h
Erase Type-3 Opcode	Opcode or FFh	51h	15:08	1101 1000	D8h
Erase Type-4 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	52h	23:16	0000 0000	00h
Erase Type-4 Opcode	Opcode or FFh	53h	31:24	1111 1111	FFh
Erase Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	54h 55h 56h 57h	03:00	0011	33h 62h D5h 00h
Erase type-1 Typical time	Count or 00h		08:04	0 0011	
Erase type-1 Typical units	00b: 1 ms 01b: 16 ms 10b: 128 ms 11b: 1 s		10:09	01	
Erase type-2 Typical time	Count or 00h		15:11	0110 0	
Erase type-2 Typical units	00b: 1 ms 01b: 16 ms 10b: 128 ms 11b: 1 s		17:16	01	
Erase type-3 Typical time	Count or 00h		22:18	101 01	
Erase type-3 Typical units	00b: 1 ms 01b: 16 ms 10b: 128 ms 11b: 1 s		24:23	01	
Erase type-4 Typical time	Count or 00h		29:25	00 000	
Erase type-4 Typical units	00b: 1 ms 01b: 16 ms 10b: 128 ms 11b: 1 s		31:30	00	

Table 8-10. SFDP Parameters Table 1 *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Program Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	58h	03:00	0100	84h
Page Size	2^N bytes		07:04	1000	
Program Page Typical time	Count or 00h	59h 5Ah 5Bh	12:08	0 1001	29h 01h C4h
Program Page Typical units	0: 8 µs, 1: 64 µs		13	1	
Program Byte Typical time, 1st byte	Count or 00h		17:14	01 00	
Program Byte Typical units, 1st byte	0: 1 µs, 1: 8 µs		18	0	
Program Additional Byte Typical time	Count or 00h		22:19	000 0	
Program Additional Byte Typical units	0: 1 µs, 1: 8 µs		23	0	
Erase Chip Typical time	Count or 00h		28:24	0 0100	
Erase Chip Typical units	00b: 16 ms 01b: 256 ms 10b: 4 sec 11b: 64 sec		30:29	10	
Reserved	1h		31	1	
Prohibited Op during Program Suspend	See datasheet	5Ch	03:00	11010	ECh
Prohibited Op during Erase Suspend	See datasheet		07:04	1110	

Table 8-10. SFDP Parameters Table 1 *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Reserved	1h	5Dh 5Eh 5Fh	08	1	A1h 07h 3Dh
Program Resume to Suspend time	Count of 64us		12:09	0 000	
Program Suspend Maximum time	Count or 00h		17:13	11 101	
Program Suspend Maximum units	00b: 128 ns 01b: 1 µs 10b: 8 µs 11b: 64 µs		19:18	01	
Erase Resume to Suspend time	Count of 64 µs		23:20	0000	
Erase Suspend Maximum time	Count or 00h		28:24	1 1101	
Erase Suspend Maximum units	00b: 128 ns 01b: 1 µs 10b: 8 µs 11b: 64 µs		30:29	01	
Suspend / Resume supported	0: Program and Erase suspend supported 1: not supported		31	0	
Program Resume Opcode	Opcode or FFh	60h	7:0	0111 1010	7Ah
Program Suspend Opcode	Opcode or FFh	61h	15:8	0111 0101	75h
Resume Opcode	Opcode or FFh	62h	23:16	0111 1010	7Ah
Suspend Opcode	Opcode or FFh	63h	31:24	0111 0101	75h
Reserved	11b	64h	01:00	11	F7h
Status Register Busy Polling	xxxxx1b: Opcode = 05h, bit-0 = 1 Busy, xxxx1xb: Opcode = 70h, bit-7 = 0 Busy, others: reserved		07:02	1111 01	
Exit Deep Powerdown time	Count or 00h	65h 66h 67h	12:08	0 0010	A2h D5h 5Ch
Exit Deep Powerdown units	00b: 128 ns 01b: 1 µs 10b: 8 µs 11b: 64 µs		14:13	01	
Exit Deep Powerdown Opcode	Opcode or FFh		22:15	101 0101 1	
Enter Deep Powerdown Opcode	Opcode or FFh		30:23	101 1100 1	
Deep Powerdown Supported	0: Deep Powerdown supported, 1: not supported		31	0	

Table 8-10. SFDP Parameters Table 1 *(continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Disable 4-4-4 Read Mode		68h 69h 6Ah	03:00	1001	19h F6h 1Ch
Enable 4-4-4 Read Mode			08:04	0 0001	
Fast Quad I/O Continuous (0-4-4) supported	0: not supported, 1: Quad I/O 0-4-4 supported		09	1	
Fast Quad I/O Continuous (0-4-4) Exit			15:10	1111 01	
Fast Quad I/O Continuous (0-4-4) Enter			19:16	1100	
Quad Enable Requirements (QER)			22:20	001	
HOLD or RESET Disable	0: not supported, 1: use Configuration Register bit-4		23	0	
Reserved	FFh	6Bh	31;24	1111 1111	FFh
Status Register Opcode		6Ch	06:00	110 1000	E8h
Reserved	1h		07	1	
Soft Reset Opcodes		6Dh	13:08	01 0000	10h C0h
4-Byte Address Exit		6Eh	23:14	1100 0000 00	
4-Byte Address Enter		6Fh	31:24	1000 0000	80h

Table 8-11. SFDP Parameters Table 2

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
VCC Minimum Voltage	1650h: 1.65V, 1700h: 1.70V, 2300h: 2.30V, 2500h: 2.50V, 2700h: 2.70V	80h 81h	15:0	0000 0000 0001 0111	00h 17h
VCC Maximum Voltage	1950h: 1.95V, 3600h: 3.60V, 4000h: 4.00V, 4400h: 4.40V	82h 83h	31:16	0000 0000 0010 0000	00h 20h
Array Protection Method	10b: use non-volatile status register	84h 85h	01:00	00	00h 00h
Power up Protection default	0: power up unprotected, 1: power up protected		02	0	
Protection Disable Opcodes	011b: use status register		05:03	00 0	
Protection Enable Opcodes	011b: use status register		08:06	0 00	
Protection Read Opcodes	011b: use status register		11:09	000	
Protection Register Erase Opcode	00b: not supported, 01b: Opcodes 3Dh, 2Ah, 7Fh, CFh,		13:12	00	
Protection Register Program Opcode	00b: not supported, 01b: Opcodes 3Dh, 2Ah, 7Fh, FCh		15:14	00	
Reserved	FFh	86h	23:16	1111 1111	FFh
Reserved	FFh	87h	31:24	1111 1111	FFh
Reserved	FFh	88h - FFh			Reserved

8.37 Enter Secured OTP (B1h)

The Enter Secured OTP instruction is for entering the additional 4 kbit secured OTP mode. The additional 4 kbit secured OTP is independent from main array, which can be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down

Please note that Write Status Register-1, Write Status Register-2 and Write Security Register instructions are not acceptable during the access of secure OTP region. Once security OTP is lock down, only commands related with read are valid. The Enter Secured OTP instruction sequence is shown in Figure 8-59.

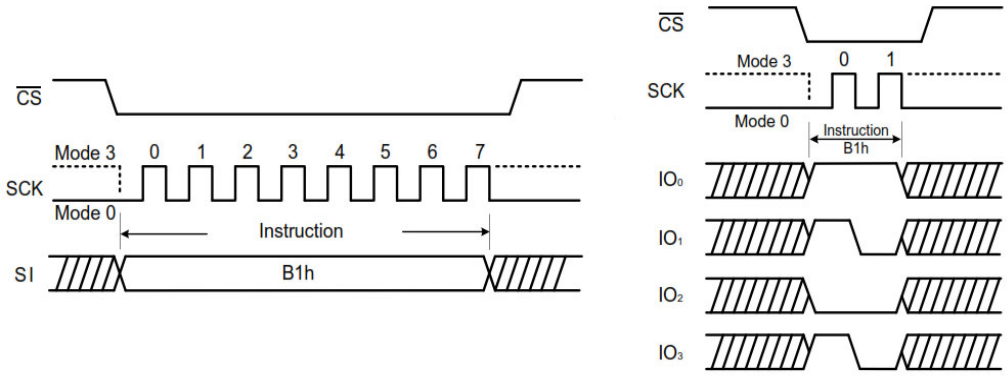


Figure 8-59. Enter Secured OTP Instruction for SPI Mode (left) and QPI Mode (right)

8.38 Exit Secured OTP (C1h)

The Exit Secured OTP instruction is for exiting the additional 4 kbit secured OTP mode. See Figure 8-60.

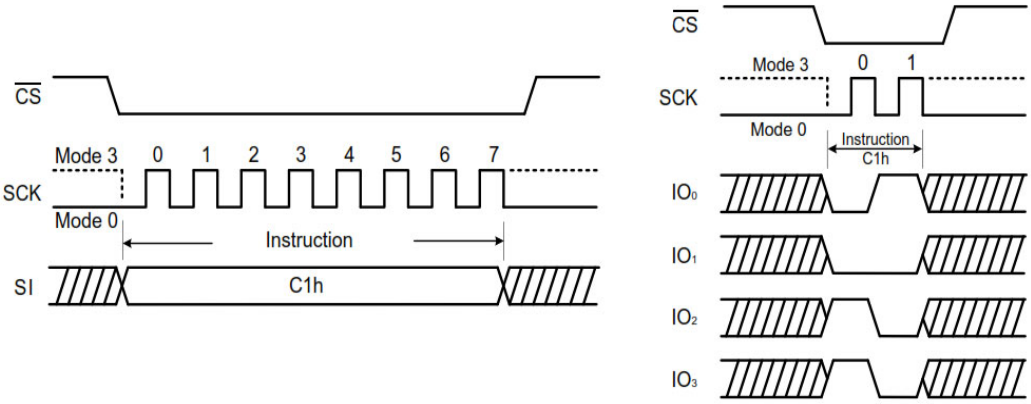


Figure 8-60. Exit Secured OTP instruction for SPI Mode (left) and QPI Mode (right)

8.39 Read Security Register (2Bh)

The Read Security Register can be read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition) and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex-factory or not. When it is '0', it indicates non-factory lock, '1' indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing Write Security Register instruction, the LDSO bit can be set to "1" for customer lock-down purpose. However, once the bit it set to "1" (Lock-down), the LDSO bit and the 4 kbit Secured OTP area cannot be updated any more. While it is in 4 kbit Secured OTP mode, array access is not allowed to write.

Table 8-12. Security Register Definition

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	x	x	x	x	x	LDSO (indicate if lock- down)	Secured OTP indicator bit
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0 = not lock-down 1 = lock down (cannot program/ erase OTP)	0 = non factory lock 1 = factory lock
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non- Volatile bit	Non- Volatile bit

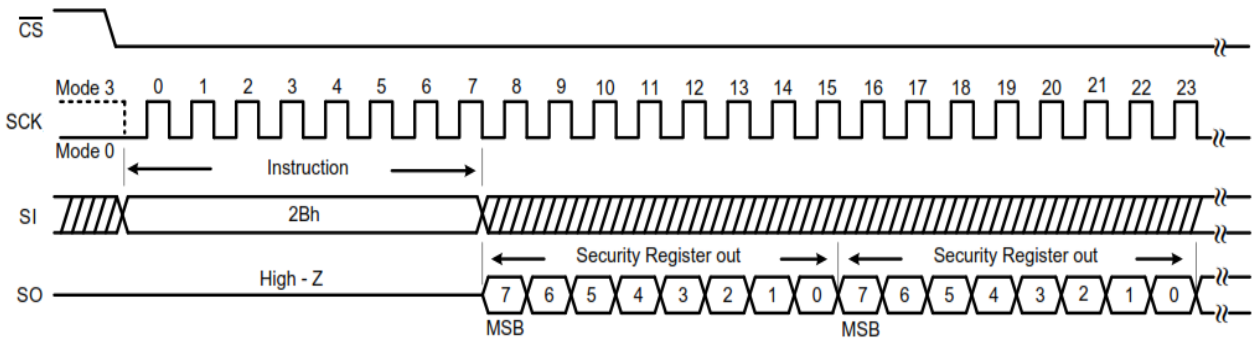


Figure 8-61. Read Security Register instruction (SPI Mode)

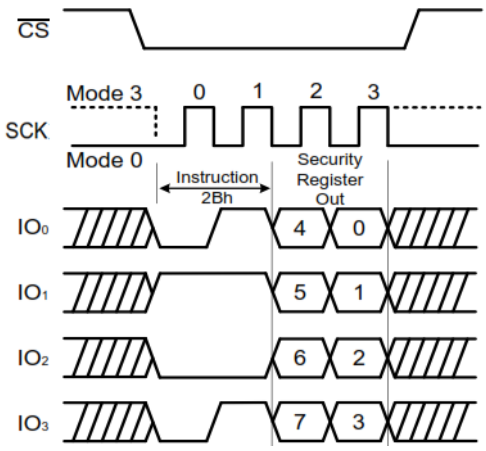


Figure 8-62. Read Security Register instruction (QPI Mode)

8.40 Write Security Register (2Fh)

The Write Security Register instruction is for changing the values of Security Register bits. Unlike the Write Status Register instruction, the Write Enable instruction is not required before writing Write Security Register instruction. The Write Security Register instruction can change the value of bit1 (LDSO bit) for customer to lock-down the 4 kbit Secured OTP area. Once the LDSO bit is set to “1”, the Secured OTP area cannot be updated any more.

The $\overline{CS}$ must go high exactly at the boundary; otherwise, the instruction are rejected and not executed.

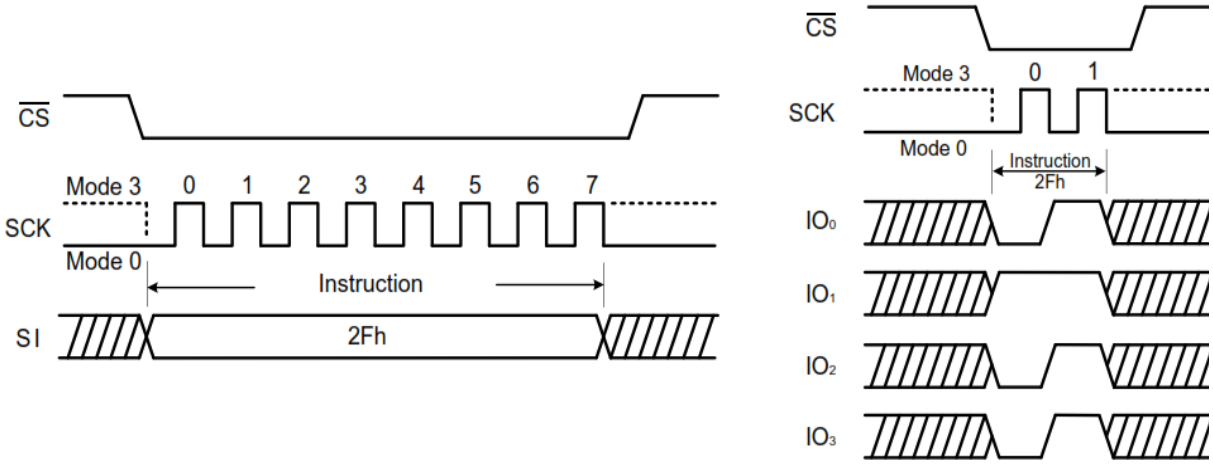


Figure 8-63. Write Security Register Instruction for SPI Mode (left) and QPI Mode (right)

8.41 4 kbit Secured OTP

It’s for unique identifier to provide 4 kbit one-time-program area for setting device unique serial number which can be set by factory or system customer. See Table 8-13, Secured OTP Address Space.

- Security register bit 0 indicates whether the chip is locked by the factory or not.
- To program the 4 kbit secured OTP by entering 4 kbit secured OTP mode (with ENSO command) and going through normal program procedure, and then exiting 4 kbit secured OTP mode by writing the EXSO command.
- Customer might lock-down bit 1 as ‘1’. See Table 8-13, Secured OTP Address Space.

Note. Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4 kbit secured OTP mode, write access to the array is not allowed.

Table 8-13. Secured OTP Address Space

Address Range	Size	Standard	Customer Lock
000000 ~ 00000F	128-bit	ESN (Electrical Serial Number)	Determined by customer
000010 ~ 0001FF	3968-bit	N/A	

9. Electrical Characteristics

9.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Range	Units
Supply Voltage	VCC		-0.6 to VCC+0.4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.6 to VCC +0.4	V
Transient Voltage on any Pin	VIOT	<20 ns Transient Relative to Ground	-1.0V to VCC +1.0V	V
Storage Temperature	TSTG		-65 to +150	˚C
Lead Temperature	TLEAD		See Note[2]	˚C
Electrostatic Discharge Voltage	VESD	Human Body Model[3]	-2000 to +2000	V

Notes:

1. Stresses beyond those listed under “Absolute Maximum Ratings” cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

Parameter	Symbol	Conditions	Min	Max	Units
Power Supply Voltage	VCC	FR = 104 MHz (Single/Dual/Quad SPI) fR = 50 MHz (Read Data 03h)	1.7	2.0	V
Ambient Operating Temperature	T_A	Industrial	-40	+85	˚C

9.3 Endurance and Data Retention

Parameter	Symbol	Conditions		Min
Erase/Program Cycles	4 kB Block, 32/64 kB block, or full chip.	100,000		Cycles
Data Retention	Full temperature range		20	years

9.4 Power-up Timing and Write Inhibit Threshold

Parameter	Symbol	Min	Max	Units
VCC (min) to $\overline{CS}$ Low	t_{VSL}(1)	10		µs
Time Delay Before Write Instruction	t_{PUW}(1)	1	10	ms
Write Inhibit Threshold Voltage	VWI(1)	1.0	1.4	V

Note:

1. These parameters are characterized at -10C & +85C only

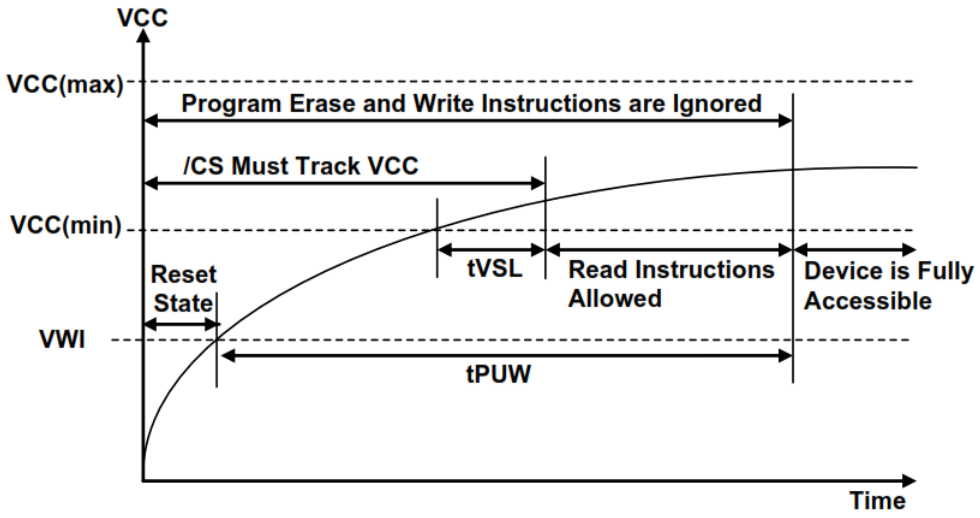


Figure 9-1. Power-up Timing and Voltage Levels

9.5 Program Acceleration via ACC Pin

Parameter	Symbol	Min	Max	Units
$\overline{WP}$ pin High Voltage	V_{HH}(1)	8.5	9.5	V
$\overline{WP}$ pin Voltage rise and fall time	t_{VHH}(1)	2.2		µs
$\overline{WP}$ at V_{HH} and V_{IL} or V_{IH} to first instruction	t_{WC}(1)	5		µs

1. These parameters are characterized only.

Figure 9-2. ACC Program Acceleration Timing and Voltage Levels

9.6 DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	CIN(1)	VIN = 0V(2)			6	pF
Output Capacitance	COUT(1)	VOUT = 0V(2)			8	pF
Input Leakage	ILI				±2	µA
I/O Leakage	ILO				±2	µA
Standby Current	ICC1	$\overline{CS}$ = VCC VIN = GND or VCC		10	50	µA
Power Down Current	ICC2	$\overline{CS}$ = VCC VIN = GND or VCC		2	20	µA
Current Read Data/ Dual/Quad 1 MHz(2)	ICC3	C = 0.1 VCC / 0.9VCC IO = Open			7	mA
Current Read Data/ Dual/Quad 50 MHz(2)	ICC3	C = 0.1 VCC / 0.9VCC IO = Open			15	mA
Current Read Data/ Dual/Quad 80 MHz(2)	ICC3	C = 0.1 VCC / 0.9VCC IO = Open			18	mA
Current Read Data/ Dual/Quad 104 MHz2)	ICC3	C = 0.1 VCC / 0.9VCC IO = Open			20	mA
Current Write Status Register	ICC4	$\overline{CS}$ = VCC		10	20	mA
Current Page Program	ICC5	$\overline{CS}$ = VCC		15	25	mA
Current Block Erase	ICC6	$\overline{CS}$ = VCC		15	25	mA
Current Chip Erase	ICC7	$\overline{CS}$ = VCC		15	25	mA
Input Low Voltages	VIL		-0.5		VCC x0.2	V
Input High Voltages	VIH		VCC x0.8		VCC +0.4	V
Output Low Voltages	VOL	IOL = 100µA			0.2	V
Output High Voltages	VOH	IOH = -100µA	VCC -0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data, TA = 25˚C, VCC = 1.8V.
2. Checked Board Pattern.

9.7 AC Measurement Conditions

Parameter	Symbol	Min	Max	Units
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven

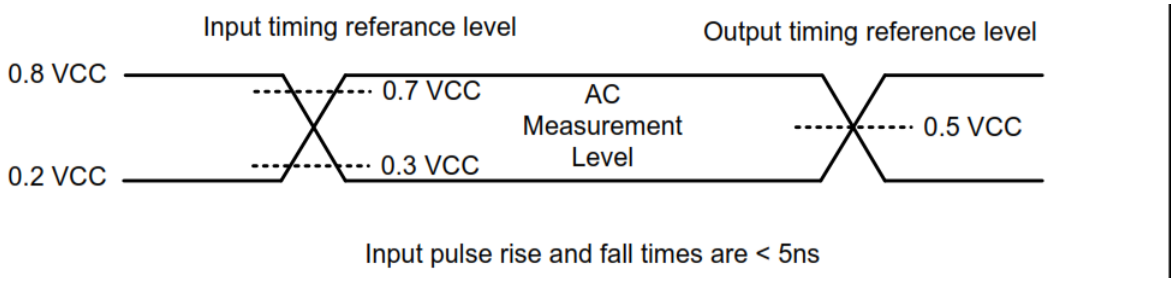


Figure 9-3. AC Measurement I/O Waveform

9.8 AC Electrical Characteristics

Parameter	Symbol	Alt	Min	Typ	Max	Units
Clock frequency. For all instructions, except Read Data (03h) 1.7V-1.95V VCC & Industrial Temperature	F_R	f_c	DC		104	MHz
Clock freq. Read Data instruction (03h)	f_R		DC		50	MHz
Clock High, Low Time except Read Data (03h)	t_{CLH}, t_{CLL} [1]		4.5			ns
Clock High, Low Time for Read Data (03h)instructions	t_{CRLH}, t_{CRLL} [1]		8			ns
Clock Rise Time peak to peak	t_{CLCH} [2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL} [2]		0.1			V/ns
$\overline{CS}$ Active Setup Time relative to Clock	t_{SLCH}	t_{CSS}	5			ns
$\overline{CS}$ Not Active Hold Time relative to Clock	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
$\overline{CS}$ Active Hold Time relative to Clock	t_{CHSH}		5			ns
$\overline{CS}$ Not Active Setup Time relative to Clock	t_{SHCH}		5			ns
$\overline{CS}$ Deselect Time (for Read instructions/ Write, Erase and Program instructions)	t_{SHSL}	t_{CSH}	100			ns

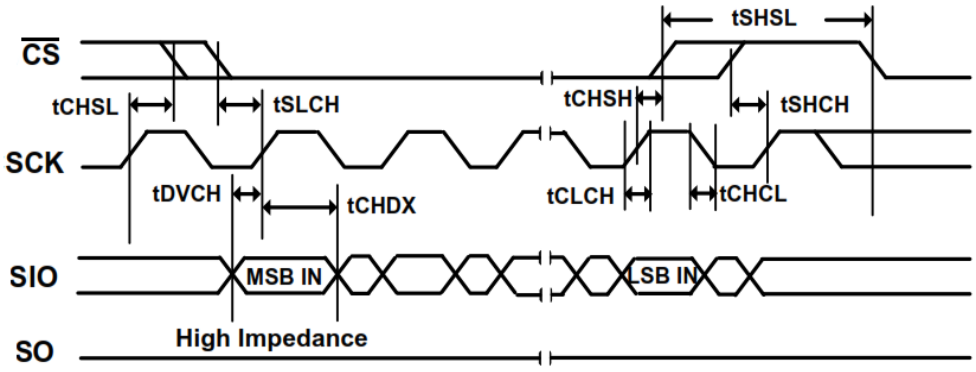
9.8 AC Electrical Characteristics *(continued)*

Parameter	Symbol	Alt	Min	Typ	Max	Units
Output Disable Time	t_{SHQZ} [2]	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_{V1}			7	ns
Clock Low to Output Valid (Except Main Read) (3)	t_{CLQV}	t_{V2}			8	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns
$\overline{HOLD}$ Active Setup Time relative to Clock	t_{HLCH}		5			ns
$\overline{HOLD}$ Active Hold Time relative to Clock	t_{CHHH}		5			ns
$\overline{HOLD}$ Not Active Setup Time relative to Clock	t_{HHCH}		5			ns
$\overline{HOLD}$ Not Active Hold Time relative to Clock	t_{CHHL}		5			ns
$\overline{HOLD}$ to Output Low-Z	t_{HHQX} [2]	t_{LZ}			7	ns
$\overline{HOLD}$ to Output High-Z	t_{HLQZ} [2]	t_{HZ}			12	ns
Write Protect Setup Time Before $\overline{CS}$ Low	t_{WHSL} [4]		20			ns
Write Protect Setup Time After $\overline{CS}$ High	t_{SHWL} [4]		100			ns
$\overline{CS}$ High to Power Down Mode	t_{DP} [2]				3	µs
$\overline{CS}$ High to Standby Mode without Electronic Signature Read	t_{RES1} [2]				3	µs
$\overline{CS}$ High to Standby Mode with Electronic Signature Read	t_{RES2} [2]				1.8	µs
$\overline{CS}$ High to next Instruction after Suspend	t_{SUS} [2]				30	µs
$\overline{CS}$ High to next Instruction after Reset	t_{RST} [2]				30	µs
Write Status Register Time	tw			10	15	ms
Byte Program Time	t_{BP}			10	150	µs
Page Program Time	t_{PP}			0.6	5	ms
Page Program Time (ACC = 9V)	t_{EP}			0.3	3	ms
Block Erase Time (4 kB)	t_{SE}			0.06	0.4	s
Block Erase Time (32 kB)	t_{BE1}			0.20	1.5	s
Block Erase Time (64 kB)	t_{BE2}			0.35	2	s
Chip Erase Time	t_{CE}			20	80	s

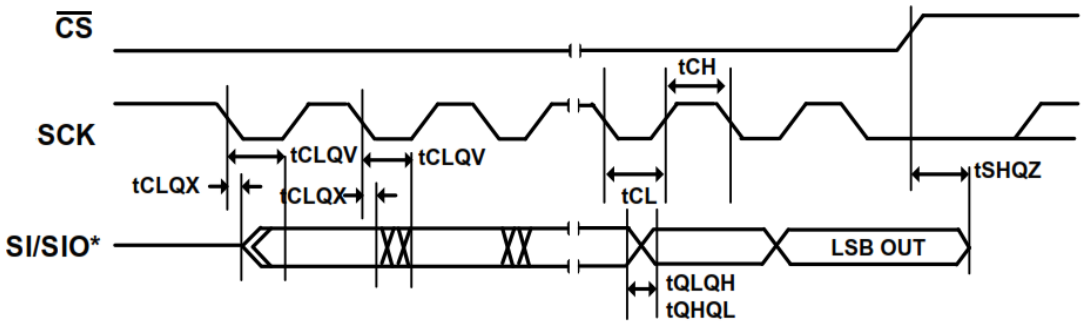
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Contains: Read Status Register-1,2/ Read Manufacturer/Device ID, Dual, Quad/ Read JEDEC ID/ Read Security Register/ Read Serial Flash Discovery Parameter.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.

9.9 Input Timing

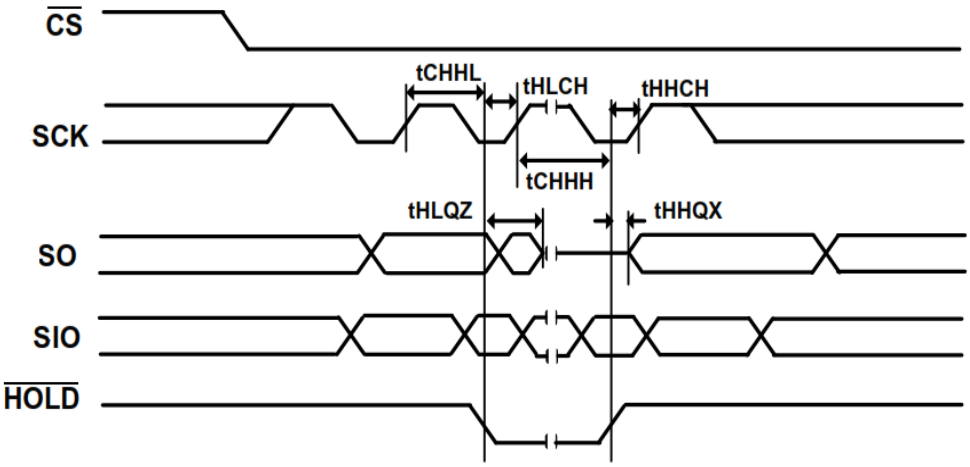


9.10 Output Timing



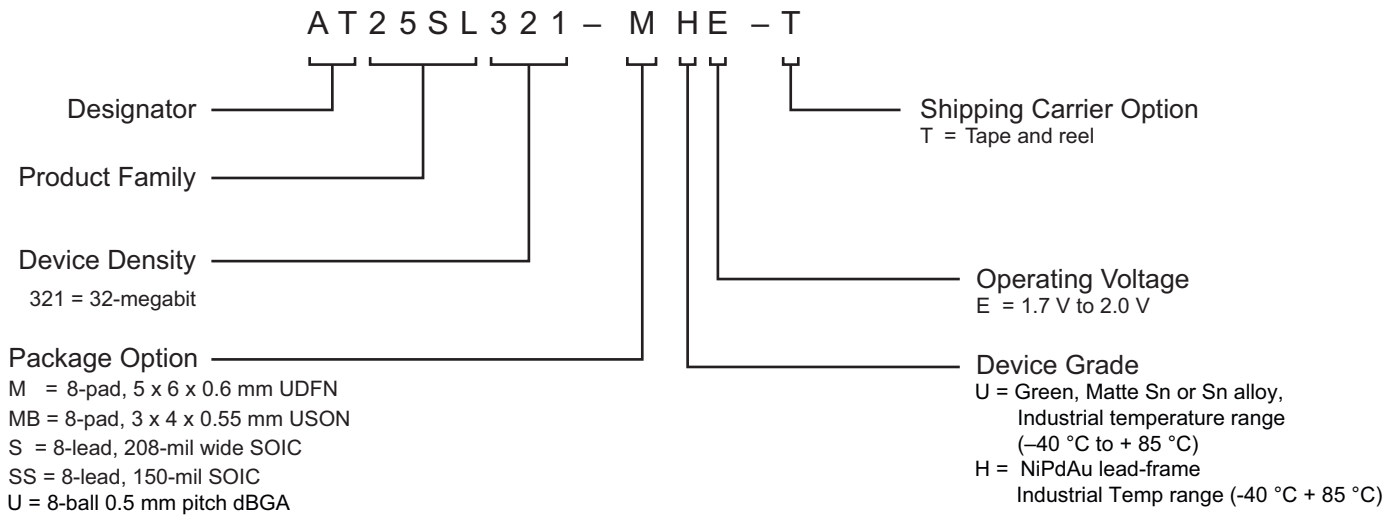
* SIO IS AN OUTPUT ONLY FOR THE FAST READ DUAL OUTPUT INSTRUCTION (3Bh)

9.11 Hold Timing



10. Ordering Information

10.1 Ordering Code Detail



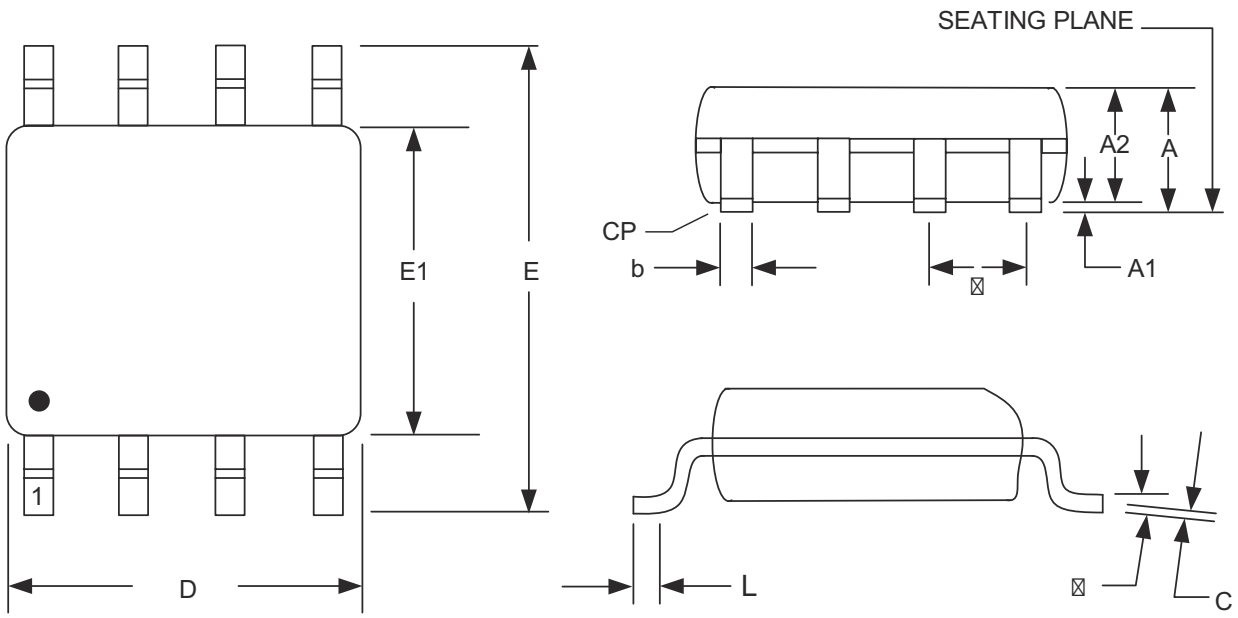
Ordering Code [1]	Package	Lead Finish	Operating Voltage	Max. Freq. (MHz)	Operation Range
AT25SL321-MHE-T	8MA1	NiPdAu	1.7 V - 2.0 V	104 MHz [2]	-40 ℃ to 85 ℃ (Industrial Temperature Range)
AT25SL321-SSHE-T	8S1				
AT25SL321-MBUE-T	8MA2				
AT25SL321-SUE-T	8S4	SnAgCu			
AT25SL321-UUE-T [3]	8-WLCSP				

1. The shipping carrier option code is not marked on the devices.
2. Contact Adesto for availability of 133 MHz operating frequency.
3. Contact Adesto for mechanical drawing or sales information.

Package Type	
8S4	8-lead, 0.208" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8S1	8-lead, 150-mil narrow body JEDEC SOIC
8MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN)
8MA2	8-pad (3 x 4 x 0.55 mm body), Thermally Enhanced Plastic Ultra-Thin Small Outline No-lead (USON)
8-WLCSP	8-ball, 0.5mm pitch, die Ball Grid Array (dBGA)

11. Packaging Information

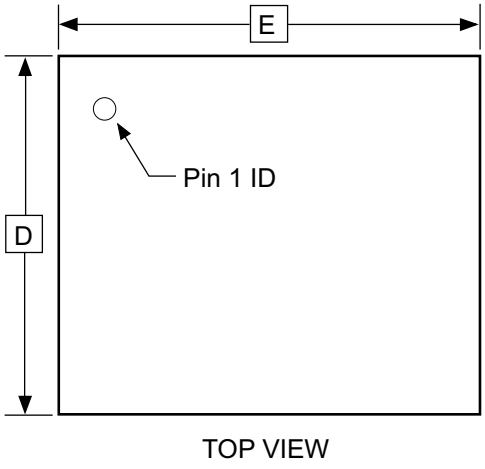
11.1 8S4 – 8-lead, 208 mil EIAJ SOIC



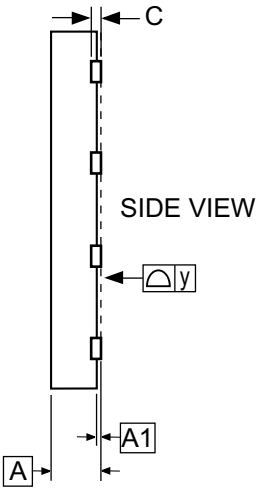
SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
B	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	1.27 BSC			0.050 BSC		
L	0.50	0.65	0.80	0.020	0.026	0.031
□	0°	—	8°	0°	—	8°
Y	—	—	0.10	—	—	0.004

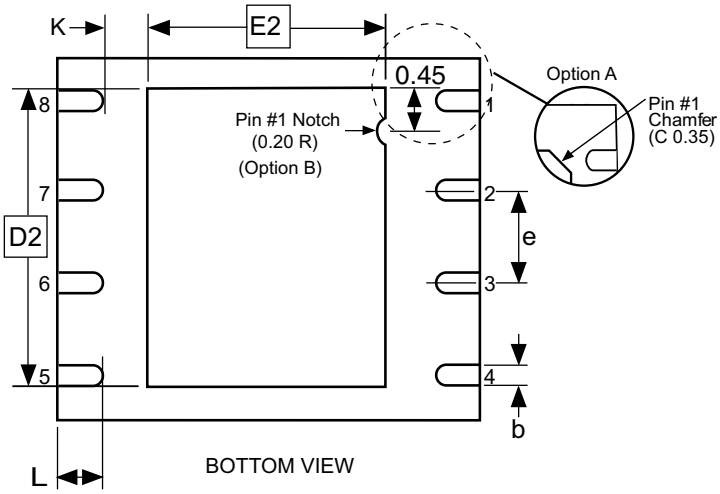
Adesto Package Drawing Contact: contact@adestotech.com	TITLE 8S4, 8-lead, 0.208" Wide Body, Plastic Small Outline Package (EIAJ)	GPC STN	DRAWING NO. 8S4	REV. B

11.2 8MA1 – UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

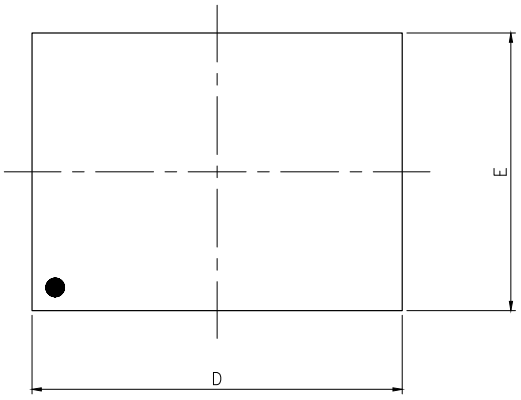
SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

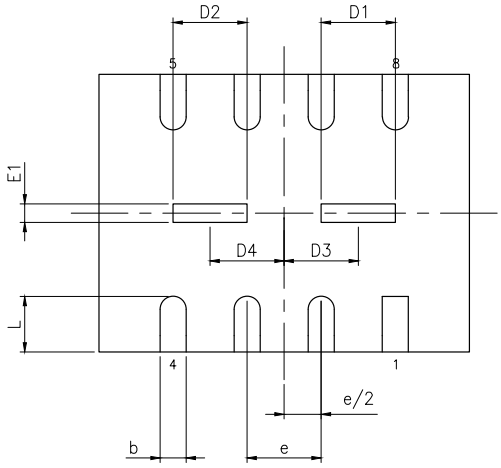
4/15/08

Adesto **Package Drawing Contact:** contact@adestotech.com	TITLE 8MA1, 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	GPC YFG	DRAWING NO. 8MA1	REV. D

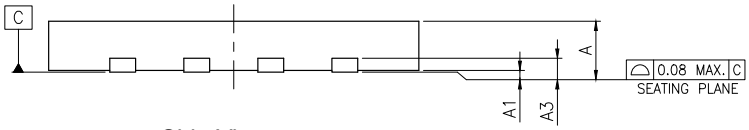
11.3 8MA2 – USON



Top View



Bottom View



Side View

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

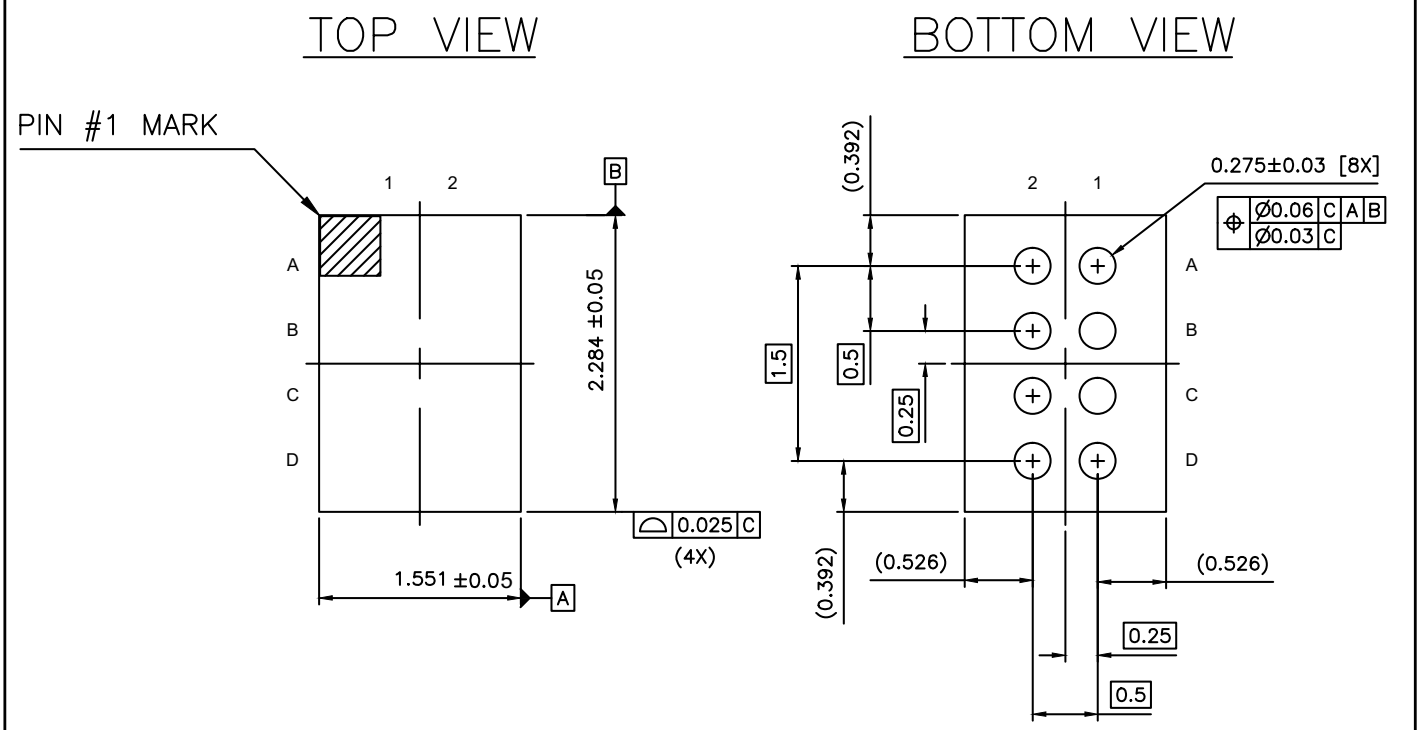
JEDEC OUTLINE	N/A		
PKG CODE	UDFN(W4OH)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	2.90	3.00	3.10
e	0.80 BSC		
L	0.55	0.60	0.65

PAD SIZE	D1			D2			D3			D4			E1			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
24X11* MIL	0.70	0.80	0.90	0.70	0.80	0.90	0.80 BSC			0.80 BSC			0.10	0.20	0.30	V	X	N/A

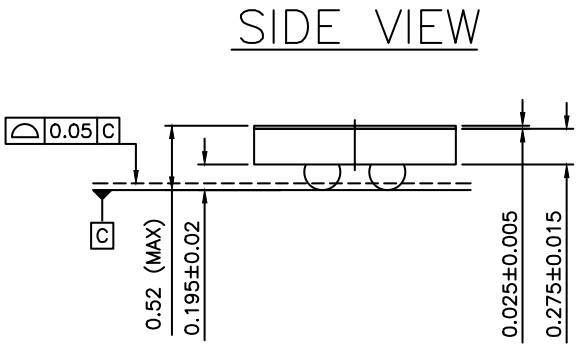
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Adesto Package Drawing Contact: contact@adestotech.com	TITLE 8MA2, 8-pad (3 x 4 x 0.55 mm Body), Thermally Enhanced Plastic Ultra Thin Small Outline No Lead Package (USON)	GPC YFG	DRAWING NO. 8MA2	REV. A

11.4 8-WLCSP — Die Ball Grid Array



ALL DIMENSIONS ARE IN MM



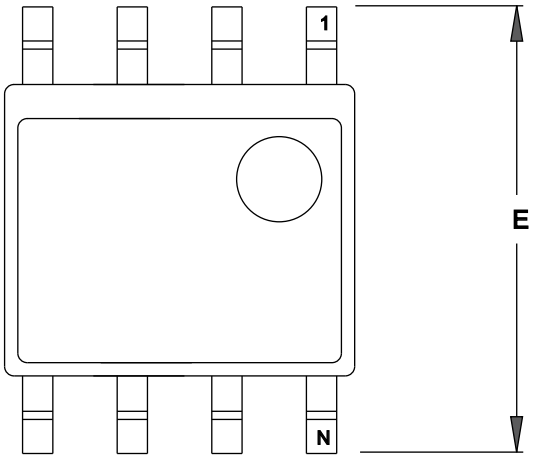
Pin Assignment Matrix

	A	B	C	D
1	V_{CC}	$I/O_3(\overline{HOLD})$	SCK	I/O_0(SI)
2	$\overline{CS}$	I/O_1(SO)	$I/O_2(\overline{WP})$	GND

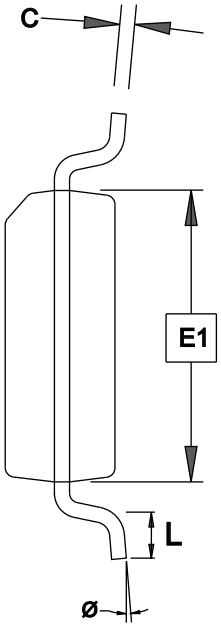
1/4/2017

Adesto Package Drawing Contact: contact@adestotech.com	TITLE 8WLCSP, 8-ball, die Ball Grid Array	GPC	DRAWING NO. 8WLCSP-A	REV. C

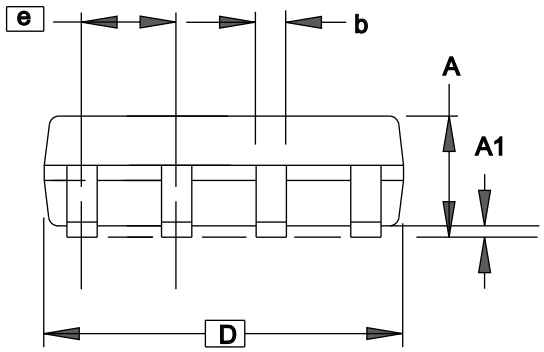
11.5 8S1 - 8-Lead 150-mil JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

5/19/10

Adesto **Package Drawing Contact:** contact@adestotech.com	**TITLE** **8S1, 8-lead (150 mil Narrow Body),** Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** F

12. Revision History

Revision	Date	Change History
A	06/2016	Initial release of AT25SL321A datasheet.
B	08/2016	Updated 8-WLCSP package outline drawing. Added 10-WLCSP package. Updated voltage range. Removed Sector and Block Protect descriptions. Removed Status Register Memory Protection tables. Updated tCSH specification.
C	10/2016	Updated UDFN package drawing and dimensions. Added USON package drawing and dimensions. Updated command description for 50h. Updated SFDP tables.
D	11/2016	Updated SFDP tables (to version 1.6).
E	02/2017	Updated Note 1 on Table 8.1.
F	03/2017	Updated document status from Advanced to Complete.
G	6/2020	Corrected Figure 7-50, Word Read Quad I/O. Updated text in Sections 7.25, 7.26, and 7.27 for clarity (no technical changes). Updated legal page. Changed ordering code from AT25SL321-MBUE-T to AT25SL321-MBUEKE-T.
H	10/2020	Removed references to the following packages: 24CC BGA, 10-ball WLCSP. Removed references to Die Wafer Form. Added 8S1, 8-lead 150-mil SOIC references and package drawing.

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