## General description

The SC14CVMDECT SF is a member of the Cordless Module family with integrated radio transceiver and baseband processor in a single package. It is designed for hosted and embedded cordless voice and data applications in the DECT frequency band. Its simple to use API commands allow easy setup of a wireless link between two or more nodes.

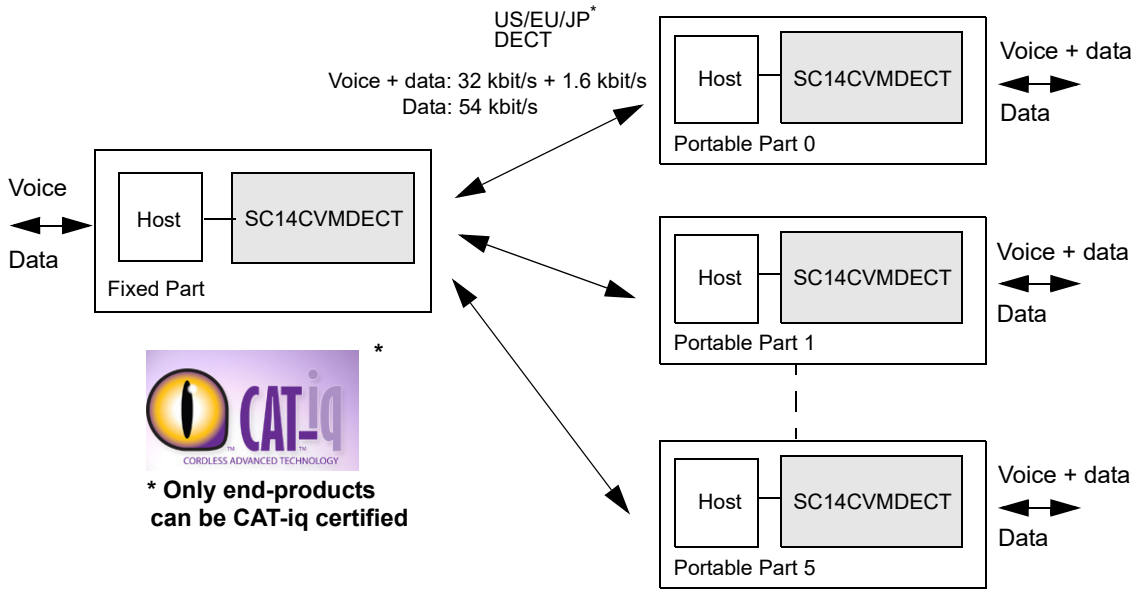
## Features

- Supports EU-DECT (CAT-iq V2.0, v3.0 partly), DECT6.0 for North America and Japan DECT
- ETSI (EU-DECT) and FCC (DECT 6.0) certified
- J-DECT pre-certified
- ETSI 300 444 (DECT GAP) compliant
- Up to 64 Portable Parts or ULE devices registered per Fixed Part
- UART interface to external host
- Controllable via API command set
- Supports voice and data
- RF range: 1870 MHz to 1930 MHz
- Receiver sensitivity < -93 dBm
- Transmit power
  - EU: 23 dBm: 1881 MHz - 1897 MHz
  - USA: 20 dBm: 1921 MHz - 1928 MHz
  - JP: 23 dBm: 1895 MHz - 1903 MHz
- Antenna embedded, supports external antennas
- Contains both PP and FP functionality
- Program memory available for custom software
- Supports both internal and external (hosted) applications
- Power supply voltage: 2.1 V to 3.45 V
- Supports NiMH and Alkaline batteries
- Small form factor (19.6 mm x 18.0 mm x 2.7 mm)
- Operating temperature range: -40 °C to +85 °C

## Applications

- Cordless intercom
- Cordless baby monitor
- Wireless data applications up to 54 kbit/s
- FP supports ULE sensors and actuators

## System diagram



# Table of Contents

# Table of Contents

## 1.0 Connection diagram

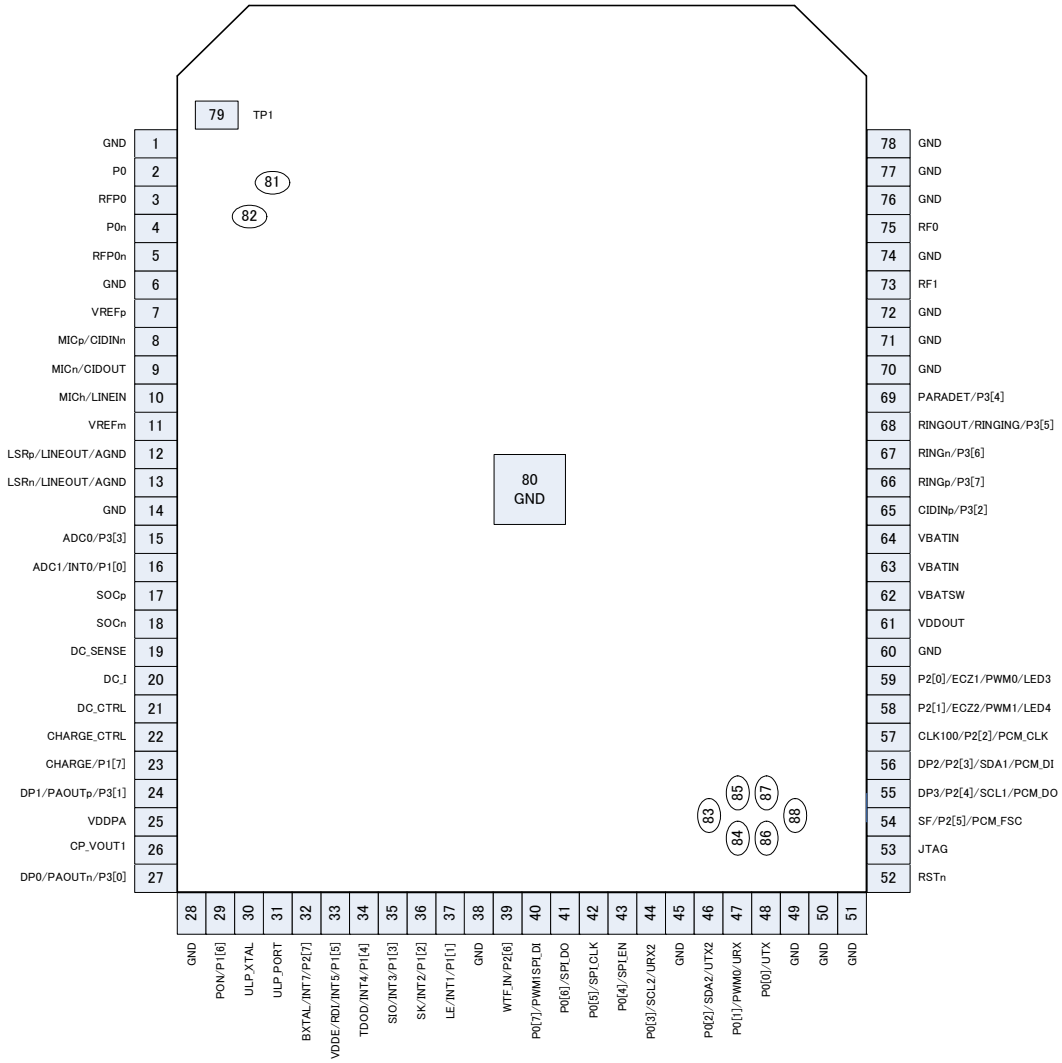



**Figure 1: Connection diagram (top view, leads face down)**

**Table 1: Ordering information**

| Part number | Package | Size (mm) | Shipment form | Pack quantity |
|---|---|---|---|---|
| SC14CVMDECT SF01T **(Note 2)** | MOD88 | 18 x 19.6 | Tray | 60 **(Note 1)** |
| SC14CVMDECT SF02T **(Note 3)** | MOD88 | 18 x 19.6 | Tray | 60 **(Note 1)** |

**Note 1:** MOQ = 600 pcs.
**Note 2:** Up to 6 PPs can be registered.
**Note 3:** Up to 64 PPs can be registered.

### 1.1 PIN DESCRIPTION

**Table 2: Pin description**

| Pin | Module Pin name (Note 4) | In/ Out | Iout Drive (mA) | Reset State (Note 5) | Description |
|---|---|---|---|---|---|
| 1 | GND | - | - | - | Ground |
| 2 | P0 | O | 8 | Hi-Z | Control port for FAD. See 4.13 |
| 3 | RFP0 | O | 8 | Hi-Z | Control port for FAD. See 4.13 |
| 4 | P0n | O | 8 | Hi-Z | Control port for FAD. See 4.13 |
| 5 | RFP0n | O | 8 | Hi-Z | Control port for FAD. See 4.13 |
| 6 | GND | - | - | - | Ground |
| 7 | VREFp | O | - | I | Positive microphone supply voltage |
| 8 | MICp | I | - | I | Positive microphone input |
| 9 | MICn | I | - | I | Negative handset microphone input |
| 10 | MICh | I | - | I | Headset microphone input with fixed input protection |
| 11 | VREFm | - | - | - | Negative microphone reference (star point), connect to GND. |
| 12 | LSRp | O | - | O | Positive loudspeaker output |
| 13 | LSRn | O | - | O | Negative loudspeaker output |
| 14 | GND | - | - | - | Ground |
| 15 | P3[3] | IO | 8 | I | I/O Port |
| 16 | P1[0] | IO | 2 | I-PU | I/O Port |
| 17 | SOCp | I | - | I | Battery state of charge positive input. Connect to GND if not used. See 4.9 |
| 18 | SOCn | I | - | I | Battery state of charge negative input. Star point connected to the SOC resistor. Connect to GND if not used. See 4.9 |
| 19 | DC_SENSE | I | | I | Voltage sense input. Connect to GND if not used. |
| 20 | DC_I | I | | I | Current sense input of DC/DC converter. Connect to GND if not used |
| 21 | DC_CTRL | O | 2 | O-0 | Switching clock for the DC/DC converter. |
| 22 | CHARGE_CTRL | O | 1 | O-0 | Charge control pin. Leave unconnected if not used. See 4.9 |
| 23 | CHARGE | I | - | I-PD (270k fixed pull-down) | Charger connected indication. Switches on the device if voltage > 1.5 V. Must be connected to charger via resistor R > (Vcharger_max-3 V)/10 mA (round to next largest value in range). See 4.9 |
| 24 | PAOUTp | IO | 500 | O-0 (5k fixed pull-down) | CLASSD loudspeaker positive outputs |
| 25 | VDDPA | I | - | - | CLASSD Audio Amplifier supply voltage up to 3.45 V. GND or leave unconnected if CLASSD Audio Amplifier is not used. |
| 26 | CP_VOUT1 | O | - | I | Charge Pump Output 1. A capacitor of 1 µF to GND is internally connected to this pin. |
| 27 | PAOUTn | IO | 500 | O-0 (5k fixed pull-down) | CLASSD loudspeaker positive output |
| 28 | GND | - | - | - | Ground |

**Table 2: Pin description (Continued)**

| Pin | Module Pin name (Note 4) | In/ Out | Iout Drive (mA) | Reset State (Note 5) | Description |
|---|---|---|---|---|---|
| 29 | PON | I | - | I (270k fixed pull-down) | Power on, Switches on the device if Voltage > 1.5 V.<br>May be directly connected to VBAT, also with Li-Ion batteries.<br>After startup the software takes over then PON pin to keep the device on after which the PON pin may be released. |
| 30 | ULP_XTAL | I | - | I | 32.768 kHz XTAL clock input. Connect to GND if not used. (Note 6) |
| 31 | ULP_PORT | I | - | I | Ultra Low Power Port Pin. Connect to GND if not used. (Note 6) |
| 32 | P2[7] | IO | 8 | I-PU | I/O port |
| 33 | P1[5] | IO | 8 | O-1 | I/O Port |
| 34 | P1[4] | IO | 1/2 | I-PD | I/O port |
| 35 | P1[3] | IO | 1/2 | I-PD | I/O Port |
| 36 | P1[2] | IO | 2 | I-PD | I/O Port |
| 37 | P1[1] | IO | 2 | I-PU | I/O Port |
| 38 | GND | - | - | - | Ground |
| 39 | P2[6] | IO | 2 | I-PU | I/O port |
| 40 | P0[7] / SPI_DI | IO | 8 | I-PU | I/O Port<br>SPI Data Input |
| 41 | P0[6] / SPI_DO | IO | 8 | I-PU | I/O Port<br>SPI Data Out |
| 42 | P0[5] / SPI_CLK | IO | 8 | I-PU | I/O Port<br>SPI Clock |
| 43 | P0[4] / SPI_EN | IO | 8 | I-PU | I/O port<br>SPI_EN: Active low. |
| 44 | P0[3] / SCL2 / URX2 | IO | 8 | I-PU | I/O port<br>Access bus clock, UART Serial In. |
| 45 | GND | - | - | - | Ground |
| 46 | P0[2] / SDA2 / UTX2 | IO | 8 | I-PU | I/O port<br>Access bus data, UART Serial Out. |
| 47 | P0[1] / URX | IO | 8 | I-PD (10k) | I/O port<br>UART Serial In |
| 48 | P0[0] / UTX | O | 8 | I-PU | I/O Port<br>UART Serial Out |
| 49 | GND | - | - | - | Ground |
| 50 | GND | - | - | - | Ground |
| 51 | GND | - | - | - | Ground |
| 52 | RSTn | I | 1 | I-PU (200k) | Active low Reset input with Schmitt-trigger input, open-drain output. Input may not exceed 2.0 V. An internal capacitor of 47 nF is mounted on this pin. |
| 53 | JTAG | IO | 8 | I-PU (1k) | JTAG-SDI+; one wire Debug interface with open-drain. |
| 54 | P2[5]/PCM_FSC | IO | 8 | I-PU | I/O Port<br>PCM_FSC: PCM Frame Sync |
| 55 | P2[4]/SCL1/ PCM_DO | IO | 8 | I-PU | I/O port<br>SCL1; I2C clock<br>PCM_DO: PCM Data output |

**Table 2: Pin description (Continued)**

| Pin | Module Pin name (Note 4) | In/ Out | Iout Drive (mA) | Reset State (Note 5) | Description |
|---|---|---|---|---|---|
| 56 | P2[3]/SDA1 / PCM_DI | IO | 8 | I-PU | I/O Port<br>SDA1: I2C Data<br>PCM_DI: PCM Data input |
| 57 | P2[2]/PCM_CLK | I/O | 8 | I-PD | I/O Port<br>PCM_CLK: PCM clock input/output |
| 58 | P2[1] / PWM1 / LED4 | IO | 8 | I | I/O Port<br>PWM1: Pulse Width Modulation output<br>LED4: 2.5 mA/5 mA LED current sink |
| 59 | P2[0]/ PWM0 / LED3 | IO | 8 | I | I/O Port<br>PWM0: -<br>LED3: 2.5 mA/5 mA LED current sink |
| 60 | GND | - | - | - | Ground |
| 61 | VDDOUT | - | - | - | Test purpose only. Must be left unconnected. |
| 62 | VBATSW | | | | Test purpose only. Must be left unconnected. |
| 63 | VBATIN | I | - | - | Main supply voltage < 3.45 V. |
| 64 | VBATIN | I | - | - | Main supply voltage < 3.45 V. |
| 65 | P3[2] | IO | 8 | I | I/O Port |
| 66 | P3[7] | IO | 4 | I | I/O Port |
| 67 | P3[6] | IO | 4 | I | I/O Port |
| 68 | P3[5] | IO | 4 | I | I/O Port |
| 69 | P3[4] | IO | 8 | I | I/O Port |
| 70 | GND | - | - | - | Ground |
| 71 | GND | - | - | - | Ground |
| 72 | GND | - | - | - | Ground |
| 73 | RF1 | - | - | - | RF signal for external antenna. See 4.13 |
| 74 | GND | - | - | - | Ground |
| 75 | RF0 | - | - | - | RF signal for external antenna. See 4.13 |
| 76 | GND | - | - | - | Ground |
| 77 | GND | - | - | - | Ground |
| 78 | GND | - | - | - | Ground |
| 79 | TP1 | - | - | - | Tuning point for internal antenna. Follow instructions of Section 8.5. |
| 80 | GND | - | - | - | Ground |
| 81-88 | TP2 to TP9 | NC | | | Must be left unconnected. See section 8.3.2 and Figure 36. |

**Note 4:** "NC" means: leave unconnected.
"GND" means internally connected to the module ground plane. Every GND pin should be connected to the main PCB.ground plane.

**Note 5:** All digital inputs have Schmitt trigger inputs. After reset all I/Os are set to input and all pull-up or pull-down resistors are enabled unless otherwise specified.
PU = Pull-up resistor enabled, PD = Pull-down resistor enabled, I = input,
O = output, Hi-Z = high impedance, 1 = logic HIGH level, 0 = logic LOW level
Refer also to Px_DIR_REGs for INPUT/OUTPUT and Pull-up/Pull-down configurations

**Note 6:** All ULP pins use snap-back devices as ESD protection, which (when triggered) have a holding voltage below the typical battery voltage. This means that the snap-back device of a ULP pin may remain conductive, when triggered while the pin is directly connected to the battery voltage. If any of the ULP pins are directly or indirectly electrically accessible on the outside of the application, system level ESD precautions must be taken to ensure that the snap-back device is not triggered while in active mode, to prevent the chip from being damaged.

# 2.0 Introduction

## 2.1 SCOPE

The SC14CVMDECT SF is a programmable DECT module for voice and data services. The internal software stack receives commands and data from the application, for instance to set up a link to other modules. The application software can be implemented on the module itself or on an external host processor. The internal FLASH provides user space where custom applications can be located.

The module converts analog signals to a digital stream, compresses/decompresses them according to the DECT standards and transmits/receives them over the air interface. The DECT protocol stack in each module supports both PP and FP functionality.

The embedded software running on the internal microcontroller (CR16) supports all protocol layers up to the network layer. The module can be controlled by software running on the internal controller as well as from an external controller via the UART.

## 2.2 REFERENCES

1. CVM FP API Documentation package.
2. CVM PP API Documentation package.
3. Athena Eclipse User Manual, v1.02, Dialog Semiconductor, Cordless Software and Tools.
4. SC14CVMDECT EEPROM (VES) map for PP (NatalieV3PpCvm Eeprom_vXXXX.html).
5. AN-D-174, SC14480 Battery Management; using the State of Charge function, Application Note, Dialog Semiconductor.
6. AN-D-212, SC14CVMDECT_SFxx_DB External Antenna Design and Leveraging Modular Approval, Application Note, Dialog Semiconductor.
7. AN-D-222, SC14CVMDECT production pairing, Application Note, Dialog Semiconductor.

## 2.3 GLOSSARY AND DEFINITIONS

| | |
|---|---|
| AFE | Analog Front End |
| API | Application Programming Interface |
| Baby monitor | Same as intercom but optionally voice activated |
| CAT-iq | Cordless Advanced Technology, Internet and Quality |
| CODEC | COder and DECoder |
| CoLA | Co-Located Application |
| Conference | Same as intercom, but including an external party |
| CRC | Cyclic Redundancy Check |
| CVM | Cordless Voice Module |
| DECT | Digital Enhanced Cordless Telephone |
| DSP | Digital Signal Processor |
| EMC | Equipment Manufacturer's Code |
| ESD | ElectroStatic Discharge |
| FAD | Fast Antenna Diversity |
| FP | Fixed Part |
| GAP | Generic Access Profile (DECT) |
| GFSK | Gaussian Frequency Shift Keying |
| HPM | High Power Mode |
| Inband tones | Tones played by the application itself and not from external e.g. line. |
| Intercom | Internal call between FP and PP(s) |
| IPEI | International Portable Equipment Identity (ETSI EN 300 175-6) |
| IWU | InterWorking Unit (ETSI EN 300 175-1) |
| LCD | Liquid Crystal Display |
| LDO | Low Drop Out (regulator) |
| LDR | Low Data Rate |
| LPM | Low Power Mode |
| MCU | Micro Controller Unit |
| MMI | Man Machine Interface (keypad, LCD, buzzer, microphone, earpiece, etc.) |
| NTP | Normal Transmitted Power |
| PAEC | Perceptual Acoustic Echo Canceller |
| PC | Personal Computer, IBM compatible |
| PCB | Printed Circuit Board |
| PP | Portable Part |
| PSTN | Public Switched Telephone Network |
| RF | Radio Frequency |
| RFPI | Radio Fixed Part Identity (ETSI EN 300 175-6) |
| RLR | Receive Loudness Rating |
| RSSI | Radio Signal Strength Indication (ETSI EN 300 175-1) |
| Sidetone | Feedback of microphone signal to earpiece |
| SLR | Sending Loudness Rating |
| SPI | Serial Peripheral Interface Bus |
| UART | Universal Asynchronous Receiver and Transmitter |
| ULE | Ultra Low Energy |
| VAD | Voice Activity Detection |
| VES | Virtual EEPROM Storage |
| Walkie Talkie | Call between two PPs without an FP |

## 3.0 Cordless Voice Module functions

This section describes the key functions and features supported by the SC14CVMDECT SF as shown in Figure 2.

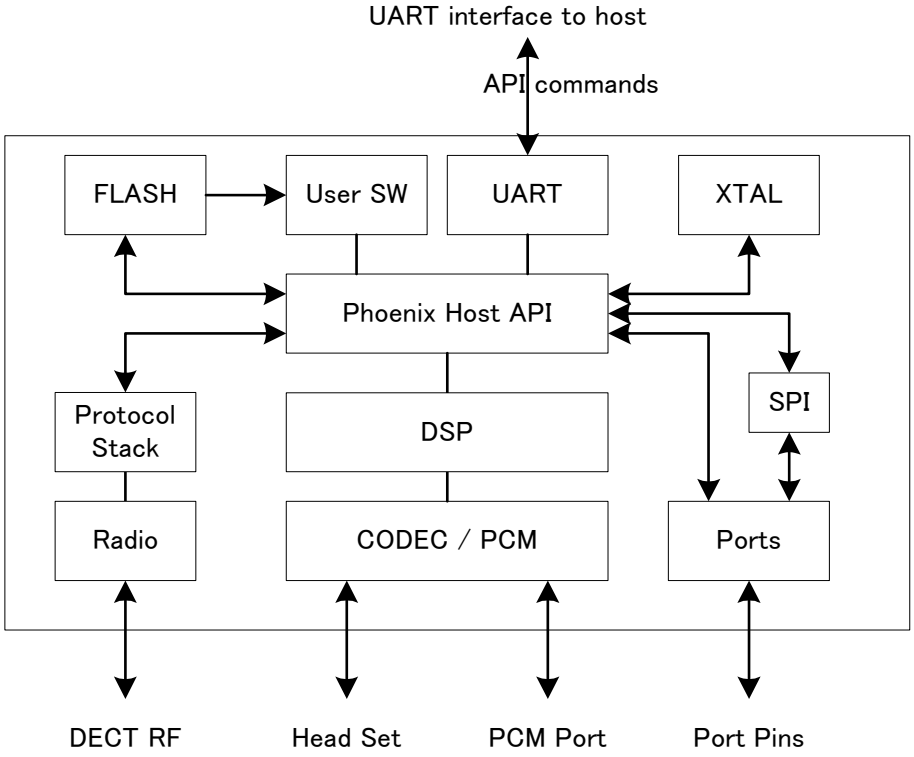



**Figure 2: SC14CVMDECT SF functional overview**

### 3.1 MODULE HARDWARE

The SC14CVMDECT SF internal hardware consists of:

- An internal microprocessor is running from FLASH and handles the API call coming from UART or embedded user software.
- A 4 kB VES (Virtual EEPROM Storage) used by the protocol stack and for user variables.
- A DSP for the audio signal processing like ADPCM voice compression towards the CODEC.
- A CODEC converts the analog signals to digital signals and vise versa.
- Input/Output ports which can be toggled high/low as an output or a high/low digital level can be read as an input.
- A 20.736 MHz XTAL. This crystal is automatically tuned by the PP module software for optimal radio performance.
- Voltage regulators convert the external supply voltage (VBAT) to stable supply voltages for the core and the I/Os.
- A DECT radio transceiver with a built-in antenna circuit. The antenna itself is integrated into the module, relieving the product designer from RF expertise.
- A full duplex UART for communication with an optional host processor.

### 3.2 SOFTWARE CONTROL

The application software is written by the customer and has to manage the call control and also the MMI functions. The supported API software includes the Network layer that is defined in figure 1 of the EN300 175-3 document, which describes the DECT protocol stack. Detailed functions and data flows, including some example sequences, can be found in document reference [1] for FP and [2] for PP.

The default configuration of the SC14CVMDECT SF module software is: US DECT, FP and CoLA enabled.

### 3.3 DECT PROTOCOL STACK

The SC14CVMDECT SF internal protocol stack is based on the ETSI DECT specifications and is compliant with ETSI 300 444 (GAP).

The product supports up to 6 DECT GAP compliant PP units to one FP station.

### 3.4 PORTABLE PART CONFIGURATION

A Portable Part configuration with SC14CVMDECT SF requires additional external parts as shown in Figure 3.

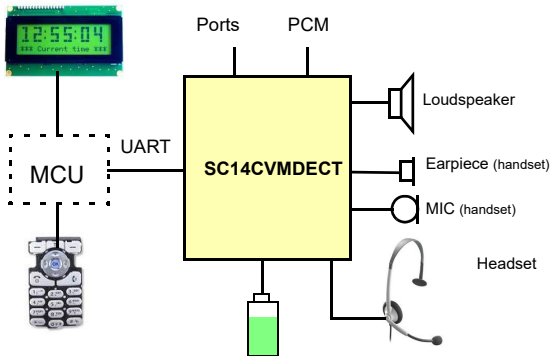



**Figure 3: PP configuration**

Table 3 provides an overview of the supported interfaces for a portable part.

**Table 3: PP support overview**

| Item | Supported | Remark |
|---|---|---|
| Battery management | Yes | Supported by API |
| Keypad | No | On external MCU |
| Display | No | On external MCU |
| I/O Ports | Yes | All digital I/O port pins can be controlled by API |
| PCM interface | Yes | 1x 16 bits serial I/O, PCM_FSC 8 kHz/16 kHz |
| UART | Yes | 115.2 kbit/s, used for API-commands |
| Headset detection | Yes | Supported by API |
| LSR (Earpiece, headset) | Yes | Connected to LSRp and/or LSRn<br>supports single-end and differential **(Note 7)** |
| MIC (Earpiece, headset, handsfree) | Yes | Connected to MICp and/or MICn and/or MICh<br>supports single-ended and differential **(Note 7)** |
| Handsfree speaker | Yes | Connected to PAOUTp/n **(Note 7)** |
| Radio | Yes | Integrated single antenna and support for external antenna(s) |

**Note 7:** AFE setting is configurable, refer to document [2].

### 3.5 FIXED PART CONFIGURATION

A Fixed Part configuration with SC14CVMDECT SF requires additional external parts as shown in Figure 4.

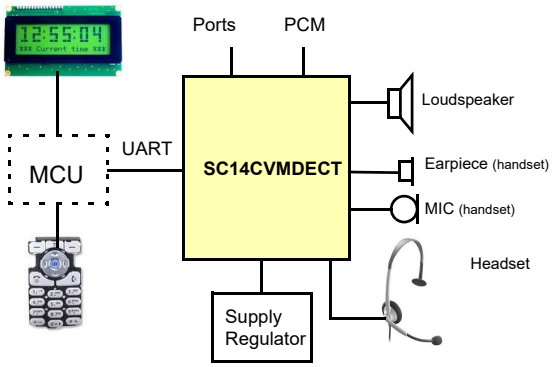



**Figure 4: FP configuration**

Table 4 provides the overview of required and available interfaces for a basic or a feature rich cordless FP with the SC14CVMDECT SF.

**Table 4: FP support overview**

| Item | Supported | Remark |
|---|---|---|
| Supply Regulator | No | Use external 3.3 V LDO |
| Keypad | No | On external MCU |
| Display | No | On external MCU |
| I/O Ports | Yes | All digital I/O port pins can be controlled via API |
| PCM interface | Yes | 4x 16 bits serial I/O, PCM_FSC 8 kHz/16 kHz |
| UART | Yes | 115.2 kbit/s, used for API-commands |
| Headset detection | No | Not supported by API |
| LSR (Earpiece, headset) | Yes | Connected to LSRp and/or LSRn<br>supports single-end and differential **(Note 8)** |
| MIC (Earpiece, headset, handsfree) | Yes | Connected to MICp and/or MICn and/or MICh<br>supports single-end and differential **(Note 8)** |
| Handsfree speaker | Yes | Connected to PAOUTp/n **(Note 8)** |
| PSTN Line interface | No | Not supported by API |
| Radio | Yes | Integrated single antenna and support for external antenna(s) |

**Note 8:** AFE setting is configurable, refer to document [1].

### 3.6 VOICE COMMUNICATION

An FP supports up to 64 registered PPs, where 4 of these PPs can be in a call at the same time. Multiple simultaneous calls are supported. Supported voice codec is G.726 (32 kbit/s ADPCM) and G.722 (64 kbit/s ADPCM). See Figure 5.

### 3.7 LIGHT DATA APPLICATION

The SC14CVMDECT SF supports Low Data Rate (LDR) transmission up to 1.6 kbit/s with IWU to IWU messaging. The LDR can be used in combination with voice communication. See Figure 5.

### 3.8 LU10 DATA APPLICATION

The SC14CVMDECT SF supports CAT-iq LU10 data transmission up to 54 kbit/s. Since LU10 data communication uses the B-Field it cannot be used in combination with voice communication. See Figure 6.

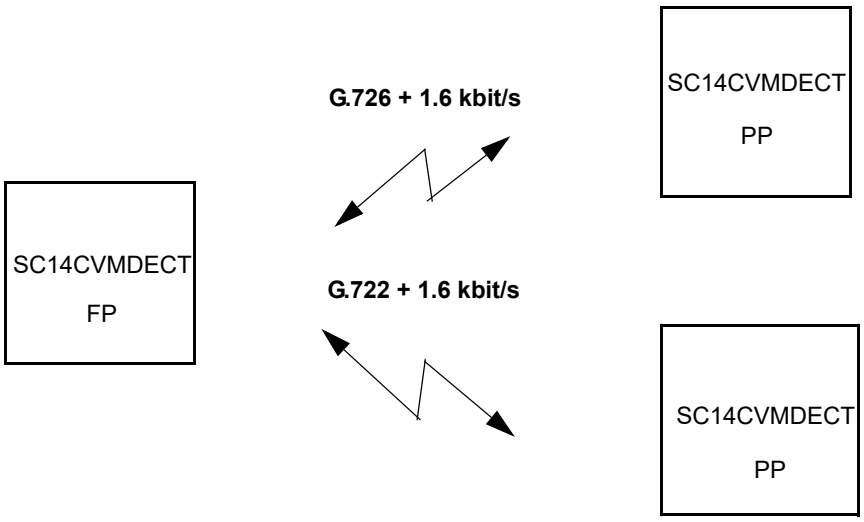



**Figure 5: Voice and LDR data communication**

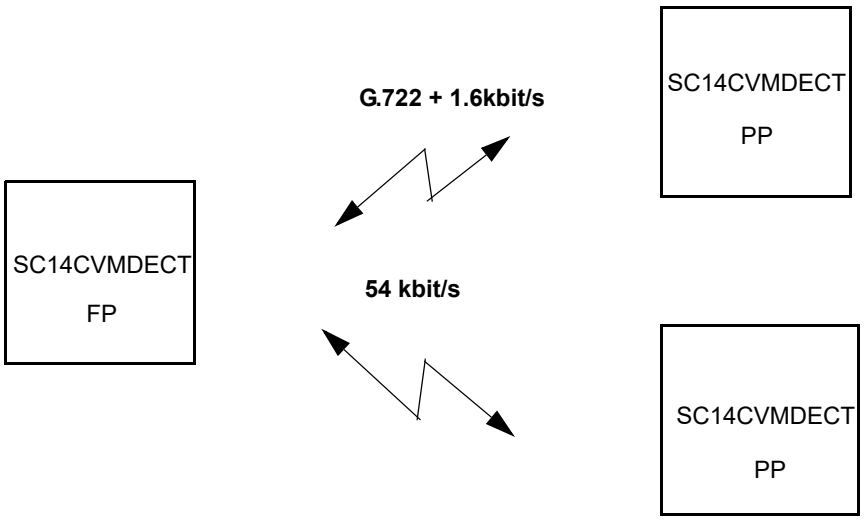



**Figure 6: LU10 data application**

### 3.9 GENERAL FEATURES

**Table 5: Supported general features**

| Functionality (Note 9) | PP support | FP support | Remark |
|---|---|---|---|
| **Call handling** | | | |
| Conferencing | - | Yes | Call between FP and 4x PP |
| Intercom | Yes | Yes | Call between FP and 4x PP |
| Walkie Talkie mode | Yes | - | Call between PP and PP without FP |
| Baby monitor | Yes | - | Voice Activated PP. See document reference [2] |
| Voice over PCM interface | Yes | Yes | µ-law (64 kbit/s), A-law (64 kbit/s), G.726 ADPCM (32 kbit/s), G.722 ADPCM (64 kbit/s), Linear (128 kbit/s) |
| Call transfer | Yes | Yes | Transfer call between PPs on FP |
| Page call | Yes | Yes | FP pages all PPs (PP locator) |
| **Protocol** | | | |
| Manual registration | Yes | Yes | |
| Wire registration | Yes | Yes | See document reference [7] |
| Number of CVM PP registrations per FP | - | Yes | 1 to 6 for SF01 |
| | | | 1 to 64 for SF02 **(Note 10)** |
| Number of ULE PP registrations per FP | - | Yes | 1 to 180 for SF01 |
| | | | 1 to 64 for SF02 **(Note 10)** |
| **Audio and tone** | | | |
| Microphone mute | Yes | Yes | |
| Tone generation | Yes | No | Melody generator with 7 polyphonic tones |
| Audio Volume control | Yes | Yes | |
| Tone Volume control | Yes | No | |
| Headset support | Yes | Yes | |
| Handsfree/Speakerphone | Yes | No | |
| **General** | | | |
| Real time clock | Yes | Yes | Accuracy depending directly on crystal |
| Real time clock synchronization | Yes | Yes | All PP clocks are kept in synchronization with the FP |
| SW EEPROM (VES) Storage | Yes | Yes | Internal on module |
| Battery Charge Management | Yes | No | |
| PSTN line interface support | - | No | PSTN software on request |
| I/O port support | Yes | Yes | |
| Port Interrupt support | No | No | |
| Automatic headset detection | Yes | No | |
| Low speed data | Yes | Yes | 1.6 kbit/s |
| LU10 data channel | Yes | Yes | 54 kbit/s **(Note 11)** |
| CAT-iq up to version 2.0, 3.0 | Yes | Yes | |

**Note 9:** These features can be supported by combined API commands in user software.
**Note 10:** The number of PP registrations includes both CVMDECT PP and ULE PP devices.
**Note 11:** SF02 supports one channel LU10 simultaneously.

# 4.0 Functional description

## 4.1 UART INTERFACE

The UART is normally used for API commands, but can also be used for software upgrades and debugging.

The UART is a full duplex UART with frame type:

1 start bit,
8 data bits (LSB first),
1 stop bit,
no parity,
up to 115.2 kBd.

The UART hardware interface uses only TX/RX (see Figure 7).

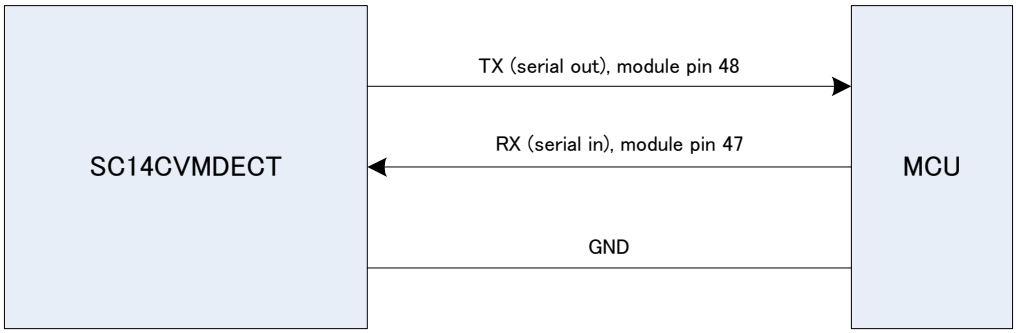



**Figure 7: UART hardware configuration**

**Caution:** All UART signals are 1.8 V, input max. 3.45 V (see Table 18, Table 21 and Table 22). An external V.24 line driver must be provided if the UART port of the module is connected to a standard V.24 device (±12 V). Connecting the module without a driver may damage the module.

## 4.2 VES (VIRTUAL EEPROM STORAGE)

### 4.2.1 VES layout

The SC14CVMDECT SF PP and FP include a 4 kB VES which is divided into two areas (see Table 6).

**Table 6: VES map**

| VES space | Size | Usage |
|---|---|---|
| SC14CVMDECT SF | 3.6 kB | Used for RF, audio, battery, tone setup, data base, etc. |
| User | 0.4 kB | Can be used for MMI applications such as User information. |

VES is supported as virtual EEPROM with the internal FLASH.

A detailed overview of the VES parameters can be found in document reference [4].

Some parts of the VES parameters are read into the SC14CVMDECT SF during the start up and other parts are used by the SC14CVMDECT SF software during execution.

The VES parameters are divided into two types:

- Factory type
- Normal type

The “factory” type is specific for the SC14CVMDECT SF and should only be set by production. The “factory” type parameters are either adjustments used by the baseband or the radio interface, or are used to set up the SC14CVMDECT SF into special modes. The “factory” type parameters will only be modified by changing the factory programmed default value. See document reference [4].

The “normal” VES parameters can be reset to their default values via software.

### 4.2.2 VES access by MCU

The host is able to read or modify the VES parameters or limited free VES areas via API command.

### 4.3 AUDIO CONFIGURATIONS

The SC14CVMDECT SF audio supports standard DECT audio qualities. The audio gain and volume parameters are placed in the VES. The DECT gains can be adjusted to meet the TBR38 and TBR10 audio level requirements by using the SC14CVMDECT SF application reference design. For other line and acoustic designs it is required to adjust and tune the audio setup.

#### 4.3.1 Audio connection

The SC14CVMDECT SF PP audio connections are shown in Figure 8. Refer to "Example application diagram" on page 49 for detailed component values.

.

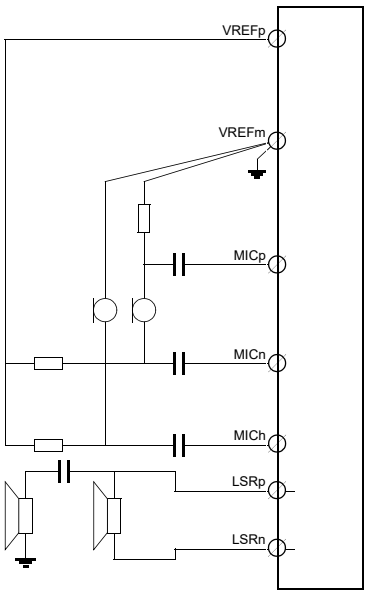



**Figure 8: Audio connections**

**Earpiece or small loudspeaker connection**

The earpiece loudspeaker can be connected either differentially or single-ended. Dynamic loudspeakers with an impedance of 30 Ω can be connected, as well as ceramic loudspeakers equivalent to 600 Ω and 30 µF. Refer to Table 28 for a detailed specification or the earpiece loudspeakers.

The earpiece is connected to the LSRp and LSRn pins.

**Microphone connection**

The microphone can be connected either single-ended via MICp or differentially to MICp and MICn.

**Headset connection**

The headset microphone must be connected to the MICh pin. The headset earpiece is connected to the LSRp.

**Microphone supply connection**

For active microphones a voltage source with high supply voltage rejection ratio is provided on supply pins VREFp/VREFm. Filtering of internal and external reference voltages is provided by an internal capacitor. No external capacitor shall be connected to pin VREFp. To avoid audible switching noise it is important that the ground supply signals are directly "star point" connected to the VREFm and **not** via a common ground plane. From this VREFm star point, one connection is made to the common ground plane.

**Loudspeaker connection**

For the handsfree operation a 4 Ω loudspeaker must be connected to the PAOUTp and PAOUTn pins as shown in Figure 9. The VDDPA is the supply pin.

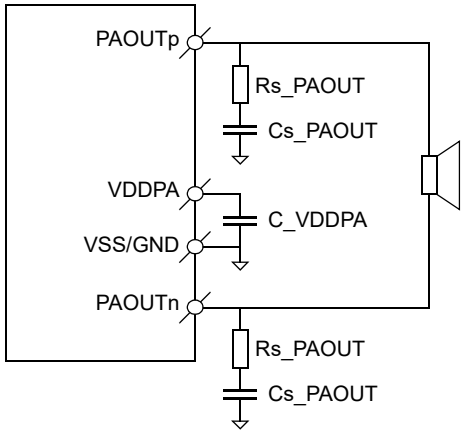



**Figure 9: Loudspeaker connection**

Refer to Table 31 for a detailed specification of the external components around the loudspeaker. These components are necessary to guarantee the lifetime of the module.

## 4.4 AUDIO ROUTING

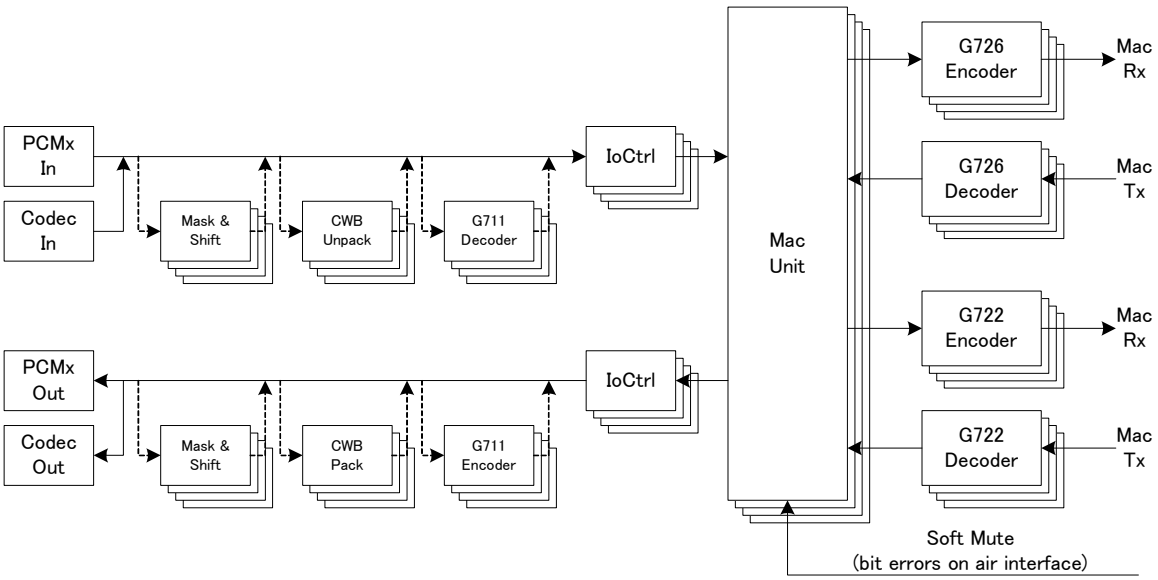



**Figure 10: FP audio routing**

### 4.4.1 FP audio routing

Figure 10 shows the audio routing for an FP. Input and output signals are supported both for the internal codec and the PCM, and the Air interface supports G.726 (32 kbit/s ADPCM) and G.722 (64 kbit/s ADPCM). The internal software supports up to 4 audio channels simultaneously. Supported sample rates are 8 kHz and 16 kHz.

FP does not support acoustic or line echo cancellation.

### 4.4.2 FP audio level adjustment

The internal codec audio levels can be controlled with the parameters MicGain and LsrGain.

The MicGain range is 0 to 30 dB in steps of 2 dB and a value of -128 will mute the input signal, default is 0 dB.

The LsrGain range is +2 dB to -12 dB in steps of 2 dB, default is +2 dB. See document reference[1].

### 4.4.3 PP audio routing

Figure 11 and Figure 12 show the different audio routing modes of a PP. Figure 11 shows an overall audio routing and Figure 12 shows the detailed audio routing for the speakerphone of PP (FP does not support speakerphone).

### 4.4.4 PP audio codec adjustment

The audio codec settings for the loudspeaker and microphone must be pre-configured in the VES for each mode. The VES parameter fields for

Audio.Earp.xxx
Audio.Heads.xxx
Audio.SpkPh.xxx

have a default value and maybe fine-tuned for the application. See document reference [4].

### 4.4.5 General audio adjustment

For each audio mode, the receive (RLR) and transmit (SLR) audio paths must be adjusted. RLR and SLR are adjusted in the registers in the VES for each audio state; see document reference [4]. Figure 13 shows this image.

### 4.4.6 PP volume

The PP supports 6 volume steps, which are VES configurable through parameter fields Audio.Earp.Vol.xxx, the Audio.Heads.Vol.xxx and Audio.SpkPh.Vol.xxx. The volume steps must be set initially in the VES during production; see document reference [4].

### 4.4.7 PP audio equalization

To enable adjustments of the frequency response the PP contains four programmable filters: 2 in RX direction and 2 in TX direction (see Figure 11).

By default these filters are loaded with bypass coefficients. These can be modified by loading new coefficients via API commands.

Equalizer filters are part of the audio routes for all audio modes and are placed as shown in Figure 11.

For a detailed description of the filter functionality refer to the API documentation; see document reference [2].

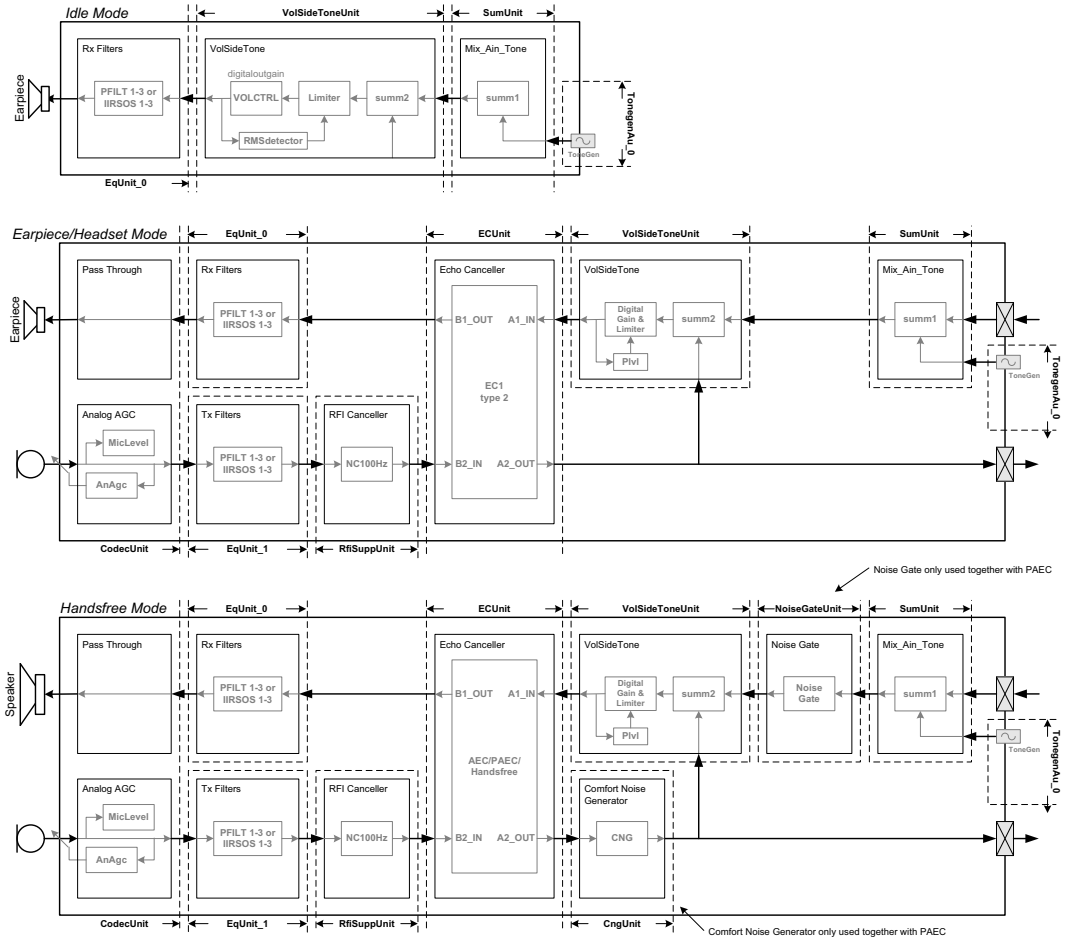



**Figure 11: PP audio routing**

.

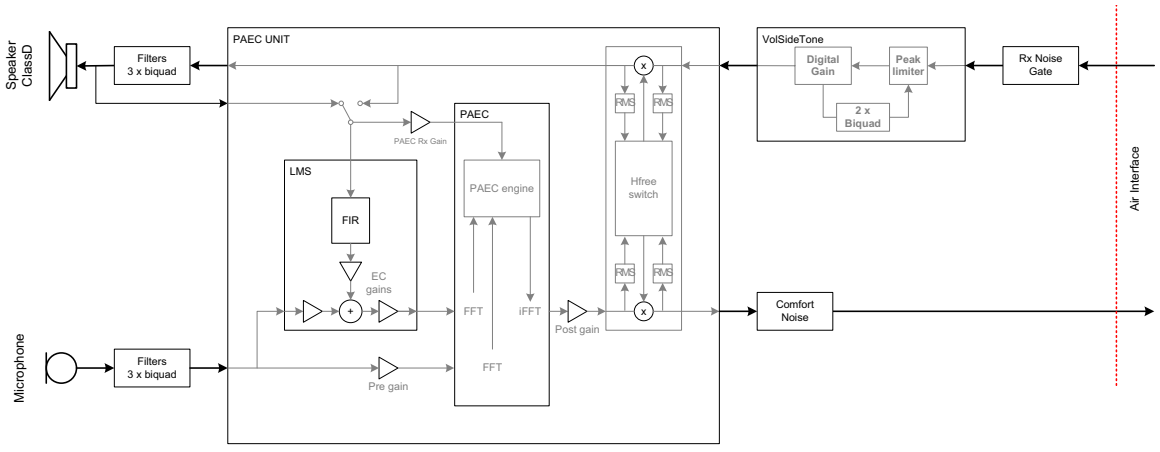



**Figure 12: Extended speakerphone for PP**

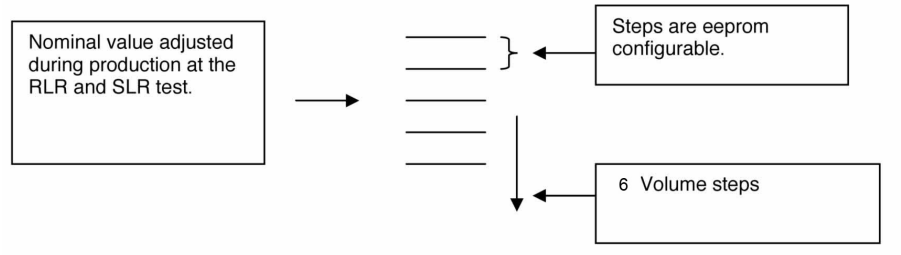



**Figure 13: Handset volume configuration**

### 4.5 PP AUDIO MODES

The PP audio handling consists of four audio states (see Figure 14). In these states the audio subsystem is configured for a certain audio mode:

1. Idle mode (not relevant for microphone configuration)
2. Earpiece mode (Handset speaker)
3. Handsfree or Speakerphone mode
4. Headset mode

Selection between the modes is done via API calls; see document reference [2].

The Alert state is for tone playing and is entered automatically when tones are played using the API calls. The Alert state can originate from idle, earpiece, handsfree or headset mode.

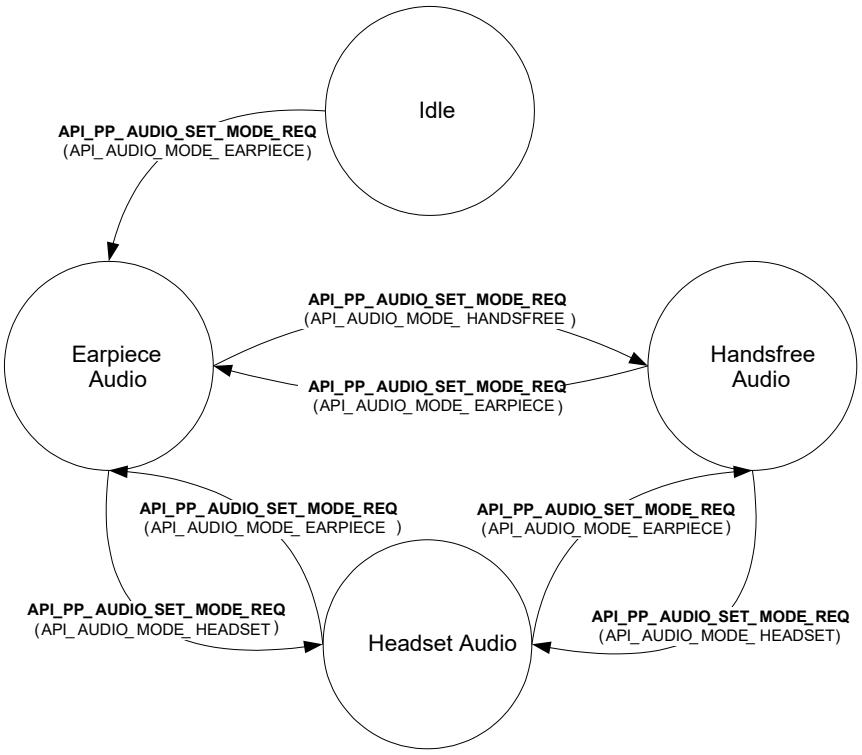



**Figure 14: PP audio modes**

#### 4.5.1 Power management

To minimize the current consumption the PP will shut down all codec amplifiers in Idle mode. This means that all reference voltages in the analog front-end will be disabled. This feature can be disabled in the VES if the reference voltages for some reasons are needed in Idle mode.

### 4.5.2 Earpiece mode

In Earpiece mode (Handset speaker) an artificial sidetone is generated. The level of the sidetone can be adjusted and setup in the VES through parameter fields Audio.Earp.Vol.Elementx, SideToneGain and Audio.Heads. Elementx.SideToneGain. In Earpiece mode it is possible to adjust the volume in the Earpiece via API calls. In Earpiece mode the PP audio is routed as shown in Figure 11.

### 4.5.3 Alert mode

The Alert mode is for generating tones and melodies on the Speakerphone loudspeaker. In Alert mode it is possible to adjust the volume in the speaker via API calls. Inband tones will be affected by the volume adjustments, since the volume control takes place after tones are added to the signal. Figure 11 shows the Audio flow.

## 4.6 CALL HANDLING

### 4.6.1 FP to PP call

When the FP initializes a call to a PP, a radio connection is set up to all PP applications to make it possible for the PP application software to indicate that there is an incoming call.

It is possible to configure the ringing indication using broadcast to make all 64 PPs ringing.

### 4.6.2 PP to FP call

When the MMI software signals the PP to establish a call, the PP opens the radio connection to the FP.

### 4.6.3 Intercom

Figure 15 shows the audio routing of an internal call between PP1 and PP2. In the FP no transcoding takes place.

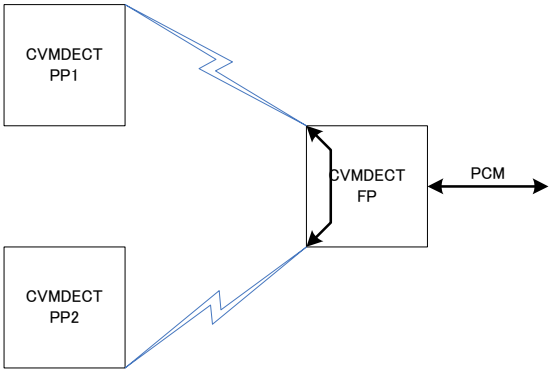



**Figure 15: Intercom connection**

### 4.6.4 Conference

Figure 16 shows the audio routing of a 9-party conference call.

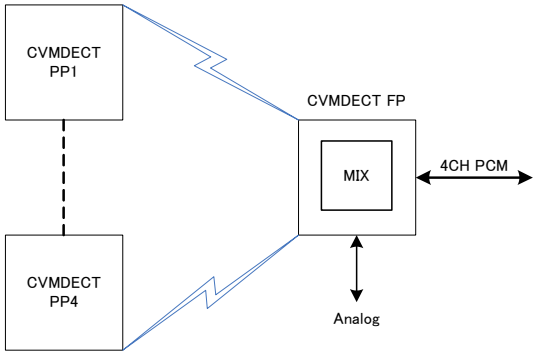



**Figure 16: Conference connection**

### 4.6.5 Page call

The Page call is an FP functionality used to locate the registered PPs. FP paging does not establish a normal audio connection and is terminated when answered by the PP.

## 4.7 TONE/MELODY HANDLING

The tone component handles the generation of various tones in the device. Both tones/melodies in a PP configuration are supported.

The main features of the tone component are:

- Ringer tones and melodies (7-tone polyphonic)
- Alert tones (key sound, error tones, confirmation tones, etc.)
- Inband tones (dial tone, net-congestion tone, busy tone, etc.)
- Single tone generation

## 4.8 DATE AND REAL-TIME CLOCK

The FP has a real-time clock feature, which (when activated) broadcasts the date and time of day to the PPs. Activation of the date and real-time clock is done by setting the date and time via the PP.

The clock supports hours, minutes and date. The date supports leap years. Daylight saving time is not supported and must be handled by the MMI application.

The PP clock is synchronized with the FP every time a broadcast is received. If the PP goes out-of-lock, the PP itself calculates the clock time until the PP is again within the range of the FP. The updated clock time can be read locally via the MMI software.

To adjust the clock in the FP, a service connection can be set up via commands from the PP.

The clock can also be read and set directly from an external microprocessor or through the MMI software on the FP.

The real-time clock accuracy depends directly on the SC14CVMDECT SF crystal.

When the SC14CVMDECT SF is configured as a PP, the clock has the same accuracy as the FP clock. When the PP synchronises with an FP, the PP crystal is synchronized with the FP crystal and the PP clock will change accordingly.

The accuracy is expected to be within 1 minute for up to 6 weeks without being locked to an FP.

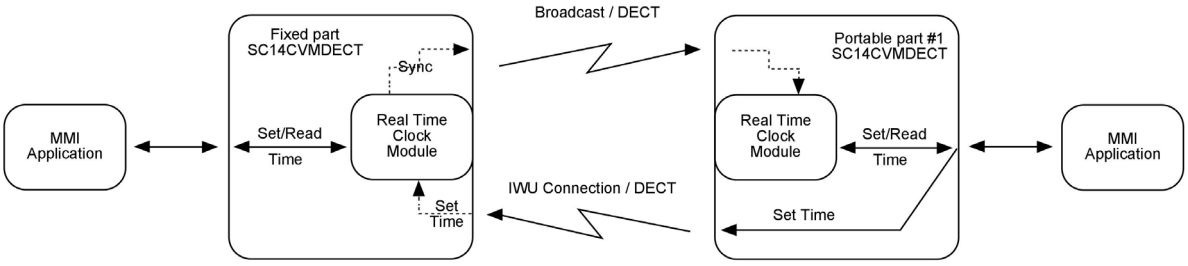



**Figure 17: Clock synchronization**

## 4.9 BATTERY MANAGEMENT

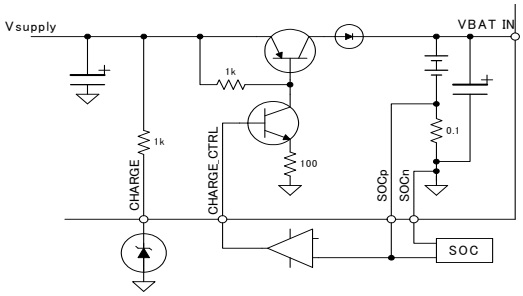



**Figure 18: Handset (PP) application with 2x NiMH**

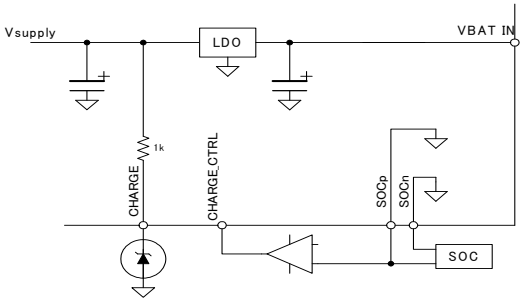



**Figure 19: Base station (FP) application**

Figure 18 shows a handset application with NiMH. SOC (State Of Charge) is used to measure the amount of charge in the rechargeable batteries.

Figure 19 shows an FP application. The FP uses an external LDO, so the SOC pins are not used and can be connected to GND.

The PP API supports battery management to calculate the battery capacity and to indicate charge status. Refer to API document [2].

The SOC circuit is used to very accurately determine the amount of charge in rechargeable batteries as well as the discharge state of Alkaline batteries. This information is essential for the battery charging algorithm and necessary for battery status indication to the user. Battery status information is supported by the API. Detailed information can be found in AN-D-174 (Battery Management) [5].

Pin CHARGE_CTRL is driven high when either the “sensed voltage on the VBAT pin” is lower than the voltage setting or “sensed current via SOCp” is lower than the current setting. Pin CHARGE_CTRL can drive up to 500 µA as source current (see Table 32). Detailed setting information can be found in document [4] under “Battery settings”.

## 4.10 PROTOCOL STACK

The protocol stack handles the RF interface, the MAC-, DLC-, NWK-layer and encryption according to the DECT standard EN300 175 1-9.

### 4.10.1 DECT TBR22

The SC14CVMDECT SF supports the DECT GAP standard according to EN300 444. For TBR22 type approval (optional) switching off the authentication and encryption is required, which can be done with the VES parameter Tbr_22.

### 4.10.2 Out-of-Range handling

When the PP goes in-range or out-of-range a signal is sent from the PP to the MMI software indicating whether the PP is in-lock or is out-of-lock with the FP.

### 4.10.3 Preamble antenna diversity

To optimise the audio quality caused by rapidly changing radio paths (fading), the SC14CVMDECT SF supports preamble antenna diversity. The preamble diversity algorithm uses RSSI measurements to judge the radio signal strength on both antennas and, as a result, the choice of the best performing antenna is determined. This antenna will then be used for the receive slot and the next transmit slot.

The preamble antenna diversity is supported with two antennas. The preamble diversity can be controlled by VES. See document reference [4] and section 4.13 for more information about antenna diversity.

### 4.10.4 Broadcasting messages

Messages consisting of up to 19 bytes can be broadcasted from FP to all registered PPs. Broadcasting does not require an active connection. Broadcasting does not use retransmission, therefore broadcasting is not secured. If the real time clock is enabled this data is also broadcasted to all PPs.

### 4.10.5 IWU to IWU messaging

The protocol in the SC14CVMDECT SF module is made according to the DECT/GAP standard as defined in EN 300 175 and EN 300 444.

The DECT standard defines an EMC code (see EN 300 175-5, chapter 7.7.23.). This code is unique for a DECT product and must be programmed by the DECT manufacturer to the correct manufacturer code.

The EMC code must be the same for SC14CVMDECT SF based product families when using the IWU to IWU messaging.

If the Dialog default EMC VES value is changed the IWU to IWU messaging may not operate correctly.

IWU data is transferred in a FA format frame; see chapter 6.1 in EN 300 175-4. This frame has an information field of maximum 63 bytes of which maximum 52 bytes can be used for IWU data. With the SC14CVMDECT SF it is only possible to send 5 frames in a row without pause. The following frame must be an acknowledge-frame to secure that the internal buffers within the SC14CVMDECT SF are emptied.

The FA frame is segmented in 5 byte fragments and transferred over the air-interface in the A-field. The 2-bytes CRC is used to determine if the data is received correctly. If the data is not received correctly this is signalled back to the transmitter by the Q2 bit, and the data is retransmitted.

The FA frame has a 2 bytes checksum, used to determine if the complete packet is received correctly. If A checksum error is signalled back to the transmitter and the complete packet is retransmitted. The packet will be retransmitted until it is received correctly, or until the link is closed.

More transmitted packets will be received in the same order as they were transmitted. The application must handle flow control, if needed.

## 4.11 REGISTRATION

The PP and the FP must be paired using a procedure called Registration. Without Registration, the PP will be out-of-lock and will not be able to establish a link to an FP and therefore not be able to make a call. The registration uses the unique product identities and secures the PP and FP to allow no cross-communication.

The PP can be de-registered from an FP either via the FP or PP MMI Software using the command interface. It is also possible to deregister a PP from another registered PP.

It is possible to pair a PP and FP during the production.

### 4.11.1 Handling product identities

To secure that the FP and PPs do not make cross-communications a unique ID must be entered into the VES of an FP or PP. For the DECT version the ID for the FP is named RFPI and for the PP the ID is named IPEI. These numbers are factory settings.

After a successful registration, the IPEI is stored in the FP and the RFPI is stored in the PP. In this way the two parts are known to each other and are allowed to make connections. The registration data are automatically stored in VES of the FP and PP while making the registration.

It is possible to register the same PP to 2 FPs, but it can only be used in one FP at the same time.

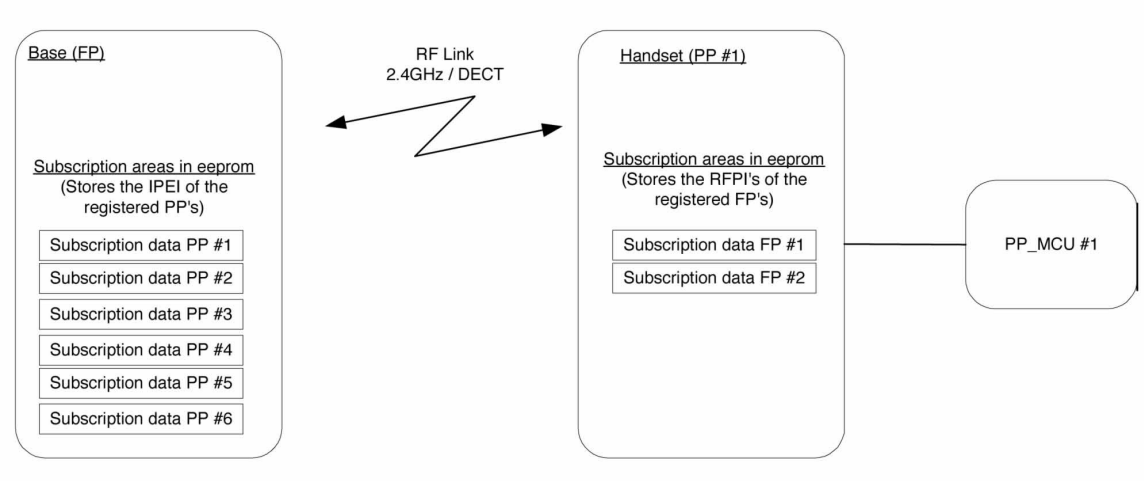



**Figure 20: Handling product identities**

### 4.11.2 Deregistration

There are two ways of deregistering a PP from an FP:

- Remote FP and PP deregistration
  The correct way to deregister a PP from an FP is to deregister it remotely in the FP. If this is done over a service connection from the PP to the FP, the FP actually performs the deregistration and then it is automatically signalled to the PP which in turn will drop out-of-lock. Using this method it is also possible to deregister other PPs registered to the FP from one PP.
- Removing all registrations at once from the FP (e.g. in case the original PPs are lost).

## 4.12 PCM INTERFACE

The PCM supports the following modes:

- SLAVE mode clock sync. In this mode the clock of the module will be adjusted to follow the PCM provided by the external PCM master clock. All audio samples are kept if the provided PCM clock accuracy is +/- 5 ppm, which is a DECT radio requirement.
- SLAVE no clock sync. In this mode the clock of the module is not synchronized. This means audio sample will be discarded in case the master PCM clock is faster than the clock of the module or samples will be repeated in case the master PCM clock is slower.
- MASTER mode. The FP is master on PCM interface and therefore provides PCM clock and PCM_FSC to an external device.

### 4.12.1 PCM Interface for FP

The SC14CVMDECT SF supports PCM interface functionality to connect to an external audio source/destination.

The different PCM interface modes and timings are shown in Figure 21 to Figure 26. Refer to document [1] for detailed information.

### 4.12.2 PCM_FSC frequency

The PCM interface supports the following options:

- 8 kHz
- 16 kHz

### 4.12.3 Length of PCM_FSC

The PCM interface supports the following options:

- 1: The length of PCM_FSC pulse is equal to 1 data bit.
- 8: The length of PCM_FSC pulse is equal to 8 data bits.
- 16: The length of PCM_FSC pulse is equal to 16 data bits.
- 32: The length of PCM_FSC pulse is equal to 32 data bits.

### 4.12.4 Start position of FSC

The PCM interface supports the following options:

- The FSC pulse starts 1 data bit before the MSB bit of the PCM channel 0 data.
- The FSC pulse starts at the same time as the MSB bit of the PCM channel 0 data.

### 4.12.5 PCM clock frequency

The PCM interface supports the following options in master mode:

- 1.152 MHz
- 2.304 MHz
- 4.608 MHz
- 1.536 MHz

### 4.12.6 PCM data mode

The PCM interface supports the following PCM data formats:

- Linear PCM, 8 kHz sample rate. Used for narrowband calls (G.726).
- Linear PCM, 16 kHz sample rate. Used for wideband calls (G.722).
- G.711 – A-law, 8 kHz sample rate. Used for narrowband calls (G.726).
- G.711 – μ-law, 8 kHz sample rate. Used for narrowband calls (G.726).
- Compressed wideband using A-law, 16 kHz sample rate. The 16 bit PCM data is encoded as two 8 bit audio samples if 8 kHz frame sync is used. Used for wideband calls (G.722).
- Compressed wideband using μ-law, 16 kHz sample rate. The 16 bit PCM data is encoded as two 8 bit audio samples if 8 kHz frame sync is used. Used for wideband calls (G.722).

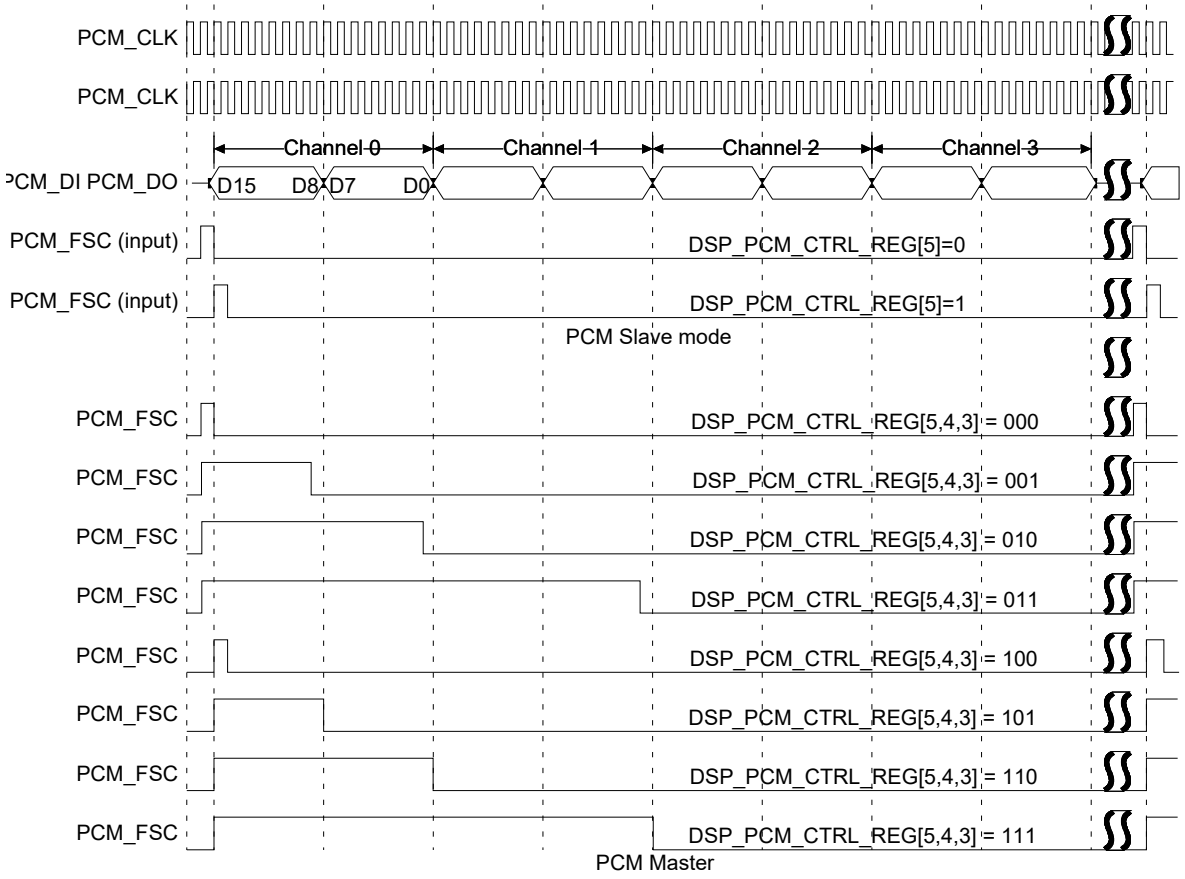



**Figure 21: PCM interface formats**

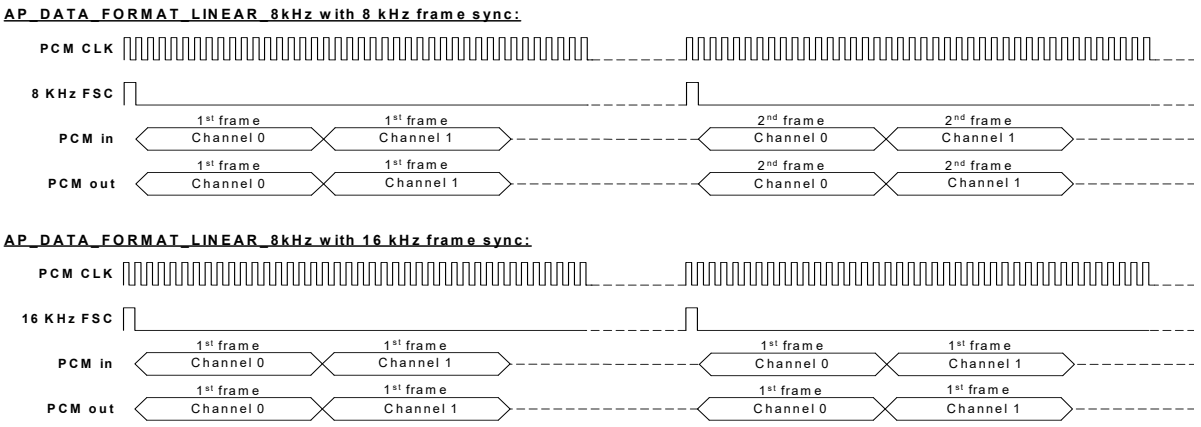



**Figure 22: PCM bus with linear PCM, 8 kHz sample rate**

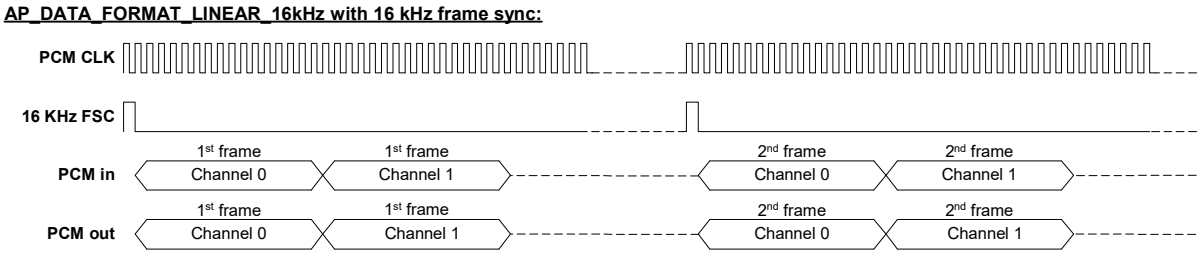



**Figure 23: PCM bus with linear PCM, 16 kHz sample rate**

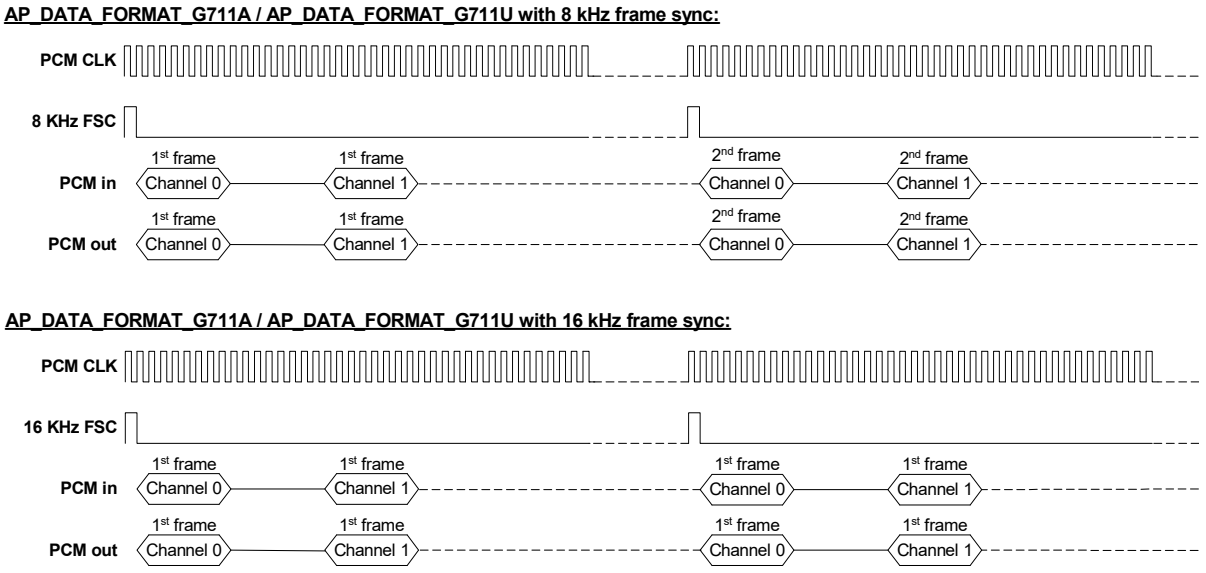



**Figure 24: PCM bus with G.711 – A-law/μ-law, 8 kHz sample rate**

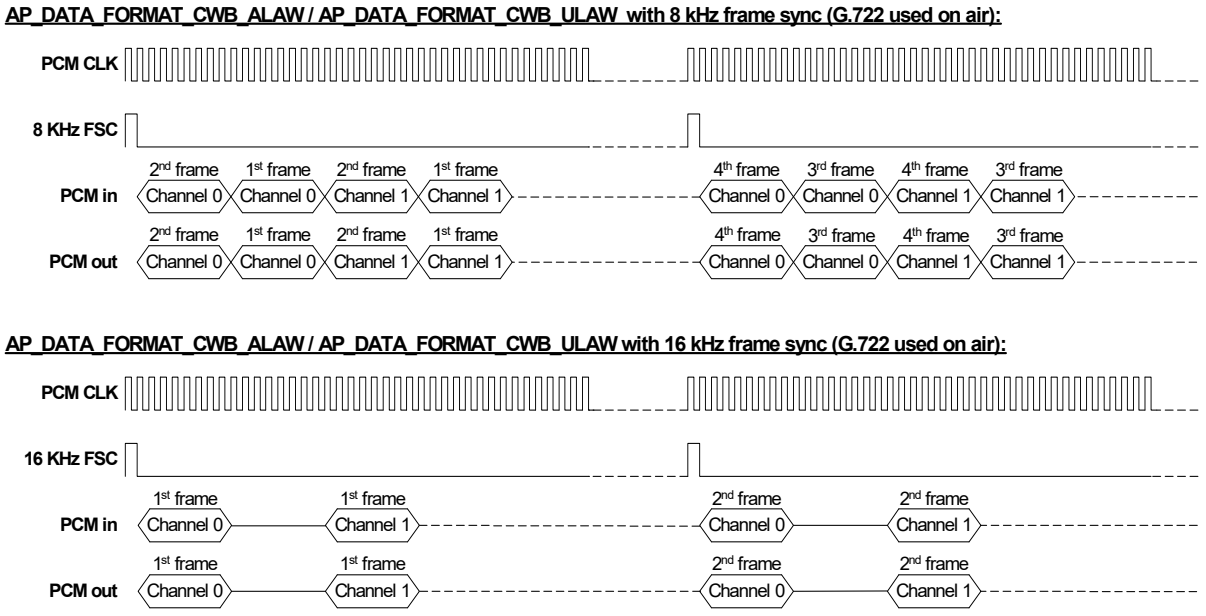



**Figure 25: PCM bus with compressed wideband using A-law/ μ-law, G722 used on air interface**

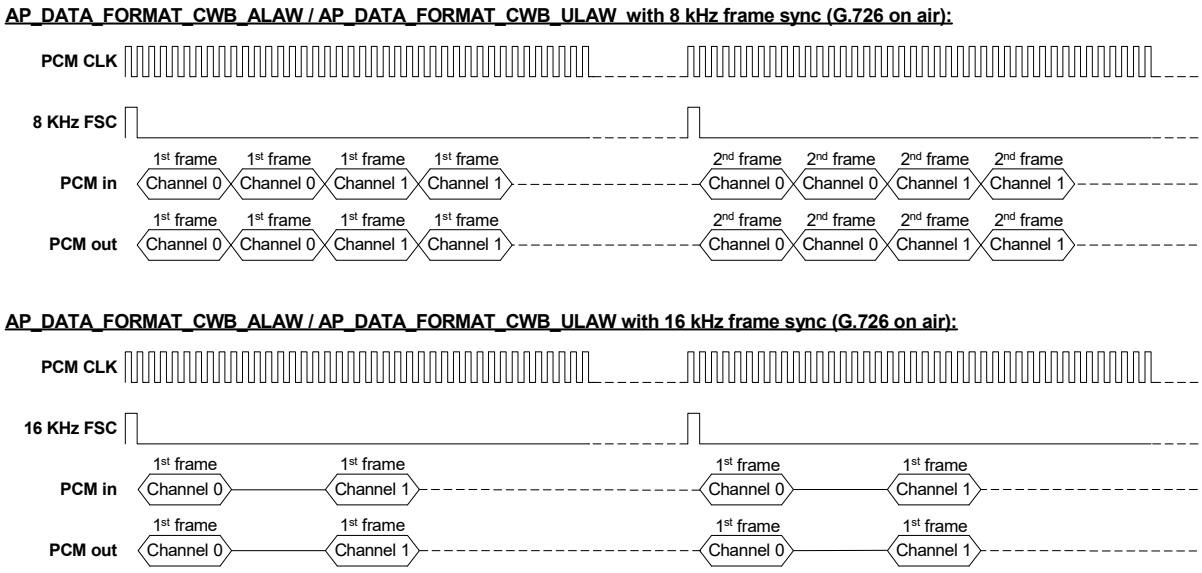



**Figure 26: PCM bus with compressed wideband using A-law/ μ-law, G726 used on air interface**

### 4.12.7 PCM Interface for PP

The SC14CVMDECT SF supports PCM interface functionality to connect to an external audio source/destination. Refer to document [2] for detailed information.

- PCM interface mode

  supports only master mode.

- PCM_FSC frequency

  supports 8 kHz and 16 kHz.

- LENGTH of PCM_FSC

  The PCM interface supports the following options:

  - 1: The length of PCM_FSC pulse is equal to 1 data bit.
  - 8: The length of PCM_FSC pulse is equal to 8 data bits.
  - 16: The length of PCM_FSC pulse is equal to 16 data bits.
  - 32: The length of PCM_FSC pulse is equal to 32 data bits.

- Start position of FSC

  The PCM interface supports the following options:

  - The FSC pulse starts 1 data bit before MSB bit of the PCM channel 0 data.
  - The FSC pulse starts at the same time as the MSB bit of the PCM channel 0 data.

- PCM clock

  PCM clock is delivered to an external slave PCM device from SC14CVMDECT SF.

- PCM Data mode

  Supports only linear 16 bit PCM.

### 4.13 ANTENNA OPERATION

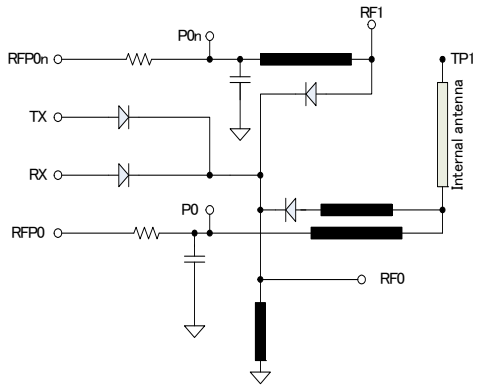



**Figure 27: Internal circuit of the SC14CVMDECT SF**

Figure 27 shows the internal circuit of the SC14CVMDECT SF. Pin RF0 is used for two external antennas and can also be used for RF test purposes. Therefore it is recommended to add a 10 pF capacitor as reserve pattern, even when the two external antennas are not used.

Re-certification of the SC14CVMDECT SF is required if at least one external antenna is added. On request, Dialog Semiconductor can provide a pre-certified PCB layout for an external antenna circuit.

RF1 is also recommended to use and can be connected to the RF cable to be able to do the JPN DECT type approval test.

#### 4.13.1 Internal antenna only

The FAD function is not enabled if only the internal antenna is used. In this case pins RFP0, RFP0n, P0 and P0n must be left unconnected.

#### 4.13.2 Internal and external antenna with FAD

Figure 28 shows one external antenna that is connected to RF1 of the SC14CVMDECT SF. This configuration supports the FAD function. In this case pins RFP0, RFP0n, P0 and P0n must be left unconnected.

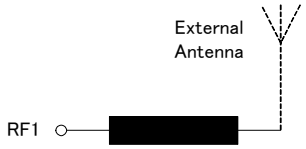



**Figure 28: One external antenna**

# 5.0 CAT-iq

## 5.1 INTRODUCTION

CAT-iq stands for Cordless Advanced Technology, Internet and Quality. It is the new global technology initiative from the DECT Forum, designed for IP-voice services in the next generation networks. CAT-iq is based on the regulatory framework of the mature and reliable DECT technology. It is fully backward compatible to DECT GAP and, as the new cordless phone standard, focuses on high definition VoIP (HD voice) as well as data applications as the next generation Cordless Phone standard.

## 5.2 CAT-IQ PROFILE OVERVIEW

The CAT-iq profiles are split between voice and data services, with CAT-iq 1.0 and CAT-iq 2.0 providing features to support key voice enhancements, and CAT-iq 3.0 and CAT-iq 4.0 providing features to support data.

### 5.2.1 Supported main features

- Narrowband (G.726) and wideband (G.722) audio and switching between these two codecs is supported.
- CLIP, CNIP, CLIR: Calling Line Identification Presentation, Calling Name Identification, Calling Line Identity Restriction for internal and external calls.
- Synchronization of call lists and telephone books, missed calls list, incoming accepted calls list, internal names list (unique identifier of each handset), base telephone book
- Synchronization of system settings: PPs are enabled to change partly the configuration of the system consisting of FP and PPs, these system settings are handled using the list access method. Using this method, the FP and the PPs support:
  - Synchronization of time and date for FP and PPs, that FP is enabled to transmit time and date to the PPs.
  - Reset to factory settings, means that PP is enabled to reset the FP configuration to its factory setting.
  - Obtaining FP versions, means that a PP can obtain the software release of the FP.
- Multiple lines handling: The behaviour of DECT systems connected to multiple network lines. These lines may be of different types (VoIP and PSTN for example). This feature details how calls are placed in a multiple lines context. This feature also impacts the behaviour of other services in order to ensure attachment of PPs to a line, line settings and several lists properly.
- Parallel calls: initiating a second call in parallel to the first call, toggling between calls, putting a call on hold, resuming calls from on hold, call transfer, 3-party conference with established external and/or internal calls
- DTMF and tones
- Headset support
- Easy PIN code registration
- Easy pairing
- handset location
- Supports SUOTA (Software Update Over The Air) and LU10 (max 54 kbit/s).

## 6.0 Register descriptions

Register access requires the use of the API functions API_HAL_READ_REQ and API_HAL_WRITE_REQ. The register address is shown in the table title.

**Table 7: PAD_CTRL_REG (0xFF481E)**

| BIT | MODE | SYMBOL | DESCRIPTION | RESET |
|---|---|---|---|---|
| 15 | - | | Reserved | 0 |
| 14 | R/W | LED34_C_MODE | 0 = 2.5 mA/5 mA mode select for LED3/LED4<br>1 = 5 mA/10 mA mode select for LED3/LED4 | 0 |
| 13 | R/W | LED4_PWM | 0 = Timer 0 PWM control on LED4 disabled<br>1 = TImer 0 PWM control on LED4 enabled | 0 |
| 12 | R/W | LED3_PWM | 0 = Timer 0 PWM control on LED3 disabled<br>1 = TImer 0 PWM control on LED3 enabled | 0 |
| 11 | - | | Reserved, keep 0 | 0 |
| 10 | - | | Reserved, keep 0 | 0 |
| 9 | R/W | LED4_CUR | If LED34_C_MODE = 0<br>0 = 2.5 mA<br>1 = 5 mA<br>If LED34_C_MODE = 1<br>0 = 5 mA<br>1 = 10 mA | 0 |
| 8 | R/W | LED3_CUR | If LED34_C_MODE = 0<br>0 = 2.5 mA<br>1 = 5 mA<br>If LED34_C_MODE = 1<br>0 = 5 mA<br>1 = 10 mA | 0 |
| 7 | R/W | P20_OD | 0 = P2[0] normal mode.<br>1 = P2[0] is forced to open drain if output and pull-up resistor is always disabled if input | 1 |
| 6 | R/W | P21_OD | 0 = P2[1] normal mode.<br>1 = P2[1] is forced to open drain if output and pull-up resistor is always disabled if input | 1 |
| 5 | R/W | P234_OD | 0 = P2[3-4] normal mode<br>1 = P2[3-4] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |
| 4 | R/W | P225_OD | 0 = P2[2,5] normal mode<br>1 = P2[2.5] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |
| 3 | R/W | P27_OD | 0 = P2[7] normal mode<br>1 = P2[7] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |
| 2 | R/W | P001_OD | 0 = P0[0-1] normal mode<br>1 = P0[0-1] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |
| 1 | R/W | P023_OD | 0 = P0[2-3] normal mode<br>1 = P0[2-3] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |
| 0 | R/W | P04567_OD | 0 = P0[4-7] normal mode<br>1 = P0[4-7] is forced to open drain if output and pull-up resistor is always disabled if input | 0 |

**Table 8: P0_DATA_REG, P1_DATA_REG, P2_DATA_REG, P3_DATA_REG (0xFF4830, 0xFF4840, 0xFF4850, 0xFF4860)**

| Bit | Mode | Symbol | Description | Reset P0-P3 |
|---|---|---|---|---|
| 15-8 | - | | | 0 |
| 7 | R/W | Px_7_DATA | If output, set Px[7], else returns the value of Px[7] | 0 |
| 6 | R/W | Px_6_DATA | If output, set Px[6], else returns the value of Px[6] | 0 |
| 5 | R/W | Px_5_DATA | If output, set Px[5], else returns the value of Px[5] | 0,1,0,0 |
| 4 | R/W | Px_4_DATA | If output, set Px[4], else returns the value of Px[4] | 0 |
| 3 | R/W | Px_3_DATA | If output, set Px[3], else returns the value of Px[3] | 0 |
| 2 | R/W | Px_2_DATA | If output, set Px[2], else returns the value of Px[2] | 0 |
| 1 | R/W | Px_1_DATA | If output, set Px[1], else returns the value of Px[1] | 0 |
| 0 | R/W | Px_0_DATA | If output, set Px[0], else returns the value of Px[0] | 0 |
| NOTE: x = 0, 1, 2, 3 These registers are not reset with a SW reset | | | | |

**Table 9: P0_SET_DATA_REG, P1_SET_DATA_REG, P2_SET_DATA_REG, P3_SET_DATA_REG (0xFF4832, 0xFF4842, 0xFF4852, 0xFF4862)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 15-8 | - | | | 0 |
| 7 | R0/W | Px_7_SET | If Px[7] output, writing a 1 sets Px[7] to 1. Writing 0 is discarded, Reading returns 0 | 0 |
| 6 | R0/W | Px_6_SET | If Px[6] output, writing a 1 sets Px[6] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 5 | R0/W | Px_5_SET | If Px[5] output, writing a 1 sets Px[5] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 4 | R0/W | Px_4_SET | If Px[4] output, writing a 1 sets Px[4] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 3 | R/0W | Px_3_SET | If Px[3] output, writing a 1 sets Px[3] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 2 | R0/W | Px_2_SET | If Px[2] output, writing a 1 sets Px[2] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 1 | R0/W | Px_1_SET | If Px[1] output, writing a 1 sets Px[1] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| 0 | R0/W | Px_0_SET | If Px[0] output, writing a 1 sets Px[0] to 1. Writing 0 is discarded. Reading returns 0 | 0 |
| NOTE: x = 0, 1, 2, 3 These registers are not reset with a SW reset | | | | |

**Table 10: P0_RESET_DATA_REG, P1_RESET_DATA_REG, P2_RESET_DATA_REG, P3_RESET_DATA_REG (0xFF4834, 0xFF4844, 0xFF4854, 0xFF4864)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 15-8 | - | | | 0 |
| 7 | R0/W | Px_7_RESET | If Px[7] output, writing a 1 resets Px[7] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 6 | R0/W | Px_6_RESET | If Px[6] output, writing a 1 resets Px[6] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 5 | R0/W | Px_5_RESET | If Px[5] output, writing a 1 resets Px[5] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 4 | R0/W | Px_4_RESET | If Px[4] output, writing a 1 resets Px[4] to 0. Writing 0 is discarded. Reading returns 0 | 0 |

**Table 10: P0_RESET_DATA_REG, P1_RESET_DATA_REG, P2_RESET_DATA_REG, P3_RESET_DATA_REG (0xFF4834, 0xFF4844, 0xFF4854, 0xFF4864)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 3 | R0/W | Px_3_RESET | If Px[3] output, writing a 1 resets Px[3] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 2 | R0/W | Px_2_RESET | If Px[2] output, writing a 1 resets Px[2] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 1 | R0/W | Px_1_RESET | If Px[1] output, writing a 1 resets Px[1] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| 0 | R0/W | Px_0_RESET | If Px[0] output, writing a 1 resets Px[0] to 0. Writing 0 is discarded. Reading returns 0 | 0 |
| NOTE: x = 0, 1, 2, 3 These registers are not reset with a SW reset | | | | |

**Table 11: P0_DIR_REG, P1_DIR_REG, P2_DIR_REG, P3_DIR_REG (0xFF4836, 0xFF4846, 0xFF4856, 0xFF4866)**

| Bit | Mode | Symbol | Description | Reset P0-P5 |
|---|---|---|---|---|
| 15-14 | R/W | Px_7_DIR | 00 = Input, no resistors selected<br>01 = Input, pull-up selected<br>10 = Input, Pull-down selected<br>11 = Output, no resistors selected<br>In analog mode, these bits must be set to 0 to disable resistors and digital output mode. | 1,-,1,0 |
| 13-12 | R/W | Px_6_DIR | | 1,-,1,0 |
| 11-10 | R/W | Px_5_DIR | | 1,3,1,0 |
| 9-8 | R/W | Px_4_DIR | | 1,2,1,0 |
| 7-6 | R/W | Px_3_DIR | | 1,2,1,0 |
| 5-4 | R/W | Px_2_DIR | | 1,1,1,0 |
| 3-2 | R/W | Px_1_DIR | | 1,1,1,- |
| 1-0 | R/W | Px_0_DIR | | 1,1,1,- |
| NOTE:x = 0,1,2,3,4,5 These registers are not reset with a SW reset | | | | |

**Note 12:** P1[5] is output from reset to supply an external EEPROM.
P1[6] and P1[]7 are pull-down only., P3[0], P3[1] are output only
P2[0], P2[1] pull-up resistors are disabled in PAD_CTRL_REG[P20_OD, P21_OD] = 1.
If P3[3] and P1[0] are set to output, the ADC0 and ADC1 inputs are automatically disabled.

**Table 12: P0_MODE_REG (0xFF4838)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 15-14 | - | | | 0 |
| 13-12 | R/W | P0_7_MODE | 00 = P0_OUT_DATA_REG[7] on P0[7]<br>01 = SPI_DI on P0[7] (don't care)<br>10 = Timer 0 PWM1 on P0[7]<br>11 = Reserved | 0 |
| 11-10 | R/W | P0_6_MODE | 00 = P0_OUT_DATA_REG[6] on P0[6]<br>01 = SPI_DO on P0[6]<br>10 = Reserved<br>11 = Reserved | 0 |
| 9-8 | R/W | P0_5_MODE | 00 = P0_OUT_DATA_REG[5] on P0[5]<br>01 = SPI_CLK on P0[5]<br>10 = Reserved<br>11 = Reserved | 0 |
| 7-6 | R/W | P0_4_MODE | 00 = P0_OUT_DATA_REG[4] on P0[4]<br>01 = SPI_EN **input** on P0[4] (don't care)<br>10 = Reserved<br>11 = Reserved | 0 |

**Table 12: P0_MODE_REG (0xFF4838)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 5-4 | R/W | P0_3_MODE | 00 = P0_OUT_DATA_REG[3] on P0[3]<br>01 = SCL2 on P0[3] **(Note 14)**<br>1x = Reserved | 0 |
| 3-2 | R/W | P0_2_MODE | 00 = P0_OUT_DATA_REG[2] on P0[2]<br>01 = SDA2 on P0[2] **(Note 14)**<br>10 = UART UTX2 on P0[2]<br>1x = Reserved | 0 |
| 1 | R/W | P0_1_MODE | 0 = P0_OUT_DATA_REG[1] on P0[1]<br>1 = Timer 0 PWM0 on P0[1] | 0 |
| 0 | R/W | P0_0_MODE | 0 = P0_OUT_DATA_REG[0] on P0[0]<br>1 = UART UTX on P0[0] | 0 |
| NOTE: This register is not reset with a SW reset | | | | |

**Table 13: P1_MODE_REG (0xFF4848)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 15-10 | - | | | 0 |
| 9-8 | R/W | RF_BB_MODE | 00 / 01 / 10<br>P1[5]: See P1_5_MODE / RDI output / RDI input<br>P1[4]: See P1_4_MODE / TDOD output / TDOD output<br>P1[3]: See P1_3_MODE / SIO output / SIO input/output<br>P1[2]: See P1_2_MODE / SK output / SK output<br>P1[1]: See P1_1_MODE / LE output / LE output | 0 |
| 7-5 | - | P1_5_MODE | Reserved | 0 |
| 4 | R/W | P1_4_MODE | 0 = P1_OUT_DATA_REG[4] on P1[4] (2 mA drive)<br>1 = P1_OUT_DATA_REG[4] on P1[4] (1 mA drive) for direct connection to base of external NPN transistor. | 0 |
| 3 | R/W | P1_3_MODE | 0 = P1_OUT_DATA_REG[3] on P1[3] (2 mA drive)<br>1 = P1_OUT_DATA_REG[3] on P1[3] (1 mA drive) for direct connection to base of external NPN transistor. | 0 |
| 2 | - | P1_2_MODE | Reserved | 0 |
| 1 | - | P1_1_MODE | Reserved | 0 |
| 0 | R/W | P1_0_MODE | 0 = P1_OUT_DATA_REG[0] on P1[0]<br>ADC1 input disabled, input up-to VDD+0.3 V<br>1 = Analog ADC1 mode, input up to 1.98 V!!<br>P1_DIR_REG[0] must be set to 0, to disable Pull-up, pull-down and digital output mode. | 1 |
| NOTE: This register is not reset with a SW reset | | | | |

**Table 14: P2_MODE_REG (0xFF4858)**

| BIT | MODE | SYMBOL | DESCRIPTION | RESET |
|---|---|---|---|---|
| 15 | R/W | P2_7_MODE | 0 = P2_OUT_DATA_REG[7] on P2[7]<br>1 = BXTAL on P2[7] (Can be used as RFCLK for external RF) | 0 |
| 14 | R/W | INT7_MODE | 0 = P2[7] input to INT7<br>1 = P1[2] input to INT7 | 0 |
| 13 | R/W | P2_6_MODE | 0 = P2_OUT_DATA_REG[6] on P2[6]<br>1 = WTF_IN on P2[6] (monitor Gen2DSP load) | 0 |
| 12 | R/W | INT6_MODE | 0 = P2[6] to INT6<br>1 = P1[1] to INT6 | 0 |

**Table 14: P2_MODE_REG (0xFF4858)**

| BIT | MODE | SYMBOL | DESCRIPTION | RESET |
|---|---|---|---|---|
| 11-10 | R/W | P2_5_MODE | 00 = P2_OUT_DATA_REG[5] on P2[5]<br>01 = PCM_FSC on P2[5]<br>10 = SF on P2[5]<br>11 = Reserved | 0 |
| 9-8 | R/W | P2_4_MODE | 00 = P2_OUT_DATA_REG[4] on P2[4]<br>01 = PCM_DO on P2[4] **(Note 13)**<br>10 = SCL1 on P2[4] **(Note 14)**<br>11 = DP3 on P2[4] | 0 |
| 7-6 | R/W | P2_3_MODE | 00 = P2_OUT_DATA_REG[3] on P2[3]<br>01 = PCM_DI input on P2[3]<br>10 = SDA1 on P2[3] **(Note 14)**<br>11 = DP2 on P2[3] | 0 |
| 5-4 | R/W | P2_2_MODE | 00 = P2_OUT_DATA_REG[2] on P2[2].<br>01 = PCM_CLK on P2[2]<br>10 = CLK100 on P2[2]<br>11 = Reserved | 0 |
| 3-2 | R/W | P2_1_MODE | 00 = P2_OUT_DATA_REG[1] on P2[1]<br>01 = ECZ2 (from DSP) on P2[1]<br>10 = Timer 0 PWM1 on P2[1]<br>11 = LED4 mode on P2[1]. PAD_CTRL_REG[P21_OD] must kept '1' if LED is connected to VBAT. Set PAD_CTRL_REG [LED4_PWM] = 1 for PWM on LED4 current source. | 0 |
| 1-0 | R/W | P2_0_MODE | 00 = P2_OUT_DATA_REG[0] on P2[0]<br>01 = ECZ1 (from DSP) on P2[0]<br>10 = Timer0 PWM0 on P2[0]<br>11 = LED3 mode on P2[0]. PAD_CTRL_REG[P20_OD] must kept '1' if LED is connected to VBAT. Set PAD_CTRL_REG [LED3_PWM] =1 for PWM on LED4 current source. | 0 |
| NOTE: This register is not reset with a SW reset | | | | |

**Note 13:** Push/pull or open drain function is controlled from the sub-block's DSP_PCM_CTRL_REG, resp. ACCESSx_CTRL_REG.
**Note 14:** To enable outputs, the corresponding P2_DIR_REG[y] bit(s) do **not** have to be controlled, this is done by the sub block.

**Table 15: P3_MODE_REG (0xFF4868)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 15-14 | R/W | P3_7_MODE | 00 = P3_OUT_DATA_REG[7] on P3[7]<br>01 = Analog mode RINGp on P3[7] **(Note 15)**<br>1x = Reserved | 1 |
| 13-12 | R/W | P3_6_MODE | 00 = P3_OUT_DATA_REG[6] on P3[6]<br>01 = Analog mode RINGn on P3[6] **(Note 15)**<br>1x = Reserved | 1 |
| 11-10 | R/W | P3_5_MODE | 00 = P3_OUT_DATA_REG[5] on P3[5]<br>01= Analog mode RINGING/RINGout on P3[5] **(Note 15)**<br>1x = Reserved | 1 |
| 9-8 | R/W | P3_4_MODE | 00 = P3_OUT_DATA_REG[4] on P3[4].<br>01 = Analog mode PARAdet on P3[4]<br>1x = Reserved | 1 |
| 7-6 | R/W | P3_3_MODE | 00 = P3_OUT_DATA_REG[2] on P3[3]<br>ADC0 input disabled, input up to VDD+0.3 V<br>01 = Analog ADC0 mode, input up to 1.98 V!!<br>1x = Reserved | 1 |
| 5-4 | R/W | P3_2_MODE | 00 = P3_OUT_DATA_REG[2] on P3[2]<br>01 = Analog mode CIDINp on P3[2]<br>1x = Reserved | 1 |

**Table 15: P3_MODE_REG (0xFF4868)**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 3-2 | R/W | P3_1_MODE | 00 = P3_OUT_DATA_REG[1] on P3[1].<br>01 = PAOUTp on P3[1]<br>10 = DP1 on P3[1]<br>11 = DCACHE_HIT on P3[1] /PAOUTp | 1 |
| 1-0 | R/W | P3_0_MODE | 00 = P3_OUT_DATA_REG[0] on P3[0].<br>01 = PAOUTn on P3[0]<br>10 = DP0 on P3[0]<br>11 = ICACHE_HIT on P3[0] /PAOUTn | 1 |
| NOTE: This register is not reset with a SW reset | | | | |

**Note 15:** For the RINGp, RINGn, RINGout function, the Ringing opamp must be enabled with CODEC_TONE_REG[RNG_PD].
For the RINGING input, the RINGING comparator must be enabled CODEC_TONE_REG[RNG_CMP_PD]

**Note 16:** In analog mode make sure P3_DIR_REG[7-3] is set to 0 to disable Pull-up, pull-down and digital output mode.

# 7.0 Specifications

**All MIN/MAX specification limits are guaranteed by design, or production test, or statistical methods unless note 17 is added to the parameter description. Typical values are informative.**

**Note 17:** This parameter will not be tested in production. The MIN/MAX values are guaranteed by design and verified by characterization.

## 7.1 GENERAL

**Table 16: SC14CVMDECT SF module**

| ITEM | CONDITIONS | VALUE | UNIT |
|---|---|---|---|
| Dimensions | l x w x h | **18.0 x 19.6 x 2.7** | **mm** |
| Weight | | **1.5** | **g** |
| Temperature range | | **-40 to +85** | **°C** |
| Frequency range | According to DECT standard | **1870 to 1930** | **MHz** |
| Antenna range | According to DECT standard; **(Note 18)** | | |
| | - typical outdoor | **350** | **m** |
| | - typical indoor | **75** | **m** |
| Standards compliancy | ETS 300 444 (DECT GAP), former TBR2214<br>FCC part 15 | | |
| Power supply | 2 cell NiCd/NiMH<br>Note: for 1 Li-Ion battery an external LDO is required. | **2.10 to 3.45** | **V** |
| Maximum PCB warpage | For entire reflow range | **0.1** | **mm** |

**Note 18:** The resulting range is very dependent of the mechanical design. Dialog Semiconductor is not responsible for this design and as such Dialog Semiconductor is not responsible for the resulting performance range of the final product.

## 7.2 ABSOLUTE MAXIMUM RATINGS

**Table 17: Absolute Maximum Ratings (Note 19)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Vbat_max | Max voltage on pin VBATIN, VDDPA | | | **3.45** | **V** |
| Vpon_max | Max voltage on pin PON | | | **5.5** | **V** |
| Vled_max | Max voltage on pin LED4, LED3 | | | **3.6** | **V** |
| Vdig_bp_max | Max voltage on digital pins with back drive protection; ports P0 and P2 (except P2.6) | | | **3.6** | **V** |
| Vdig_max | Max voltage on other digital pins | | | **2.0** | **V** |
| Vana_max | Max voltage on analog pins | | | **2.2** | **V** |
| Vesd_hbm | ESD voltage according to human body model; all pins | | | **2000** | **V** |
| Vesd_mm | ESD voltage according to machine model; all pins | | | **150** | **V** |

**Note 19:** Absolute maximum ratings are those values that may be applied for maximum 50 hours. Beyond these values, damage to the device may occur.

## 7.3 OPERATING CONDITIONS

**Table 18: Operating conditions (Note 20)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vbat | Supply voltage on pin VBATIN | | **2.1** | | **3.45** | **V** |
| Vdd_pa | CLASSD supply voltage on pin VDDPA | | **2.1** | | **3.45** | **V** |
| Vpon | Voltage on pin PON | | | | **5.5** | **V** |
| Vdig_bp | Voltage on digital pins with back drive protection; ports P0 and P2 (except P2.6) | | | | **3.45** | **V** |

**Table 18: Operating conditions (Note 20)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vdig | Voltage on other digital pins | VDD = 1.8 V | | | 1.98 | V |
| Vana | Voltage on analog pins | AVD = 1.8 V | | | 2.1 | V |
| Icharge | Current through pin CHARGE | Rseries > (Vcharge-3 V)/ 10 mA | | | 10 | mA |
| Ipa | Current through pin PAOUTp, PAOUTn | (Note 21) | | | 500 | mA |
| Iout_vrefp | Output current through pin VREFp | | | | 1 | mA |
| TA | Ambient temperature | (Note 22) | -40 | | +85 | °C |

**Note 20:** Within the specified limits, a life time of 10 years is guaranteed.
**Note 21:** A life time of 10 years of the CLASS-D amplifier is guaranteed if switched on for 10% of the time.
**Note 22:** Within this temperature range full operation is guaranteed.

## 7.4 SUPPLY CURRENTS

**Table 19: Supply currents (full slot)**

| PARAMETER | DESCRIPTION | CONDITIONS (Note 23) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Ibat_FP_stby | standby supply current | FP; HPM; Vbat = 2.6 V | | 60 | | mA |
| | | FP; HPM/U; Vbat = 2.6 V | | 59 | | mA |
| | | FP; HPM/J; Vbat = 2.6 V | | 80 | | mA |
| Ibat_FP_talk | talk supply current | FP; HPM; Vbat = 2.6 V | | 87 | | mA |
| | | FP; HPM/U; Vbat = 2.6 V | | 80 | | mA |
| | | FP; HPM/J; Vbat = 2.6 V | | 110 | | mA |
| Ibat_PP_stby | standby supply current | PP; Vbat = 2.6 V | | 10 | | mA |
| Ibat_PP_talk | talk supply current | PP; LPM; Vbat = 2.6 V | | 34 | | mA |
| | | PP; HPM; Vbat = 2.6 V | | 47 | | mA |
| | | PP; HPM/U; Vbat = 2.6 V | | 42 | | mA |
| | | PP; HPM/J; Vbat = 2.6 V | | 49 | | mA |

**Note 23:** RF output power settings for full-slot operation: see Table 36.

**Table 20: Supply currents (long slot)**

| PARAMETER | DESCRIPTION | CONDITIONS (Note 24) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Ibat_FP_stby | standby supply current | FP; HPM; Vbat = 2.6 V | | 60 | | mA |
| | | FP; HPM/U; Vbat = 2.6 V | | 59 | | mA |
| | | FP; HPM/J; Vbat = 2.6 V | | 80 | | mA |
| Ibat_FP_talk | talk supply current | FP; HPM; Vbat = 2.6 V | | 107 | | mA |
| | | FP; HPM/U; Vbat = 2.6 V | | 96 | | mA |
| | | FP; HPM/J; Vbat = 2.6 V | | 117 | | mA |
| Ibat_PP_stby | standby supply current | PP; Vbat = 2.6 V | | 10 | | mA |
| Ibat_PP_talk | talk supply current | PP; LPM; Vbat = 2.6 V | | 55 | | mA |
| | | PP; HPM; Vbat = 2.6 V | | 80 | | mA |
| | | PP; HPM/U; Vbat = 2.6 V | | 66 | | mA |
| | | PP; HPM/J; Vbat = 2.6 V | | 66 | | mA |

**Note 24:** RF output power settings for long-slot operation: see Table 36. Japan DECT uses the HPM/U settings for long-slot operation.

### 7.5 DIGITAL INPUT/OUTPUT PINS

**Table 21: Digital input levels**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vil_dig | Logic 0 input level; all digital input pins except PON, CHARGE and RSTn | VDD = 1.8 V | | | **0.3*VDD** | **V** |
| Vil_pon | Logic 0 input level; pin PON | | | | **0.9** | **V** |
| Vil_charge | Logic 0 input level; pin CHARGE | | | | **0.9** | **V** |
| Vil_rst | Logic 0 input level; pin RSTn | VDD = 1.8 V | | | **0.2*VDD** | **V** |
| Vih_dig | Logic 1 input level; all digital input pins except PON, CHARGE and RSTn | VDD = 1.8 V | **0.7*VDD** | | | **V** |
| Vih_pon | Logic 1 input level; pin PON | | **1.5** | | | **V** |
| Vih_charge | Logic 1 input level; pin CHARGE | | **1.5** | | | **V** |
| Vih_rst | Logic 1 input level; pin RSTn | VDD = 1.8 V | **0.8*VDD** | | | **V** |

**Table 22: Digital output levels**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vol_dig | Logic 0 output level | VDD = 1.8 V; Iout = 2, 4, 8 mA **(Note 25)** | | | **0.2*VDD** | **V** |
| Voh_dig | Logic 1 output level | VDD = 1.8 V; Iout = 2, 4, 8 mA **(Note 25)** | **0.8*VDD** | | | **V** |

**Note 25:** For output drive capability, see section "Pin Description" on page 5.

### 7.6 ANALOG FRONT END

**Table 23: Microphone amplifier**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vmic_0dB_unt | Untrimmed differential RMS input voltage between MICp and MICn (0 dBm0 reference level) **(Note 17)** | 0 dBm0 on COUT **(Note 27)** MIC_GAIN[3:0] = 0, @ 1020 Hz; Tolerance: • 13% when untrimmed (BANDGAP_REG=8) **(Note 26)** • 6% when trimmed **(Note 28)** | **114** | **131** | **149** | **mV** |
| Rin_mic | Resistance of activated microphone amplifier inputs (MICp, MICn and MICh) to internal GND **(Note 17)** | | **75** | **150** | | **kΩ** |
| Vmic_offset | Input referred DC-offset **(Note 17)** | MIC_GAIN[3..0] = 1111 3 sigma deviation limits | **-2.6** | | **+2.6** | **mV** |

**Note 26:** BANDGAP_REG will be tuned at the factory.

**Note 27:** 0 dBm0 on COUT = -3.14 dB of max PCM value. COUT is CODEC output in test mode

**Note 28:** Trimming possibility is foreseen. At system production the bandgap reference voltage can be controlled within 2% accuracy and data can be stored in Flash. Either AVD or VREF can be trimmed within 2% accuracy. If AVD is trimmed VREF will be within 2% accuracy related to either AVD. Or vice versa VREF can be trimmed. For Vref trimming measure Δ (VREFp, VREFm) and update BANDGAP_REG[3..0].

**Table 24: Microphone amplifier (Operating Condition)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vmic_cm_level | MICp and MICn common mode voltage | MICp and MICn are set to GND with internal resistors (Rin_mic). If DC coupled the input voltage must be equal to this voltage. | | **(0.9 V/1.5)* VREFp** | | **V** |

**Table 25: Microphone supply voltages**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vref_unt | VREFp-VREFm untrimmed **(Note 29)** | $I_{LOAD}$ = 0 mA BANDGAP_REG = 8 **(Note 28)** | **1.41** | **1.5** | **1.59** | **V** |
| Rout_vrefp | VREFp output resistance | Figure 29 | | **1** | | Ω |
| Nvrefp_idle | Peak noise on VREFp-VREFm **(Note 17)** | CCITT weighted | | | **-120** | **dBV** |
| PSRRvrefp | Power supply rejection Vref output **(Note 17)** | See Figure 29, AVD to VREFp/m, f = 100 Hz to 4 kHz BANDGAP_REG[5:4] = 3 | **40** | | | **dB** |

**Note 29:** Vrefm is a clean ground input and is the 0 V reference.

**Table 26: VREFp load circuit**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Cload_vrefp | VREFp (parasitic) load capacitance | | | | **20** | **pF** |
| Iout_vrefp | VREFp output current | | | | **1** | **mA** |

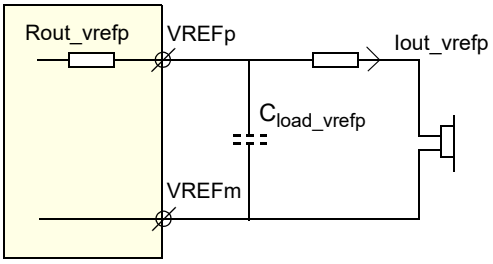



**Figure 29: VREFp load circuit**

**Table 27: LSRp/LSRn outputs**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vlsr_0dB_unt | Untrimmed differential RMS output voltage between LSRp and LSRn in audio mode (0 dBm0 reference level) | 0 dBm0 on CIN **(Note 30)**, LSRATT[2:0] = 001, @ 1020 Hz Load circuit A (see Figure 30, Table 28) with RL1= ∞ Ω, Cp1 or load circuit B (see Figure 31) with RL2, Cp2 and Cs2<br><br>Tolerance:<br>• 13% when untrimmed (BANDGAP_REG=8)<br>• 6% when trimmed **(Note 28)** | **621** | **714** | **807** | **mV** |
| Rout_lsr | Resistance of activated loudspeaker amplifier outputs LSRp and LSRn | | | **1** | | Ω |
| Vlsr_dc | DC offset between LSRp and LSRn **(Note 17)** | LSRATT[2:0] = 3<br>$R_{L1}$ = 28 Ω<br>3 sigma deviation limits | **-20** | | **20** | **mV** |

**Note 30:** 0 dBm0 on CIN = -3.14 dB of max PCM value.

**Table 28: LSRp/LSRn load circuits**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Cp1_Rl1_inf | Load capacitance | see Figure 30, $R_{L1}$ = ∞ | | | **30** | **pF** |
| Cp1_Rl1_1k | Load capacitance | see Figure 30, $R_{L1} \leq 1$ kΩ | | | **100** | **pF** |
| Rl1 | Load resistance | | **28** | | | Ω |

**Table 28: LSRp/LSRn load circuits**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Cp2 | Parallel load capacitance | see Figure 31 | | | **30** | **pF** |
| Cs2 | Serial load capacitance | | | | **30** | **µF** |
| Rl2 | Load resistance | | **600** | | | Ω |

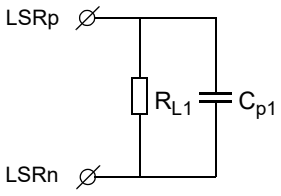



**Figure 30: Load circuit A: Dynamic loudspeaker**

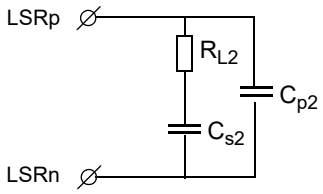



**Figure 31: Load circuit B: Piezo loudspeaker**

**Table 29: PAOUTp, PAOUTn outputs**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vpa_4v | Differential rms output voltage between PAOUTp and PAOUTn | Trimmed bandgap input = 0 dBm0, 1 kHz **(Note 27)** Output low-pass filtered CLASSD_VOUT = 0 | | **0.985** | | **Vrms** |
| Vpa_6v | | As above CLASSD_VOUT = 1 | | **1.478** | | **Vrms** |
| Zload_pa_4v | Speaker impedance, connected between PAOUTp and PAOUTn | With these values, the peak currents stays within the operating range. | **4** | | | Ω |
| Zload_pa_6v | | | **6** | | | Ω |

**Table 30: PAOUTp, PAOUTn outputs (Note 31)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rout_pa | Differential output resistance between PAOUTp and PAOUTn | See **(Note 31)** | | **1** | | Ω |

**Note 31:** Clipping of the outputs occurs when the VDDPA drops and the following conditions becomes true. If CLASSD_CTRL_REG[CLASSD_CLIP] is not equal to zero then upon a programmable number of clipping occurrences a CLASSD_INT is generated:
The software can stop clipping by reducing the gain via the GENDSP:

Clipping occurs if $\frac{\text{peak}(\text{LowPassFiltered}(\text{PAOUTp} - \text{PAOUTm}))}{\text{VDDPA} - \text{VSSPA}} > \frac{\text{Zload}}{\text{Zload} + \text{Rout\_pa}}$

**Table 31: PAOUTp, PAOUTn external components**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| C_VDDPA | Decoupling capacitor on VDDPA | Required when Class-D is used and guaranteed life time. (see Figure 32) | | **1** | | **µF** |
| Cs_PAOUT | Snubber capacitor (to reduce ringing at PAOUTp/n) | Required when Class-D is used to prevent EMI and guaranteed life time. (see Figure 32) | | **1** | | **nF** |
| Rs_PAOUT | Snubber resistor (to reduce ringing at PAOUTp/n) | Required when Class-D is used to prevent EMI and guaranteed life time. (see Figure 32) | | **1** | | Ω |

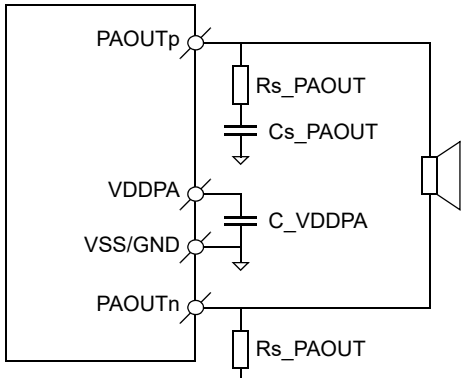



**Figure 32: Class-D external components**

Efficiency 75% at 300 mW@2 V, 500 mW@2.5 V into a 4 Ω transducer.

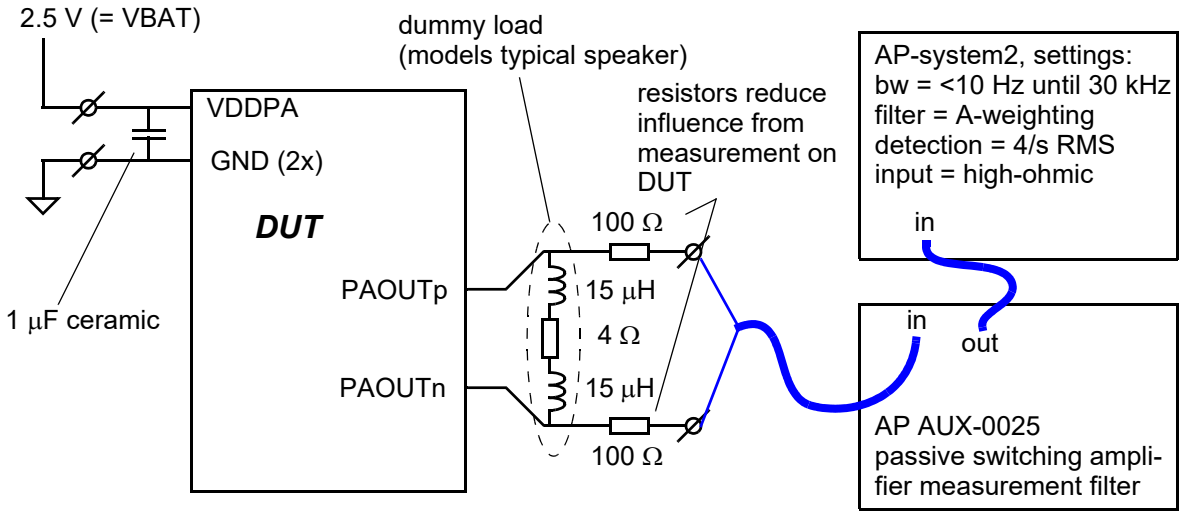



**Figure 33: CLASS-D amplifier measurement setup**

### 7.7 BATTERY MANAGEMENT

**Table 32: CHARGE_CTRL pin**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Voh_charge_ctrl | Drive capability of pin CHARGE_CTRL | sourcing 500 µA | **1.6** | | | **V** |
| Vol_charge_ctrl | | sinking 100 µA | | | **0.2** | **V** |

**Table 33: State of charge circuit (SoC) (Operating condition)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Vsocp_socn | Input voltage between SOCp and SOCn | With the prescribed 0.1 Ω sense resistor this results in the usable current range | **-100** | | **+100** | **mV** |

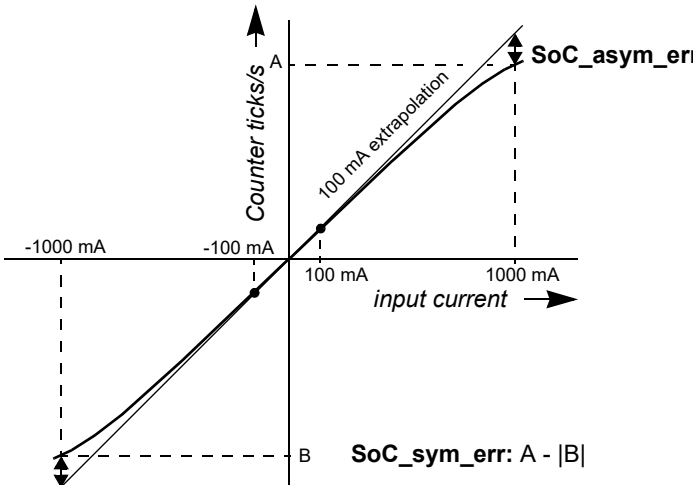



**Figure 34: State of charge (SOC) counter accuracy**

### 7.8 BASEBAND PART

**Table 34: Baseband specifications**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Fbit_uart | Serial interface bit rate | UART; Interface for external microprocessor or PC | | | **115.2** | **kbit/s** |
| Fbit_flash | Flash download bit rate | Via UART | | | **115.2** | **kbit/s** |

### 7.9 RADIO (RF) PART

Standards compliancy: ETS 301 406 (former TBR6).

**Table 35: Radio specifications**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| P_Rx | Receiver sensitivity | BER = 0.001; TA = 25 °C | **-93** | **-92** | **-89** | **dBm** |
| P_Rx_T | Receiver sensitivity, full temperature range | BER = 0.001;<br>-40 °C ≤ TA ≤ +85 °C | | | **-87** | **dBm** |
| IPL | Intermodulation performance level (EN 301 406 section 4.5.7.6) | TA = 25 °C;<br>Pw = -80 dBm;<br>∆f = 2 channels | **-35** | | | **dBm** |
| NTP | Normal transmitted power | HPM (DECT);<br>HPM/J (J-DECT) | **21** | **23** | **24.5** | **dBm** |
| | | HPM/U (DECT6.0) | | | **20.0** | **dBm** |
| | | LPM (any DECT mode) | | **12** | | **dBm** |
| dPrfpa_T | RFPA power variation, full temperature range | -40 °C ≤ TA ≤ +85 °C | | **2.5** | **4** | **dB** |
| Fbit | Bit rate | GFSK modulation | | **1.152** | | **Mbit/s** |
| BW_Tx | Transmitter bandwidth | DECT GFSK;<br>NTP = 20 dB | | | **1.728** | **MHz** |

**Table 36: RFPA preferred settings for various power modes**

| Address (VES) | Register / Parameter | HPM/U (USA) | HPM (Europe) | HPM/J (Japan)(Note 32) |
|---|---|---|---|---|
| 0x39 | RF_PA_CTRL1_REG | 0x09A0 | 0x0CF0 | 0x2CE0 |
| 0x3B | RF_TEST_MODE2_REG | 0x0056 | 0x0062 | 0x0068 |
| 0x3D | RF_BBADC_CTRL_REG | 0x0380 | 0x03A0 | 0x0398 |
| 0x05 | RF_PLL_CTRL2_REG[MODINDEX] | 0x25 | 0x25 | 0x23 |
| 0x23 | Upper RSSI threshold | 0x2C | N/A | 0x28 |
| 0x24 | Lower RSSI threshold | 0x22 | N/A | 0x1E |

**Note 32:** This power setting is used only for full-slot operation. Japan DECT uses the HPM/U settings for long-slot and double-slot operation.

### 7.10 RF POWER SUPPLY

**Table 37: Requirements for linear supply regulator**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| VBAT IN | Voltage at VBAT SW | Unloaded $V_B$<br>Loaded $V_B$-$V_1$-$V_2$-$V_3$ | **2.1** | **3** | **3.45** | **V** |
| $V_1$ | Settling time | I = 50 mA | | | **20** | **mV** |
| $V_2$ | Receive period | I = 130 mA | | | **100** | **mV** |
| $V_2$ | Transmit period | I = 550 mA | | | **200** | **mV** |
| $V_3$ | Drop during transmit | | | | **25** | **mV** |

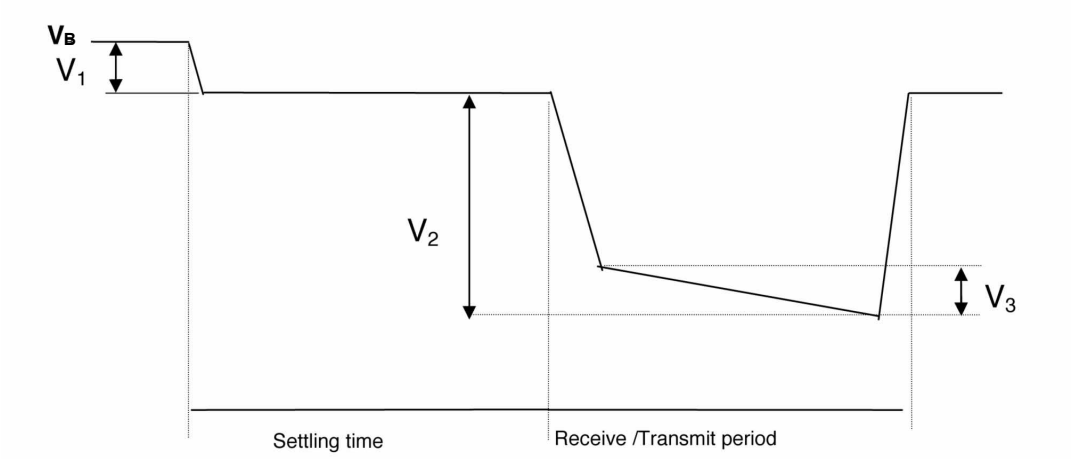



**Figure 35: RF power supply**

### 7.11 RF CHANNEL FREQUENCIES

**Table 38: RF frequencies and channel numbers**

| Frequency (MHz) | DECT CH | J-DECT CH | DECT6.0 CH |
|---|---|---|---|
| 1881.792 | 9 | | |
| 1883.520 | 8 | | |
| 1885.248 | 7 | | |
| 1886.976 | 6 | | |
| 1888.704 | 5 | | |
| 1890.432 | 4 | | |
| 1892.160 | 3 | | |
| 1893.888 | 2 | | |
| 1895.616 | 1 | 4 | |
| 1897.344 | 0 | 3 **(Note 33)** | |
| 1899.072 | | 2 **(Note 33)** | |
| 1900.800 | | 1 **(Note 33)** | |
| 1902.528 | | 0 | |
| 1921.536 | | | 4 |
| 1923.264 | | | 3 |
| 1924.992 | | | 2 |
| 1926.720 | | | 1 |
| 1928.448 | | | 0 |

**Note 33:** For J-DECT the use of this channel is not allowed when a PHS signal is detected.

**The RF setting values according to Table 36 must be followed when the DECT country is changed.**

# 8.0 Design guidelines

This section describes the software and hardware considerations to be taken into account when designing the target application.

The SC14CVMDECT SF can be used standalone or next to an MCU that controls the module. In case the module is used standalone the application will be stored in its on-board Flash. In total 324 kB of Flash is available for this purpose.

Applications can be developed with the Athena software development environment (see reference [3]).

## 8.1 APPLICATION SOFTWARE FOR PP

In a PP application the following software tasks must be handled by the MCU or within the module itself:

- UART communication (external microprocessor only)
- PP MMI
- Display interface (optional)
- Keyboard interface (optional)
- Battery Charge interface (optional)
- Audio handling
- Tone / Melodies handling

For control commands see document reference [2].

**UART communication**

The UART communication is the main control interface of the SC14CVMDECT SF.

**PP MMI**

The MMI state machine must handle the call setup and call termination on the PP.

**Display Interface**

The MCU / PP handles the display interface including the display driver.

**Keyboard Interface**

The MCU/ PP handles the keyboard interface including the keyboard driver.

**Audio handling**

The Application Software state machine must control when to open and close the audio. The headset plug-in detection must handled by the host, and a status is send to the PP MMI from the PP stack software. The PP MMI must handle the volume control.

Headset detection boundaries can be adjusted in VES. When headset indication is received from the PP Headset detection logic, the Application Software can decide if audio should be switched to the headset and sends a request to the PP stack software.

The PP audio handling basically consists of 4 audio modes (see Figure 14):

1. Idle (Alert) mode
2. Earpiece mode
3. Handsfree mode (Speakerphone)
4. Headset mode

Shifting between modes is done through the API.

**Tone handling**

The Application Software state machine must control when to play tones and the volume setting. Custom melodies can be defined in the VES.

## 8.2 APPLICATION SOFTWARE FOR FP

In an FP application the following software tasks must be handled by the MCU or within the module itself:

- UART communication (external microprocessor only)
- FP MMI
- Display interface (optional)
- Keyboard interface (optional)
- Audio handling
- Tone / Melodies handling

For control commands see document reference [1].

**UART communication**

The UART communication forms the basic of the FP operation because via this interface the SC14CVMDECT SF is controlled.

**FP MMI**

The MMI state machine must handle the call setup and call termination on the FP.

**Display interface**

The MCU/ FP handles the display interface including the display driver.

**Keyboard interface**

The MCU/ FP handles the keyboard interface including the keyboard driver.

**Audio handling**

The Application Software state machine must control when to open and close the audio. The FP MMI must handle the volume control.

**Tone handling**

The Application Software state machine must control when to play tones and the volume setting. Custom melodies can be defined in VES.

## 8.3 HARDWARE DESIGN GUIDELINES

Within this section general design guidelines for SC14CVMDECT SF FP and PP applications are given.

### 8.3.1 Circuit design guidelines

For a reference schematic refer to the SC14CVMDECT SF reference kit. With the reference kit package a non-cost optimised reference design is presented.

For an FP hardware design the following hardware parts will be needed besides the SC14CVMDECT SF:

- Supply voltage
- Battery charge
- LED and buttons
- Audio:
  - Headset
  - External PCM device.

For a PP hardware design the following hardware parts will be needed besides the SC14CVMDECT SF:

- Power
- Battery Charger
- Audio:
  - Microphone
  - Earpiece
  - Speaker
  - Headset

### 8.3.2 PCB Design Guidelines

- Because of the presence of the digital radio frequency burst with 100 Hz time division periods (TDD noise), supply ripple and RF radiation, special attention is needed for the power supply and ground PCB layout.
- Power supply considerations
  Both high and low frequency bypassing of the supply line connections should be provided and placed as close as possible to the SC14CVMDECT SF. In order to get the best overall performance for both FP and PP applications, a number of considerations for the PCB has to be taken into account.
  - Make angle breaks on long supply lines to avoid resonance frequencies in respect to DECT frequencies. Maximum 8 cm before an angle break is recommended.
  - Supply lines should be placed as far as possible away from sensitive audio circuits. If it is necessary to cross supply lines and audio lines, it should be done with right angles between supply and audio lines/circuits (microphone, ear-speaker, speakerphone, etc.)
  - Ground plane considerations
    In order to achieve the best audio performance and to avoid the influence of power supply noise, RF radiation, TDD noise and other noise sources, it is important that the audio circuits on both FP and PP applications boards are connected to the VREFM pin (analog ground: AGND, see Figure 38) on the SC14CVMDECT SF with separate nets in the layout.
    It is advised to provide the following audio circuits with separate ground nets connected to the VREFM pin:
    - Microphone(s)
    - Headset microphone and speaker
    - Speakerphone (signal grounds)

Depending on the layout it may also be necessary to bypass a number of the audio signals listed above to avoid humming, noise from RF radiation and TDD noise with. It is also important to choose a microphone of appropriate quality with a high RF immunity (with built-in capacitor).

- ESD performance
  Besides TDD noise, the ESD performance is important for the end-application. In order to achieve a high ESD performance supply lines should be placed with a large distance from charging terminals, display, headset connector and other electrical terminals with direct contact to the ESD source.
  On a two-layer PCB application it is important to keep a simulated one layer ground. With a stable ground ESD and TDD noise performance will always improve.
- Clearance around test patterns
  Pin number 81 to 88 are used for production test purposes. In order to avoid any interference or disturbance the area around these signal pins must be kept clear of any signal and/or GND. The recommended clearance is at least 1 mm as shown in Figure 36.

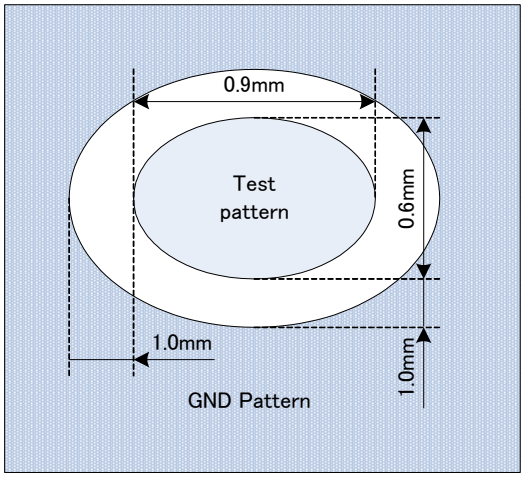



**Figure 36: Clearance around test patterns**

### 8.4 MODULE PLACEMENT ON THE MAIN BOARD

In order to ensure FCC compliance, proper coverage and to avoid detuning of the antennas, it is required to place the module free on the main board in relation to other surrounding materials.

Keep a distance of at least 10 mm from the antenna elements to conducting objects and at least 5 mm to non-conducting objects.

Keep in mind that electrical shielding objects, even partly surrounding the antennas, will normally cause a significant degradation of the coverage.

Place the module at the edge of the main-board as shown in Figure 37.

If the module has to be placed away from the edge of the main board, then avoid conducting areas in front of the antennas and make a cut-out in the main board underneath the antennas as shown in the figure.

Keep solid ground on layer 2 out to the edges of the main board as shown in the figure.

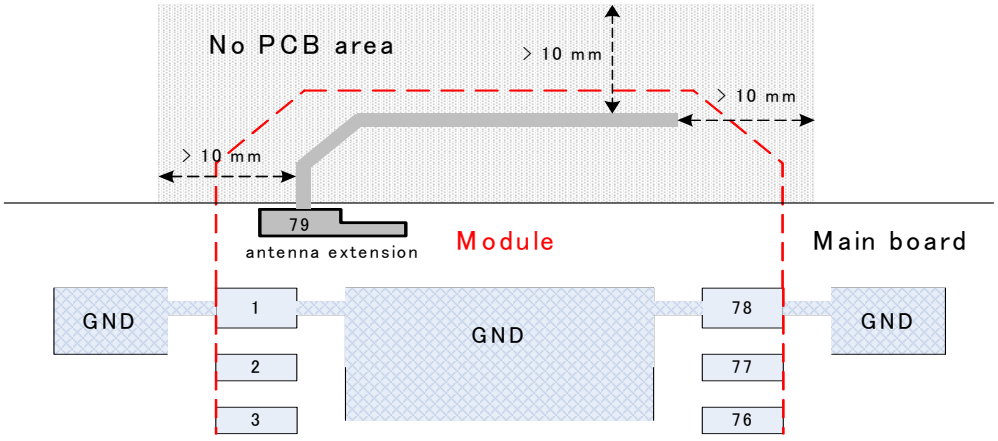



**Figure 37: Module placement on the main board (top view)**

### 8.5 PATTERN FOR PIN 79 ON THE MAIN BOARD

The copper pattern for pin 79 on the main board is very important because it is part of the internal antenna of the module. It is used to extend the internal antenna for optimum RF performance.

The PCB pattern shown in Figure 41 under “pads C” for pin 79 on the main board was used during module certification.

### 8.6 PRECAUTIONS REGARDING UNINTENDED COUPLING

The SC14CVMDECT SF includes an internal antenna, so at integration on the main board precautions shall be taken in order to avoid any kind of coupling from the main board to the RF part of the module.

If there is any doubt about this, a brief radio test should be performed.

## 9.0 Example application diagram

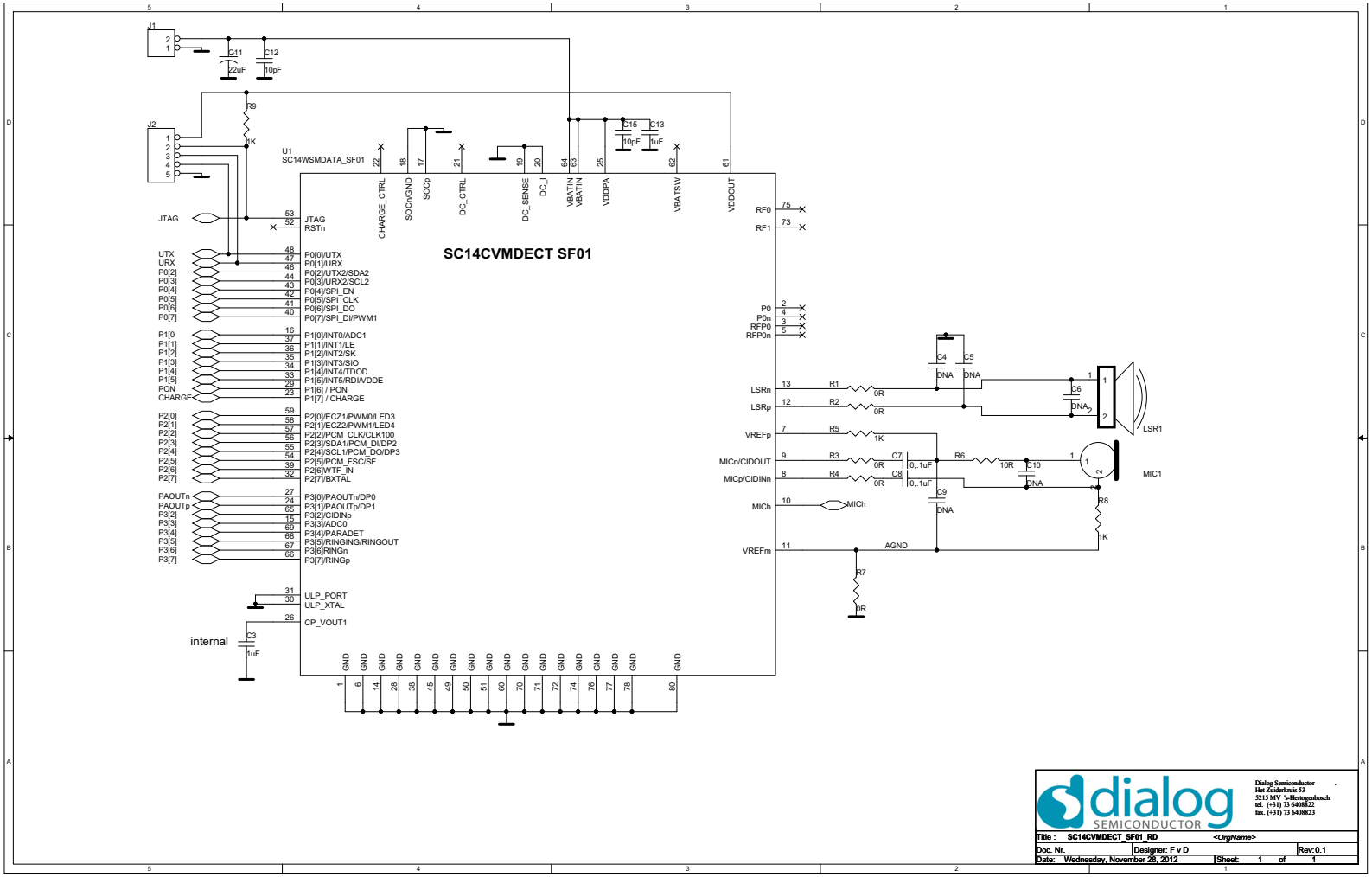



**Figure 38: Example application diagram**

## 10.0 Notices to OEM

**The end product has to be certified again if it has been programmed with other software than Dialog standard software stack for portable part and/or uses one or two external antenna(s). (See [6] for more detailed information).**

### 10.1 FCC REQUIREMENTS REGARDING THE END PRODUCT AND THE END USER.

The end product that the module is integrated into must be marked as follows:

“Contains Transmitter Module FCC ID: Y82-SC14S / IC: 9576A-SC14S”

The literature provided to the end user must include the following wording:

**FCC compliance statement**

This device complies with Part 15 of the FCC Rules for **only portable part**.

Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation of the device.

Module transmetteur ID IC: 9576A-SC14S.

Son fonctionnement est soumis aux deux conditions suivantes: (1) cet appareil ne doit pas causer d’interférences nuisibles et (2) appareil doit accepter toute interférence reçue, y compris les interférences qui peuvent perturber le fonctionnement.

Changes or modifications to the equipment not expressly approved by the Party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generate, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Privacy of communications may not be ensured when using this phone.

### 10.2 INDUSTRY CANADA REQUIREMENTS REGARDING THE END PRODUCT AND THE END USER

The host device shall be properly labelled to identify the modules within the host device. The Industry Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the Industry Canada certification number of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains transmitter module IC: 9576A-SC14S

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification d'Industrie Canada d'un module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une etiquette donnant le numéro de certification du module d'Industrie Canada, précédé des mots " Contient un module d'émission ", du mot " Contient " ou d'une formulation similaire exprimant le même sens, comme suit :

Contient le module d'émission IC: 9576A-SC14S

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

CAN ICES-3 (B)/NMB-3(B)

### 10.3 END APPLICATION APPROVAL

The module is intended to be used in an end application. Type approval concerning the end product, except for the module, should of cause be done. Please contact a test house in order to clarify what is needed.

### 10.4 SAFETY REQUIREMENTS

This section provides of an overview of the safety requirements that must be adhered to when working with the SC14CVMDECT SF.

- The specific external power supply for the SC14CVMDECT SF has to fulfil the requirements according to clause 2.5 (Limited power source) of this standard EN 60950-1:2006.
- Interconnection circuits shall be selected to provide continued conformance to the requirements of clause 2.2 for SELV (Safety Extra Low Voltage) circuits according to EN 60950-1:2006 after making connections.
- Interface type: not subjected to overvoltages (i.e. does not leave the building).
- Requirements additional to those specified in this standard may be necessary for:
  - Equipment intended for operation in special environments (for example, extremes of temperature, excessive dust, moisture or vibration, flammable gases and corrosive or explosive atmospheres).
  - Equipment intended to be used in vehicles, on board ships or aircraft, in tropical countries or at altitudes greater than 2000 m.
  - Equipment intended for use where ingress of water is possible.
- Installation by qualified personnel only!
- The product is a component intended for installation and use in complete equipment. The final acceptance of the component is dependent upon its installation and use in complete equipment.

# 11.0 Package information

## 11.1 SOLDERING PROFILE

The SC14CVMDECT SF should be soldered using a lead-free reflow soldering profile as shown below. Adjustments to the profile may be necessary depending on process requirements.

Recommended solder paste for lead-free soldering:

Sn 96.5 % - Ag 3.0 % - Cu 0.5 %.

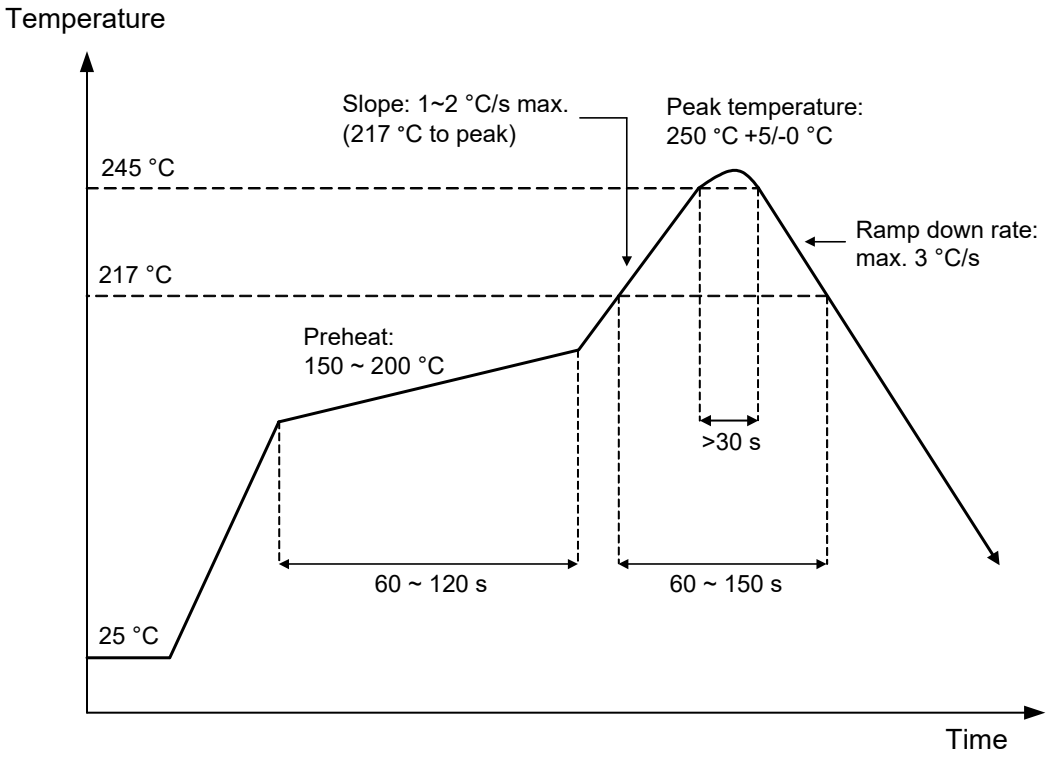



**Figure 39: Reflow profile (lead-free)**

## 11.2 MOISTURE SENSITIVITY LEVEL (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH. before the solder reflow process.

The SC14CVMDECT SF is qualified to MSL 3.

| MSL Level | Floor Life Time |
|---|---|
| MSL 4 | 72 hours |
| MSL 3 | 168 hours |
| MSL 2A | 4 weeks |
| MSL 2 | 1 year |
| MSL 1 | Unlimited at 30 °C/85 % RH |

### 11.3 COPPER PAD, SOLDER OPENING AND STENCIL

For the stencil a thickness of 0.130 mm is recommended. Recommended copper pad, solder mask opening and stencil are shown below.

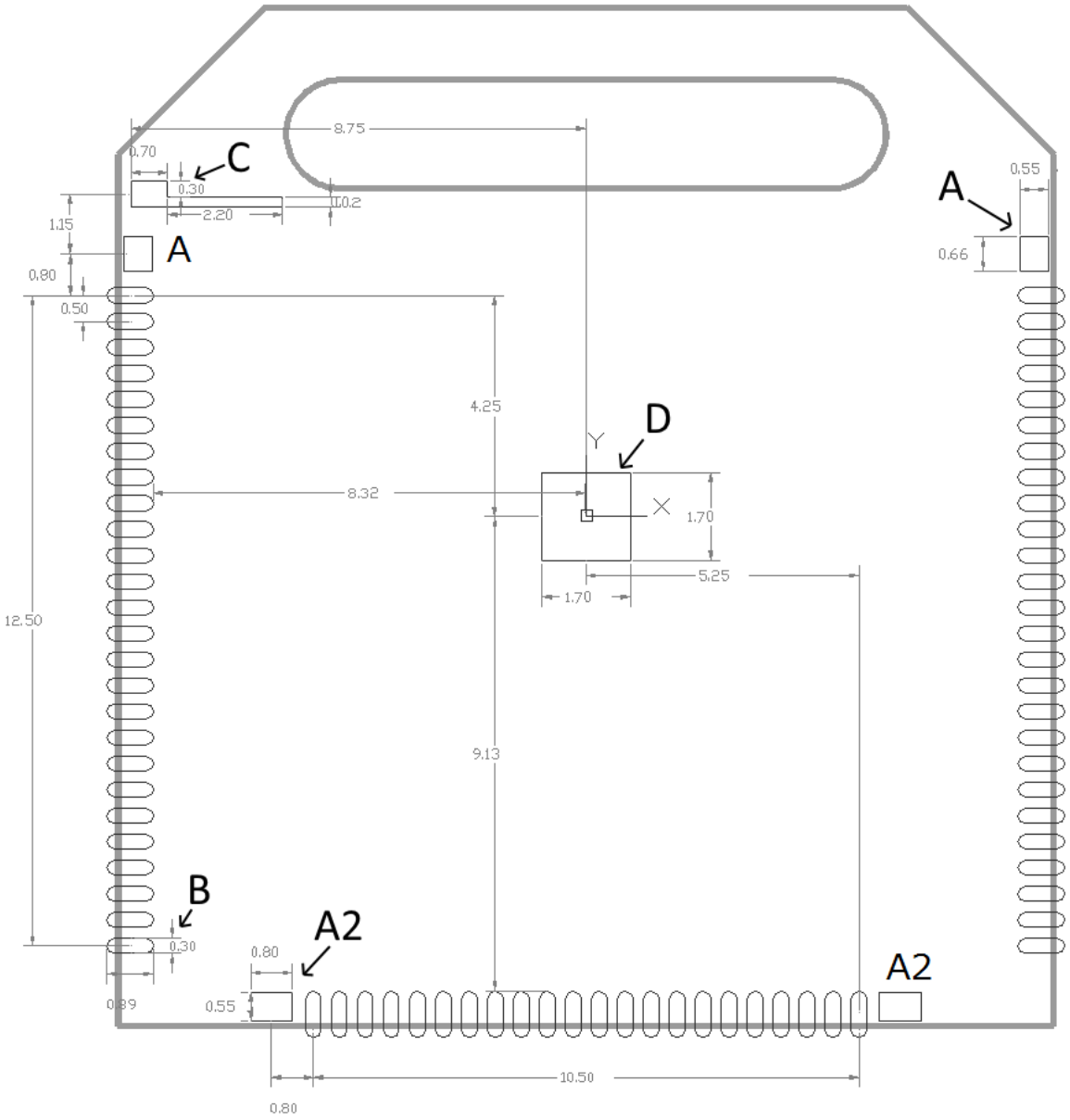



**Figure 40: Pad dimensions**

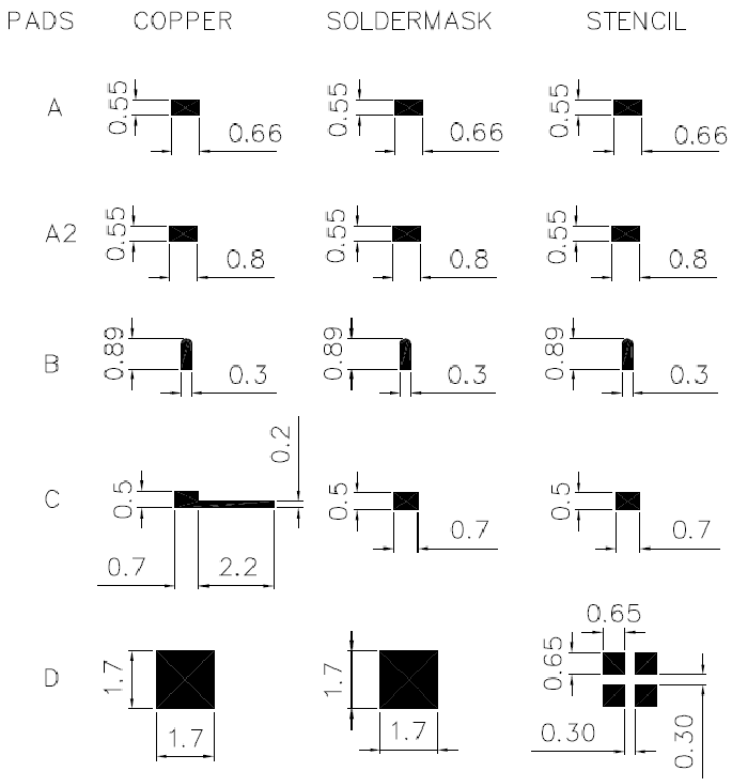



**Figure 41: Copper pad, Solder mask opening and Stencil**

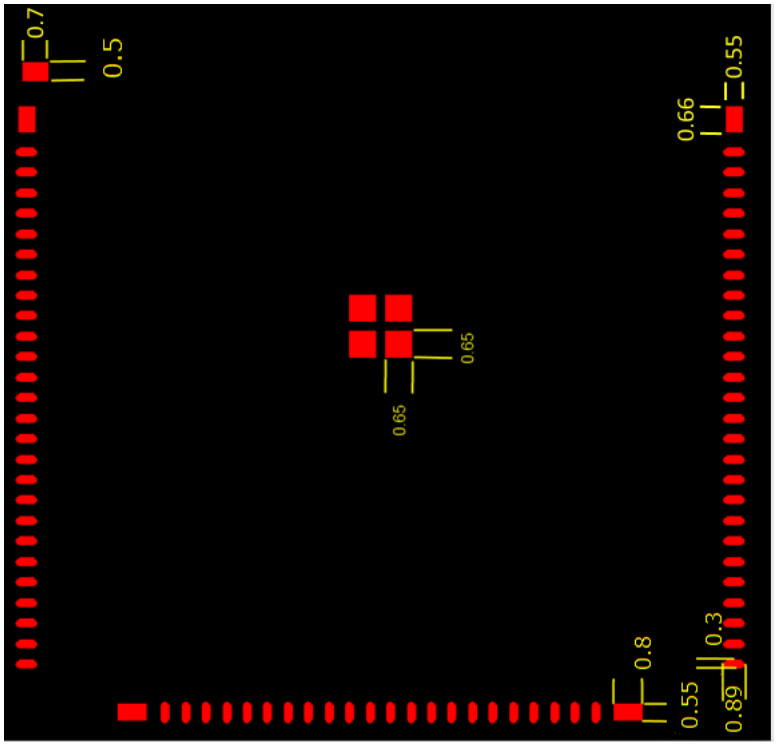
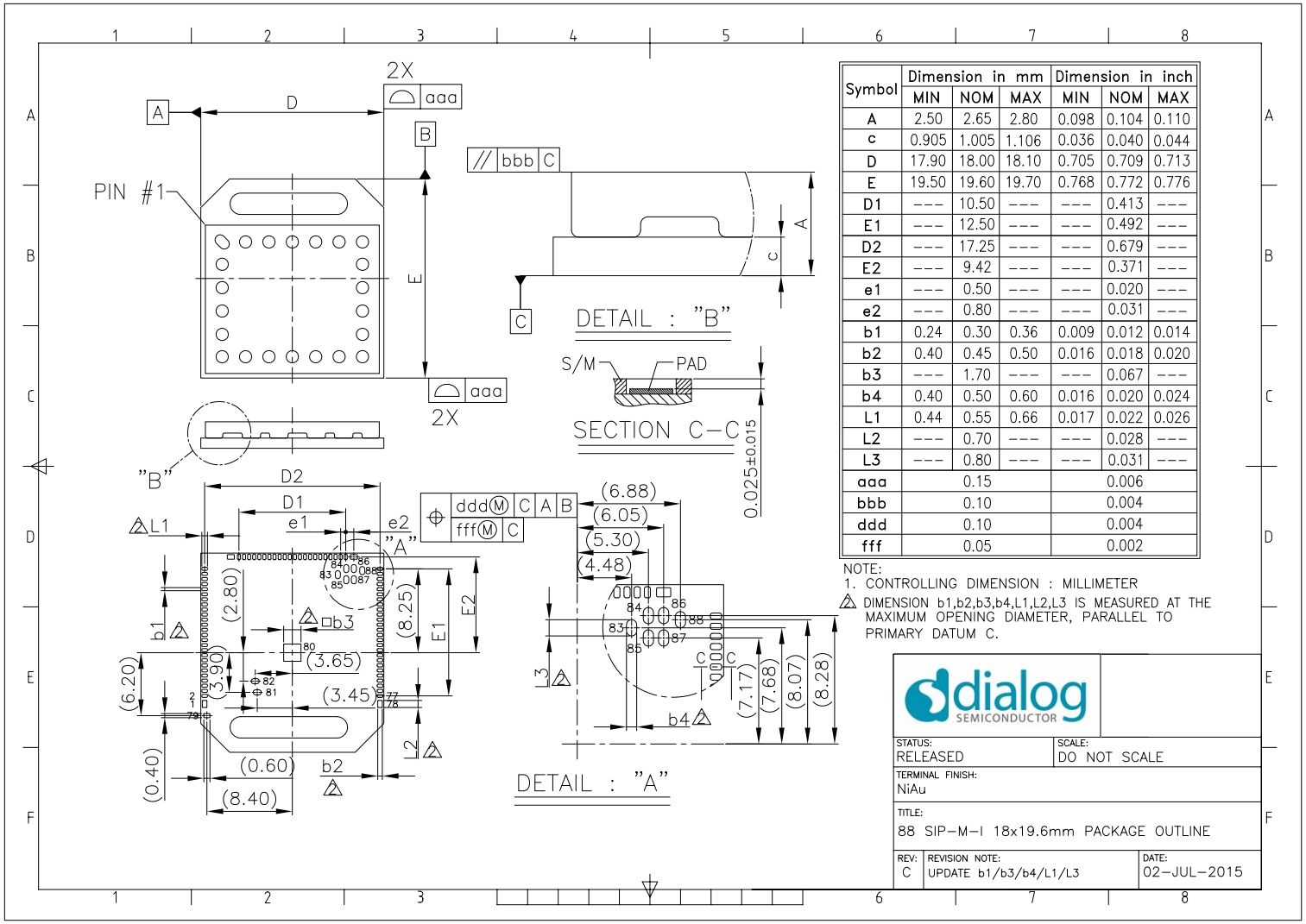



**Figure 42: Solder stencil**

### 11.4 MECHANICAL DIMENSIONS




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 2.50 | 2.65 | 2.80 | 0.098 | 0.104 | 0.110 |
| c | 0.905 | 1.005 | 1.106 | 0.036 | 0.040 | 0.044 |
| D | 17.90 | 18.00 | 18.10 | 0.705 | 0.709 | 0.713 |
| E | 19.50 | 19.60 | 19.70 | 0.768 | 0.772 | 0.776 |
| D1 | --- | 10.50 | --- | --- | 0.413 | --- |
| E1 | --- | 12.50 | --- | --- | 0.492 | --- |
| D2 | --- | 17.25 | --- | --- | 0.679 | --- |
| E2 | --- | 9.42 | --- | --- | 0.371 | --- |
| e1 | --- | 0.50 | --- | --- | 0.020 | --- |
| e2 | --- | 0.80 | --- | --- | 0.031 | --- |
| b1 | 0.24 | 0.30 | 0.36 | 0.009 | 0.012 | 0.014 |
| b2 | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| b3 | --- | 1.70 | --- | --- | 0.067 | --- |
| b4 | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.44 | 0.55 | 0.66 | 0.017 | 0.022 | 0.026 |
| L2 | --- | 0.70 | --- | --- | 0.028 | --- |
| L3 | --- | 0.80 | --- | --- | 0.031 | --- |
| aaa | | 0.15 | | | 0.006 | |
| bbb | | 0.10 | | | 0.004 | |
| ddd | | 0.10 | | | 0.004 | |
| fff | | 0.05 | | | 0.002 | |

**Figure 43: Package outline drawing**

## 12.0 Revision history

**09-Jul-2013 v1.0:**

- Initial version.

**12-Sep-2013 v1.1:**

- Ordering code for tray version corrected.
- Ordering code for tape-on-reel version removed.

**08-Nov-2013 v1.2:**

- Added section 10.2 (Industry Canada requirements regarding the end product and the end user).

**31-Jan-2014 v1.3:**

- Updated section 11.3 (Copper pad, solder opening and stencil).

**11-Feb-2014 v1.4:**

- Corrected section 11.3 (Copper pad, solder opening and stencil).

**16-Apr-2014 v1.5:**

- Added an explanation for RF1 in section 4.13.

**29-Aug-2014 v1.6:**

- Changed RF output power specification.
- Added SF02 description.

**24-Dec-2014 v1.7:**

- Updated section 4.13.2 (Internal and external antenna with FAD).

**28-Jul-2015 v3.0 (Final):**

- Product status: Production.
- Features:
  - Added support for NiMH and Alkaline batteries.
- Section 1.0:
  - Ordering information table added (Table 1).
- Section 2.2:
  - Reference to AN-D-204 removed.
  - Reference [4] updated with file name.
  - Reference [6] changed from AN-D-211 to AN-D-212.
  - Reference [7] corrected to AN-D-222.
- Section 3.2:
  - Added default configuration: US DECT, FP and CoLA enabled.
- Section 4.1 (Caution):
  - Added max. UART input voltage (3.45 V).
- Section: 3.9:
  - Number of PP registrations per FP rephrased (Table 5).
- Section 6.0 (Register descriptions) added.
- Supply currents moved from section 7.8 to new section 7.4.
- Updated supply currents for full-slot operation (Table 19) and for long-slot operation (Table 20).
- Table 35 (Radio specifications):
  - Added HPM to conditions for NTP.
  - Added NTP specification for LPM.
- Table 36 (RFPA preferred settings):
  - Removed '(PP application)' from title, because RFPA settings are valid for both FP and PP.
  - Note 32: added Japan DECT specification for long-slot operation.
- Table 38 (RF frequencies and channel numbers):
  - Note 33 added for J-DECT channels 1, 2 and 3.
- Section 10.0: added link to reference [6].
- Section 11.0:
  - Reflow soldering profile updated (Figure 39).
  - Soldering stencil thickness changed to 0.130 mm.
  - Package outline drawing updated (Figure 43).
- Back page:
  - Status definition table updated.
  - Contact information updated.
- Template updated to latest version.

## Status definitions

| Version | Datasheet status | Product status | Definition |
|---|---|---|---|
| 1.<n> | Target | Development | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| 2.<n> | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
| 3.<n> | Final | Production | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications. |
| 4.<n> | Obsolete | Archived | This datasheet contains the specifications for discontinued products. The information is provided for reference only. |

## RoHS compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/


### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.