ISL80102, ISL80103

High Performance 2A and 3A Linear Regulators

FN6660
Rev.9.02
Jun 11, 2020

The ISL80102 and ISL80103 are low voltage, high-current, single output LDOs specified for 2A and 3A output current, respectively. These LDOs operate from the input voltages of 2.2V to 6V and are capable of providing the output voltages of 0.8V to 5.5V.

An external capacitor on the soft-start pin provides adjustment for applications that demand inrush current less than the current limit. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode. A submicron BiCMOS process is used for this product family to deliver best-in-class analog performance and overall value.

These CMOS (LDOs) consume significantly lower quiescent current as a function of load over bipolar LDOs, so they are more efficient and allow packages with smaller footprints. The quiescent current has been modestly compromised to enable a leading class fast load transient response, and hence a lower total AC regulation band for an LDO in this category.

Related Literature

For a full list of related documents, visit our website

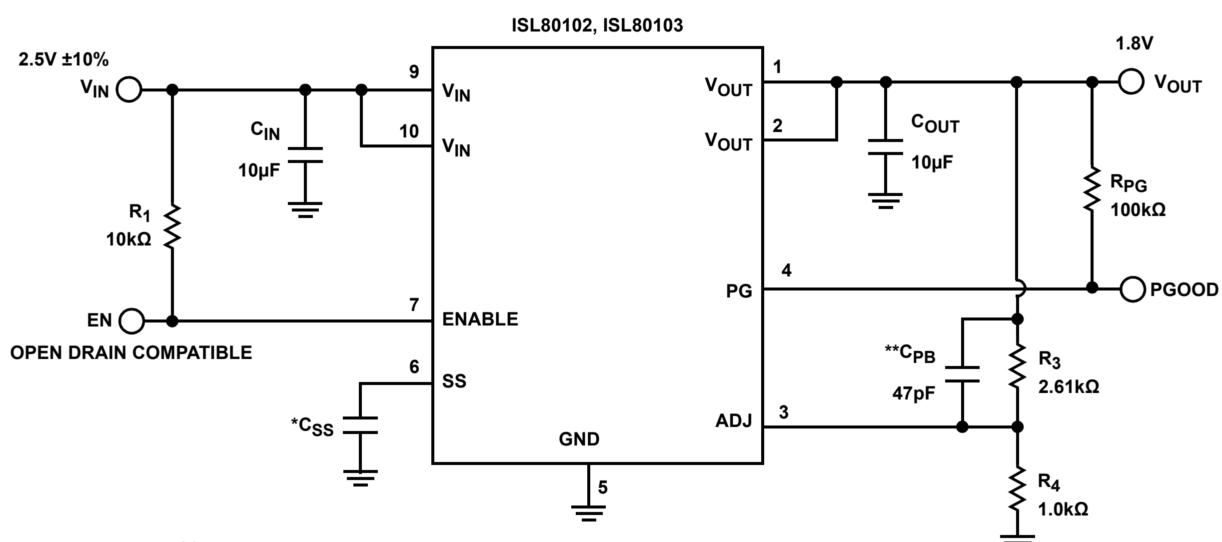
- ISL80102, ISL80103 product pages

Features

- Stable with ceramic capacitors (Note 11)
- 2A and 3A output current ratings
- 2.2V to 6V input voltage range
- ±1.8% V_{OUT} accuracy assured over line, load, and T_J = -40°C to +125°C
- Very low 120mV dropout voltage at 3A (ISL80103)
- Very fast transient response
- Excellent 62dB PSRR
- 49µV_{RMS} output noise
- Power-good output
- Adjustable inrush current limiting
- Short-circuit and over-temperature protection
- Available in a 10 Ld DFN

Applications

- Servers
- Telecommunications and networking
- Medical equipment
- Instrumentation systems
- Routers and switchers



*CSS is optional (see Note 12 on page 5).

**C_{PB} is optional (see "Functional Description" on page 12 for more information).

FIGURE 1. TYPICAL APPLICATION DIAGRAM FOR ADJUSTABLE OUTPUT VOLTAGE VERSION

TABLE 1. COMPONENTS VALUE SELECTION

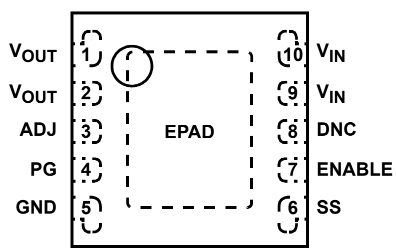
V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (Ω)	C_{PB} (pF)	C_{OUT} (µF)
5.0	2.61	287	47	10
3.3	2.61	464	47	10
2.5	2.61	649	47	10
1.8 (Note 1)	2.61	1.0k	47	10
1.8 (Note 1)	2.61	1.0k	82	22
1.5	2.61	1.3k	82	22
1.2	2.61	1.87k	150	47
1.0	2.61	2.61k	150	47
0.8	2.61	4.32k	150	47

NOTE:

1. Either option can be used depending on cost/performance requirements

Pin Configuration

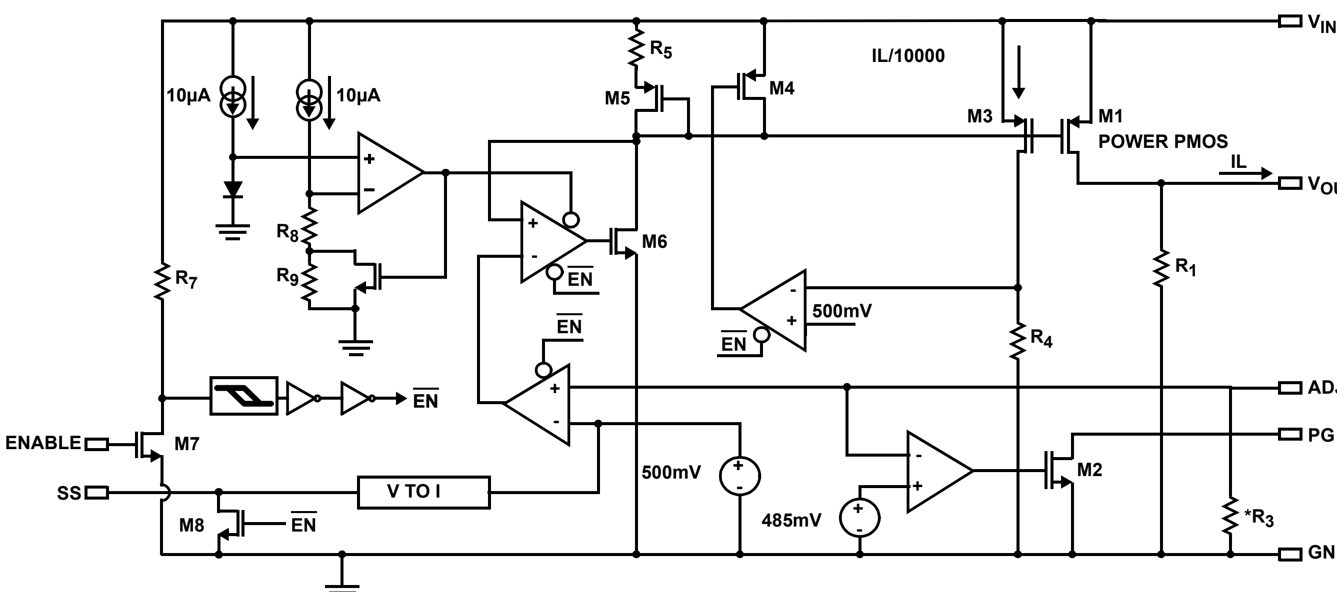
10 LD 3x3 DFN
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Output voltage pin
3	ADJ	ADJ pin for externally set V_{OUT}.
4	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
5	GND	GND pin
6	SS	External cap adjusts inrush current. Leave this pin open if not used.
7	ENABLE	V_{IN} independent chip enable. TTL and CMOS compatible.
8	DNC	Do not connect this pin to ground or supply. Leave floating.
9, 10	V_{IN}	Input supply pin
	EPAD	EPAD must be connected to a copper plane with as many vias as possible for proper electrical and optimal thermal performance.

Block Diagram



*R3 is open for ADJ versions.

FIGURE 2. BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 2, 4, 4)	PART MARKING	V_{OUT} VOLTAGE	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG DWG. #
ISL80102IRAJZ	DZJA	ADJ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3
ISL80102IRAJZ-T	DZJA	ADJ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3
ISL80102IRAJZ-TK	DZJA	ADJ	-40 to +125	1k	10 Ld 3x3 DFN	L10.3x3
ISL80102IRAJZ-T7A	DZJA	ADJ	-40 to +125	250	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ	DZAA	ADJ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ-T	DZAA	ADJ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ-TK	DZAA	ADJ	-40 to +125	4k	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ-T7A	DZAA	ADJ	-40 to +125	250	10 Ld 3x3 DFN	L10.3x3
ISL80102EVAL2Z	Evaluation Board					
ISL80103EVAL2Z	Evaluation Board					

NOTES:

2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL80102 and ISL80103 product information pages. For more information about MSL, see TB363.

Absolute Maximum Ratings (Note 8)

V_{IN} Relative to GND . . . . -0.3V to +6.5V
V_{OUT} Relative to GND . . . . -0.3V to +6.5V
PG, ENABLE, ADJ, SS, Relative to GND . . . . -0.3V to +6.5V
ESD Rating
 Human Body Model (Tested per JESD22 A114F). 2.2kV
 Charge Device Model (Tested per JESD22-C101C) 1kV
Latch-up (Tested per JESD78C, Class 2, Level A) . . . . . ±100mA at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 5, 6)	45	4

θ_{JB} at Pin 3 (Note 7). . . . . 14.7°C/W
θ_{JB} at Pin 5 (Note 7). . . . . 8.9°C/W
Maximum Junction Temperature (Plastic Package) . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Junction Temperature Range (T_J) . . . . -40°C to +125°C
V_{IN} Relative to GND . . . . .2.2V to 6V
V_{OUT} Range . . . . 800mV to 5.5V
PG, ENABLE, ADJ, SS Relative to GND. . . . . 0V to 6V
PG Sink Current 10mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at either lead #3 or lead #5, as applicable. See TB379
8. ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: 2.2V < V_{IN} < 6V, V_{OUT} = 0.5V, T_J = +25°C, I_{LOAD} = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Refer to “Functional Description” on page 12 and TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	2.2V < V_{IN} < 6V; I_{LOAD} = 0A		0.5		%
		2.2V < V_{IN} < 6V; 0A < I_{LOAD} < 3A	**-1.8**		**1.8**	%
		2.9V < V_{IN} < 6V; I_{LOAD} = 0A		0.5		%
		2.9V < V_{IN} < 6V; 0A < I_{LOAD} < full load	**-1.8**		**-1.8**	%
Feedback Pin	V_{ADJ}	0A < I_{LOAD} < full load	**491**	500	**509**	mV
DC Input Line Regulation	(V_{OUT} Low Line - V_{OUT} High Line)/ V_{OUT} Low Line	2.2V < V_{IN} < 3.6V, V_{OUT} = 1.8V	**-0.4**	0.1	**0.4**	%
		2.9V < V_{IN} < 6V, V_{OUT} = 2.5V	**-0.8**	0.1	**0.8**	%
DC Output Load Regulation	(V_{OUT} No Load - V_{OUT} High Load)/ V_{OUT} No Load	ISL80103, 0A < I_{LOAD} < 3A, 2.9V < V_{IN} < 6V; V_{OUT} = 2.5V	**-0.8**	-0.2	**0.8**	%
		ISL80102, 0A < I_{LOAD} < 2A 2.9V < V_{IN} < 6V; V_{OUT} = 2.5V	**-0.6**	-0.2	**0.6**	%
Feedback Input Current		V_{ADJ} = 0.5V		0.01	**1**	µA
Ground Pin Current	I_Q	I_{LOAD} = 0A, V_{OUT} + 0.4V < V_{IN} < 6V V_{OUT} = 2.5V		7.5	**9**	mA
		I_{LOAD} = 3A, V_{OUT} + 0.4V < V_{IN} < 6V V_{OUT} = 2.5V		8.5	**12**	mA
Ground Pin Current in Shutdown	I_{SHDN}	EN = 0V, V_{IN} = 5V		0.4		µA
		EN = 0V, V_{IN} = 6V		3.3	**16.0**	µA

Electrical Specifications Unless otherwise noted, all parameters are established over the following specified conditions: 2.2V < V_{IN} < 6V, V_{OUT} = 0.5V, T_J = +25°C, I_{LOAD} = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Refer to "Functional Description" on page 12 and TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Dropout Voltage (Note 10)	V_{DO}	ISL80103, I_{LOAD} = 3A, V_{OUT} = 2.5V		120	**185**	mV
		ISL80102, I_{LOAD} = 2A, V_{OUT} = 2.5V		81	**125**	mV
		ISL80103, I_{LOAD} = 3A, V_{OUT} = 5.5V		120	**244**	mV
		ISL80102, I_{LOAD} = 2A, V_{OUT} = 5.5V		60	**121**	mV
Output Short-Circuit Current (3A Version)	ISC	ISL80103, V_{OUT} = 0V		5.0		A
Output Short-Circuit Current (2A Version)		ISL80102, V_{OUT} = 0V		2.8		A
Thermal Shutdown Temperature	TSD			160		°C
Thermal Shutdown Hysteresis	TSDn			15		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD} = 1A; V_{IN} = 2.2V		55		dB
		f = 120Hz, I_{LOAD} = 1A; V_{IN} = 2.2V		62		dB
Output Noise Voltage		V_{IN} = 2.2V, V_{OUT} = 1.8V, I_{LOAD} = 3A, BW = 100Hz < f < 100kHz		49		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-On Threshold	$V_{EN(HIGH)}$	2.2V < V_{IN} < 6V	**0.616**	0.800	**0.950**	V
Turn-Off Threshold	$V_{EN(LOW)}$	2.2V < V_{IN} < 6V	**0.463**	0.600		V
Hysteresis	$V_{EN(HYS)}$	2.2V < V_{IN} < 6V		135		mV
Enable Pin Turn-On Delay	t_{EN}	C_{OUT} = 10µF, I_{LOAD} = 1A		150		µs
Enable Pin Leakage Current		V_{IN} = 6V, EN = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
Reset Pull-Down Resistance	RPD			323		Ω
Soft-Start Charge Current	ICHG		**-7.0**	-4.5	**-2.0**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	84	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		I_{SINK} = 500µA		47	**100**	mV
PG Flag Leakage Current		V_{IN} = 6V, PG = 6V		0.05	**1**	µA

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
10. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
11. Minimum cap of 10µF X5R/X7R on V_{IN} and V_{OUT} required for stability.
12. If the current limit for inrush current is acceptable in the application, do not use this feature (leave the SS pin open). Use only when large bulk capacitance is required on V_{OUT} for the application.

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

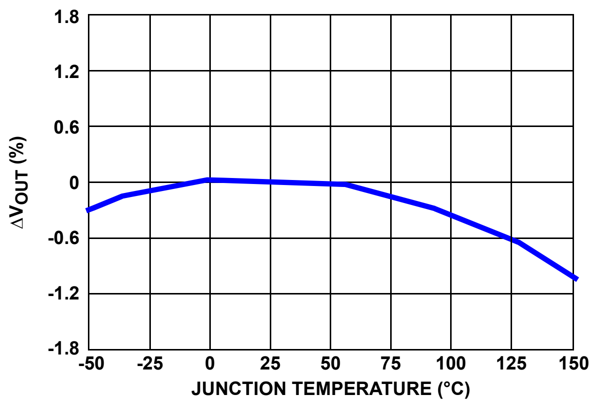


FIGURE 3. ΔV_{OUT} vs TEMPERATURE

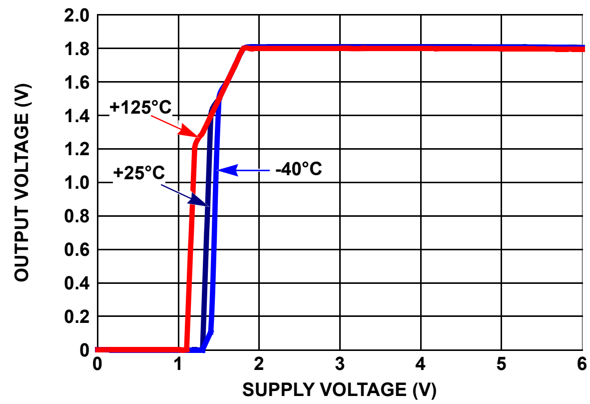


FIGURE 4. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

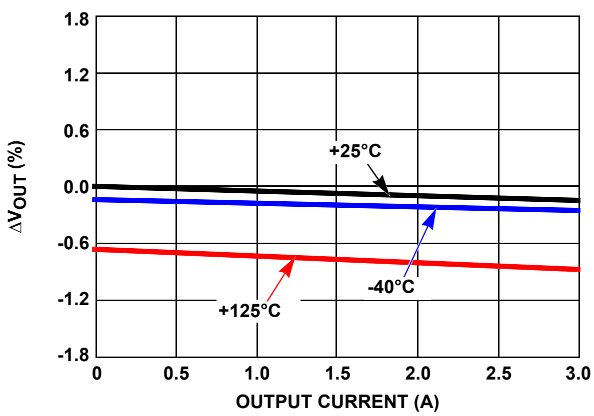


FIGURE 5. ΔV_{OUT} vs OUTPUT CURRENT

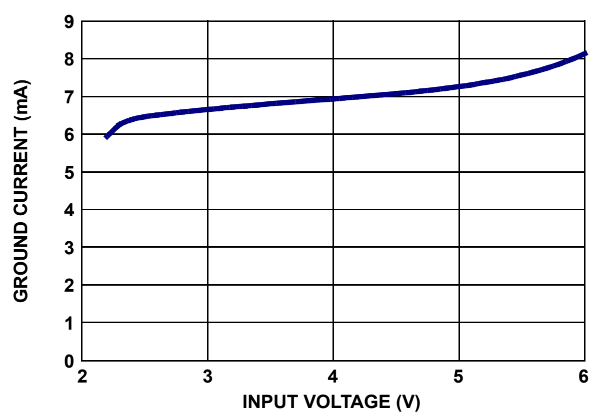


FIGURE 6. GROUND CURRENT vs SUPPLY VOLTAGE

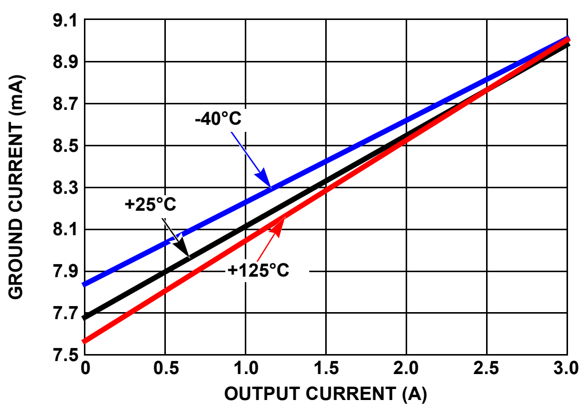


FIGURE 7. GROUND CURRENT vs OUTPUT CURRENT

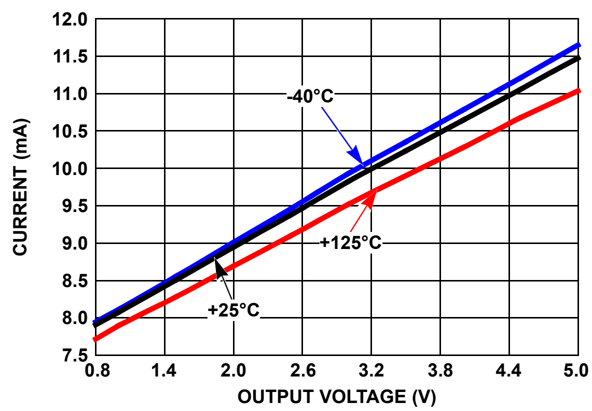


FIGURE 8. GROUND CURRENT vs OUTPUT VOLTAGE (V_{IN} = V_{OUT} + V_{DO})

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. (Continued)

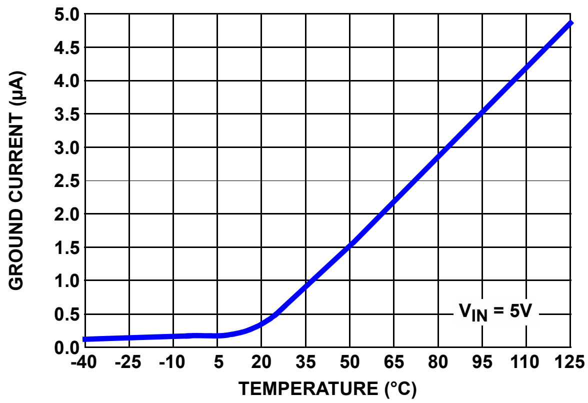


FIGURE 9. GROUND CURRENT IN SHUTDOWN vs TEMPERATURE

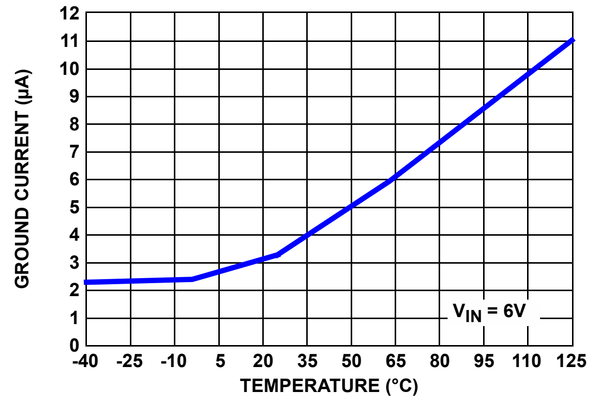


FIGURE 10. GROUND CURRENT IN SHUTDOWN vs TEMPERATURE

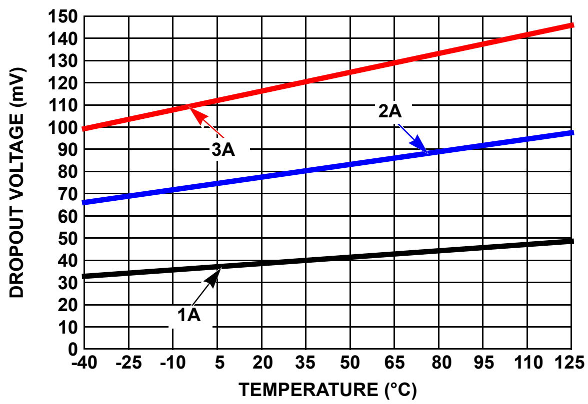


FIGURE 11. DROPOUT VOLTAGE vs TEMPERATURE

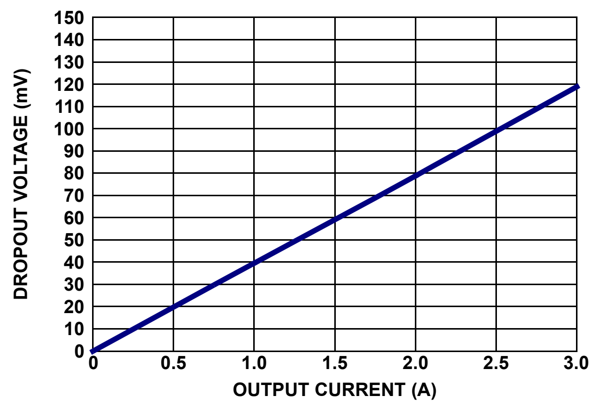


FIGURE 12. DROPOUT VOLTAGE vs OUTPUT CURRENT

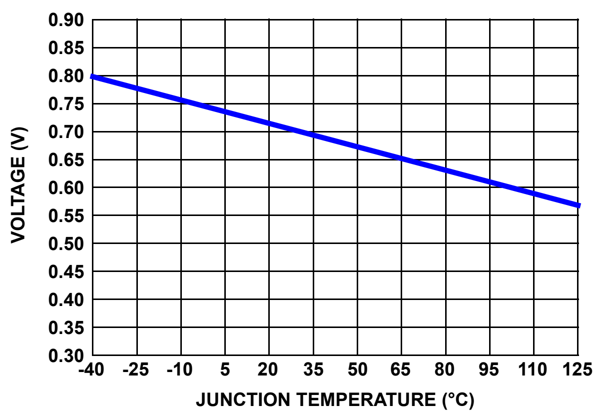


FIGURE 13. ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

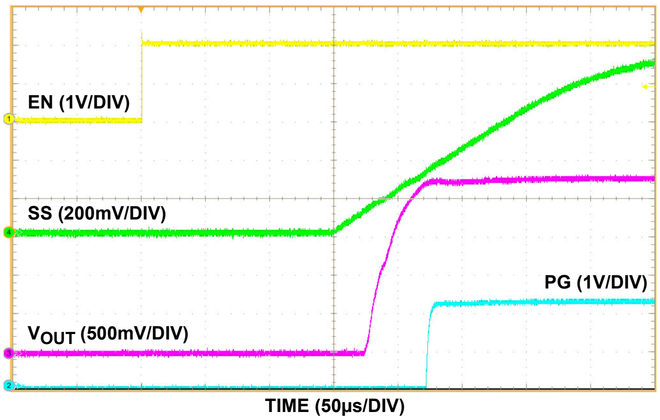


FIGURE 14. ENABLE START-UP SS CAP 1nF

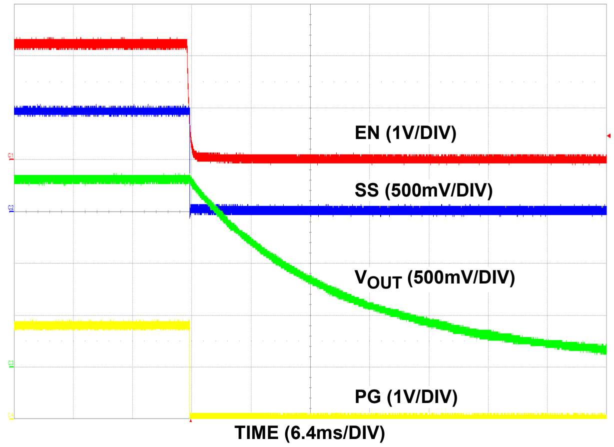


FIGURE 15. ENABLE SHUTDOWN SS CAP 1nF

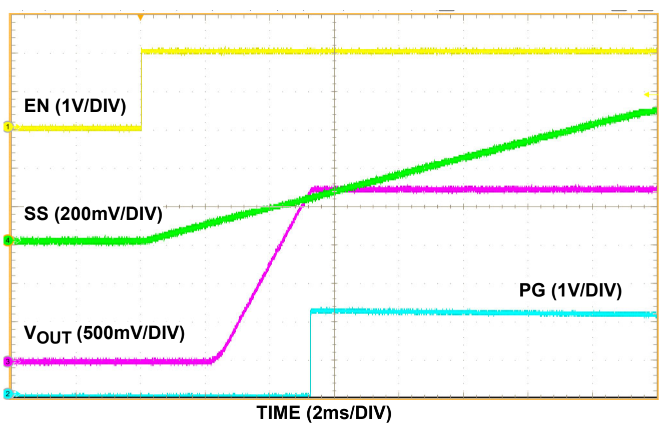


FIGURE 16. ENABLE START-UP SS CAP 100nF

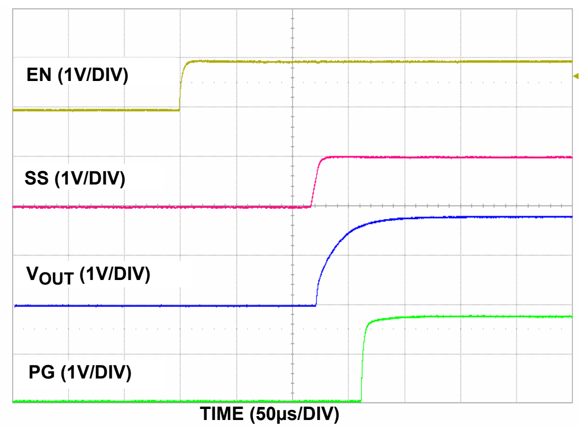


FIGURE 17. ENABLE START-UP (NO SS CAP)

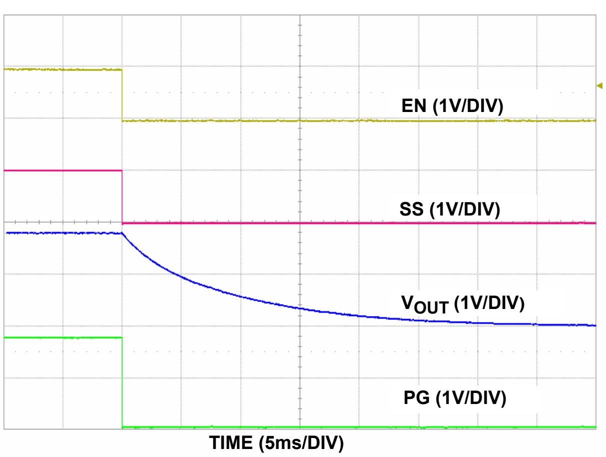


FIGURE 18. ENABLE SHUTDOWN (NO SS CAP)

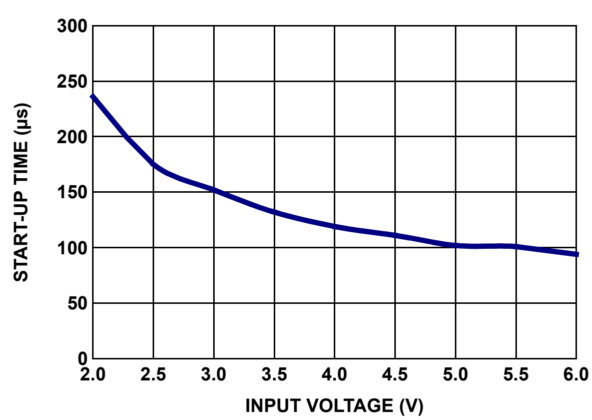


FIGURE 19. START-UP TIME vs SUPPLY VOLTAGE

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. (Continued)

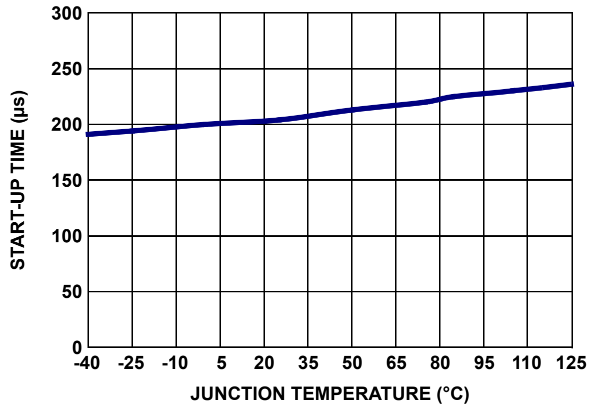


FIGURE 20. START-UP TIME vs TEMPERATURE

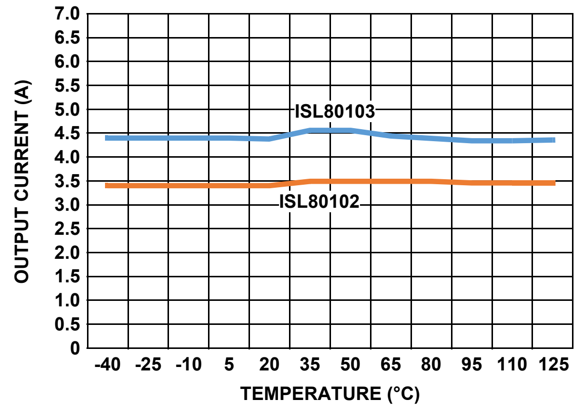


FIGURE 21. CURRENT LIMIT vs TEMPERATURE

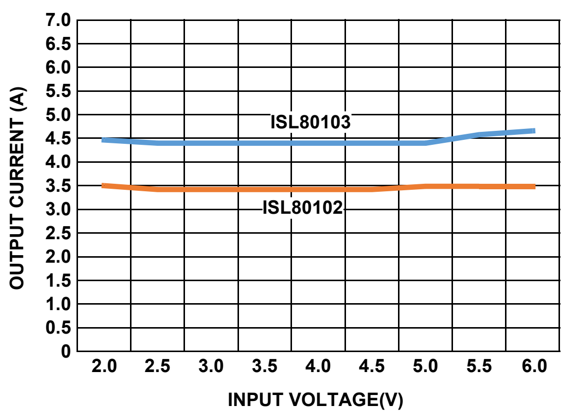


FIGURE 22. CURRENT LIMIT vs SUPPLY VOLTAGE

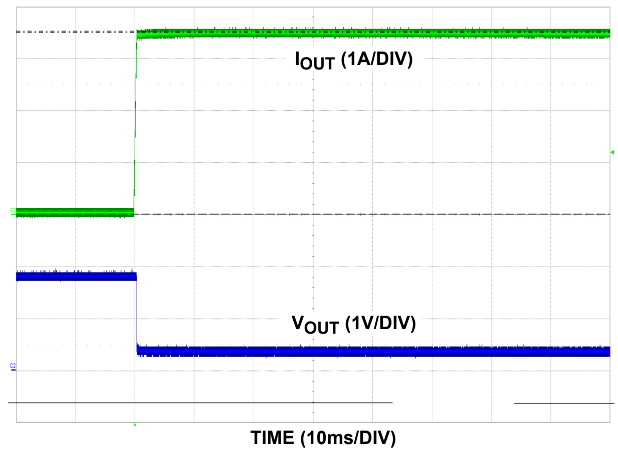


FIGURE 23. CURRENT LIMIT RESPONSE (ISL80102)

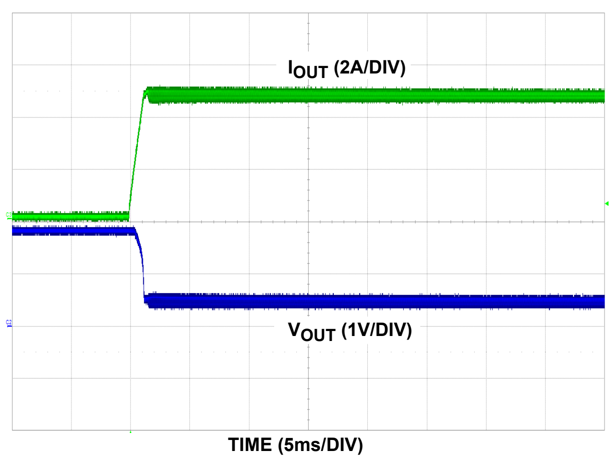


FIGURE 24. CURRENT LIMIT RESPONSE (ISL80103)

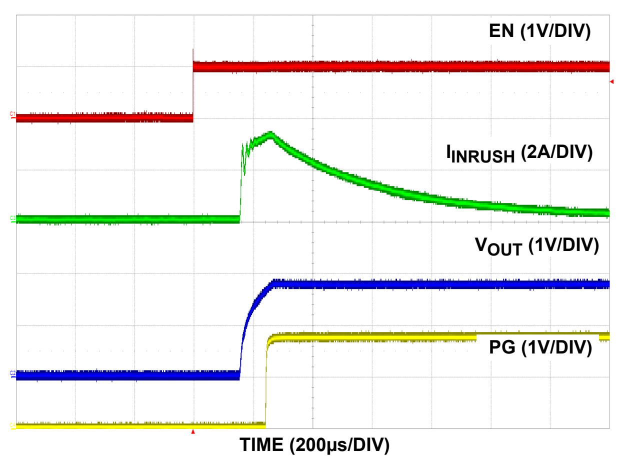


FIGURE 25. INRUSH CURRENT WITH NO SOFT-START CAPACITOR, C_{OUT} = 1000µF

Typical Operating Performance
Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

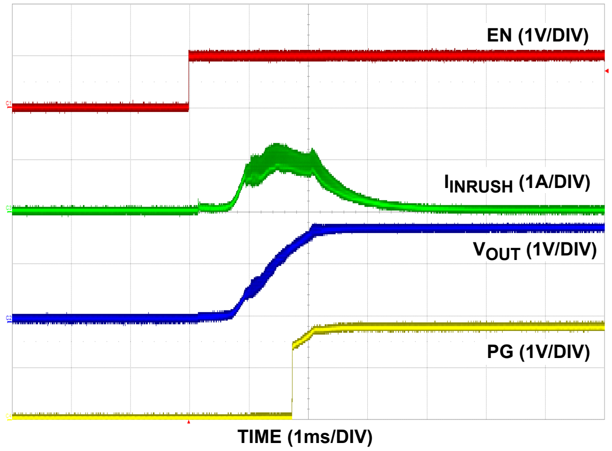


FIGURE 26. INRUSH WITH 22nF SOFT-START CAPACITOR, C_{OUT} = 1000µF

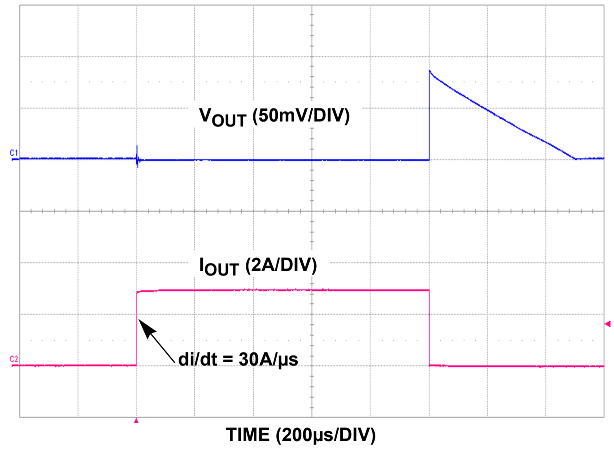


FIGURE 27. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC

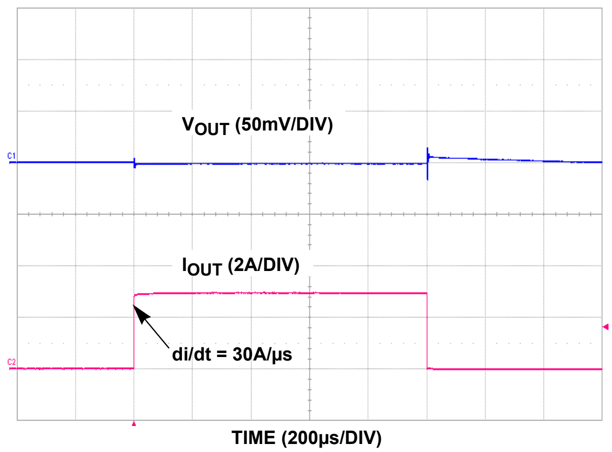


FIGURE 28. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC + 100µF OSCON

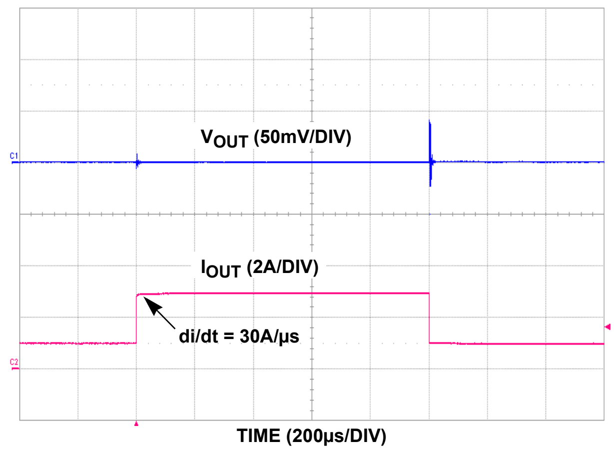


FIGURE 29. LOAD TRANSIENT 1A TO 3A, C_{OUT} = 10µF CERAMIC

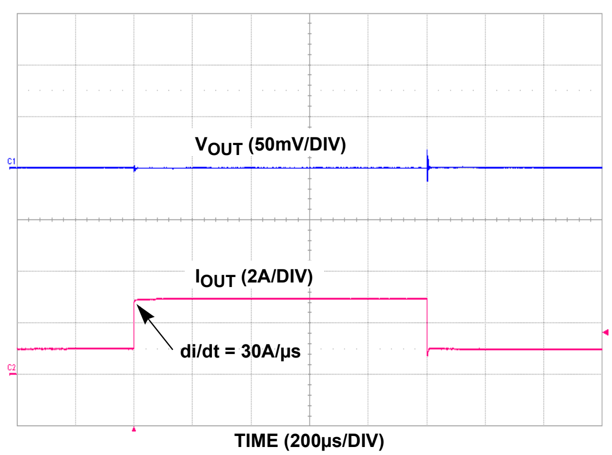


FIGURE 30. LOAD TRANSIENT 1A TO 3A, C_{OUT} = 10µF CERAMIC + 100µF OSCON

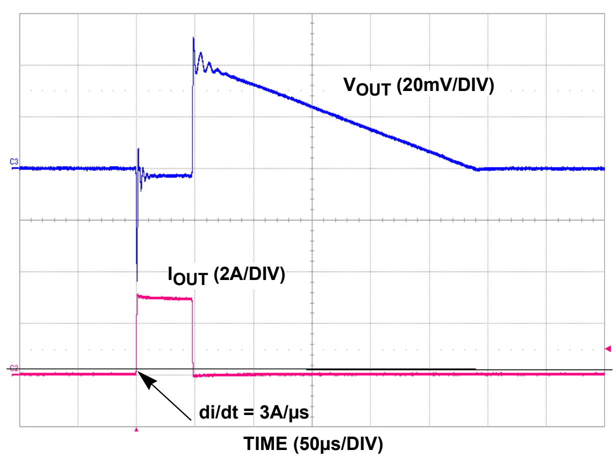


FIGURE 31. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, NO C_{PB}

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. (Continued)

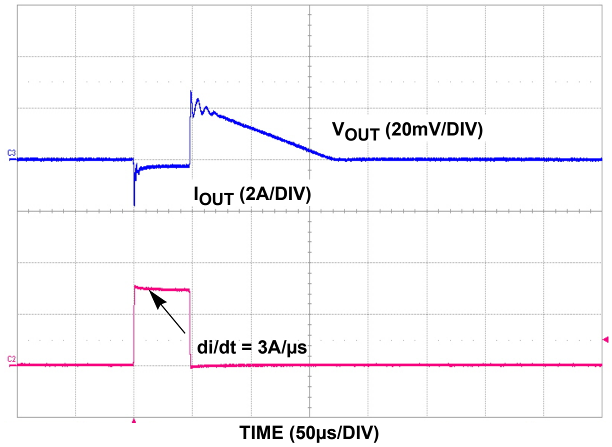


FIGURE 32. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, C_{PB} = 1500pF

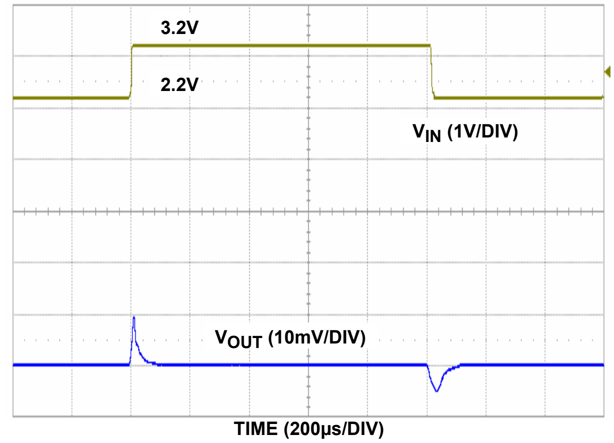


FIGURE 33. LINE TRANSIENT

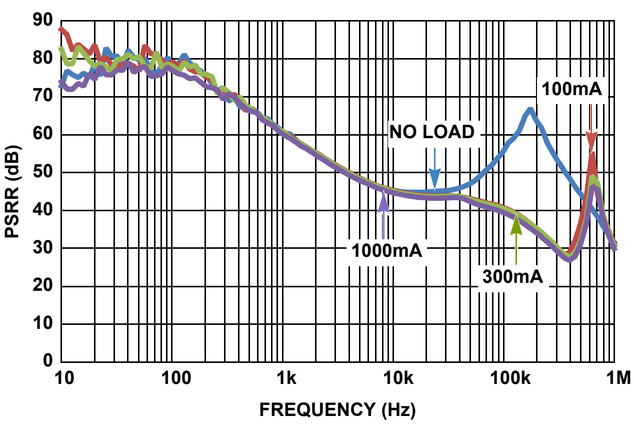


FIGURE 34. PSRR vs FREQUENCY FOR V_{OUT} = 1.0V, V_{IN} = 2.5V; C_{OUT} = 47µF, C_{PB} = 150pF

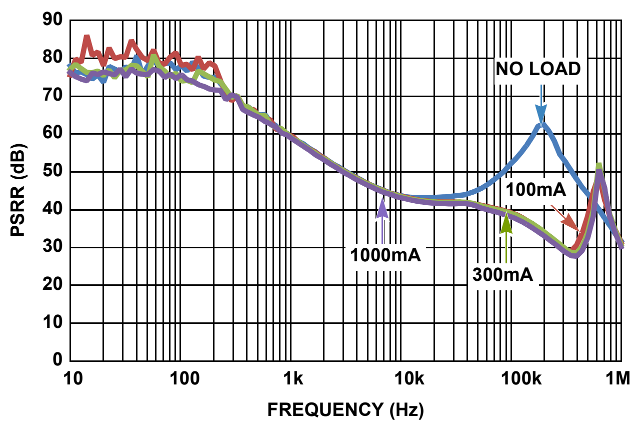


FIGURE 35. PSRR vs FREQUENCY FOR V_{OUT} = 1.2V; V_{IN} = 2.5V; C_{OUT} = 47µF, C_{PB} = 150pF

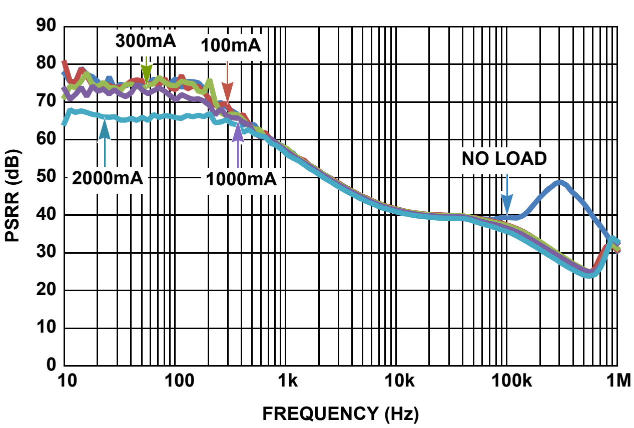


FIGURE 36. PSRR vs FREQUENCY FOR V_{OUT} = 1.5V, V_{IN} = 2.5V; C_{OUT} = 22µF, C_{PB} = 82pF

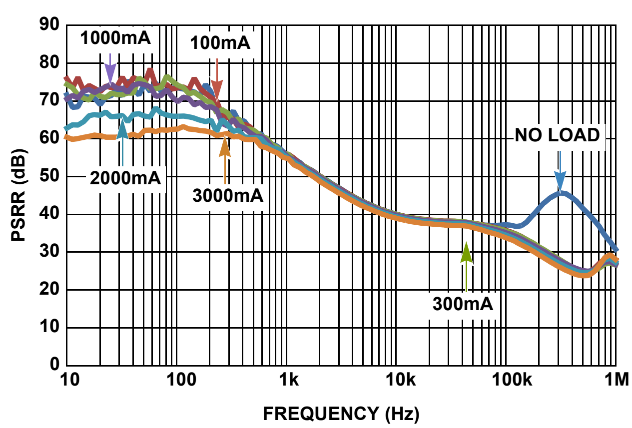


FIGURE 37. PSRR vs FREQUENCY FOR V_{OUT} = 1.8V, V_{IN} = 2.5V; C_{OUT} = 22µF, C_{PB} = 82pF

Typical Operating Performance

Unless otherwise noted, V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. (Continued)

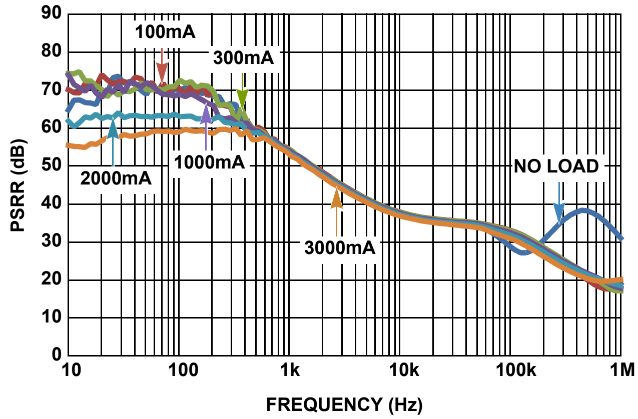


FIGURE 38. PSRR vs FREQUENCY FOR V_{OUT} = 2.5V, V_{IN} = 3.3V; C_{OUT} = 10µF, C_{PB} = 47pF

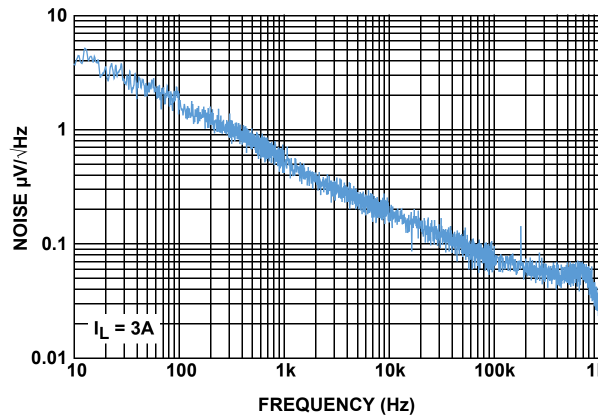


FIGURE 39. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

Input Voltage Requirements

This family of LDOs is optimized for a true 2.5V to 1.8V conversion in which the input supply can have a tolerance of as much as ±10% for conditions noted in the “Electrical Specifications” table on page 4. The minimum guaranteed input voltage is 2.2V; however, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The dropout of this family of LDOs has been generously specified to allow applications to design for a level of efficiency that can accommodate the smaller outline package.

Enable Operation

The Enable turn-on threshold is typically 800mV with a hysteresis of 135mV. This pin must not be left floating. This pin must be tied to V_{IN} if it is not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the Enable pin. The Enable pin can be connected directly to V_{IN} for applications that are always on.

Power-Good Operation

Applications not using the power-good (PGOOD) feature must connect this pin to ground. The PGOOD flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PGOOD pin requires an external pull-up resistor, which is typically connected to the V_{OUT} pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{IN}. PGOOD faults can be caused by the output voltage going below 84% of the nominal output voltage, or the current limit fault, or low input voltage. PGOOD does not function during thermal shutdown.

Soft-Start Operation (Optional)

If the current limit for inrush current is acceptable in the application, do not use the soft-start (SS) feature (leave the SS pin open). The soft-start circuit controls the rate at which the output voltage comes up to regulation at power-up or LDO enable. The external soft-start capacitor always gets discharged to ground pin potential at the beginning of start-up or enabling. After the capacitor discharges, it will immediately begin charging by a constant current source. The discharge rate is the RC time constant of R_{PD} and C_{SS}. Refer to Figures 14 through 18 in the “Typical Operating Performance Curves” beginning on page 8. R_{PD} is the ON-resistance of the pull-down MOSFET, M8. R_{PD} is typically 323Ω.

The soft-start feature effectively reduces the inrush current at power-up or LDO enable until V_{OUT} reaches regulation. The in-rush current can be an issue for applications that require large, external bulk capacitances on V_{OUT} where high levels of charging current can be seen for a significant period of time. The inrush currents can cause V_{IN} to drop below minimum which could cause V_{OUT} to shutdown. Figure 26 on page 10 shows the relationship between inrush current and C_{SS} with a C_{OUT} of 1000µF.

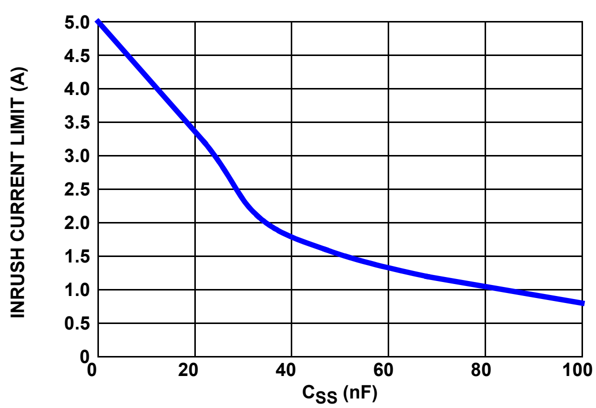


FIGURE 40. INRUSH CURRENT vs SOFT-START CAPACITANCE

Output Voltage Selection

An external resistor divider scales the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5.5V. An external resistor divider, R_3 and R_4, sets the output voltage as shown in Equation 1. The recommended value for R_4 is 200Ω to 5kΩ. R_3 is then chosen according to Equation 2:

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_4} + 1\right) \quad \text{(EQ. 1)}$$

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 2)}$$

External Capacitor Requirements

External capacitors are required for proper operation. To ensure optimal performance, pay careful attention to the layout guidelines and selection of capacitor type and value.

OUTPUT CAPACITOR

The ISL80102 and ISL80103 apply state-of-the-art internal compensation to keep selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range, and load extremes are guaranteed for all ceramic capacitors and values assuming a 10µF X5R/X7R is used for local bypass on V_{OUT}. This minimum capacitor (see Table 1 on page 2 for component value selections) must be connected to the V_{OUT} and ground pins of the LDO with PCB traces no longer than 0.5cm.

Lower cost Y5V and Z5U type ceramic capacitors are acceptable if the size of the capacitor is large enough to compensate for the significantly lower tolerance over X5R/X7R types. Additional capacitors of any value in Ceramic, POSCAP, or Alum/Tantalum Electrolytic types can be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

The minimum input capacitor required for proper operation is a 10µF with a ceramic dielectric. This minimum capacitor must be connected to V_{IN} and ground pins of the LDO with PCB traces no longer than 0.5cm.

Phase Boost Capacitor (Optional)

The ISL80102 and ISL80103 are designed to be stable with 10µF or larger ceramic capacitors.

Applications can see improved performance with the addition of a small ceramic capacitor C_{PB} as shown in Figure 1 on page 1. The conditions in which C_{PB} may be beneficial are:

- $V_{OUT} > 1.5V$
- $C_{OUT} = 10µF$
- Tight AC voltage regulation band

C_{PB} introduces phase lead with the product of R_3 and C_{PB} that results in increasing the bandwidth of the LDO. Typical R_3 x C_{PB} should be less than 0.4µs (400ns).

Current Limit Protection

The ISL80102 and ISL80103 family of LDOs incorporates protection against overcurrent due to a short overload condition applied to the output and the inrush current that occurs at start-up. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" table on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding the thermal fault condition.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions" on page 4. The power dissipation can be calculated by using Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation as shown in Equation 4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

where θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation calculated in Equation 3, P_D, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane) for heat sinking. Figure 41 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

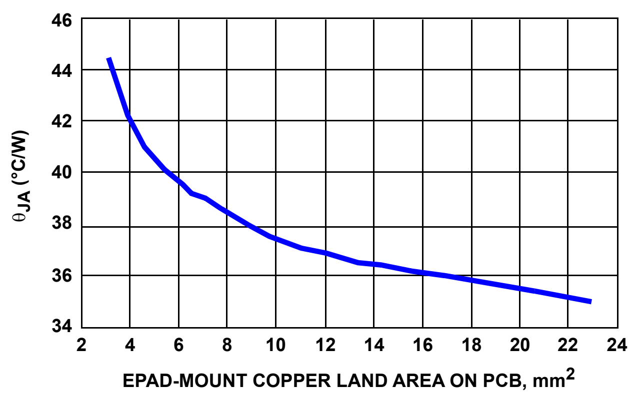


FIGURE 41. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

If the die temperature exceeds typically +160°C, the output of the LDO shuts down until the die temperature can cool down to typically +145°C. The level of power combined with the thermal impedance of the package (+48°C/W for DFN) determine if the junction temperature exceeds the thermal shutdown temperature.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jun 11, 2020	9.02	Updated Ordering Information table by removing retired parts, adding tape and reel info, and updated notes. Removed information throughout the document related to the retired parts. Added Theta JB information.
Dec 3, 2019	9.01	Updated Links throughout. Updated Figures 15 and 17. Updated disclaimer.
Mar 19, 2018	9.00	Added Related Literature section to page 1. Changed values in Output Voltage Selection section on page 13 from “500Ω to 1kΩ” to “200Ω to 5kΩ”. Removed About Intersil section and added Renesas disclaimer.
Sep 2, 2016	8.00	Removed Note 8 “Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current” from Recommended Operating Conditions.
Apr 8, 2016	7.00	Updated Ordering Information table (on page 3), Note 1 to include quantities for tape and reel options. Changed VOUT range upper limit from “5V to 5.5V” on page 1, in the “Recommended Operating Conditions (Note 7)” on page 4 and in the “Output Voltage Selection” on page 12 Electrical Spec table test conditions changed from: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10µF$, $T_J = +25°C$, $I_{LOAD} = 0A$, to: $2.2V < V_{IN} < 6V$, $V_{OUT} = 0,5V$, $T_J = +25°C$, $I_{LOAD} = 0A$ Changed Test conditions in “Output Noise Voltage” on page 5 from: ILOAD = 10mA, BW = 300Hz <f< 300kHz; to: VIN = 2.2V, VOUT = 1.8V, ILOAD = 3A, BW = 100Hz<f<100kHz and changed TYP from: 100; to: 49 Added two rows to “Dropout Voltage (Note 9)” on page 5 to show parameters for 5.5V V_{OUT} conditions. Updated verbiage for “About Intersil” on page 16. Updated POD L10.3x3 to most updated revision with changes as follows: Added missing dimension 0.415 in Typical Recommended land pattern. Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins. Changed Tiebar note 4, from: Tiebar shown (if present) is a non-functional feature. to: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
May 23, 2013	6.00	Pin Descriptions on page page 2, updated EPAD section From: EPAD at ground potential. Soldering it directly to GND plane is optional. To: EPAD must be connected to copper plane with as many vias as possible for proper electrical and optimal thermal performance. Removed obsolete part numbers: ISL80102IR33Z, ISL80102IR50Z, ISL80103IR33Z, ISL80103IR50Z from ordering information table on page 3. Added evaluation boards to ordering information table on page 3: ISL80103IR50Z and ISL80103EVAL2Z. Features on page 1: Removed 5 Ld TO220 and 5 Ld TO263. Input Voltage Requirements on page 12: Removed the sentence “those applications that cannot accommodate the profile of the TO220/TO263”.
Jun 14, 2012	5.00	In “Thermal Information” on page 4, corrected θ_{JA} from 48 to 45.
Feb 14, 2012	4.00	Increased “VEN(HIGH)” minimum limit from 0.4V to 0.616 and added the “VEN(LOW)” spec for clarity on page 5.
Dec 14, 2011	3.00	Increased “Turn-on Threshold” minimum limit on page 5 from 0.3V to 0.4V. Updated “Package Outline Drawing” on page 16 as follows: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.
Mar 4, 2011	2.00	Converted to new template On page 1 - first paragraph, changed "Fixed output voltage options are available in 1.5V, 1.8V, 2.5V, 3.3V and 5V" to "Fixed output voltage options are available in 1.8V, 2.5V, 3.3V and 5V" In “Ordering Information” table on page 2, removed ISL80102IR15Z and ISL80103IR15Z. In Note 3 on page 2, below the “Ordering Information” table, removed '1.5V', so it reads “The 3.3V and 5V fixed output voltages will be released in the future. Please contact Intersil Marketing for more details.”

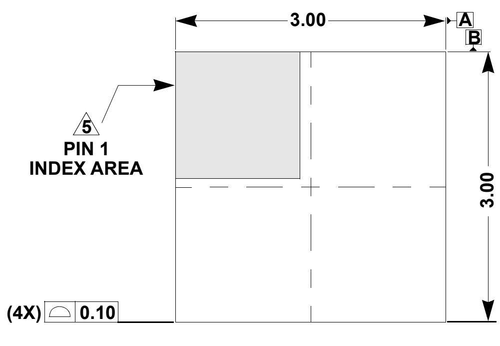
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
Mar 4, 2010	1.00	Corrected Features on page 1 as follows: -Changed bullet "• 185mV Dropout @ 3A, 125mV Dropout @ 2A" to "• Very Low 120mV Dropout at 3A" -Changed bullet "• 65dB Typical PSRR" to "• 62dB Typical PSRR" -Deleted 0.5% Initial VOUT Accuracy Modified Figure 1 and placed as "TYPICAL APPLICATION" on page 1. Moved Pinout to page 3 In "Block Diagram" on page 2, corrected resistor associated with M5 from R4 to R5 Updated "Block Diagram" on page 2 as follows" - Added M8 from SS to ground. Updated Figure 1 on page 1 as follows: -Corrected Pin 6 from SS to IRSET -Removed Note 11 callout "Minimum cap on VIN and VOUT required for stability." Added Note "*CSS is optional. See Note 12 on Page 5." and "** CPB is optional. See "Functional Description" on page 12 for more information." Added "The 1.5V, 3.3V and 5V fixed output voltages will be released in the future." to Note 3 on page 2. In "Thermal Information" on page 4, updated Theta JA from 45 to 48. In "Soft-Start Operation (Optional)" on page 12: -Changed "The external capacitor always gets discharged to 0V at start-up of after coming out of a chip disable. "The external capacitor always gets discharged to ground pin potential at start-up or enabling." -Changed "The soft-start function effectively limits the amount of inrush current below the programmed current limit during start-up or an enable sequence to avoid an overcurrent fault condition." to "The soft-start feature effectively reduces the inrush current at power-up or LDO enable until VOUT reaches regulation." -Added "See Figures 25 through 27 in the "Typical Operating Performance Curves" beginning on page 6." -Added "RPD is the on resistance of the pull-down MOSFET, M8. RPD is 300Ω typically." Added "Phase Boost Capacitor (Optional)" on page 13. In "Typical Operating Performance" on page 11, revised figure "PSRR vs VIN" which had 3 curves with "SPECTRAL NOISE DENSITY vs FREQUENCY" which has one curve. Added "Figure 33. "LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, NO CPB (ADJ VERSION)" and "Figure 34. "LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, CPB = 1500pF (ADJ VERSION)"
Sep 30, 2009	0.00	Initial Release.

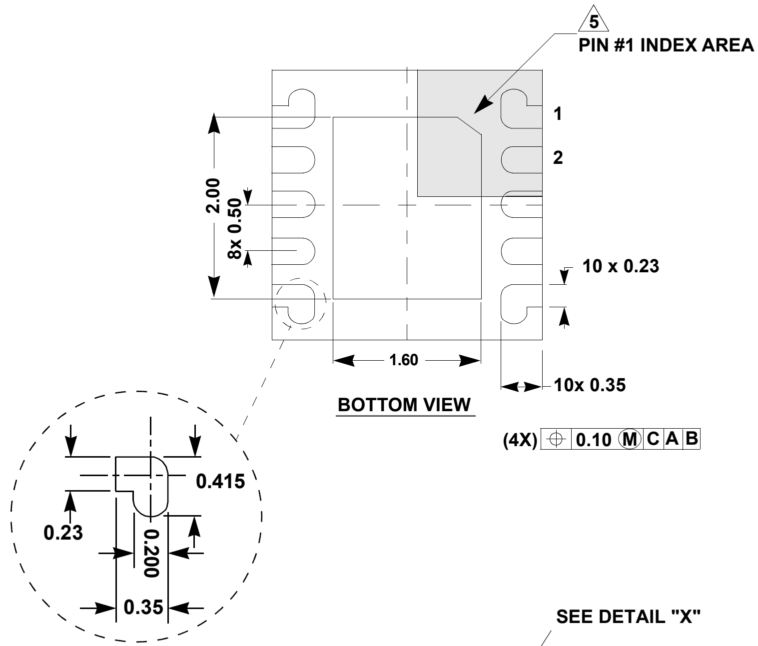
Package Outline Drawing

For the most recent package outline drawing, see L10.3x3.

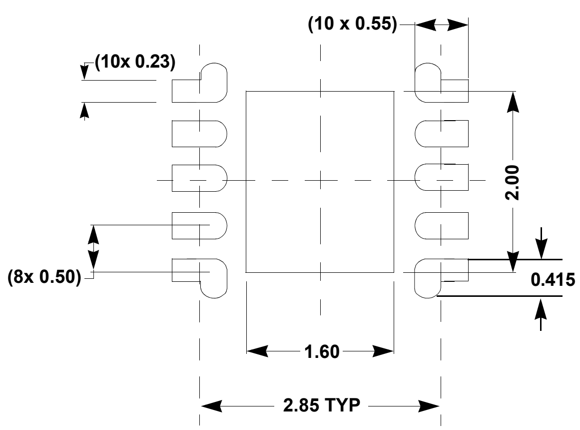
L10.3x3
10 LEAD DUAL FLAT PACKAGE (DFN)
Rev 11, 3/15



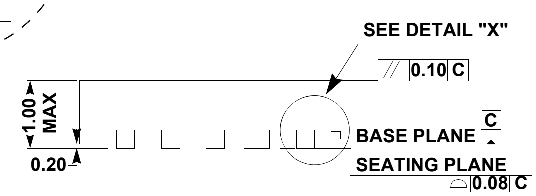
TOP VIEW



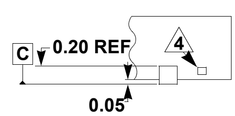
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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Contact Information

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