

ISL8487E, ISL81487L, ISL81487E

±15kV ESD Protected, 1/8 Unit Load, 5V, Low Power, High Speed or Slew Rate Limited RS-485/RS-422 Transceivers

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The [ISL8487E](#), [ISL81487L](#), and [ISL81487E](#) RS-485/RS-422 devices are ESD protected, fractional unit load (UL), BiCMOS, 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output/receiver input is protected against ±15kV ESD strikes without latch-up. Unlike competitive devices, this device family is specified for 10% tolerance supplies (4.5V to 5.5V).

All devices present a 1/8 unit load to the RS-485 bus, which allows up to 256 transceivers on the network for large node count systems (for example, process automation and remote meter reading systems). In a remote utility meter reading system, individual utility meter readings (in apartments, for example) are routed to a concentrator with an RS-485 network, so the high allowed node count minimizes the number of repeaters required to network all the meters. Data for all meters is then read out from the concentrator from a single access port or a wireless link.

Slew rate limited drivers on the ISL8487E and ISL81487L reduce EMI and minimize reflections from improperly terminated transmission lines or unterminated stubs in multidrop and multipoint applications. Data rates up to 250kbps are achievable with these devices.

Data rates up to 5Mbps are achievable by using the ISL81487E, which features higher slew rates.

The receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

The driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

The half duplex devices multiplex the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 lead packages.

Related Literature

For a full list of related documents, visit our website:

- [ISL8487E](#), [ISL81487L](#), and [ISL81487E](#) product pages

Features

- RS-485 I/O pin ESD protection ±15kV HBM
- Class 3 ESD level on all other pins >7kV HBM
- Fractional unit load allows up to 256 devices on the bus
- Specified for 10% tolerance supplies
- High data rate version (ISL81487E). up to 5Mbps
- Slew rate limited versions for error free data transmission (ISL8487E, ISL81487L) up to 250kbps
- Low current shutdown mode (except ISL81487E) 0.5µA
- Low quiescent supply current:
- ISL8487E, ISL81487L 145µA (maximum)
- ISL81487E 420µA (maximum)
- -7V to +12V common mode input voltage range
- Three state Rx and Tx outputs
- 30ns propagation delays, 5ns skew (ISL81487E)
- Half duplex pinouts
- Operate from a single +5V supply (10% tolerance)
- Current limiting and thermal shutdown for driver overload protection
- Pin compatible replacements for: MAX487E, (ISL8487E); LTC1487, ADM1487 (ISL81487L); MAX1487E, ST485ER (ISL81487E)
- Pb-free plus anneal available (RoHS compliant)

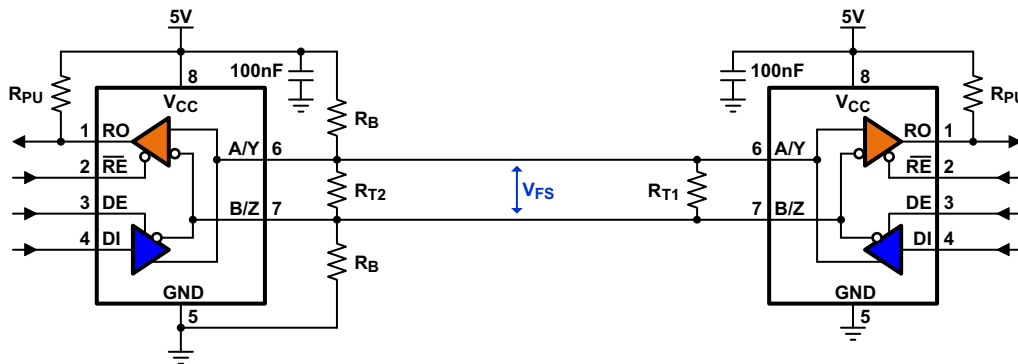
Applications

- High node count networks
- Automated utility meter reading systems
- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks

TABLE 1. SUMMARY OF FEATURES

| PART NUMBER | HALF/FULL DUPLEX | NO. OF DEVICES ALLOWED ON BUS | DATA RATE (Mbps) | SLEW RATE LIMITED? | RECEIVER/ DRIVER ENABLE? | QUIESCENT I _{CC} (µA) | LOW POWER SHUTDOWN? | PIN COUNT |
|-------------|------------------|-------------------------------|------------------|--------------------|--------------------------|--------------------------------|---------------------|-----------|
| ISL8487E | Half | 256 | 0.25 | Yes | Yes | 120 | Yes | 8 |
| ISL81487L | Half | 256 | 0.25 | Yes | Yes | 120 | Yes | 8 |
| ISL81487E | Half | 256 | 5 | No | Yes | 350 | No | 8 |

Typical Operating Circuits



To calculate the resistor values, refer to [TB509](#).

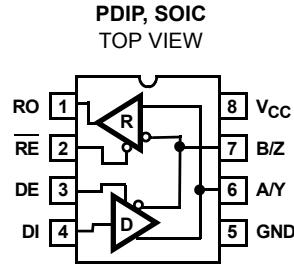
Ordering Information

| PART NUMBER () | PART MARKING | TEMP. RANGE (°C) | TAPE AND REEL (UNITS) (Note 1) | PACKAGE | PKG. DWG. # |
|---|--------------|------------------|--|--|-------------|
| ISL8487EIBZ | 8487EIBZ | -40 to +85 | - | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL8487EIBZ-T | 8487EIBZ | -40 to +85 | 2.5k | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL8487EIPZ (not recommended for new designs, recommended replacement ISL81487LIPZ) | 8487EIPZ | -40 to +85 | - | 8 Ld PDIP (Pb-free, Note 4) | E8.3 |
| ISL81487LIBZ | 81487LIBZ | -40 to +85 | - | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL81487LIBZ-T | 81487LIBZ | -40 to +85 | 2.5k | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL81487LIPZ | 81487LIPZ | -40 to +85 | - | 8 Ld PDIP (Pb-free, Note 4) | E8.3 |
| ISL81487EIBZ | 81487EIBZ | -40 to +85 | - | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL81487EIBZ-T | 81487EIBZ | -40 to +85 | 2.5k | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL81487EIPZ | ISL81487EIPZ | -40 to +85 | - | 8 Ld PDIP (Pb-free, Note 4) | E8.3 |

NOTES:

1. Refer to [TB347](#) for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
3. For Moisture Sensitivity Level (MSL), see the [ISL8487E](#), [ISL81487L](#), and [ISL81487E](#) product information pages. For more information about MSL, see [TB363](#).
4. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pinout



Pin Descriptions

| PIN | FUNCTION |
|-----------------|---|
| RO | Receiver output. RO is high if A > B by at least 0.2V; RO is low if A < B by 0.2V or more; RO is high if A and B are unconnected (floating). |
| \overline{RE} | Receiver output enable. RO is enabled when \overline{RE} is low; RO is high impedance when \overline{RE} is high. |
| DE | Driver output enable. The driver outputs Y and Z are enabled by bringing DE high. They are high impedance when DE is low. |
| DI | Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low. |
| GND | Ground connection. |
| A/Y | ± 15 kV HBM ESD protected, RS-485/422 level, noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1. |
| B/Z | ± 15 kV HBM ESD protected, RS-485/422 level, inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1. |
| V _{CC} | System power supply input (4.5V to 5.5V). |

Truth Tables

| TRANSMITTING | | | | |
|-----------------|----|----|-------------------------------------|-------------------------------------|
| INPUTS | | | OUTPUTS | |
| \overline{RE} | DE | DI | Z | Y |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | High-Z | High-Z |
| 1 | 0 | X | High-Z (Note 12) | High-Z (Note 12) |

| RECEIVING | | | |
|-----------------|----|--------------|-------------------------------------|
| INPUTS | | | OUTPUT |
| \overline{RE} | DE | A-B | RO |
| 0 | X | $\geq +0.2V$ | 1 |
| 0 | X | $\leq -0.2V$ | 0 |
| 0 | X | Inputs Open | 1 |
| 1 | X | X | High-Z (Note 12) |
| 1 | 0 | X | High-Z |

Absolute Maximum Ratings

V_{CC} to Ground 7V
 Input Voltages
 DI, DE, RE -0.5V to (V_{CC} +0.5V)
 Input/Output Voltages
 A/Y, B/Z -8V to +12.5V
 RO -0.5V to (V_{CC} +0.5V)
 Short-Circuit Duration
 Y, Z Continuous
 ESD Rating See "Electrical Specifications"

Thermal Information

Thermal Resistance (Typical, [Note 5](#)) θ_{JA} (°C/W)
 8 Ld SOIC Package 170
 8 Ld PDIP Package ([Note 6](#)) 140
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
 ISL8XXXIX -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" can permanently damage the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

5. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See [TB379](#) for details.
6. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C, [Note 7](#)

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN | TYP | MAX | UNIT | |
|---|------------------|--|-----------------------|------|------|-----------------|------|----|
| DC CHARACTERISTICS | | | | | | | | |
| Driver Differential V _{OUT} (No Load) | V _{OD1} | | Full | - | - | V _{CC} | V | |
| Driver Differential V _{OUT} (with Load) | V _{OD2} | R = 50Ω (RS-422), (Figure 1) | Full | 2 | 3 | - | V | |
| | | R = 27Ω (RS-485), (Figure 1) | Full | 1.5 | 2.3 | 5 | V | |
| Change in Magnitude of Driver Differential V _{OUT} for Complementary Output States | ΔV _{OD} | R = 27Ω or 50Ω, (Figure 1) | Full | - | 0.01 | 0.2 | V | |
| Driver Common-Mode V _{OUT} | V _{OC} | R = 27Ω or 50Ω, (Figure 1) | Full | - | - | 3 | V | |
| Change in Magnitude of Driver Common-Mode V _{OUT} for Complementary Output States | ΔV _{OC} | R = 27Ω or 50Ω, (Figure 1) | Full | - | 0.01 | 0.2 | V | |
| Logic Input High Voltage | V _{IH} | DE, DI, \overline{RE} | Full | 2 | - | - | V | |
| Logic Input Low Voltage | V _{IL} | DE, DI, \overline{RE} | Full | - | - | 0.8 | V | |
| Logic Input Current | I _{IN1} | DE, DI, \overline{RE} | Full | -2 | - | 2 | μA | |
| Input Current (A/Y, B/Z), (Note 15) | I _{IN2} | DE = 0V, V _{CC} = 4.5 to 5.5V | V _{IN} = 12V | Full | - | - | 140 | μA |
| | | | V _{IN} = -7V | Full | - | - | -120 | μA |
| | I _{IN2} | DE = 0V, V _{CC} = 0V | V _{IN} = 12V | Full | - | - | 180 | μA |
| | | | V _{IN} = -7V | Full | - | - | -100 | μA |
| Receiver Differential Threshold Voltage | V _{TH} | -7V ≤ V _{CM} ≤ 12V | Full | -0.2 | - | 0.2 | V | |
| Receiver Input Hysteresis | ΔV _{TH} | V _{CM} = 0V | 25 | - | 70 | - | mV | |
| Receiver Output High Voltage | V _{OH} | I _O = -4mA, V _{ID} = 200mV | Full | 3.5 | - | - | V | |
| Receiver Output Low Voltage | V _{OL} | I _O = -4mA, V _{ID} = 200mV | Full | - | - | 0.4 | V | |
| Three-State (High Impedance) Receiver Output Current | I _{OZR} | 0.4V ≤ V _O ≤ 2.4V | Full | - | - | ±1 | μA | |
| Receiver Input Resistance | R _{IN} | -7V ≤ V _{CM} ≤ 12V | Full | 96 | - | - | kΩ | |

Electrical Specifications Test Conditions: $V_{CC} = 4.5V$ to $5.5V$; Unless Otherwise Specified. Typical values are at $V_{CC} = 5V$, $T_A = +25^\circ C$, [Note 7](#) (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN | TYP | MAX | UNIT | |
|--|--------------------|--|---------------|------|------|------|---------|---------|
| No-Load Supply Current, (Note 8) | I_{CC} | ISL81487E, DI, $\overline{RE} = 0V$ or V_{CC} | DE = V_{CC} | Full | - | 400 | 500 | μA |
| | | | DE = 0V | Full | - | 350 | 420 | μA |
| | | ISL8487E, ISL81487L, DI, $\overline{RE} = 0V$ or V_{CC} | DE = V_{CC} | Full | - | 160 | 200 | μA |
| | | | DE = 0V | Full | - | 120 | 145 | μA |
| Shutdown Supply Current | I_{SHDN} | (Note 12), DE = 0V, $\overline{RE} = V_{CC}$, DI = 0V or V_{CC} | Full | - | 0.5 | 8 | μA | |
| Driver Short-Circuit Current, $V_O =$ High or Low | I_{OSD1} | DE = V_{CC} , $-7V \leq V_Y$ or $V_Z \leq 12V$, (Note 9) | Full | 35 | - | 250 | mA | |
| Receiver Short-Circuit Current | I_{OSR} | $0V \leq V_O \leq V_{CC}$ | Full | 7 | - | 85 | mA | |
| SWITCHING CHARACTERISTICS (ISL81487E) | | | | | | | | |
| Driver Input to Output Delay | t_{PLH}, t_{PHL} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 15 | 24 | 50 | ns | |
| Driver Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | - | 3 | 10 | ns | |
| Driver Differential Rise or Fall Time | t_R, t_F | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 3 | 12 | 25 | ns | |
| Driver Enable to Output High | t_{ZH} | $C_L = 100pF$, SW = GND, (Figure 2) | Full | - | 14 | 70 | ns | |
| Driver Enable to Output Low | t_{ZL} | $C_L = 100pF$, SW = V_{CC} , (Figure 2) | Full | - | 14 | 70 | ns | |
| Driver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 2) | Full | - | 44 | 70 | ns | |
| Driver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 2) | Full | - | 21 | 70 | ns | |
| Receiver Input to Output Delay | t_{PLH}, t_{PHL} | (Figure 4) | Full | 30 | 90 | 150 | ns | |
| Receiver Skew $t_{PLH} - t_{PHL}$ | t_{SKD} | (Figure 4) | 25 | - | 5 | - | ns | |
| Receiver Enable to Output High | t_{ZH} | $C_L = 15pF$, SW = GND, (Figure 5) | Full | - | 9 | 50 | ns | |
| Receiver Enable to Output Low | t_{ZL} | $C_L = 15pF$, SW = V_{CC} , (Figure 5) | Full | - | 9 | 50 | ns | |
| Receiver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 5) | Full | - | 9 | 50 | ns | |
| Receiver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 5) | Full | - | 9 | 50 | ns | |
| Maximum Data Rate | f_{MAX} | | Full | 5 | - | - | Mbps | |
| SWITCHING CHARACTERISTICS (ISL8487E) | | | | | | | | |
| Driver Input to Output Delay | t_{PLH}, t_{PHL} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 250 | 650 | 2000 | ns | |
| Driver Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | - | 160 | 800 | ns | |
| Driver Differential Rise or Fall Time | t_R, t_F | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 250 | 900 | 2000 | ns | |
| Driver Enable to Output High | t_{ZH} | $C_L = 100pF$, SW = GND, (Figure 3 , Note 10) | Full | 250 | 1000 | 2000 | ns | |
| Driver Enable to Output Low | t_{ZL} | $C_L = 100pF$, SW = V_{CC} , (Figure 3 , Note 10) | Full | 250 | 860 | 2000 | ns | |
| Driver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 3) | Full | 300 | 660 | 3000 | ns | |
| Driver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 3) | Full | 300 | 640 | 3000 | ns | |
| Receiver Input to Output Delay | t_{PLH}, t_{PHL} | (Figure 4) | Full | 250 | 500 | 2000 | ns | |
| Receiver Skew $t_{PLH} - t_{PHL}$ | t_{SKD} | (Figure 4) | 25 | - | 60 | - | ns | |
| Receiver Enable to Output High | t_{ZH} | $C_L = 15pF$, SW = GND, (Figure 5 , Note 11) | Full | - | 10 | 50 | ns | |
| Receiver Enable to Output Low | t_{ZL} | $C_L = 15pF$, SW = V_{CC} , (Figure 5 , Note 11) | Full | - | 10 | 50 | ns | |
| Receiver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 5) | Full | - | 10 | 50 | ns | |
| Receiver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 5) | Full | - | 10 | 50 | ns | |
| Maximum Data Rate | f_{MAX} | | Full | 250 | - | - | kbps | |
| Time to Shutdown | t_{SHDN} | (Note 12) | Full | 50 | 120 | 600 | ns | |
| Driver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$ | $C_L = 100pF$, SW = GND, (Figure 3 , Notes 12 and 13) | Full | - | 1000 | 2000 | ns | |
| Driver Enable from Shutdown to Output Low | $t_{ZL}(SHDN)$ | $C_L = 100pF$, SW = V_{CC} , (Figure 3 , Notes 12 and 13) | Full | - | 1000 | 2000 | ns | |

Electrical Specifications

Test Conditions: $V_{CC} = 4.5V$ to $5.5V$; Unless Otherwise Specified. Typical values are at $V_{CC} = 5V$, $T_A = +25^\circ C$, [Note 7 \(Continued\)](#)

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN | TYP | MAX | UNIT |
|--|-----------------------|--|-----------|-----|----------|------|------|
| Receiver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$ | $C_L = 15pF$, SW = GND, (Figure 5 , Notes 12 and 14) | Full | - | 800 | 2500 | ns |
| Receiver Enable from Shutdown to Output Low | $t_{ZL}(SHDN)$ | $C_L = 15pF$, SW = V_{CC} , (Figure 5 , Notes 12 and 14) | Full | - | 800 | 2500 | ns |
| SWITCHING CHARACTERISTICS (ISL81487L) | | | | | | | |
| Driver Input to Output Delay | t_{PLH} , t_{PHL} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 150 | 650 | 1200 | ns |
| Driver Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | - | 160 | 600 | ns |
| Driver Differential Rise or Fall Time | t_R , t_F | $R_{DIFF} = 54\Omega$, $C_L = 100pF$, (Figure 2) | Full | 250 | 900 | 1200 | ns |
| Driver Enable to Output High | t_{ZH} | $C_L = 100pF$, SW = GND, (Figure 3 , Note 10) | Full | 100 | 1000 | 1500 | ns |
| Driver Enable to Output Low | t_{ZL} | $C_L = 100pF$, SW = V_{CC} , (Figure 3 , Note 10) | Full | 100 | 1000 | 1500 | ns |
| Driver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 3) | Full | 150 | 750 | 1500 | ns |
| Driver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 3) | Full | 150 | 750 | 1500 | ns |
| Receiver Input to Output Delay | t_{PLH} , t_{PHL} | (Figure 4) | Full | 30 | 175 | 250 | ns |
| Receiver Skew $t_{PLH} - t_{PHL}$ | t_{SKD} | (Figure 4) | 25 | - | 13 | - | ns |
| Receiver Enable to Output High | t_{ZH} | $C_L = 15pF$, SW = GND, (Figure 5 , Note 11) | Full | - | 10 | 50 | ns |
| Receiver Enable to Output Low | t_{ZL} | $C_L = 15pF$, SW = V_{CC} , (Figure 5 , Note 11) | Full | - | 10 | 50 | ns |
| Receiver Disable from Output High | t_{HZ} | $C_L = 15pF$, SW = GND, (Figure 5) | Full | - | 10 | 50 | ns |
| Receiver Disable from Output Low | t_{LZ} | $C_L = 15pF$, SW = V_{CC} , (Figure 5) | Full | - | 10 | 50 | ns |
| Maximum Data Rate | f_{MAX} | | Full | 250 | - | - | kbps |
| Time to Shutdown | t_{SHDN} | (Note 12) | Full | 50 | 140 | 600 | ns |
| Driver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$ | $C_L = 100pF$, SW = GND, (Figure 3 , Notes 12 and 13) | Full | - | 1100 | 2000 | ns |
| Driver Enable from Shutdown to Output Low | $t_{ZL}(SHDN)$ | $C_L = 100pF$, SW = V_{CC} , (Figure 3 , Notes 12 and 13) | Full | - | 1000 | 2000 | ns |
| Receiver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$ | $C_L = 15pF$, SW = GND, (Figure 3 , Notes 12 and 14) | Full | - | 900 | 2000 | ns |
| Receiver Enable from Shutdown to Output Low | $t_{ZL}(SHDN)$ | $C_L = 15pF$, SW = V_{CC} , (Figure 3 , Notes 12 and 14) | Full | - | 900 | 2000 | ns |
| ESD PERFORMANCE | | | | | | | |
| RS-485 Pins (A/Y, B/Z) | | Human Body Model | 25 | - | ± 15 | - | kV |
| All Other Pins | | | 25 | - | $>\pm 7$ | - | kV |

NOTES:

- Currents into device pins are positive; currents out of device pins are negative. Voltages are referenced to ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when DE = 0V.
- Applies to peak current. See "[Typical Performance Curves](#)" for more information.
- When testing the ISL8487E and ISL81487L, keep $\overline{RE} = 0$ to prevent the device from entering shutdown (SHDN).
- When testing the ISL8487E and ISL81487L, the \overline{RE} signal high time must be short enough (typically <200ns) to prevent the device from entering SHDN.
- The ISL8487E and ISL81487L go into SHDN by bringing \overline{RE} high and DE low. If the inputs are in this state for less than 50ns, the parts are specified not to enter SHDN. If the inputs are in this state for at least 600ns, the parts are specified to enter SHDN. See "[Low Power Shutdown Mode \(Excluding ISL81487E\)](#)" for more information.
- Keep $\overline{RE} = V_{CC}$ and set the DE signal low time >600ns to ensure that the device enters SHDN.
- Set the \overline{RE} signal high time >600ns to ensure that the device enters SHDN.
- Devices meeting these limits are denoted as 1/8 unit load (1/8 UL) transceivers. The RS-485 standard allows up to 32 UL on the bus, so there can be 256 1/8 UL devices on a bus.

Test Circuits and Waveforms

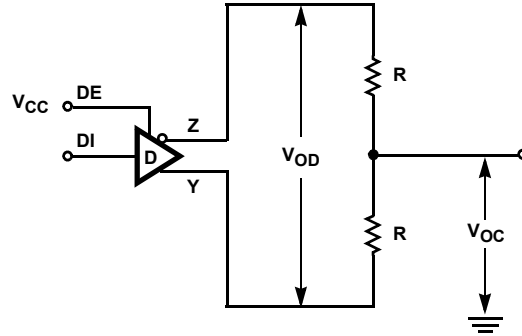


FIGURE 1. DRIVER V_{OD} AND V_{OC}

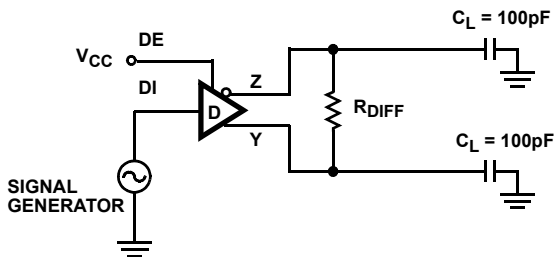
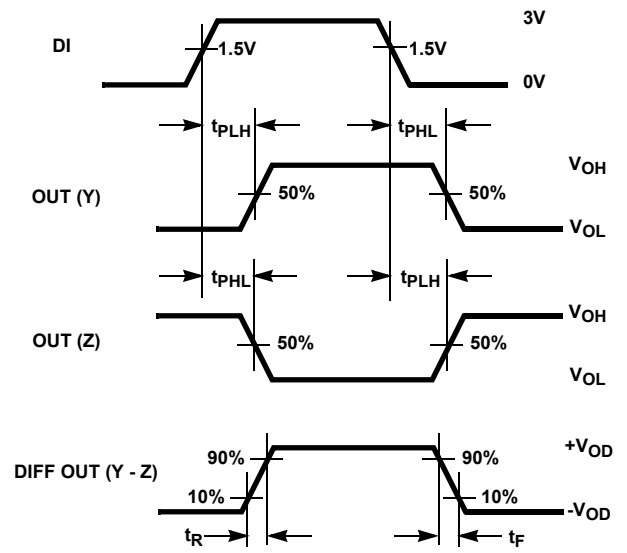


FIGURE 2A. TEST CIRCUIT

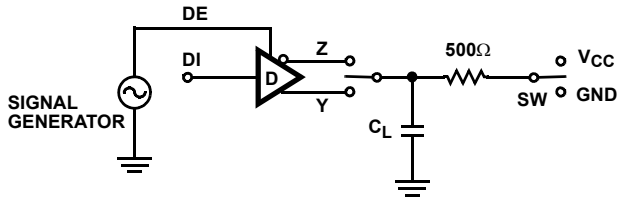


$$\text{SKEW} = |t_{PLH} (Y \text{ or } Z) - t_{PHL} (Z \text{ or } Y)|$$

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

Test Circuits and Waveforms (Continued)



(SHDN) for ISL8487E and ISL81487L only.

| PARAMETER | OUTPUT | RE | DI | SW | CL (pF) |
|----------------|--------|--------------------------------|-----|-----------------|---------|
| t_{HZ} | Y/Z | X | 1/0 | GND | 15 |
| t_{LZ} | Y/Z | X | 0/1 | V _{CC} | 15 |
| t_{ZH} | Y/Z | 0 (Note 10) | 1/0 | GND | 100 |
| t_{ZL} | Y/Z | 0 (Note 10) | 0/1 | V _{CC} | 100 |
| $t_{ZH(SHDN)}$ | Y/Z | 1 (Note 12) | 1/0 | GND | 100 |
| $t_{ZL(SHDN)}$ | Y/Z | 1 (Note 12) | 0/1 | V _{CC} | 100 |

FIGURE 3A. TEST CIRCUIT

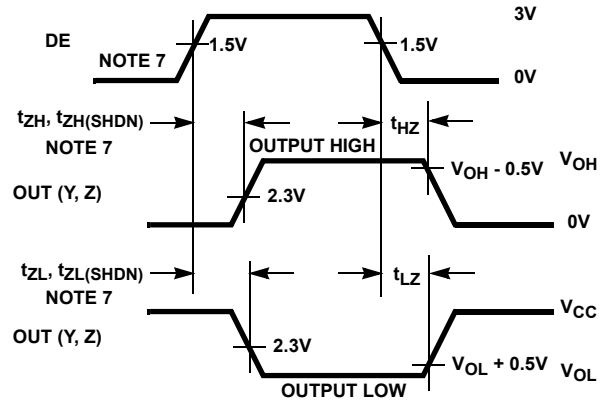


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

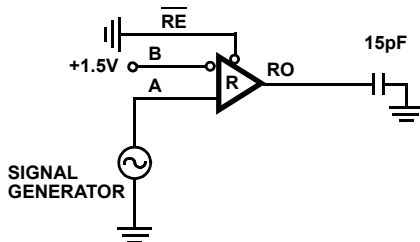


FIGURE 4A. TEST CIRCUIT

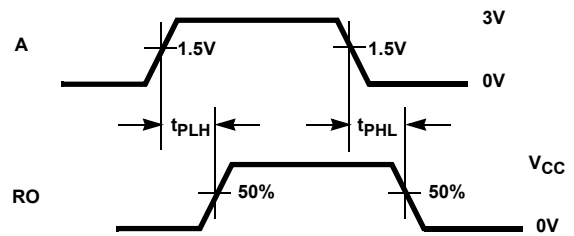
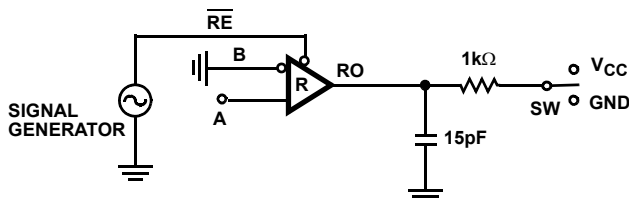


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY



(SHDN) for ISL8487E and ISL81487L only.

| PARAMETER | DE | A | SW |
|--|----|-------|-----------------|
| t_{HZ} | 0 | +1.5V | GND |
| t_{LZ} | 0 | -1.5V | V _{CC} |
| t_{ZH} (Note 11) | 0 | +1.5V | GND |
| t_{ZL} (Note 11) | 0 | -1.5V | V _{CC} |
| $t_{ZH(SHDN)}$ (Note 12) | 0 | +1.5V | GND |
| $t_{ZL(SHDN)}$ (Note 12) | 0 | -1.5V | V _{CC} |

FIGURE 5A. TEST CIRCUIT

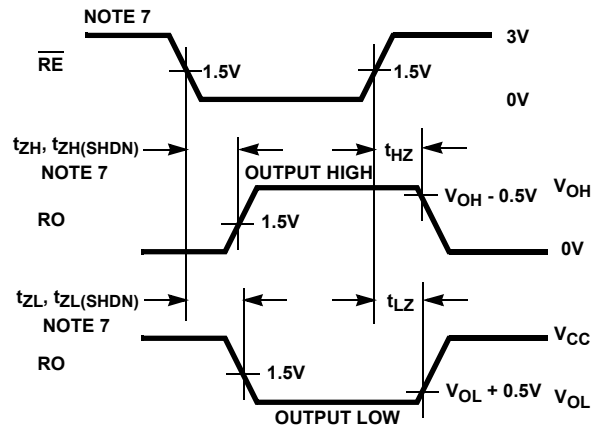


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard that allows only one driver and up to 10 receivers on each bus (assuming one unit load devices). RS-485 is a true multipoint standard that allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers handle bus contention without sustaining any damage.

An important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals ranging from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences and voltages induced in the cable by external fields.

Receiver Features

These devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is $\pm 200\text{mV}$, as required by the RS-422 and RS-485 specifications.

The receiver input resistance of $96\text{k}\Omega$ surpasses the RS-422 specification of $4\text{k}\Omega$ and is eight times the RS-485 Unit Load (UL) requirement of $12\text{k}\Omega$ minimum. Thus, these products are known as one-eighth UL transceivers. A network can host up to 256 of these devices still complying with the RS-485 loading specification.

The receiver inputs function with common-mode voltages as great as $\pm 7\text{V}$ outside the power supplies (that is, +12V and -7V), making them ideal for long networks in which induced voltages are a realistic concern.

All the receivers include a “fail-safe if open” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver. The receiver outputs are three-statable using the active low $\overline{\text{RE}}$ input.

Driver Features

The RS-485/422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485) and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

Driver outputs are three-statable using the active high DE input.

The ISL8487E and ISL81487L driver outputs are slew rate limited to minimize EMI and to minimize reflections in unterminated or improperly terminated networks. The

maximum data rate on these slew rate limited versions is 250kbps. The ISL81487E drivers are not limited, so faster output transition times allow data rates of at least 5Mbps.

Data Rate, Cables, and Terminations

RS-485/422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 5Mbps are limited to lengths less than a few hundred feet, while the 250kbps versions can operate at full data rates with lengths in excess of 1000ft.

Twisted pair cable is the cable of choice for RS-485/422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals that are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative to minimize reflections when using the 5Mbps device. Short networks using the 250kbps versions do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. In multipoint (multi-driver) systems, terminate the main cable in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

Built-In Driver Overload Protection

The RS-485 specification requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement with driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry that ensures the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. These devices also use a foldback circuit that reduces the short-circuit current and as a result, the power dissipation when the contending voltage exceeds either supply.

In the event of a major short-circuit condition, the thermal shutdown feature disables the drivers when the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°C . If the condition persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode (Excluding ISL81487E)

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but the ISL8487E and ISL81487L include a shutdown feature that reduces the already low quiescent I_{CC} to a 500nA trickle. They enter shutdown whenever the receiver and driver are simultaneously disabled ($\overline{RE} = V_{CC}$ and $DE = GND$) for a period of at least 600ns. Disabling both the driver and the receiver for less than 50ns guarantees that shutdown is not entered.

Note that receiver and driver enable times increase when enabling from shutdown. Refer to [Note 10](#) through [14](#) at the end of the “[Electrical Specifications](#)” table for more information.

ESD Protection

All pins on the interface devices include Class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of $\pm 15kV$ HBM. The RS-485 pins are particularly vulnerable to

ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a cable can cause an ESD event that destroys unprotected ICs. The ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and without degrading the RS-485 common-mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (for example, transient suppression diodes), and the associated undesirable capacitive load they present.

Human Body Model Testing

This test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge stored on a 100pF capacitor through a 1.5k Ω current limiting resistor into the pin under test. The HBM method determines an IC’s ability to withstand the ESD events typically present during handling and manufacturing. The RS-485 pin survivability on this high ESD family has been characterized to be in excess of $\pm 15kV$ for discharges to GND.

Typical Performance Curves $V_{CC} = 5V, T_A = +25^\circ C, ISL8487E, ISL81487L, \text{ and } ISL81487E; \text{ unless otherwise specified}$

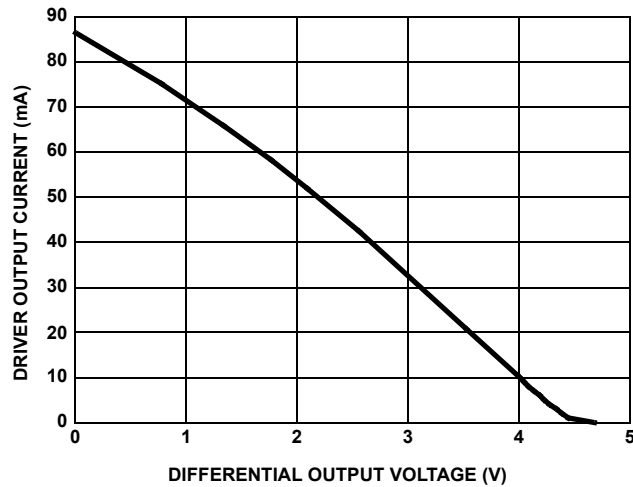


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

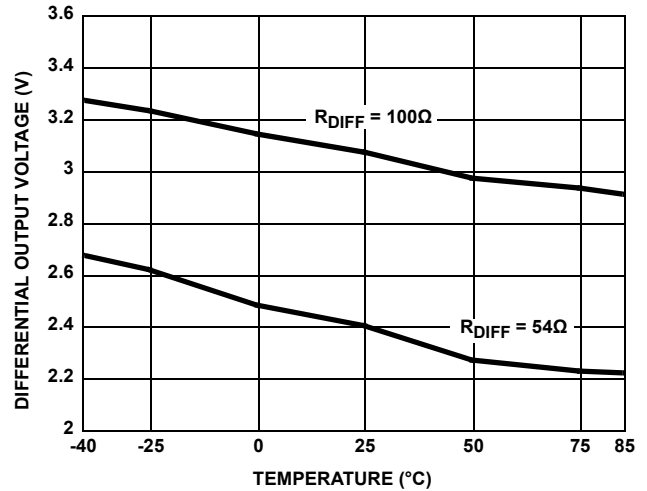


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_{CC} = 5V$, $T_A = +25^\circ C$, ISL8487E, ISL81487L, and ISL81487E; unless otherwise specified

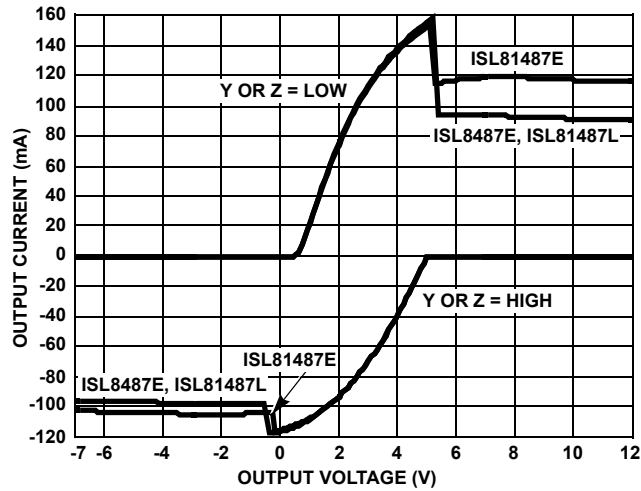


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

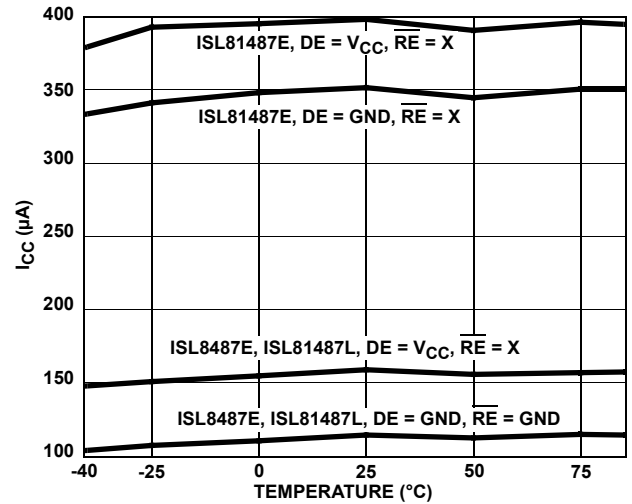


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

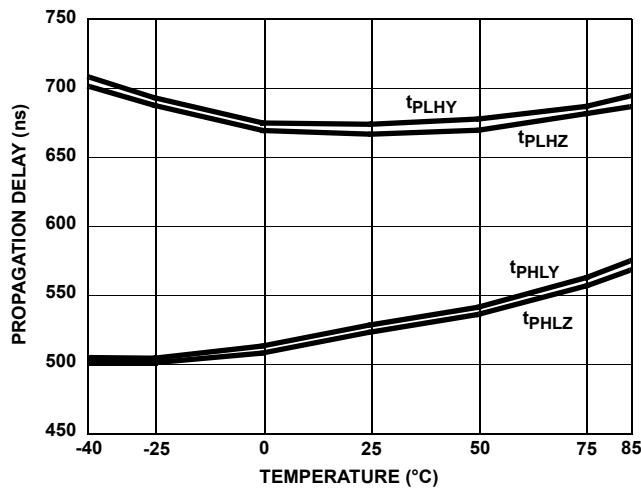


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8487E and ISL81487L)

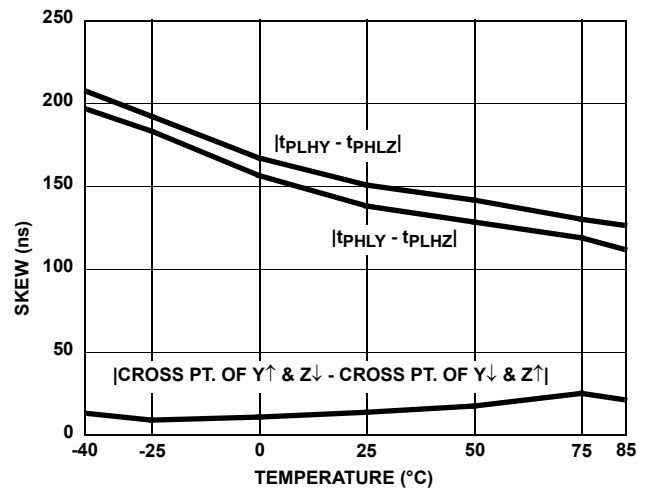


FIGURE 11. DRIVER SKEW vs TEMPERATURE (ISL8487E and ISL81487L)

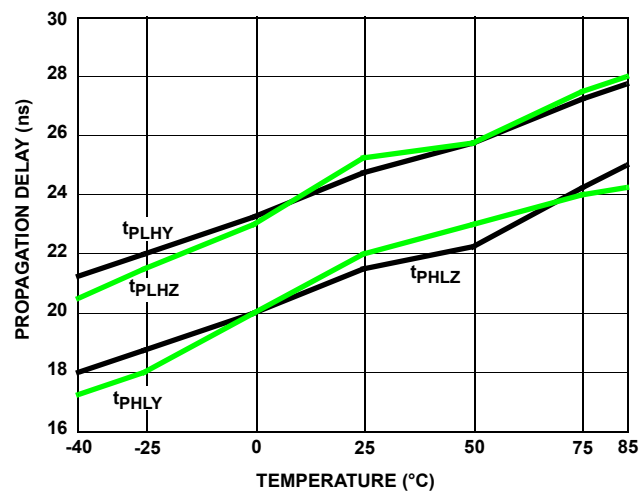


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL81487E)

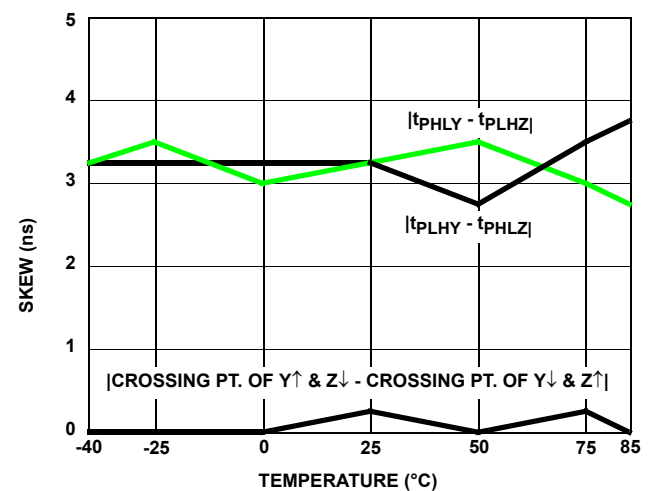


FIGURE 13. DRIVER SKEW vs TEMPERATURE (ISL81487E)

Typical Performance Curves $V_{CC} = 5V$, $T_A = +25^\circ C$, ISL8487E, ISL81487L, and ISL81487E; unless otherwise specified

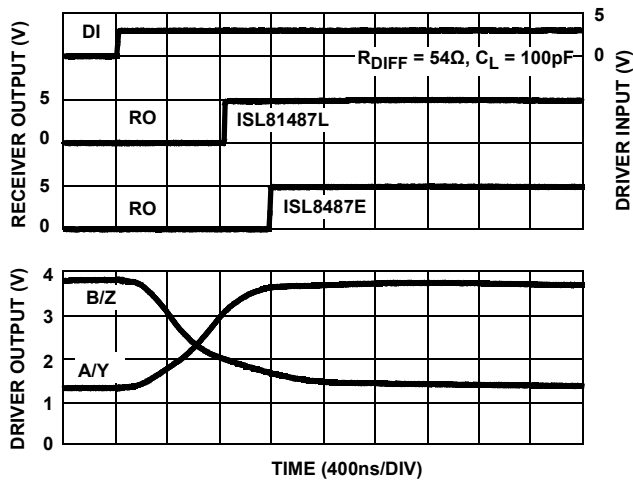


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8487E and ISL81487L)

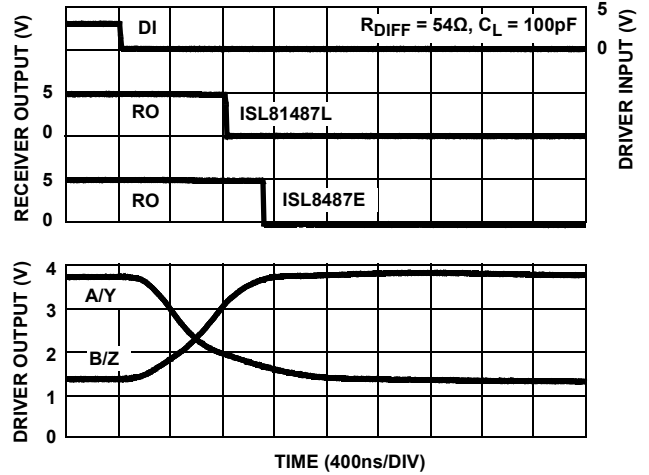


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8487E and ISL81487L)

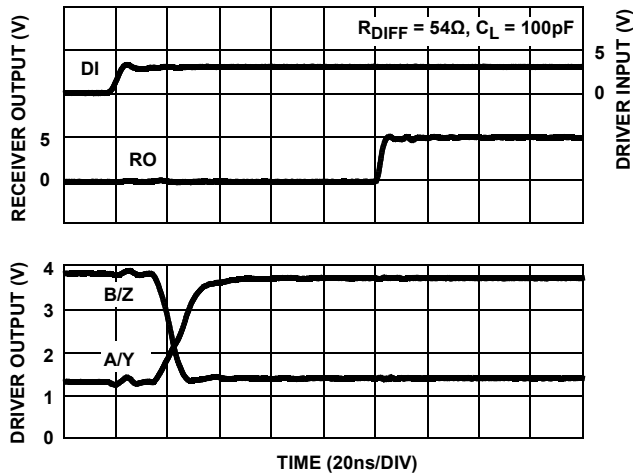


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL81487E)

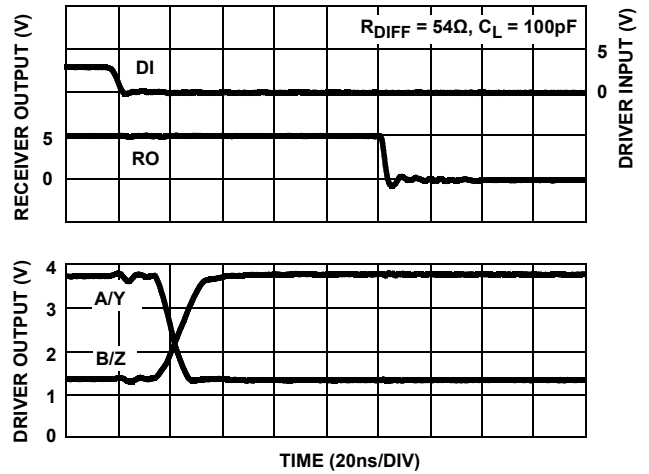


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL81487E)

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

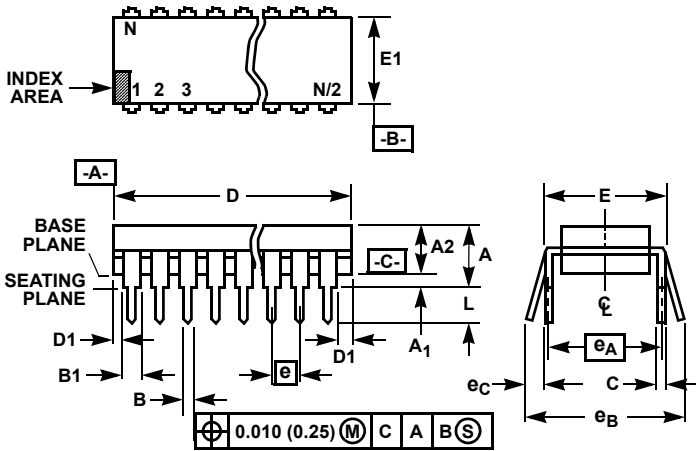
PROCESS:

Si Gate CMOS

Revision History The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|--------------|----------|--|
| Sep 20, 2018 | FN6051.8 | Applied Renesas Header/Footer. Added Related Literature section. Updated Ordering Information table by removing retired parts ISL8487EIB, ISL81487LIB, ISL81487LIP, and ISL81487EIP, adding Notes 1 and 3, and adding tape and reel parts and column. Updated the Typical Operating Circuit diagram on page 2. Added Revision History section. Updated POD M8.15 to the latest revision. Changes are as follows: -Revision 1: Initial revision -Revision 1 to revision 2: Updated to new package outline drawing format by removing table, moving dimensions onto drawing, and adding land pattern -Revision 2 to revision 3: Changed the following values in Typical Recommended Landing Pattern: 2.41(0.095) to 2.20 (0.087) 0.76(0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to revision 4: Changed text in Note 1 from "1982" to "1994" |

Package Outline Drawings



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.300 BSC | | 7.62 BSC | | 6 |
| e_B | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

Rev. 0 12/93

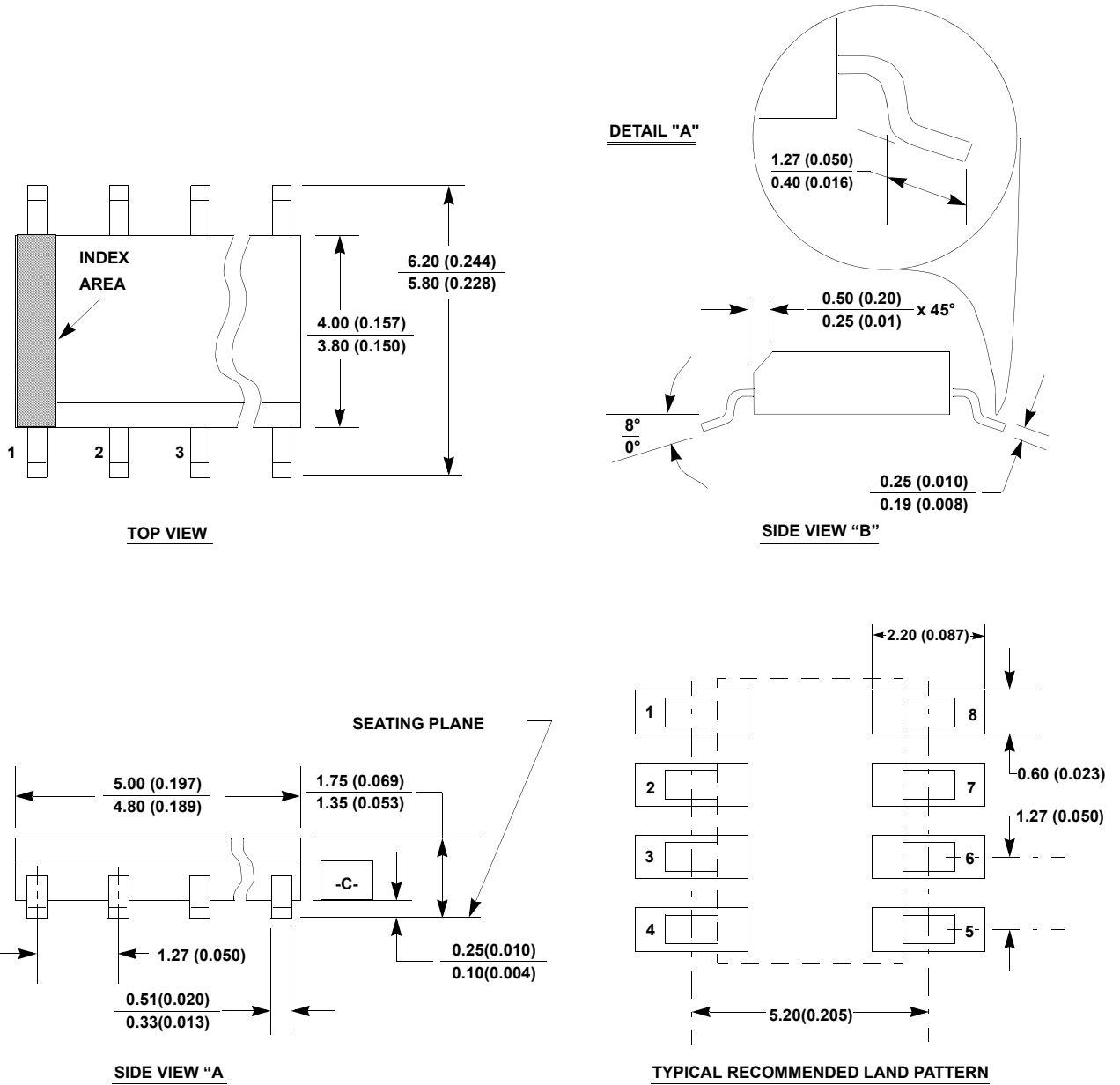
For the most recent package outline drawing, see [E8.3](#).

M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 1/12

For the most recent package outline drawing, see [M8.15](#).



NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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