User's Manual

RAA3064002GFP/RAA3064003GFP
Renesas CMOS ICs
Resolver-to-Digital Converters

User's Manual: Hardware

Renesas Electronics
www.renesas.com

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

CONTENTS

RAA3064002GFP/RAA3064003GFP

Renesas CMOS ICs
Resolver-to-Digital Converters

R03UZ0002EJ0100
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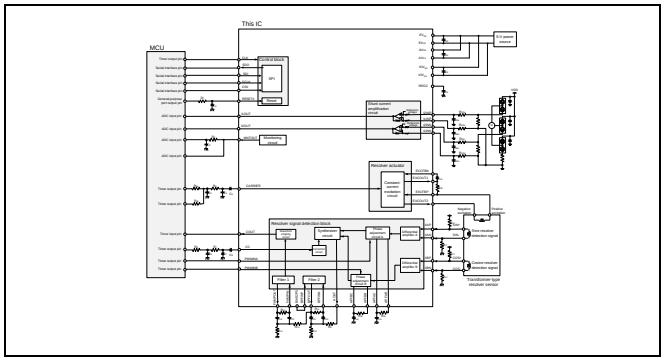
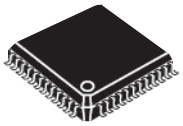
Nov 20, 2019

Intended for use with a single-phase excitation input and two-phase output type resolver sensor
Frequency of the excitation signal is selectable from 5 kHz, 10 kHz, and 20 kHz.

Features

- Intended for use with the host MCU, this IC chip converts signals (electrical angle information) detected by the resolver sensor (angle sensor) to digital signals.
  - Connectable to a transformer-type or current-detection type resolver sensor of single-phase excitation input and two-phase output structure
  - Integrated exciter amplifier (excitation frequency: 5 kHz, 10 kHz, or 20 kHz)
  - Resolution of the angle signal (electrical angle):16,000 pulses/rotation
    (excitation frequency: 5 kHz; operating frequency of the host MCU timer: 80 MHz)
- Correction of errors in the detected signals from the resolver
  - Correction of the residual carrier in the signals detected by the resolver sensor
  - Analog filters to eliminate the resolver's magnetic noise and PWM noise from motor control
- Error detection
  - Detection of disconnection from the resolver sensor
  - Detection of an excessive temperature within the IC chip





PLQP0048KB-B (7 x 7 mm, 0.5-mm pitch)

- Power-saving function
  - Single power source operating between 4.5 V to 5.5 V
  - Circuits not in use can be placed in the power-saving state to save power
- Motor control
  - Two shunt current amplifiers
    Gain: x10 or x25
- Serial interface
  - Communications with the host MCU (clock synchronous, up to 1-MHz clock)
- Clock and reset signals
  - Frequency of the externally-input clock:
    Up to 4 MHz
  - Three types of reset: Reset by the RESET# pin, voltage detection, or software
- Operating ambient temperature
  - -40°C to +85°C (RAA3064002GFP)
  - -40°C to +105°C (RAA3064003GFP)
- Application
  - Applications using motors that require high-resolution angle information, excluding those for automotive use

1. Overview

The RAA3064002GFP and RAA3064003GFP (hereinafter together referred to as “this IC”) are resolver-to-digital converters which are intended for use with single-phase excitation, two-phase output type resolver sensors (angle sensors). The resolver sensor outputs analog signals (electrical angle information) which are proportional to the angle of the mechanical rotation of the resolver. This IC converts these analog signals to digital signals.

This IC can be connected to either of two types of resolver sensor. Figure 1.1 shows the configurations of the connectable resolvers. In this user’s manual, we define the configurations of transformer-type and current-detection type resolver sensors as shown in (a) and (b) in figure 1.1, respectively.

This IC outputs a single-phase excitation signal to the resolver sensor. The signal is triggered by the excitation clock signal (rectangular excitation wave) input from the host MCU. This IC then generates an angle signal (rectangular wave) from the two-phase signals (electrical angle information) detected by the resolver sensor, and outputs the angle signal to the host MCU. Angle information can be obtained by using the host MCU to measure the phase difference between the rectangular excitation wave and angle signal. **Note 1**

The frequency of the excitation signal input to the resolver sensor is selectable as 5 kHz, 10 kHz, or 20 kHz. Select a frequency that suits the characteristics of the resolver.

This IC incorporates amplifiers that are configured with noise filters to eliminate noise in the signals detected by the resolver sensor, and a circuit to correct errors in the detected signals from the resolver. This IC also has functionality for detecting an excessive temperature within the chip and two shunt current amplifiers for use in general motor control circuits.

Note 1. See Basic Operation for Conversion of Signals from Resolver.

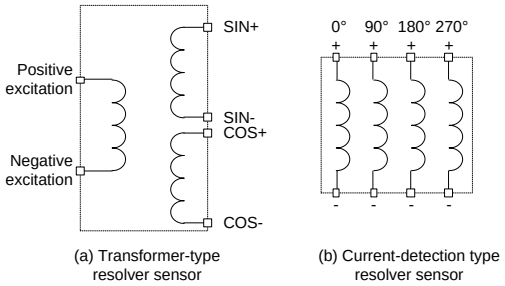


Figure 1.1 Configurations of the Connectable Types of Resolver Sensor

1.1 Features

- Integrated exciter amplifier (excitation frequency: 5 kHz, 10 kHz, or 20 kHz; host MCU: RX24T)
- Resolution of the angle signal (electrical angle): 16,000 pulses/rotation (excitation frequency: 5 kHz; operating frequency of the host MCU timer: 80 MHz)
- Correction of errors in the detected signals from the resolver
- Detection of an excessive temperature within the IC chip
- 5-V single power supply

1.2 Application

Applications using motors that require high-resolution angle information, excluding those for automotive use

1.3 Part Number

Table 1.1 lists the part numbers.

Table 1.1 List of Part Numbers

Package	Operating Temperature Range	Order Code
48-pin plastic LQFP	-40°C to +85°C	RAA3064002GFP#BA0
48-pin plastic LQFP	-40°C to +105°C	RAA3064003GFP#BA0

1.4 Overview of Functions

Table 1.2 lists the overview of functions.

Table 1.2 Overview of Functions

Item		Function
Resolver actuator	Excitation input	AC signal: 5,10, or 20 kHz (when the host MCU is RX24T)
	Excitation output	AC current: +/- 35 mA (Max.)
Resolver signal detection block	Input of the signal detected by the resolver	Variable gain: Gain of 2, 4, 8, or 16.5
	Signal conversion	Correction of errors in the detected signals from the resolver
	Angle signal output	The angle signal with its phase delayed in proportion to the resolver angle is output in response to the excitation signal.
Shunt current amplification circuit	Differential amplifier	Two amplifiers Variable gain: Gain of 10 or 25
Control block	Operating frequency	Up to 4 MHz
	Serial communication circuit	Clock synchronous serial communications (max. 1 MHz)
Detection of the chip's internal state	Detection of the input level	Detection of the input level of the signals from the resolver
	Detection of a temperature	Detection of an excessive internal temperature
	Output of the selected internal signal	Output of the detected temperature, and selected internal signal in the resolver signal detection block
Power supply voltage		AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V
Power supply current		Operating current: 20 mA (typ.) (other than the excitation output current) During a reset: 420 µA (typ.)
Operating ambient temperature		RAA3064002GFP: -40 to +85°C RAA3064003GFP: -40 to +105°C
Package		48-pin plastic LQFP (7 x 7 mm, 0.5-mm pitch)

1.5 Pin Assignment

Figure 1.2 shows a pin assignment.

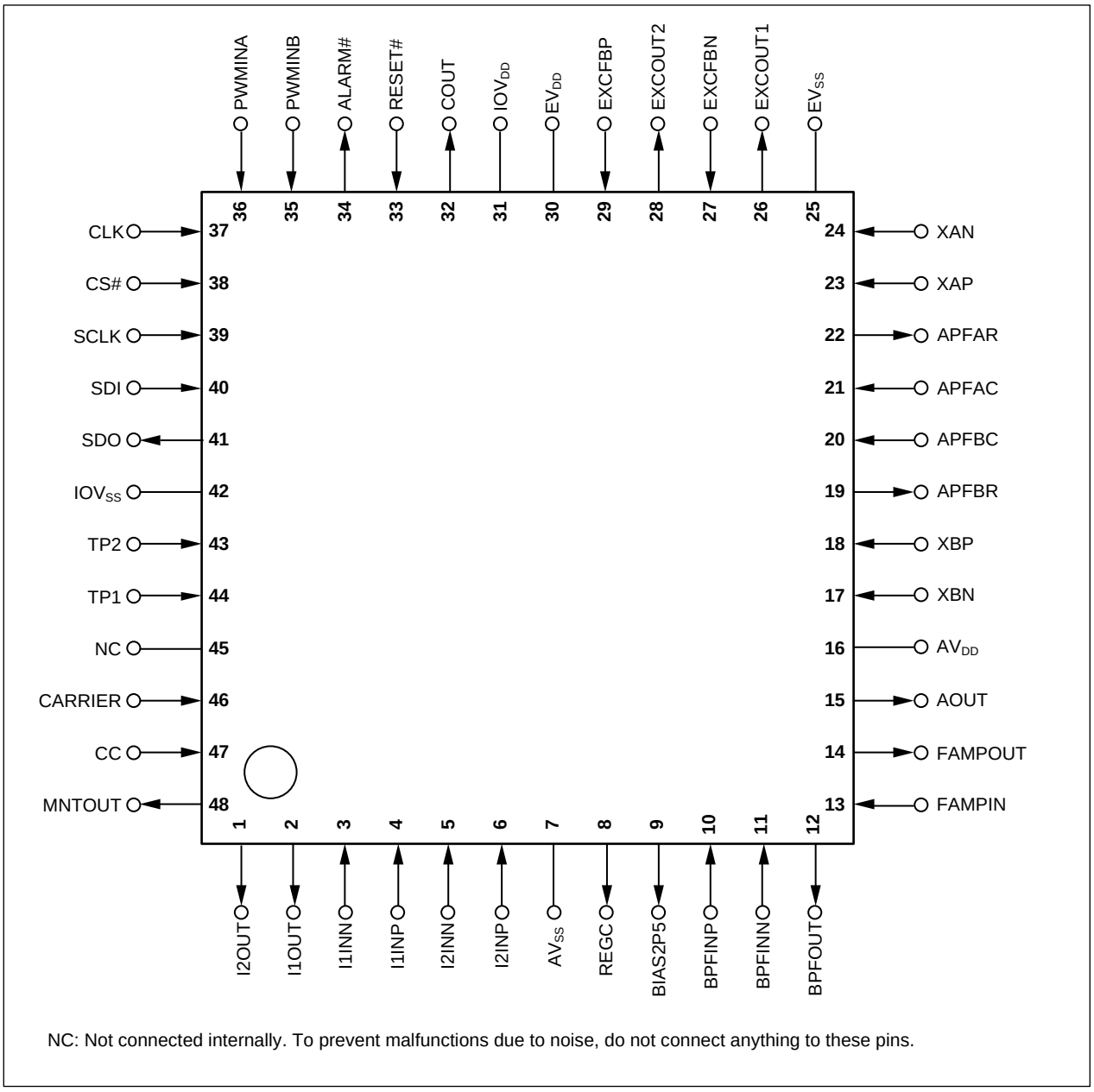


Figure 1.2 Pin Assignment (Top View)

1.6 List of Pin Functions

Table 1.3 lists the pin functions.

Table 1.3 List of Pin Functions (1/2)

Pin No.	Pin Name	Input/ Output	Function	Type	Power Supply	During and after a Reset
1	I2OUT	Output	Signal amplified by differential amplifier 2 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
2	I1OUT	Output	Signal amplified by differential amplifier 1 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
3	I1INN	Input	Negative input to differential amplifier 1 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
4	I1INP	Input	Positive input to differential amplifier 1 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
5	I2INN	Input	Negative input to differential amplifier 2 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
6	I2INP	Input	Positive input to differential amplifier 2 in the shunt current amplification circuit	Analog	AV_{DD}	Hi-Z
7	AV_{SS}	—	Ground for analog circuits	GND	—	—
8	REGC	Output	Capacitor connection pin for reference voltage (pulling down to GND by 0.1 µF is recommended.)	Analog	AV_{DD}	Hi-Z
9	BIAS2P5	Output	Reference voltage (2.5 V)	Analog	AV_{DD}	Hi-Z
10	BPFINP	Input	Positive signal input to the amplifier of filter 2	Analog	AV_{DD}	Hi-Z
11	BPFINN	Input	Negative signal input to the amplifier of filter 2	Analog	AV_{DD}	Hi-Z
12	BPFOUT	Output	Output from the amplifier of filter 2	Analog	AV_{DD}	Hi-Z
13	FAMPIN	Input	Input to the amplifier of filter 1	Analog	AV_{DD}	Hi-Z
14	FAMPOUT	Output	Output from the amplifier of filter 1	Analog	AV_{DD}	Hi-Z
15	AOUT	Output	Output from the synthesizer circuit	Analog	AV_{DD}	Hi-Z
16	AV_{DD}	—	Power supply for analog circuits	Power supply	—	—
17	XBN	Input	Negative cosine signal from the resolver	Analog	AV_{DD}	Hi-Z
18	XBP	Input	Positive cosine signal from the resolver	Analog	AV_{DD}	Hi-Z
19	APFBR	Output	Amplified cosine resolver detection signal	Analog	AV_{DD}	Hi-Z
20	APFBC	Input	Filtered cosine resolver detection signal	Analog	AV_{DD}	Hi-Z
21	APFAC	Input	Filtered sine resolver detection signal	Analog	AV_{DD}	Hi-Z
22	APFAR	Output	Amplified sine resolver detection signal	Analog	AV_{DD}	Hi-Z
23	XAP	Input	Positive sine signal from the resolver	Analog	AV_{DD}	Hi-Z
24	XAN	Input	Negative sine signal from the resolver	Analog	AV_{DD}	Hi-Z
25	EV_{SS}	—	Ground for the constant-current excitation circuit	GND	—	—
26	EXCOUT1	Output	Positive excitation current	Analog	EV_{DD}	Hi-Z
27	EXCFBN	Input	Excitation current filter input	Analog	EV_{DD}	Hi-Z
28	EXCOUT2	Output	Negative excitation current	Analog	EV_{DD}	Hi-Z
29	EXCFBP	Input	Excitation reference current	Analog	EV_{DD}	Hi-Z
30	EV_{DD}	—	Power supply for the constant-current excitation circuit	Power supply	—	—

Table 1.3 List of Pin Functions (2/2)

Pin No.	Pin Name	Input/ Output	Function	Type	Power Supply	During and after a Reset
31	IOV_{DD}	—	Power supply for digital circuits	Power supply	—	—
32	COUT	Output	Angle signal	Digital	IOV_{DD}	Hi-Z
33	RESET#	Input	Reset	Digital	IOV_{DD}	Hi-Z
34	ALARM#	Output	Alarm detection signal If an abnormality is not being detected, the level on the pin becomes high in response to clock input.	Digital	IOV_{DD}	Hi-Z
35	PWMINB	Input	Adjustment signal input for phase adjustment circuit B	Digital	IOV_{DD}	Hi-Z
36	PWMINA	Input	Adjustment signal input for phase adjustment circuit A	Digital	IOV_{DD}	Hi-Z
37	CLK	Input	Reference clock (4 MHz)	Digital	IOV_{DD}	Hi-Z
38	CS#	Input	Serial communications enable	Digital	IOV_{DD}	Hi-Z
39	SCLK	Input	Serial communications clock	Digital	IOV_{DD}	Hi-Z
40	SDI	Input	Data for serial reception	Digital	IOV_{DD}	Hi-Z
41	SDO	Output	Data for serial transmission	Digital	IOV_{DD}	Hi-Z
42	IOV_{SS}	—	Digital ground	GND	—	—
43	TP2	Input	Fixed to low level (pulling down by a resistor is recommended.)	Digital	IOV_{DD}	Hi-Z
44	TP1	Input				
45	NC	—	—	—	—	—
46	CARRIER	Input	Rectangular excitation wave signal	Analog	AV_{DD}	Hi-Z
47	CC	Input	Correction signal for the resolver detection signal	Analog	AV_{DD}	Hi-Z
48	MNTOUT	Output	Monitoring of the selected internal signal	Analog	AV_{DD}	Hi-Z

2. Circuit Configuration

2.1 Example of a System Configuration

Figures 2.1 and 2.2 show examples of system configurations. For the specifications of the recommended peripheral components, see the application note *Guide to Selecting Peripheral Components for Use with the Resolver-to-Digital Converters* (R03AN0012EJ).

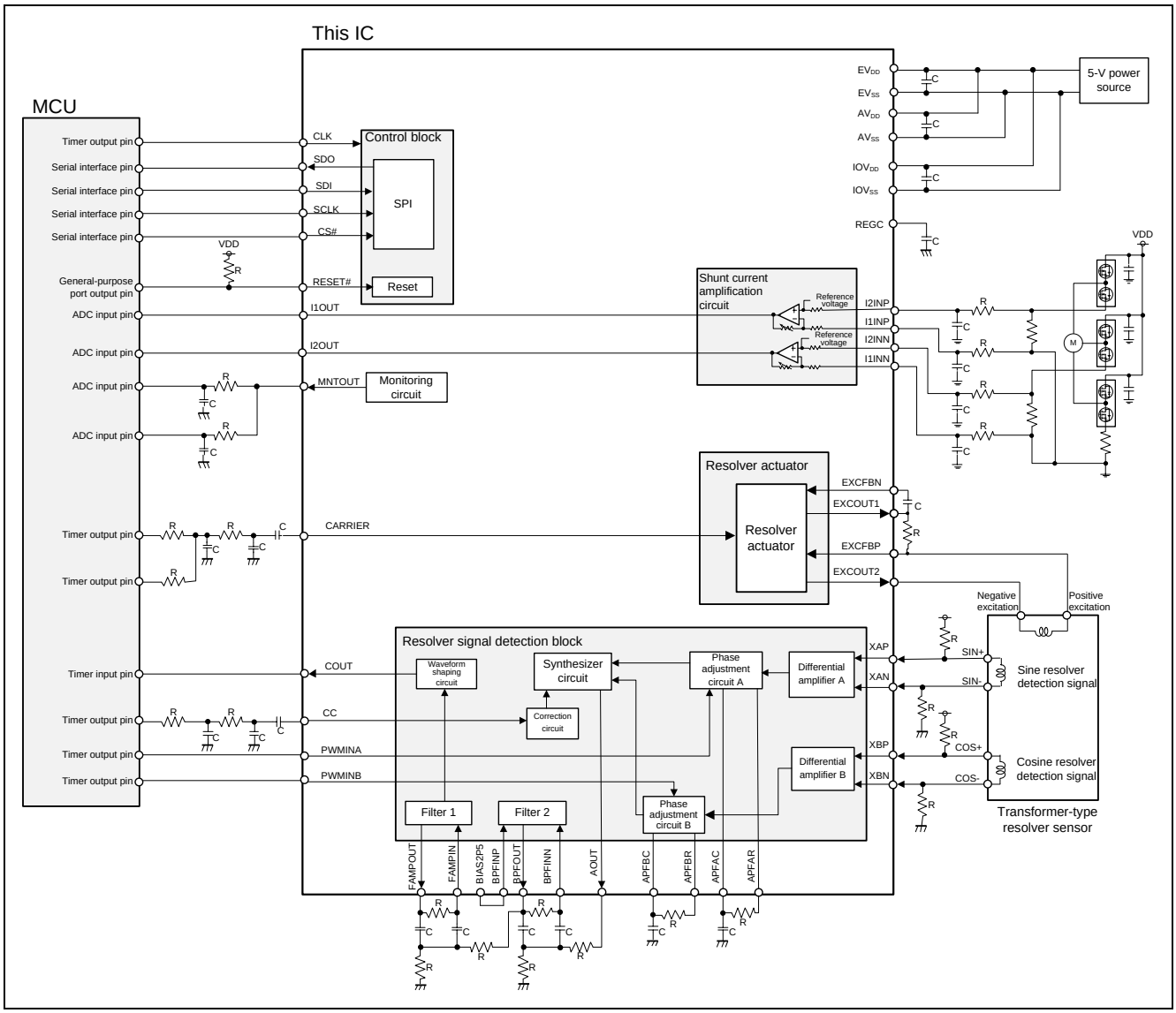


Figure 2.1 Example of a System Configuration with a Transformer-Type Resolver Sensor and Multiple-Feedback First-Order Band-Pass Filters 1 and 2

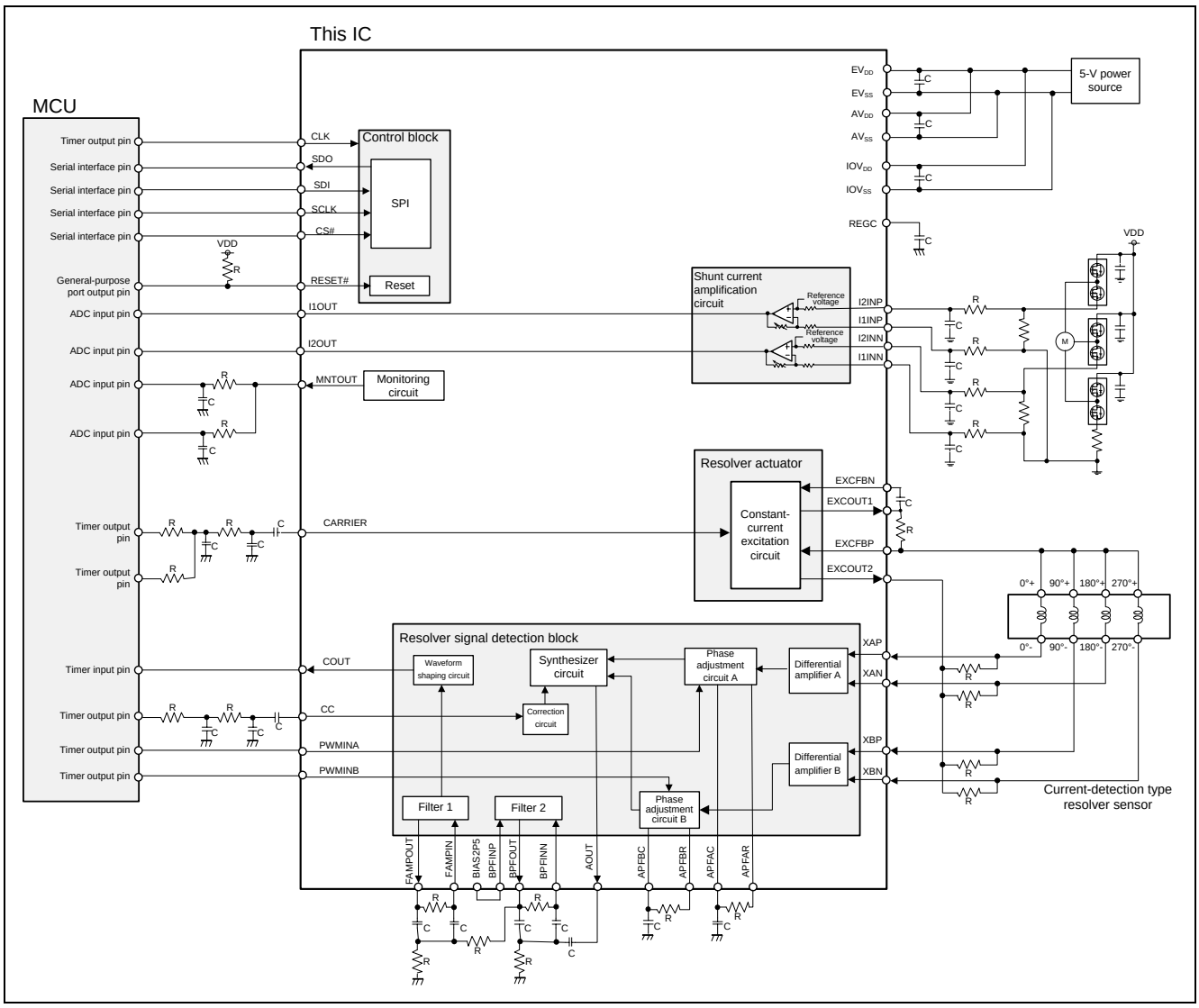


Figure 2.2 Example of the System Configuration with a Current-Detection Type Resolver Sensor, a Multiple Feedback Second-Order High-Pass Filter 1, and a Multiple-Feedback First-Order Band-Pass Filter 2

2.2 Internal Block Diagram

Figure 2.3 shows an internal block diagram.

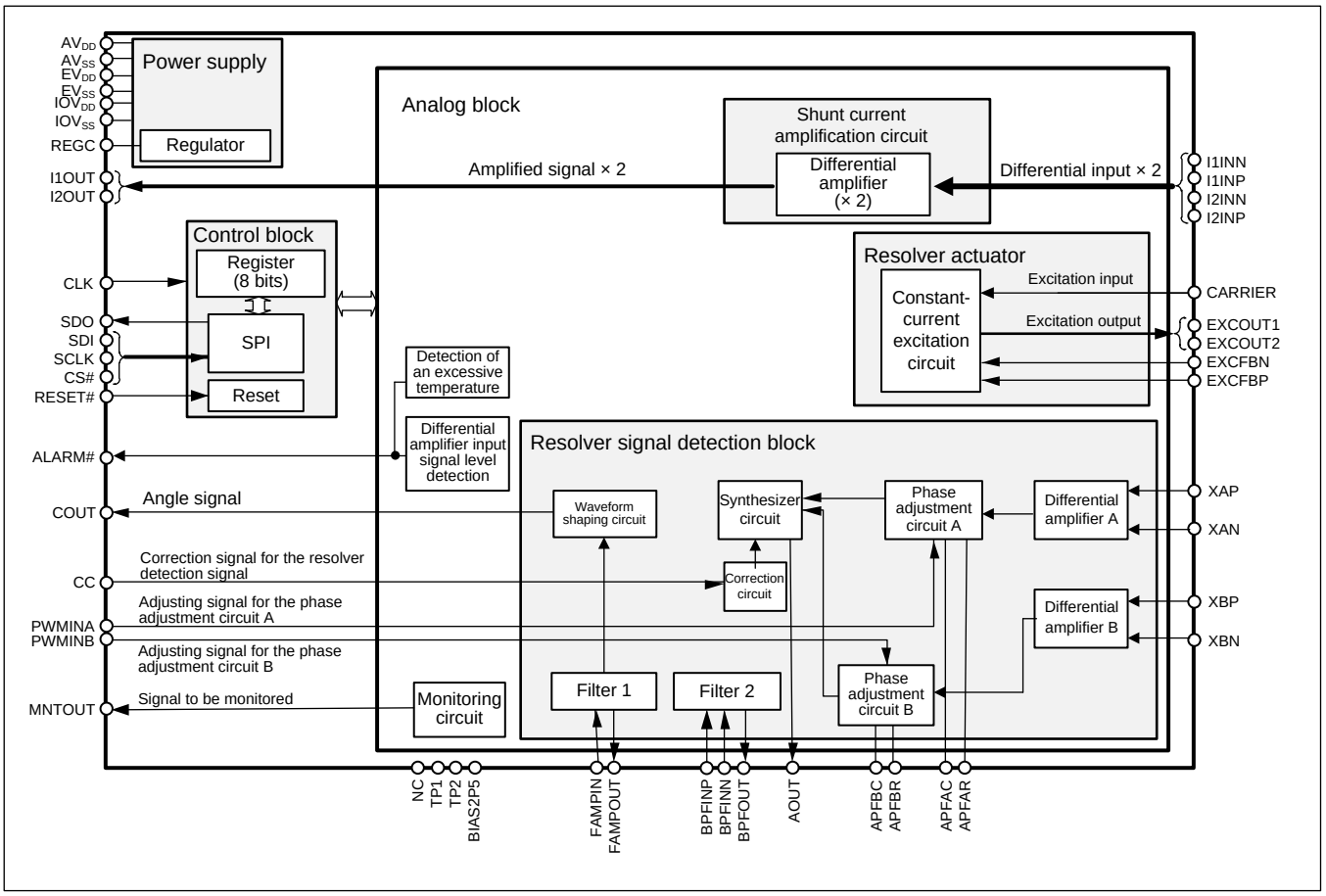


Figure 2.3 Internal Block Diagram

2.3 Internal Circuit

2.3.1 Resolver Actuator

The resolver actuator is configured by a constant-current excitation circuit. Figure 2.4 shows an actuator and its external circuit. The current that drives the resolver can be controlled by the amplitude of the excitation clock signal applied on the CARRIER pin and a current limiting resistor R connected between EXCOUT1 and EXCFBP.

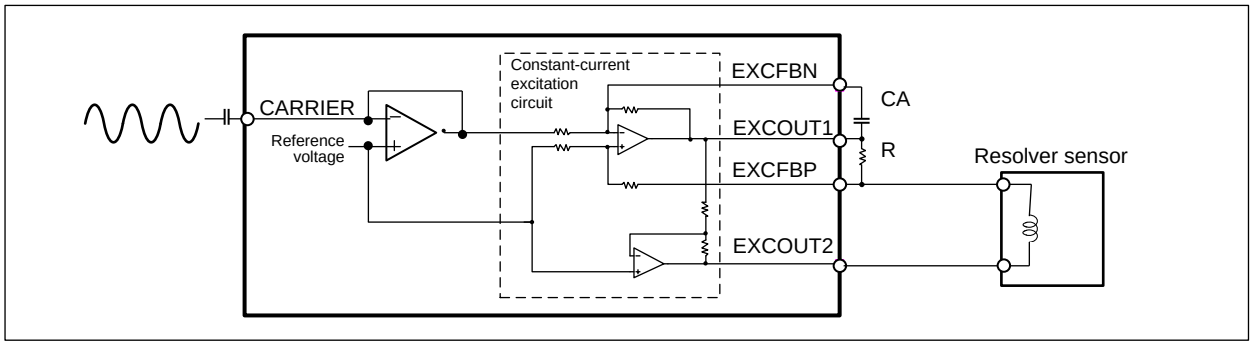


Figure 2.4 Resolver Actuator

2.3.2 Resolver Signal Detection Block

The resolver signal detection block consists of the following circuits.

- Differential amplifiers A and B
- Phase adjustment circuits A and B
- A synthesizer circuit
- Filters
- A waveform shaping circuit

Figure 2.5 shows the resolver signal detection block and its external circuit.

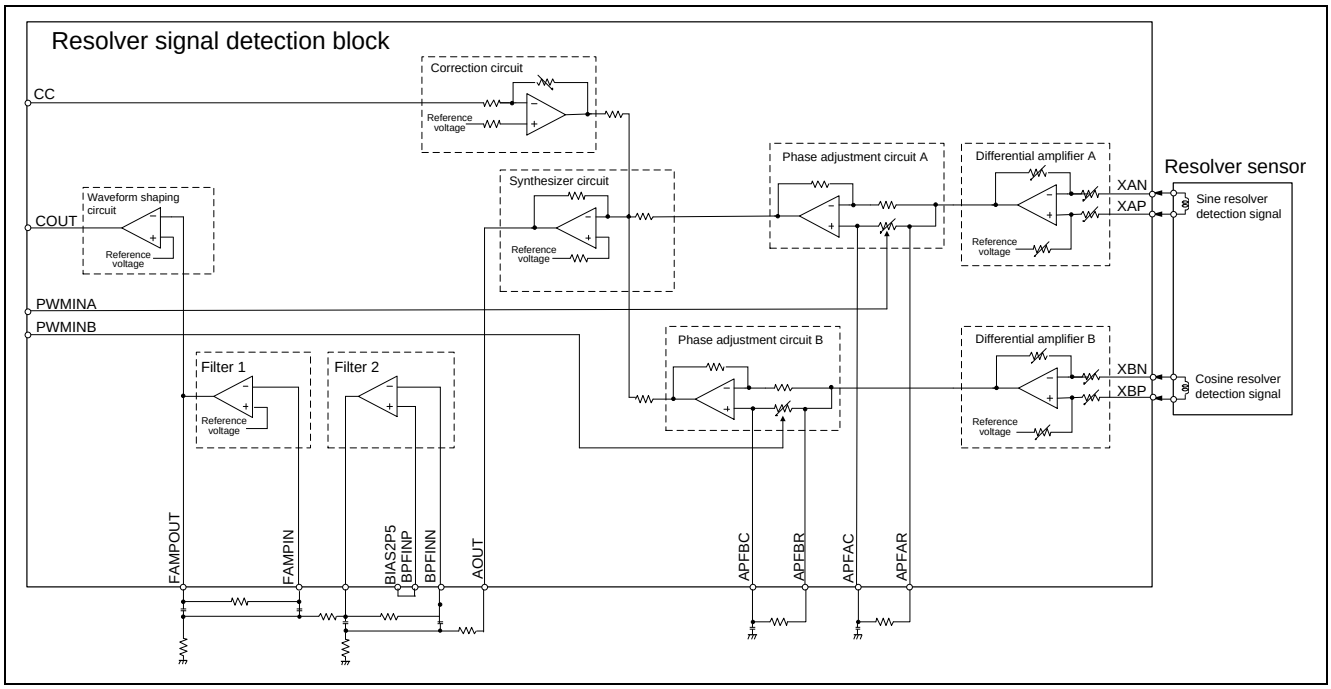


Figure 2.5 Resolver Signal Detection Block

The two-phase signals from the resolver sensor are input to the resolver signal detection block through the XAP and XAN pins, and the XBP and XBN pins. The respective pairs of signals are amplified by differential amplifiers A and B. The gain should be set to suit the type and modulation rate of the resolver.

The respective amplified two-phase signals are then adjusted by adjustment circuits A and B so that their phase differential is 90 degrees. The adjustment is handled in accord with the PWMINA and PWMINB signals.

The phase-adjusted two-phase signals are then synthesized in the synthesizer circuit. By synthesizing the correction signal input to the CC pin at the same time, the carrier errors generated by errors in the coils of the resolver sensor can be corrected.

The synthesized signal is filtered to eliminate the resolver's magnetic noise and PWM noise from motor control. This block includes filters 1 and 2 for a double-filter configuration. The filtered signal, with the noise eliminated, is then passed to the waveform shaping circuit and is shaped to form an angle signal. This angle signal is then output through the COUT pin as a rectangular waveform.

Figure 2.5 shows an example of a system configuration with the two multiple-feedback first-order band-pass filters.

The angle signal with its phase delayed in proportion to the resolver angle is output from the waveform shaping circuit in response to the excitation signal. Angle information can be obtained by using the host MCU to measure the phase between the rectangular excitation wave and the angle signal.

2.3.3 Shunt Current Amplification Circuit

The shunt current amplification circuit consists of two differential amplifiers. The differential amplifiers amplify the differential voltage between the InINP and InINN pins and outputs the results through InOUT (n = 1 or 2). The bias voltage and gain of the differential amplifiers are specifiable.

Figure 2.6 shows an example of usage of the shunt current amplifiers connected to motor drivers and shunt resistors.

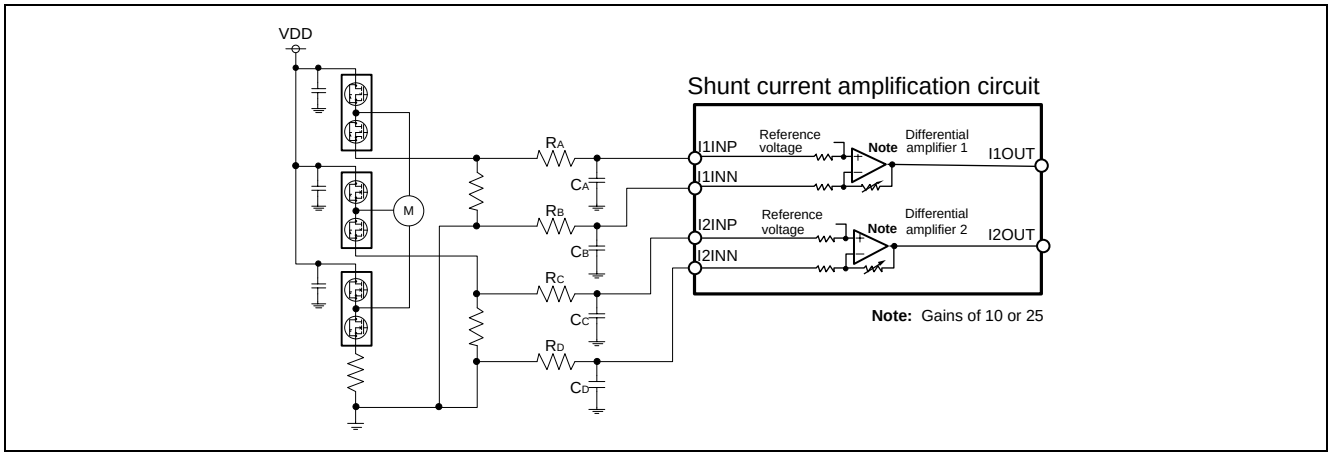


Figure 2.6 Shunt Current Amplification Circuit

Connecting the shunt resistors for use in current detection may lead to the generation of noise by the surge voltage of the MOSFET motor driver. The external components that configure low-pass filters are required to eliminate this noise. Note that, when resistors for the filter circuits (RA, RB, RC, and RD) are connected in series to the InINN and InINP pins (n = 1 or 2), the value should be no greater than 100 Ω.

Relatively larger resistances may increase the input impedance, with the result of failure to attain a value for current gain that is in the specified range.

2.3.4 Control Block

The control block consists of a reset generating circuit, an SPI interface, and registers. Operations are triggered by the clock signal input through the CLK pin.

This block can be reset by any from among the following reset sources: RESET#, voltage detection reset, or software reset. Table 2.1 shows the types of resets and sources. The reset generating circuit conveys the reset signals generated by each type of reset within the IC.

The SPI interface has four signal pins, one each for the serial communications clock (SCLK), reception and transmission of data in serial communications (SDI and SDO), and serial communications enable (CS#). Read and write access to registers in this IC by an external device is handled through these pins.

For setting and reading the data in the registers, see 3.3 Access to the Registers.

Table 2.1 Types of Reset and Sources

Type of Reset	Source
Reset by the RESET# pin	Signal on the RESET# pin being driven low
Voltage detection reset	Excessive dropping of AVDD or IOVDD
Software reset	Setting of the given bit in the SWRST register

2.3.5 Detection of the Internal State

This IC can detect the levels of the signals being input to the differential amplifiers and excessive temperatures within the chip. A signal from among these can be selected for output, allowing the external monitoring of the IC's internal state. The signal from monitoring can be handled in two ways: as an AC signal or as a DC signal following half-wave rectification and filtering by an external low-pass filter. The signal to be monitored is output from the MNTOUT pin. The internal signal to be output is specified by using the monitor output selection register (MNTSL). The output mode is specified by using the monitor output mode selection register (MDCACSEL). Figure 2.7 shows an example of the monitoring circuit and external connections.

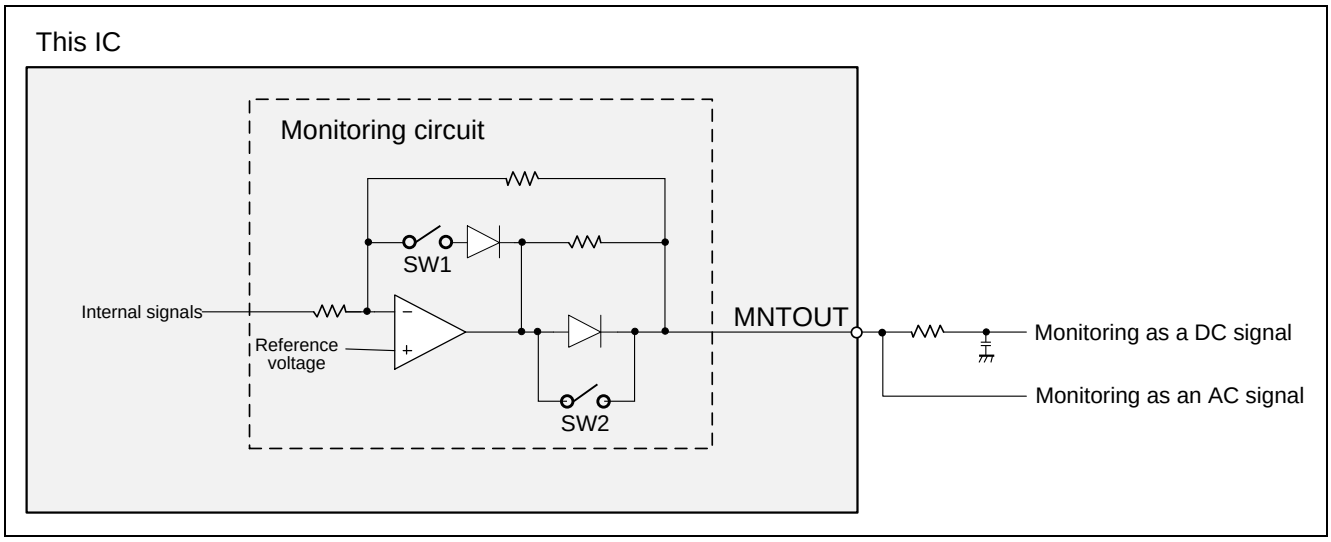


Figure 2.7 Example of the Monitoring Circuit and External Connections

Detecting whether inputs to the XAP and XAN pins and XBP and XBN pins are within the allowable voltage range is possible by reading the output from the ALARM# pin. The ALARM# pin outputs the low level when a differential signal is out of the allowable range. This function is not applicable to the inputs to the I1INN and I1INP pins and I2INN and I2INP pins.
Detection of an excessive temperature within the chip is also possible by reading the output from the ALARM# pin. The ALARM# pin outputs the low level when the temperature exceeds the specified upper limit.

2.3.6 Power Supply Circuit

This IC has three pairs of power supply pins. EVDD and EVSS are exclusively used for the constant-current excitation circuit. AVDD and AVSS are used for the other analog circuits. The reference voltage used for the analog circuits and 2.1-V power supply used for the logic circuits in the controller are generated by an on-chip regulator having AVDD as the reference voltage. IOVDD and IOVSS are used for the digital I/O and 5-V logic circuits of the controller.

Use a single +5-V ± 10% power source with this IC. Connect 0.1-uF multilayer ceramic capacitors creating the shortest possible closed loops between the pairs of pins for each of the power supplies as a measure against noise.

The REGC pin is used to connect the stabilizing capacitor for the on-chip regulator. Connect a multilayer 0.1-uF ceramic capacitor in the vicinity of the REGC pin and ground it to AVSS.

Figure 2.8 shows an example of handling of the power supply pins.

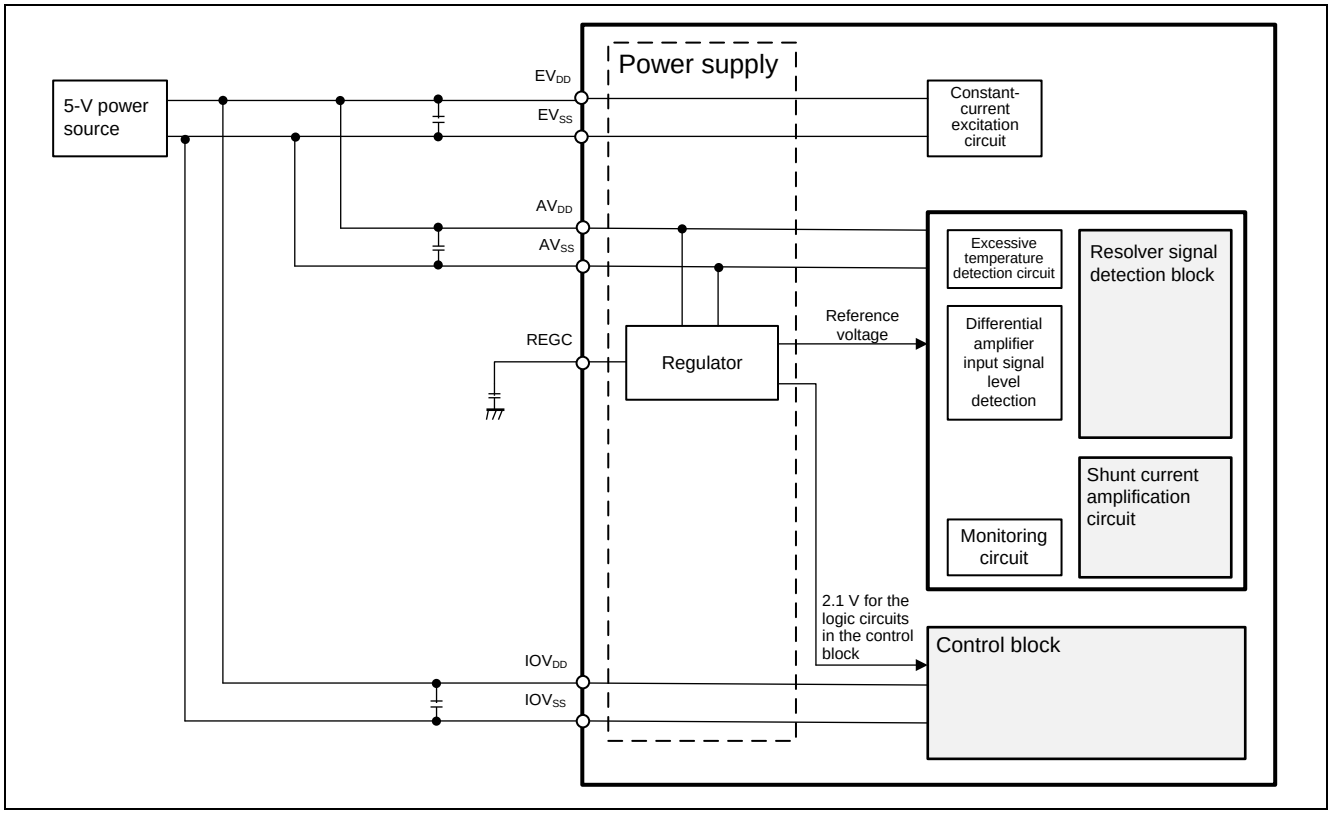


Figure 2.8 Example of Handling of the Power Supply Pins

3. Control Registers

3.1 List of Registers

Table 3.1 List of Registers

Register Name	Symbol	Number of Bits	R/W	Address	Value After a Reset
Power-saving control register 1	PS1	8	R/W	02H	00H
Power-saving control register 2	PS2	8	R/W	04H	00H
Power-saving control register 3	PS3	8	R/W	0AH	00H
Software reset register	SWRST	8	R/W	06H	00H
Differential amplifier input range monitoring register	DDMNT	8	R	0EH	00H
Alarm state register	ALMST	8	R/W	12H	FFH
ALARM# output setting register	ALMOUT	8	R/W	16H	00H
Monitor output selection register	MNTSL	8	R/W	20H	00H
Monitor output mode selection register	MDCACSEL	8	R/W	28H	00H
Differential amplification circuit gain selection register	GCGSL	8	R/W	2EH	00H
Phase adjustment circuit gain adjustment value selection register	DLCGSL	8	R/W	30H	00H
Correction circuit gain selection register	CCGSL	8	R/W	36H	00H
Shunt current amplification circuit control register	CSACTL	8	R/W	42H	00H
Differential amplifier input level detection resetting register	INITERR	8	R/W	54H	00H

3.2 Register Descriptions

3.2.1 Power-Saving Control Register 1 (PS1)

The PS1 register is used to control the power-saving state of the IC other than the control block and temperature detection circuit.

Address: 02H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PSALL

Bit	Bit Name	Function
7 to 1	—	Reserved
0	PSALL	Power-saving control of the IC other than the control block and temperature detection circuit 0: Placed in the power-saving state 1: Released from the power-saving state

Remark Bits 7 to 1 are read as 0. The write value should also be 0.

3.2.2 Power-Saving Control Register 2 (PS2)

The PS2 register is used to control the power-saving state of individual circuits.

The settings in this register has no effect when the PSALL bit in the PS1 register is set to 0 (placing the IC in the power-saving state).

Address: 04H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
PSCAR	PSDLC	PSDS	PSGC	PSBPF2	PSB2P5	0	PSREF

Bit	Bit Name	Function
7	PSCAR	Power-saving control of the correction circuit 0: Placed in the power-saving state 1: Released from the power-saving state
6	PSDLC	Power-saving control of phase adjustment circuit 0: Placed in the power-saving state 1: Released from the power-saving state
5	PSDS	Power-saving control of the circuit to detect the level of voltage input to the differential amplifiers 0: Placed in the power-saving state 1: Released from the power-saving state
4	PSGC	Power-saving control of the differential amplifiers 0: Placed in the power-saving state 1: Released from the power-saving state
3	PSBPF2	Power-saving control of the filter 2 0: Placed in the power-saving state 1: Released from the power-saving state
2	PSB2P5	Power-saving control of the reference voltage circuit 0: Placed in the power-saving state 1: Released from the power-saving state
1	—	Reserved
0	PSREF	Power-saving control of the reference current circuit 0: Placed in the power-saving state 1: Released from the power-saving state

Remark Bit 1 is read as 0. The write value should also be 0.

3.2.3 Power-Saving Control Register 3 (PS3)

The PS3 register is used to control the power-saving state of individual circuits.

The settings in this register has no effect when the PSALL bit in the PS1 register is set to 0 (placing the IC in the power-saving state).

Address: 0AH Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
PSEXC	PSCBUF	PSMON	PSCOMP	PSDITH	PSGA	PSBPF1	PSADD

Bit	Bit Name	Function
7	PSEXC	Power-saving control 1 of the excitation circuit 0: Placed in the power-saving state 1: Released from the power-saving state
6	PSCBUF	Power-saving control 2 of the excitation circuit 0: Placed in the power-saving state 1: Released from the power-saving state
5	PSMON	Power-saving control of the monitoring circuit 0: Placed in the power-saving state 1: Released from the power-saving state
4	PSCOMP	Power-saving control 1 of the waveform shaping circuit 0: Placed in the power-saving state 1: Released from the power-saving state
3	PSDITH	Reserved
2	PSGA	Power-saving control 2 of the waveform shaping circuit 0: Placed in the power-saving state 1: Released from the power-saving state
1	PSBPF1	Power-saving control of the filter 1 0: Placed in the power-saving state 1: Released from the power-saving state
0	PSADD	Power-saving control of the synthesizer circuit 0: Placed in the power-saving state 1: Released from the power-saving state

Remark Bit 3 is read as 0. The write value should also be 0.

3.2.4 Software Reset Register (SWRST)

The SWRST register is used to reset the IC by software at desired times after operation has started.

Address: 06H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SWRST

Bit	Bit Name	Function
7 to 1	—	Reserved
0	SWRST	Software reset 1: Placed in the reset state 0: Released from the reset state After writing 1, write 0 to release from the reset state.

Remark Bits 7 to 1 are read as 0. The write value should also be 0.

3.2.5 Differential Amplifier Input Range Monitoring Register (DDMNT)

The DDMNT register indicates whether inputs to the differential amplifiers are within the allowable range.

Address: 0EH Value after a reset: FFH R/W: R

7	6	5	4	3	2	1	0
0	0	0	0	XB1	1	XA1	1

Bit	Bit Name	Function
7 to 4	—	Reserved
3	XB1	Differential amplifier B input signal level detection flag 0: The input voltage between the XBP and XBN pins is within the V_{INX} range. 1: The input voltage between the XBP and XBN pins is out of the V_{INX} range.
2	—	Reserved
1	XA1	Differential amplifier A input signal level detection flag 0: The input voltage between the XBP and XBN pins is within the V_{INX} range. 1: The input voltage between the XBP and XBN pins is out of the V_{INX} range.
0	—	Reserved

3.2.6 Alarm State Register (ALMST)

The ALMST register indicates the source of the ALARM# output.

The bit corresponding to the source is set to 0. After checking the source, clear the bit by writing 1. Writing 0 has no effect.

Address: 12H Value after a reset: FFH R/W: R/W

7	6	5	4	3	2	1	0
1	1	1	BWCN	1	1	1	TSD

Bit	Bit Name	Function
7 to 5	—	Reserved
4	BWCN	Differential amplifier A or B input signal level detection flag 0: At least one input voltage is out of the V_{INX} range. 1: Both input voltages are within the V_{INX} range.
3 to 1	—	Reserved
0	TSD	Internal excessive temperature (125°C or above) detection flag 0: Excessive temperature is detected. 1: Excessive temperature is not detected.

Remark Bits 7 to 5 and 3 to 1 are read as 1. The write value should also be 1.

3.2.7 ALARM# Output Setting Register (ALMOUT)

The ALMOUT register is used to specify the source of the ALARM# output.

Address: 16H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	DDAN	0	0	0	TSDAN

Bit	Bit Name	Function
7 to 5	—	Reserved
4	DDAN	0: The active level of the ALAMR# signal is not output on detection of the input signals to a differential amplifier being out of the V_{INX} range. 1: The active level of the ALAMR# signal is output on detection of the input signals to a differential amplifier being within the V_{INX} range.
3 to 1	—	Reserved
0	TSDAN	0: The active level of the ALARM# signal is not output on detection of an excessive temperature (125°C or above). 1: The active level of the ALARM# signal is output on detection of an excessive temperature (125°C or above).

Remark Bits 7 to 5 and 3 to 1 are read as 0. The write value should also be 0.

When the DDAN and TSDAN bits are set to 1, the reason for the output of the active level of ALARM# can be checked by reading the ALMST register (see Differential Amplifier Input Range Monitoring Register (DDMNT)).

3.2.8 Monitor Output Selection Register (MNTSL)

The MNTSL register is used to select the signal to be output to the MNTOUT pin.

Address: 20H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	MNT[2:0]		

Bit	Bit Name	Function
7 to 3	—	Reserved
2 to 0	MNT[2:0]	Selection of MNTOUT output 000: Temperature sensor output 001: Filter 1 output 010: Phase adjustment circuit A output 011: Phase adjustment circuit B output 100: Differential input circuit A output 101: Differential input circuit B output 110: Reference voltage for shunt current amplifier 1 111: Reference voltage for shunt current amplifier 2

Remark Bits 7 to 3 are read as 0. The write value should also be 0.

3.2.9 Monitor Output Mode Selection Register (MDCACSEL)

The MDCACSEL register is used to select the waveform mode of the signal output from the MNTOUT pin.

Address: 28H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DCAC

Bit	Bit Name	Function
7 to 1	—	Reserved
0	DCAC	Output waveform mode select 0: Half-wave rectification 1: AC output

Remark Bits 7 to 1 are read as 0. The write value should also be 0.

3.2.10 Differential Amplification Circuit Gain Selection Register (GCGSL)

The GCGSL register is used to select the gain of the differential amplification circuits A and B.

Address: 2EH Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	0	GCG[1:0]	

Bit	Bit Name	Function
7 to 2	—	Reserved
1, 0	GCG[1:0]	Select the gain of the differential amplification circuits 00: 2 01: 4 10: 8 11: 16.5

Remark Bits 7 to 2 are read as 0. The write value should also be 0.

3.2.11 Phase Adjustment Circuit Gain Adjustment Value Selection Register (DLCGSL)

The DLCGSL register is used to select the gain adjustment value of the phase adjustment circuits.

Address: 30H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	DLCG[4:0]				

Bit	Bit Name	Function
7 to 5	—	Reserved
4 to 0	DLCG[4:0]	Select the gain adjustment value of the phase adjustment circuits 00000: 0 00001: 1 00010: 2 ⋮ 11101: 29 11110: 30 11111: 31

Remark Bits 7 to 5 are read as 0. The write value should also be 0.

3.2.12 Correction Circuit Gain Selection Register (CCGSL)

The CCGSL register is used to select the gain of the correction circuit.

Address: 36H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	CCG[2:0]		

Bit	Bit Name	Function
7 to 3	—	Reserved
2 to 0	CCG[2:0]	Select the gain of the correction circuit 000: 2/25 001: 4/25 010: 8/25 011: 1/100 100: 2/100 101: 4/100 Others: Setting prohibited

Remark Bits 7 to 3 are read as 0. The write value should also be 0.

3.2.13 Shunt Current Amplification Circuit Control Register (CSACTL)

The CSACTL register is used to control the shunt current amplification circuit.

Address: 42H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
MSLP	0	0	0	0	SW_CSREF	SHUTSL[1:0]	

Bit	Bit Name	Function
7	MSLP	Control of the shunt current amplification circuit 0: Stops operation 1: Starts operation
6 to 3	—	Reserved
2	SW_CSREF	Switching of the reference voltage 0: Internal VREF 1: IOVDD
1, 0	SHUTSL[1:0]	Set the gain of the shunt current amplification circuit 00: 10 01: 25 Others: Setting prohibited

Remark Bits 6 to 3 are read as 0. The write value should also be 0.

3.2.14 Differential Amplifier Input Signal Level Detection Resetting Register (INITERR)

The INITERR register is used to reset the differential amplifier input signal level detection circuit.

Address: 54H Value after a reset: 00H R/W: R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	INITERR

Bit	Bit Name	Function
7 to 1	—	Reserved
0	INITERR	0: Placed in the reset state 1: Released from the reset state After writing 1, write 0 to release from the reset state.

Remark Bits 7 to 1 are read as 0. The write value should also be 0.

3.3 Access to Registers

Reading and writing to registers in this IC is handled by a host MCU via SPI communications where the MCU is the master and this IC is a slave. Four lines are used for the interface: serial clock input (SCLK), serial data input and output (SDI and SDO), and chip select input (CS#).

The SPI communications format is as follows. Communications that are not in this format are invalid.

- Communication direction: Full-duplex transmission and reception
- Data length: 16 bits (1 bit for R/$\overline{W}$, 7 bits for the address, and 8 bits for transfer data)
- Bit order: MSB first

Figure 3.1 shows the timing chart of writing to register (data input). Figure 3.2 shows the timing chart of reading registers (data output).

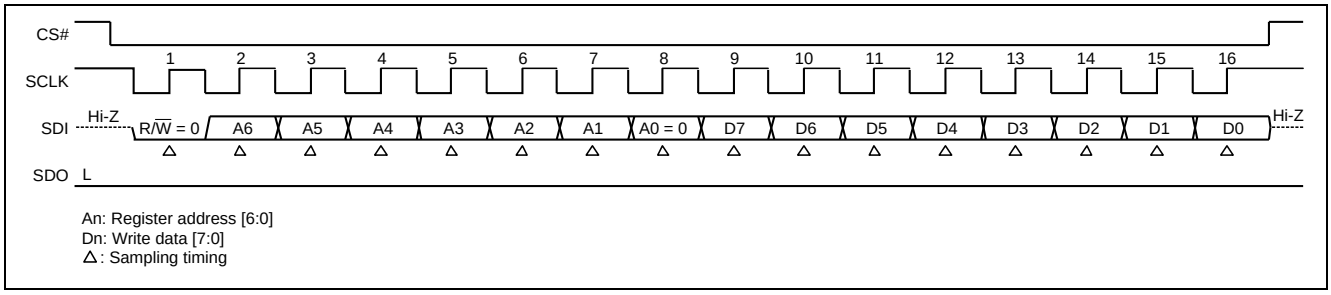


Figure 3.1 Timing Chart of Writing to Registers

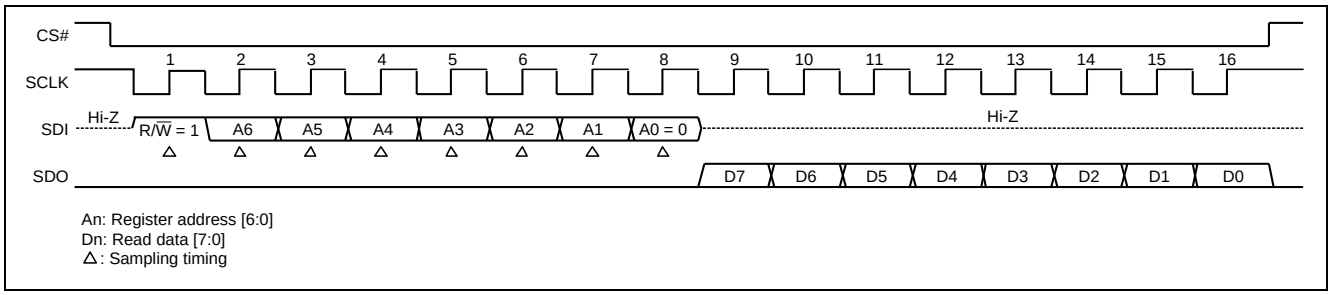


Figure 3.2 Timing Chart of Reading Registers

4. Operation

4.1 Basic Operation for Conversion of Signals from Resolver

This IC can be used to drive a single-phase excitation input and two-phase output type resolver sensor, and to convert the signals from the resolver sensor to digital signals.

Angle information can be obtained from the signal output by a resolver by using this IC with a host MCU.

A rectangular excitation wave is output by the host MCU to drive the resolver. The rectangular excitation wave is converted to a sine wave by an external low-pass filter and input to this IC. The constant-current excitation circuit then outputs a constant current in accord with the period of the cycle for driving the resolver. Driven by the excitation signal, the resolver outputs the two-phase signals it has detected to this IC. Connection between the resolver sensor and this IC varies with the type of resolver sensor. Figures 4.1 and 4.2 show examples of the connections.

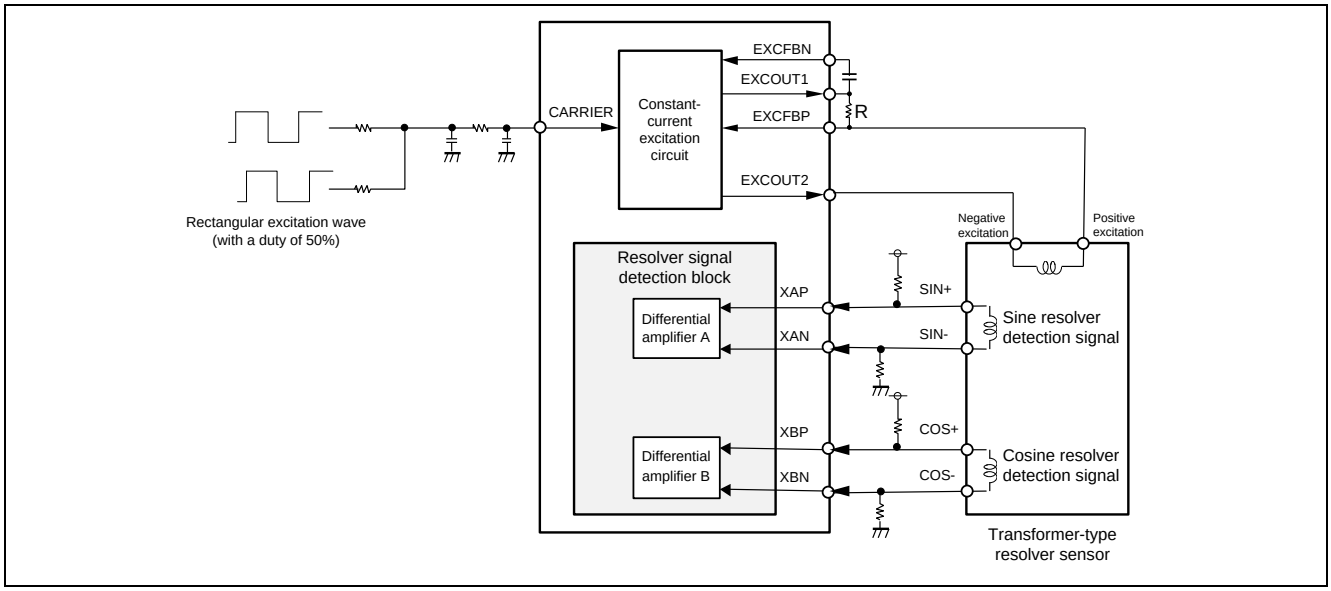


Figure 4.1 Example of Connection to a Transformer-Type Resolver Sensor

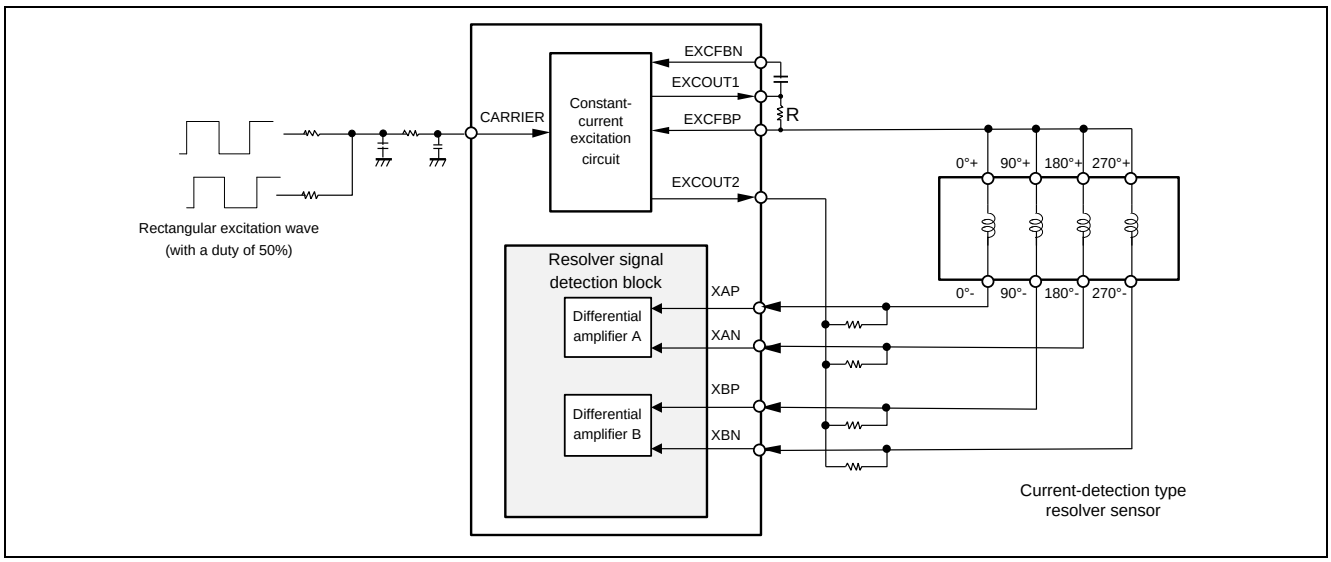


Figure 4.2 Example of Connection to a Current-Detection Type Resolver Sensor

The signal detected by the resolver sensor is converted to an angle signal in the resolver signal detection block. Figure 4.3 shows the flow of signal waveforms. The signals detected by the resolver sensor are amplified by the differential amplifier circuits. The gain should be set to suit the type and modulation rate of the resolver. The amplified signals are then input to phase adjustment circuits A and B, which adjust their phase difference to be 90 degrees. In synthesizing the angle signal, the carrier correction signal is added to correct the residual carrier in the phase-adjusted two-phase signals and the revolver detection signal.

The synthesized angle signal is filtered by the band-pass filter configured by filter circuits 1 and 2 to eliminate the resolver's magnetic noise and PWM noise from motor control.

The filtered signal is then shaped to produce the angle signal, which is output as a rectangular waveform.

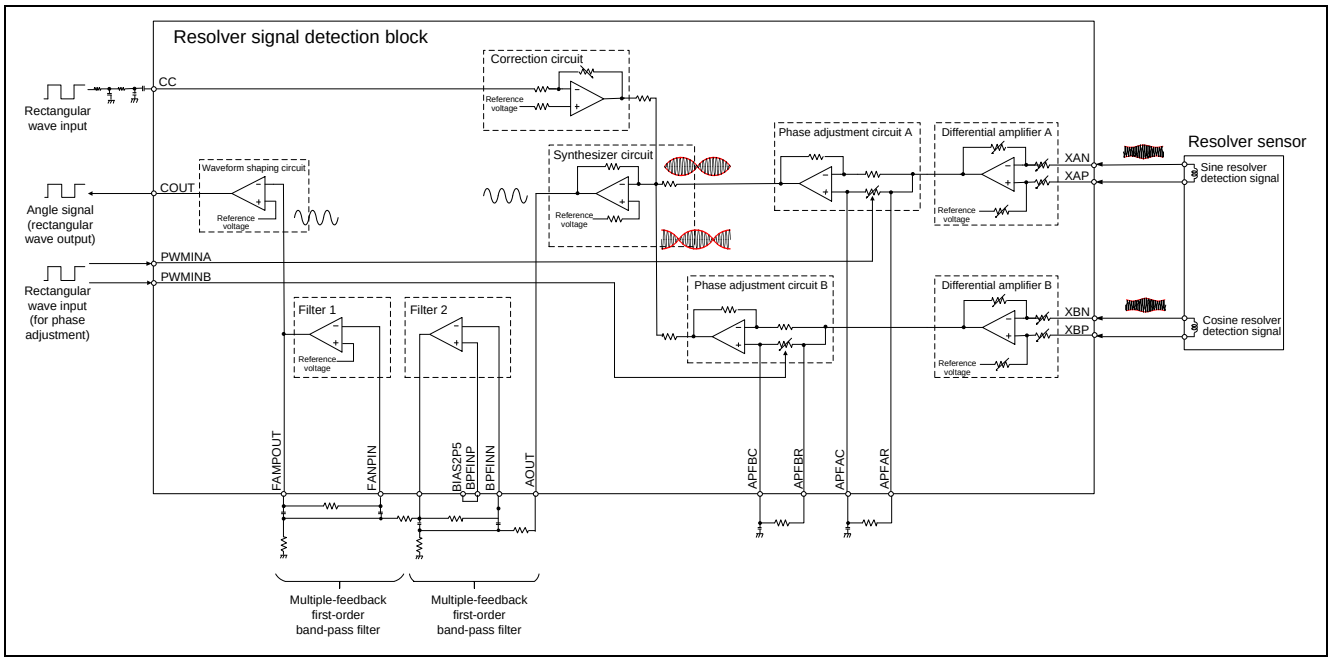


Figure 4.3 Flow of Waveforms in the Resolver Signal Detection Block

The angle signal is generated as a rectangular wave with its phase delayed in proportion to the resolver angle. Angle information can be obtained by using the MCU to measure the phase difference between the rectangular excitation wave and angle signal. Figure 4.4 shows the relation of the phase difference between the excitation signal and angle signal, to the resolver angle.

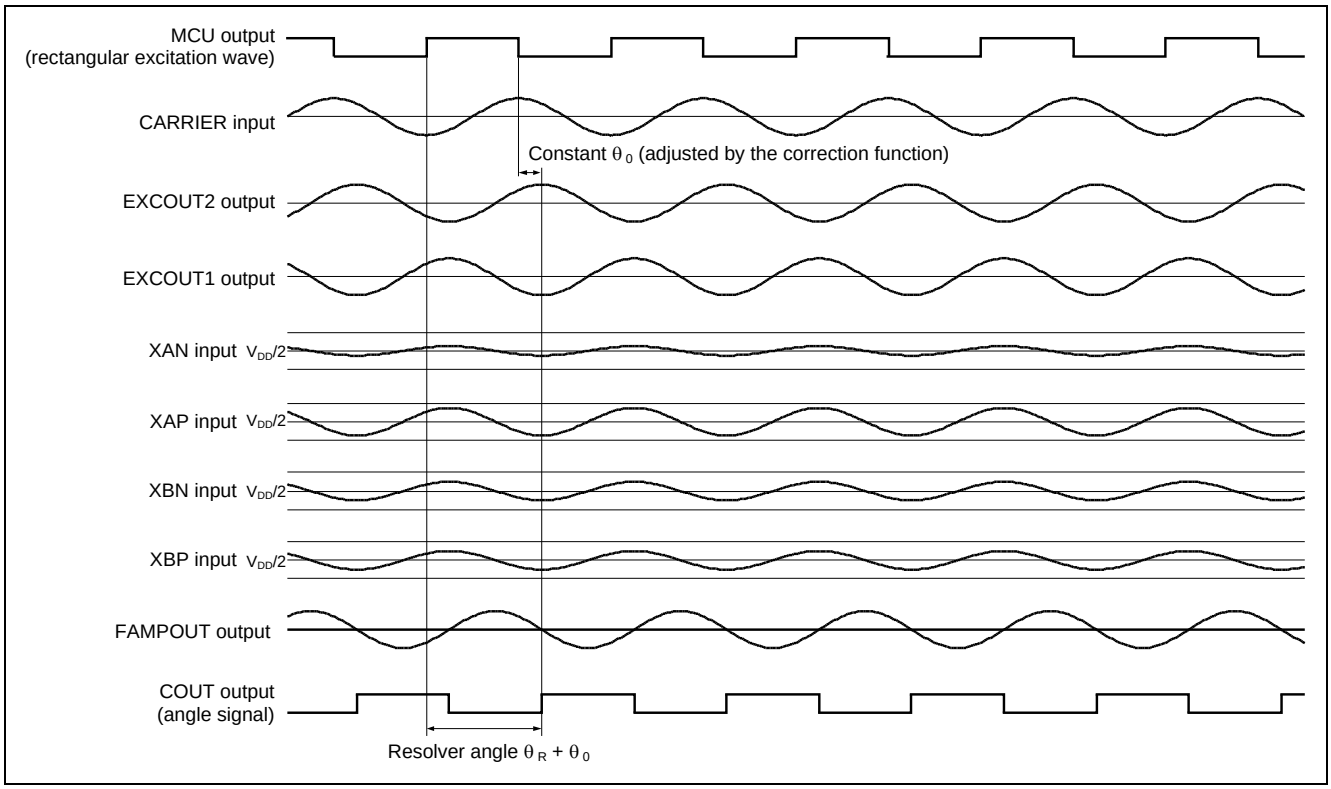


Figure 4.4 Relation between the Excitation Signal and Angle Signal

4.2 Detection of Disconnection from the Resolver Sensor

Connection of this IC to a resolver sensor can be detected by monitoring the levels of the internal signals. The selected internal signal can be output through the MNTOUT pin to an A/D converter of the host MCU for detection of the signal level.

For details on the detection of disconnection from the resolver sensor, see the application note *Guide to Selecting Peripheral Components for Use with the Resolver-to-Digital Converters* (R03AN0012EJ).

4.3 Power-up Sequences and Reset Operation

This IC has three pairs of power supply pins: those for the analog circuits (AVDD and AVSS), for the constant-current excitation circuit (EVDD and EVSS), and for the digital circuits (IOVDD and IOVSS). Connect them to a single power source. Power to these pins should be turned on or off at the same time. The sequence following the release of the reset signal varies with the type of reset. For the types of reset, see section 2.3.4, Control Block. Figure 4.5 shows the sequence of the reset operation when power is turned on, and figure 4.6 shows the sequence of a reset while power is being supplied. In the case of a reset by the signal on the RESET# pin, assertion should be over the time specified in the electrical characteristics. The internal circuits of this IC are in the power-saving state following release from the reset state. After release from the reset state, wait for the time required for the internal circuits to become stable, and release this IC from the power-saving state by setting the internal power-saving control registers. Wait for another 30 ms before using this IC.

Figure 4.7 shows the sequence of a reset on detection of the voltage falling to or below the specified level. This type of reset is triggered on detection of an excessive drop in the power supply voltage. See section 5, Electrical Characteristics for the voltage level that triggers a reset. Release from the reset state depends on the power supply voltage rising to the required level. The internal circuits of this IC will also be in the power-saving state following release from this type of reset. After release from the reset state, wait for the time required for the internal circuits to become stable, and release this IC from the power-saving state by setting the internal power-saving control registers. Wait for another 30 ms before using this IC.

Figure 4.8 shows the sequence of a software reset. A software reset is triggered by writing 1 to the SWRST register. Release from the reset state is initiated by writing 0 to the SWRST register. After release from the reset, release this IC from the power-saving state, and then wait for another 30 ms before using it.

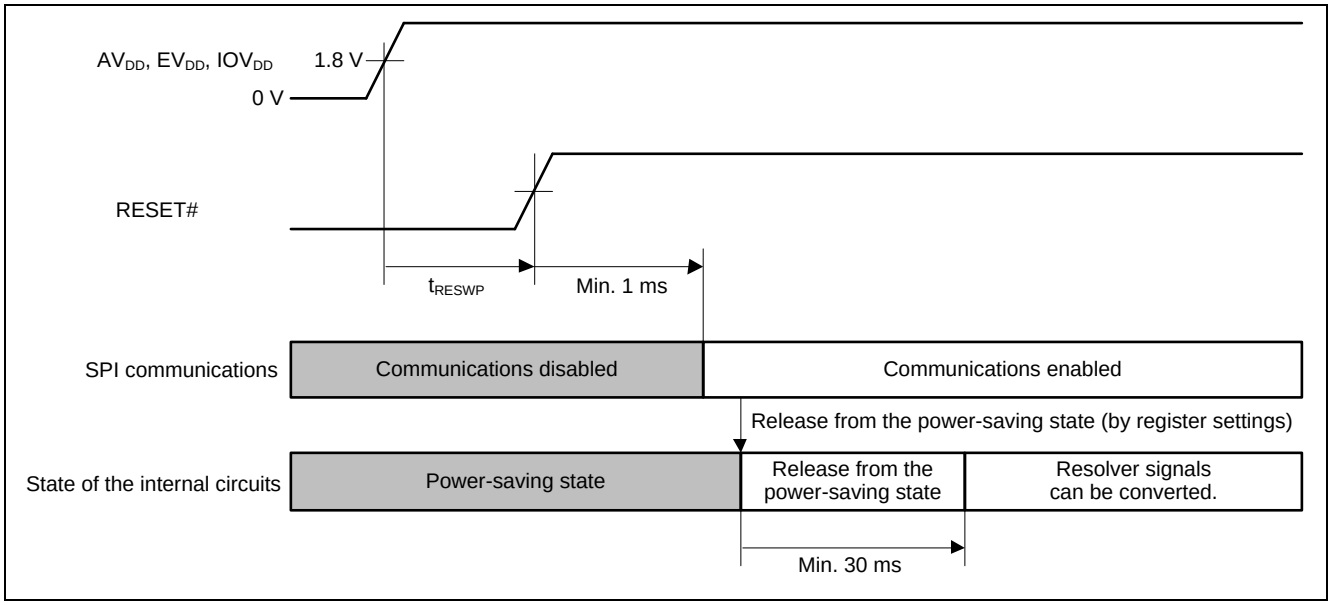


Figure 4.5 Sequence of a Reset when Power is Turned On

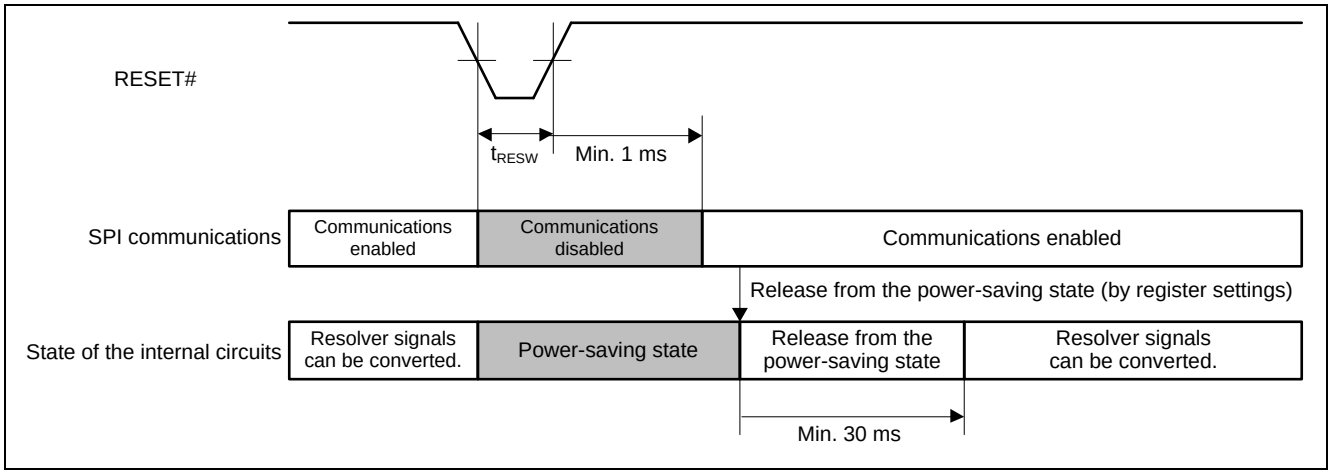


Figure 4.6 Sequence of a Reset while Power is being Supplied

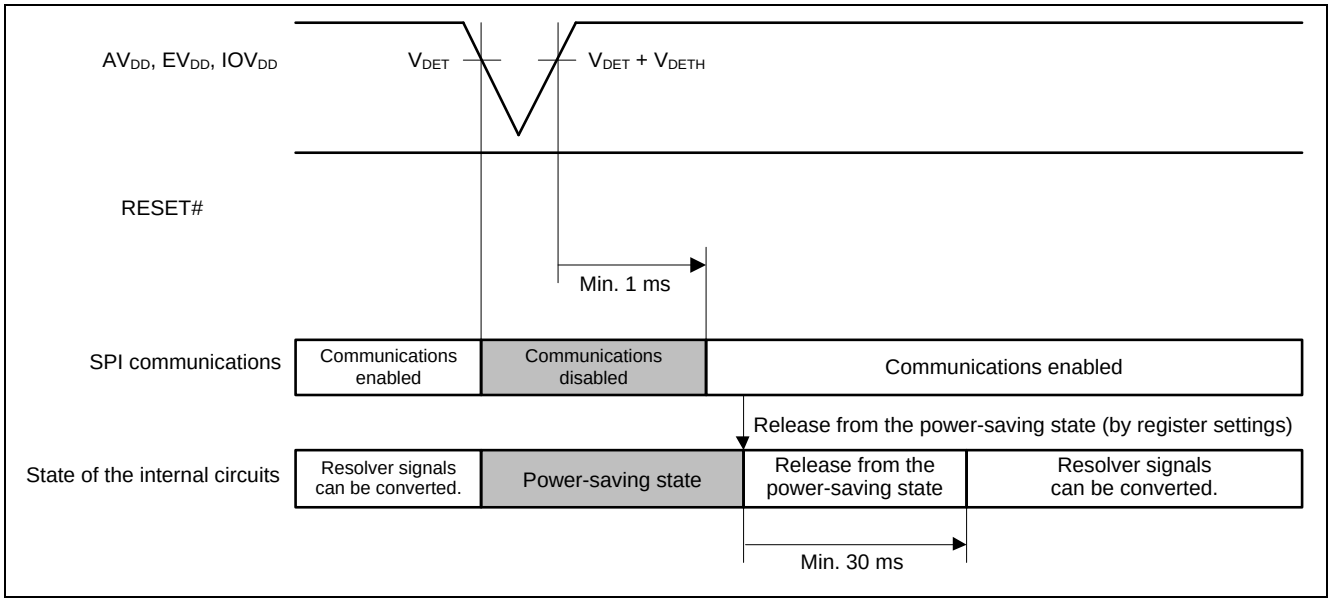


Figure 4.7 Sequence of a Reset on Detection of the Voltage Falling to or Below the Specified Level

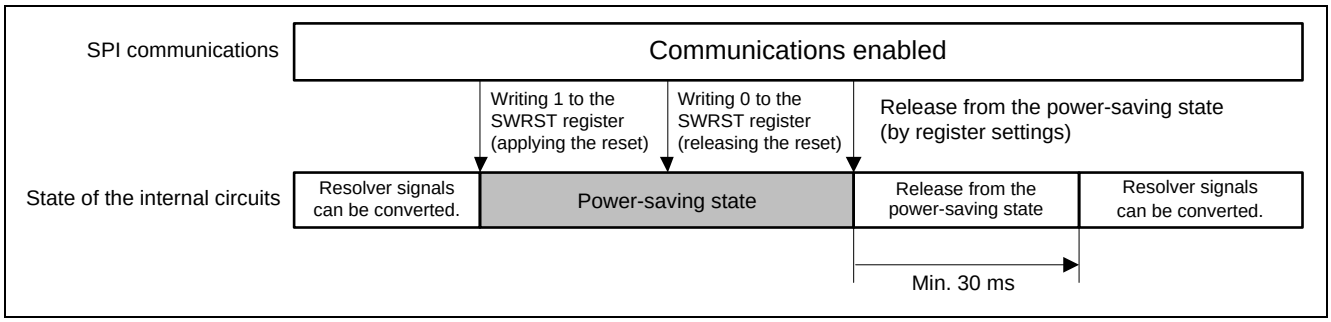


Figure 4.8 Sequence of a Software Reset

4.4 Calibration of the Errors

This IC is capable of calibration in the following three ways to correct the corresponding types of error.

1. Gain calibration to correct the relative errors in gain between the combination of differential amplifier A and phase adjustment circuit A, and between the combination of differential amplifier B and phase adjustment circuit B
2. Phase calibration to adjust the phase difference between phase adjustment circuits A and B to be 90°
3. Carrier error calibration to correct for errors due to the coils of the resolver sensor

For the usage of calibrations, see the application notes *Using the Driver for Resolver-to-Digital Converter Control* (R03AN0013EJ) and *Usage Notes on Correcting Errors in Angles Detected by the Resolver-to-Digital Converter* (R03AN0015EJ).

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Rating	Unit
Power supply voltage Note	AV_{DD}, EV_{DD}, IOV_{DD}		-0.5 to +6.5	V
Input voltage on analog pins Note	V_I		-0.3 to AV_{DD} + 0.3	V
Input voltage on digital pins Note	IOV_I		-0.3 to IOV_{DD} + 0.3	V
Junction temperature	T_J	RAA3064002GFP	-40 to +105	°C
	T_J	RAA3064003GFP	-40 to +125	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note AV_{SS}, EV_{SS}, and IOV_{SS} are reference values.

Caution **Permanent damage to the IC may result if absolute maximum ratings are exceeded.**

To prevent any malfunctions caused by noise interference, insert capacitors that have stable characteristics over a wide range of frequency between the AV_{DD} and AV_{SS} pins, EV_{DD} and EV_{SS} pins, and IOV_{DD} to IOV_{SS} pins. Place capacitors of approximately 0.1 µF as close as possible to each power supply pin and use the shortest and thickest possible patterns for the connections.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	AV_{DD}, EV_{DD}, IOV_{DD}		4.5	5	5.5	V
	AV_{SS}, EV_{SS}, IOV_{SS}		—	0	—	V
Operating ambient temperature	Topr	RAA3064002GFP	-40	—	+85	°C
		RAA3064003GFP	-40	—	+105	°C

5.3 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	RESET#, CLK, SDI, SCLK, CS#, PWMINA, PWMINB	V_{IH}		0.8 x IOV_{DD}	—	IOV_{DD} + 0.3	V
Low-level input voltage	RESET#, CLK, SDI, SCLK, CS#, PWMINA, PWMINB	V_{IL}		-0.3	—	0.2 x IOV_{DD}	V
Input leakage current	RESET#, CLK, SDI, SCLK, CS#, PWMINA, PWMINB	$\|_{IL}$		—	—	1.0	µA
High-level output voltage	ALARM#, SDO, COUT	V_{OH}	I_{OH} = -2 mA	IOV_{DD} - 0.8	—	—	V
Low-level output voltage	ALARM#, SDO, COUT	V_{OL}	I_{OL} = 2 mA	—	—	0.8	V
High-level output current	ALARM#, SDO, COUT	I_{OH}		—	—	-2	mA
Low-level output current	ALARM#, SDO, COUT	I_{OL}		—	—	2	mA
Input capacitance	RESET#, CLK, SDI, SCLK, CS#, PWMINA, PWMINB	C_I		—	—	15	pF
Bias pin output voltage	BIAS2P5	V_{BIAS}			2.5		V
Bias pin output current	BIAS2P5	I_{BIAS}		—	—	100	µA

Note Pin output currents (load-dependent) are not included.

Table 5.4 DC Characteristics (2)

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-saving state	I_{PS}	Initial state of the registers after the release from the reset state. A 4-MHz clock is being input to the CLK pin. Digital input pins other than the CLK pin are fixed to the low level. The analog input pins are left open-circuit, with the exception of those for the excitation current.	—	420	650	µA
During operation	I_{CC}	A 4-MHz clock is being input to the CLK pin. Digital input pins other than the CLK pin are fixed to the low level. The analog input pins are left open-circuit, with the exception of those for the excitation current.	—	20	40	mA
Supply current for the shunt current detection block	I_{CS}		—	2.0	2.8	mA

Note Pin output currents (load-dependent) are not included.

5.4 AC Characteristics

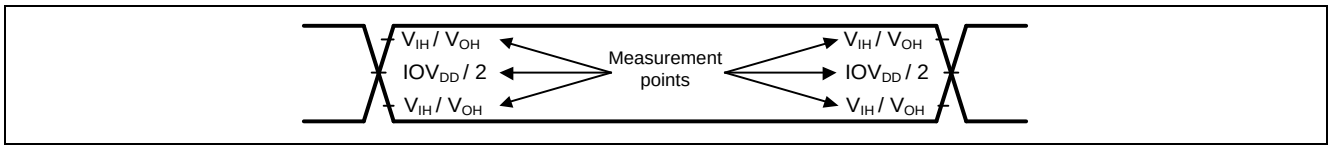


Figure 5.1 AC Timing Measurement Points

Table 5.5 Clock Timing

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK frequency	f_X			4	—	MHz
CLK cycle	t_{XCY}		—	250		ns
CLK high-level width	t_{XH}		70	—	—	ns
CLK low-level width	t_{XL}		70	—	—	ns
CLK rising time	t_{XR}		—	—	5	ns
CLK falling time	t_{XF}		—	—	5	ns

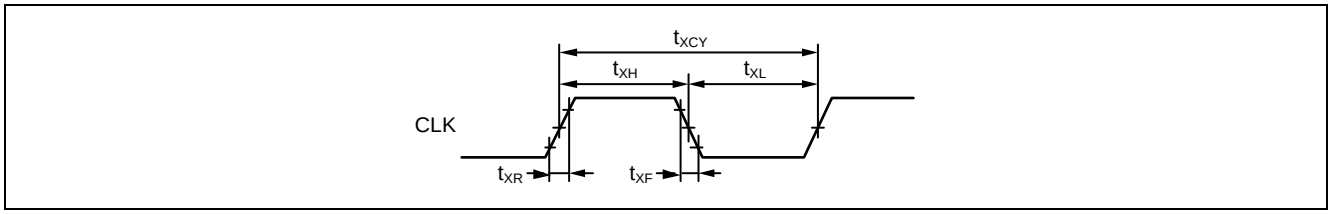


Figure 5.2 Clock Timing

Table 5.6 Reset Input Timing

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET# low-level width	t_{RESWP}	When power is turned on	100	—	—	µs
	t_{RESW}	Other than above	350	—	—	ns
Waiting time after release from the reset state	t_{RESWT}	Period between release of the reset and SPI communications become possible	1	—	—	ms
Waiting time after release from the power-saving state	t_{PSWT}	Period between release of the power-saving mode and conversion of resolver signals becomes possible	30	—	—	ms

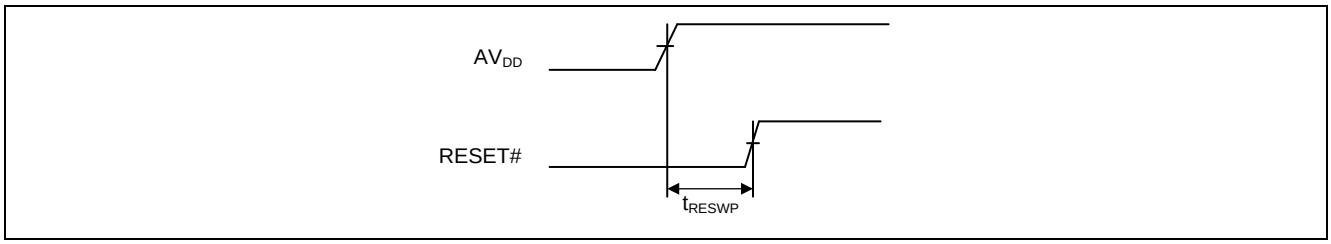


Figure 5.3 Reset Input Timing (1)

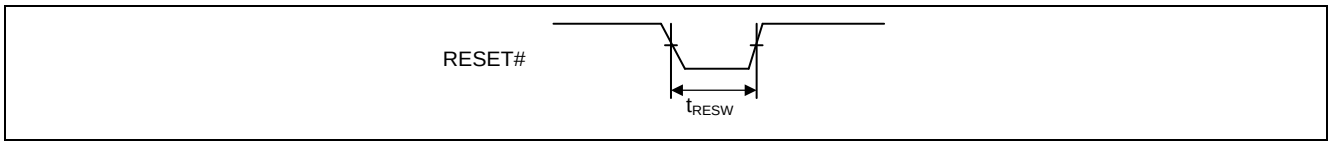


Figure 5.4 Reset Input Timing (2)

Table 5.7 Voltage Detection Reset

Conditions: T_A = -40 to +105°C, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage detection level	V_{DET}		1.1	1.7	2.3	V
Hysteresis	V_{DETH}		—	100	—	mV
Waiting time after release from the reset state	t_{RESWT}	Period between release of the reset and SPI communications become possible	1	—	—	ms
Waiting time after release from the power-saving state	t_{PSWT}	Period between release of the power-saving mode and conversion of resolver signals becomes possible	30	—	—	ms

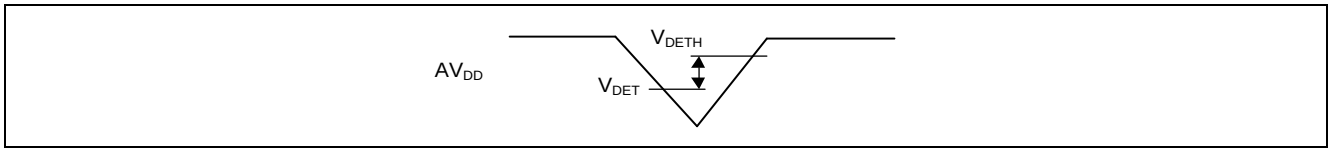


Figure 5.5 Timing of the Voltage Detection Reset

Table 5.8 SPI Timing

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK cycle	t_{SKCY}		4	—	—	t_{XCY}
SCLK high-level width	t_{SKH}		375	—	—	ns
SCLK rising/falling time	t_{SKR}, t_{SKF}		—	—	20	ns
SDI input setup time (to the rising edge of SCLK)	t_{SDI}		60	—	—	ns
SDI input hold time (from the rising edge of SCLK)	t_{HDI}		20	—	—	ns
Delay from the falling edge of SCLK to valid SDO	t_{DDO}	Load capacitance on the SDO pin: 20 pF	—	—	40	ns

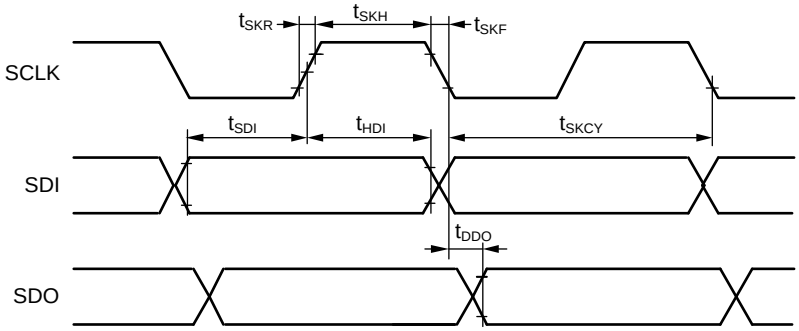


Figure 5.6 SPI Timing

Table 5.9 Phase Adjustment Signal Input Timing

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PWMINA/PWMINB period	t_{PWMF}		2.5	—	—	µs
PWMINA/PWMINB duty	t_{DDO}		10	—	90	%

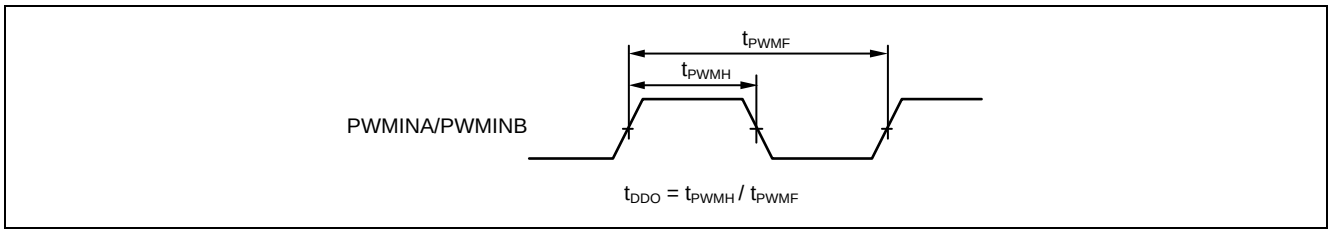


Figure 5.7 Phase Adjustment Signal Input Timing

5.5 Analog Characteristics

Table 5.10 Resolver Actuator

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage on the CARRIER pin	V_{INCAR}		0.35	—	AVDD - 0.85	V
Frequency of the input signal on the CARRIER pin	f_{INCAR}		5	—	20	kHz
Input resistance on the CARRIER pin	Z_{INCAR}		130	190	—	kΩ
Output current on the EXCOUT1 and EXCOUT2 pins	I_{OUTEXC}	Load impedance: 10 to 100 Ω	—	±30	±35	mA
Output voltage on the EXCOUT1 and EXCOUT2 pins	V_{OUTEXC}	Load impedance: 10 to 100 Ω	—	—	3.3	V_{p-p}

Table 5.11 Resolver Signal Detection Block

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage on the XAP, XAN, XBP, and XBN pins	V_{INX}		1.0	—	AVDD - 1.5	V
Carrier frequency of the input signal on the XAP, XAN, XBP, and XBN pins	f_{INX}		5	—	20	kHz
Input resistance on the XAP, XAN, XBP, and XBN	Z_{INX}	G_X = 2	60	90	—	kΩ
		G_X = 4	30	50	—	kΩ
		G_X = 8	20	30	—	kΩ
		G_X = 16.5	10	15	—	kΩ
Differential input circuit gain setting	G_X		—	2	—	Gain
	G_X		—	4	—	Gain
	G_X		—	8	—	Gain
	G_X		—	16.5	—	Gain
Input voltage on the CC pin	V_{INCC}		0.2	—	AVDD - 0.2	V
Frequency of the input signal on the CC pin	f_{INCC}		5	—	20	kHz
Input resistance on the CC pin	Z_{INX}		140	200	—	kΩ
Jitter of the COUT output (RMS)	Jitter	When output from the FAMPOUT pin is 3.1 Vp-p	—	4.0	—	ns

Table 5.12 Detection of IC Internal State

Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage on the MNTOUT pin	V_{OUTM}	Rectification mode	V_{BIAS}	—	3.5	V
	V_{OUTM}	Inverted output mode	0.2	—	4.3	V
Permissible load capacitance on the MNTOUT pin	C_M		—	—	30	pF
Output current	I_{OUTM}		—	—	100	uA

Table 5.13 Shunt Current Amplification Circuit

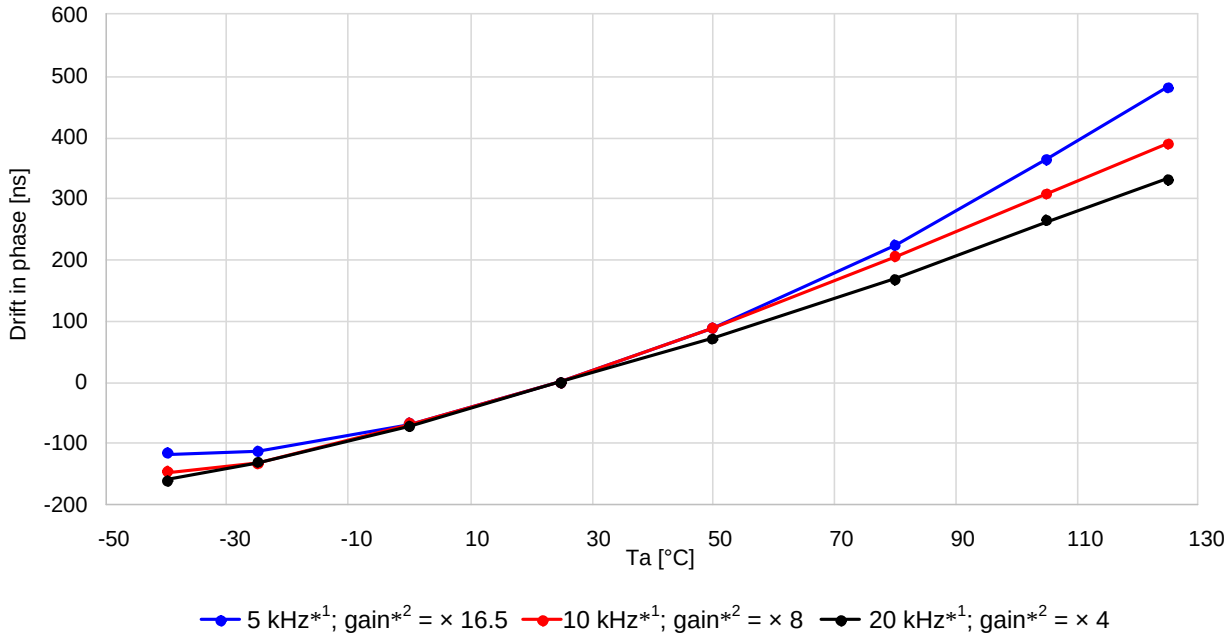
Conditions: T_A = -40 to +105°C, AV_{DD} = EV_{DD} = IOV_{DD} = 4.5 to 5.5 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage on the I1INN, I1INP, I2INN, and I2INP pins	V_{INI}		-0.2		0.2	V
Input resistance on the I1INN, I1INP, I2INN, and I2INP pins	Z_{INI}			5	—	kΩ
Amplification circuit gain	G_I		—	10	—	Gain
	G_I		—	25	—	Gain
Relative error between the amplifiers 1 and 2	G_{ERRI}			0.1		%
Output voltage on the I1OUT and I2OUT pins	V_{OUTI}		0.2	—	AVDD - 0.2	V
Permissible load capacitance on the I1OUT and I2OUT pins	C_I		—	—	20	pF
Slew rate of the I1OUT and I2OUT pins	SR_I	C_I = 20 pF	1.6	—	—	V/us
Output current on the I1OUT and I2OUT pins	I_{OUTI}		—	—	100	uA

6. Characteristics of Circuits

6.1 Drift in Phase with Temperature

Conditions: AV_{DD} = EV_{DD} = IOV_{DD} = 5.0 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V



Notes 1: Frequency of the excitation signal
2: Gain of the differential amplifier

Figure 6.1 Drift in Phase with Temperature

6.2 Output Jitter (Histogram)

Conditions: AV_{DD} = EV_{DD} = IOV_{DD} = 5.0 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V, FAMPOUT=3.1 Vpp

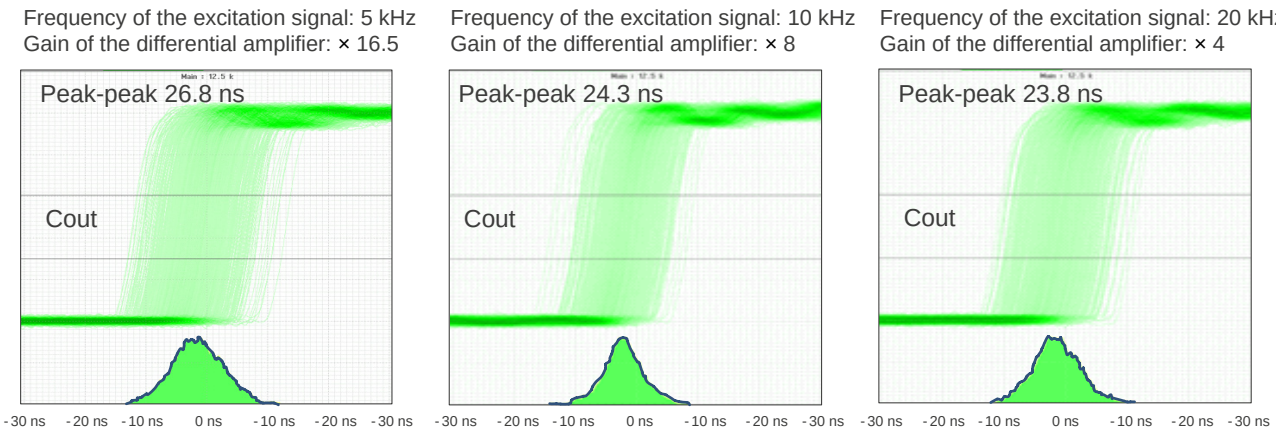
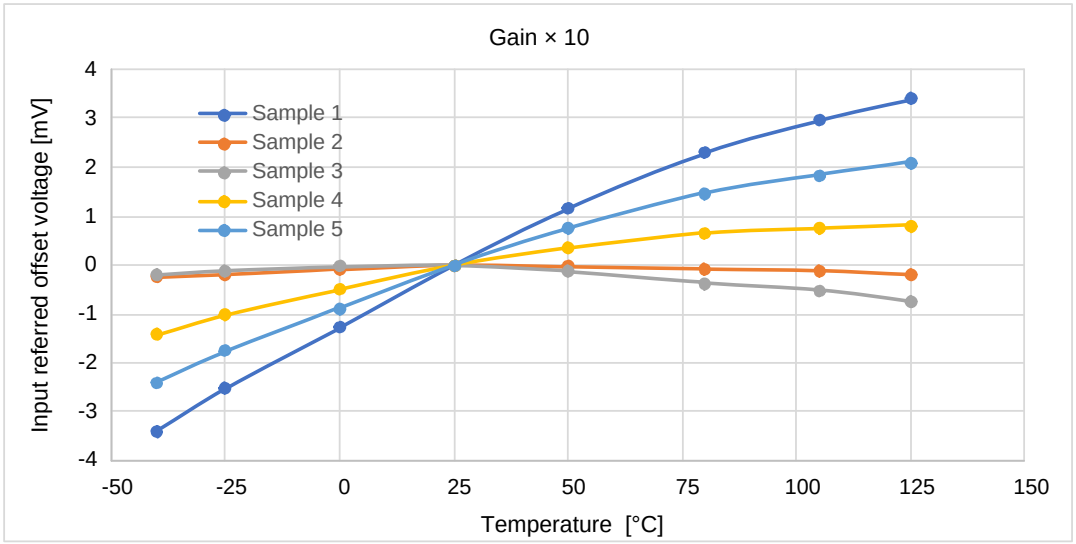


Figure 6.2 Output Jitter (Histogram)

6.3 Drift in the Offset of Operational Amplifiers in the Shunt Current Amplifier Circuits with Temperature

Conditions: AV_{DD} = EV_{DD} = IOV_{DD} = 5.0 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

I1OUT



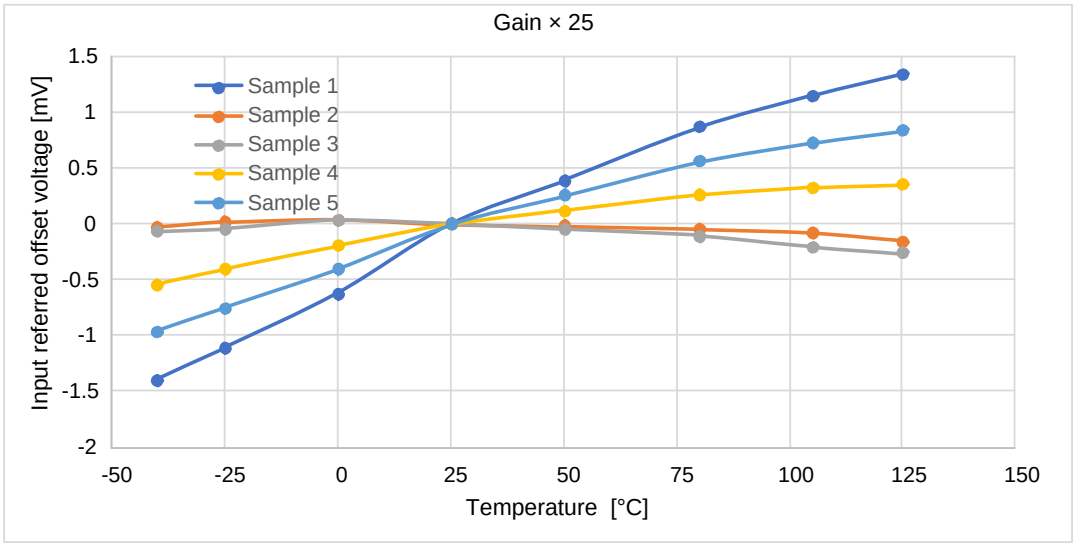
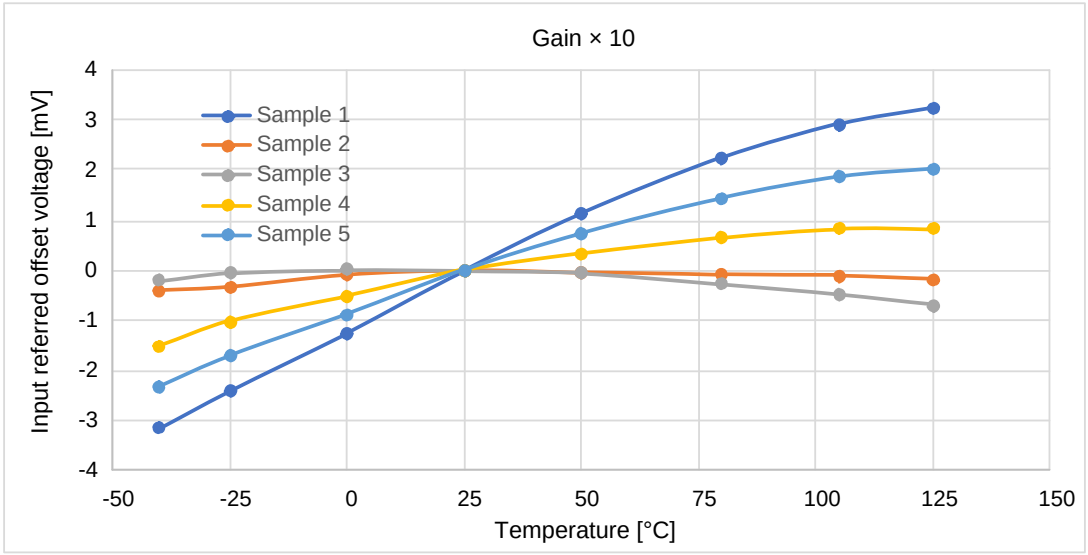


Figure 6.3 Drift in the Offset of Operational Amplifiers in the Shunt Current Amplifier Circuits with Temperature (1/2)

Conditions: AV_{DD} = EV_{DD} = IOV_{DD} = 5.0 V, AV_{SS} = EV_{SS} = IOV_{SS} = 0 V

I2OUT



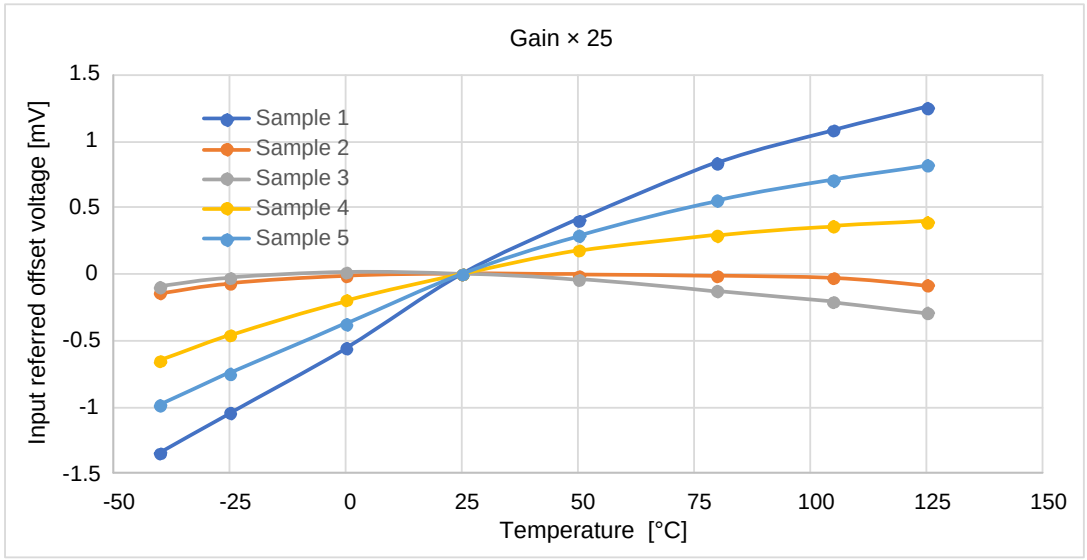


Figure 6.3 Drift in the Offset of Operational Amplifiers in the Shunt Current Amplifier Circuits with Temperature (2/2)

Appendix 1. Resolution of the Angle Signal

This IC outputs a single-phase excitation signal to the resolver sensor. The signal is triggered by the excitation clock signal (rectangular excitation wave) input from the host MCU. This IC then generates an angle signal (rectangular wave) from the two-phase signals (electrical angle information) detected by the resolver sensor, and outputs the angle signal to the host MCU. Angle information can be obtained by using the host MCU to measure the phase difference between the rectangular excitation wave and angle signal.

The frequency of the excitation signal input to the resolver sensor is selectable as 5 kHz, 10 kHz, or 20 kHz. Select a frequency that suits the characteristics of the resolver.

The host MCU generates the rectangular excitation wave and handles sampling of the angle signal by using a timer.

The timer's operating frequency and the excitation signal frequency determine the resolution of the angle signal. See figure A for the relation of the timer operating frequency to the cycle of sampling the angle signal. Figure A shows how raising the operating frequency of the timer shortens the cycle of sampling the angle signal, i.e. increases the resolution. The cycle of the rectangular excitation wave also affects the resolution. The points where the angle signal is sampled depend on the cycle of the rectangular excitation wave. Table A shows how the resolution varies with the timer operating frequency and the excitation frequency.

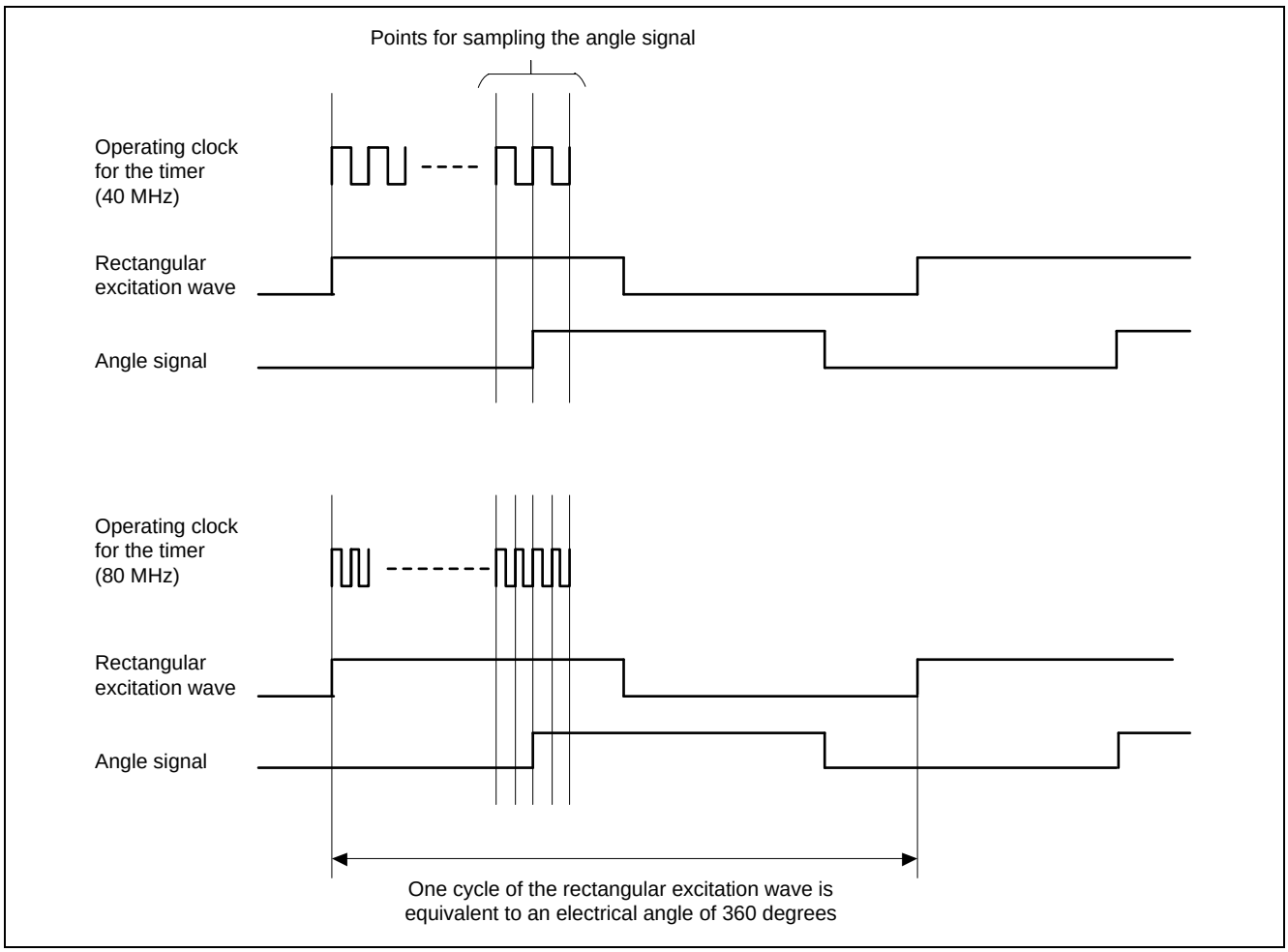


Figure A Relation of the Timer Operating Frequency to the Cycle of Sampling the Angle Signal

Table A Resolution by Timer Operating Frequency in Relation to the Excitation Frequency

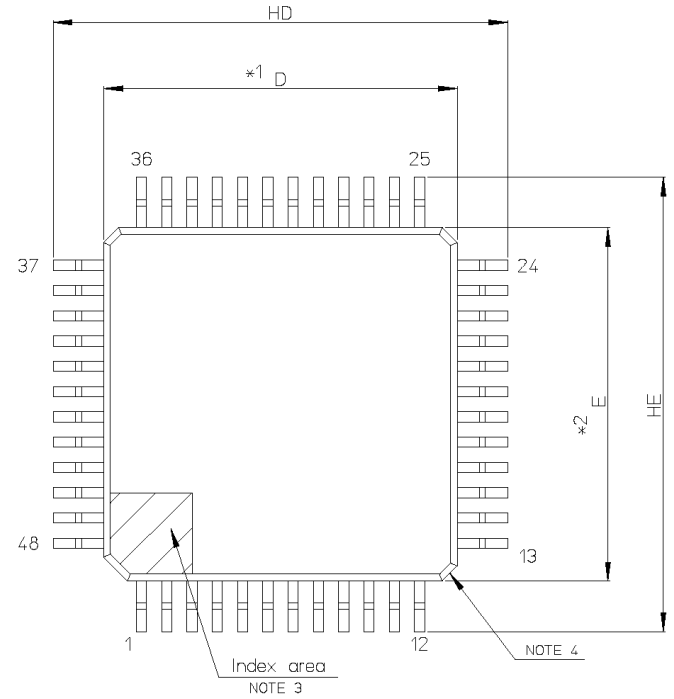
	Excitation Frequency		
Timer operating frequency	5 kHz	10 kHz	20 kHz
40 MHz	8,000	4,000	2,000
80 MHz	16,000	8,000	4,000

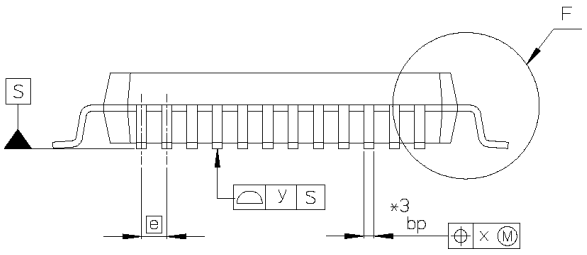
Note that the actual motor angle information (mechanical angle) varies with the number of pole pairs of the resolver that is in use.

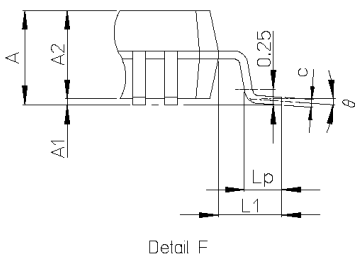
Appendix 2. Package Dimensions

For the latest information on package dimensions and mounting, see “Packaging Information” on the Renesas website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Revision History

Rev.	Date	Description	
		Page	Summary
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