

Microprocessor Supervisory Circuit for Automotive Applications

NO.EC-159-210408

OUTLINE

The R5105N Series are CMOS-based microprocessor supervisory circuit and have high accuracy and ultra low supply current voltage detector with built-in delay circuit and watchdog timer. When the supply voltage is down across the threshold, or the watchdog timer does not detect the system clock from the microprocessor, the reset output is generated.

The voltage detector circuit is used for the system reset, etc. The detector threshold is fixed internally, and the accuracy is $\pm 1.0\%$. The released delay time (Power-on Reset Delay) circuit is built-in, and output delay time is adjustable with an external capacitor, and the accuracy is $\pm 16\%$ (R5105Nxx1x-TR-JE: $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)⁽¹⁾. When the supply voltage becomes higher than the released voltage, the reset state will be maintained during the delay time. The output type of the reset is selectable, Nch open-drain, or CMOS.

The time out period of the watchdog timer can be also set with an external capacitor, and the accuracy is $\pm 33\%$ ⁽¹⁾. The package of R5105N is SOT-23-6.

FEATURES

- Supply Current (I_{ss}) Typ. $11\mu\text{A}$
- Operating Voltage Range (V_{DD}) 0.9V to 6.0V

< Voltage Detector Part >

- Detector Threshold Range 1.5V to 5.5V (0.1V steps)
- Detector Threshold Accuracy $\pm 1.0\%$
- Detector Threshold Temperature Coefficient Typ. $\pm 100\text{ ppm}/^{\circ}\text{C}$ Typ. $\pm 100\text{ ppm}/^{\circ}\text{C}$
R5105Nxx1x-TR-AE: $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$
R5105Nxx1x-TR-JE: $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$
- Power-on Reset Delay Time accuracy⁽¹⁾ $\pm 18\%$ (R5105Nxx1x-TR-AE: $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$)
 $\pm 16\%$ (R5105Nxx1x-TR-JE: $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Power-on reset delay time of the voltage detector Typ. 370ms with an external capacitor : $0.1\mu\text{F}$

< Watchdog Timer Part >

- Built-in a watchdog timer's time out period accuracy⁽¹⁾ $\pm 33\%$
R5105Nxx1x-TR-AE: $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$
R5105Nxx1x-TR-JE: $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$
- Timeout period for watchdog timer Typ. 310ms with an external capacitor : $0.1\mu\text{F}$
- Reset timer for watchdog timer Typ. 34ms with an external capacitor : $0.1\mu\text{F}$
- Package SOT-23-6

APPLICATIONS

- Voltage monitoring for electronic control units such as EV inverter and battery charge control unit.
- Supervisory circuit for car accessories including car audio systems, car navigation systems, and ETC systems.

⁽¹⁾ Accuracy to center value of (Min.+Max.)/2

SELECTION GUIDE

The detector threshold, the output type and the taping type for the ICs can be selected at the users' request. The selection can be made with designating the part number as shown below;

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5105Nxx1*-TR-#E	SOT-23-6	3,000 pcs	Yes	Yes

xx: The detector threshold ($-V_{DET}$) can be designated in the range from 1.5V(15) to 5.5V(55) in 0.1V steps.

* : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

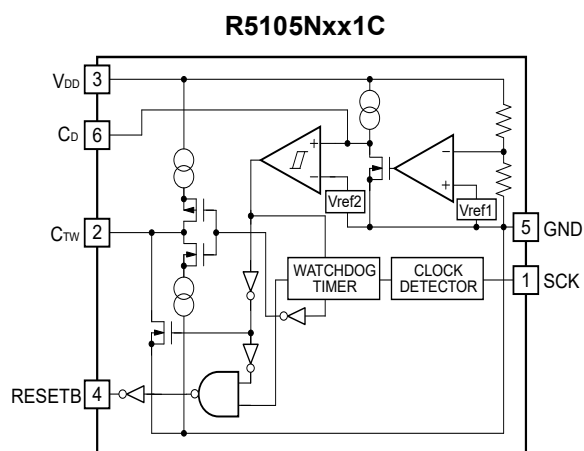
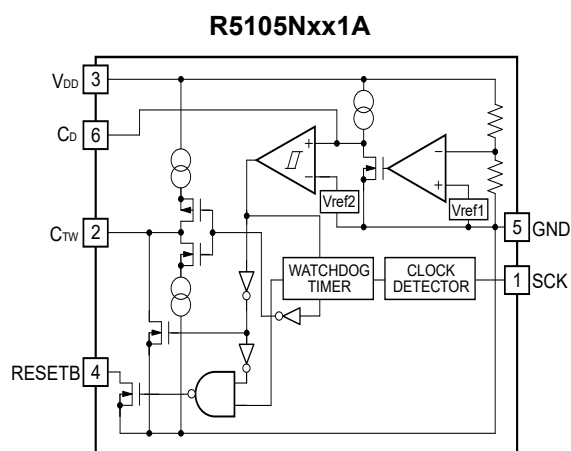
: Quality Class

	Operating Temperature Range	Test Temp.
A	-40°C to 125°C	25°C, High
J	-40°C to 105°C	Low, 25°C, High

Series Selection

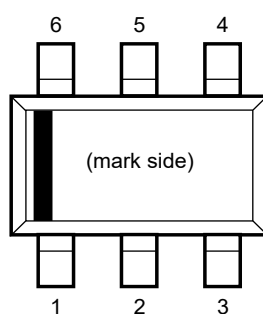
	R5105N	R5106N	R5107G	R5108G	R5109G
Package	SOT-23-6		SSOP-8G		
With INH pin (Inhibit)	No	Yes			
2 clock input	No				Yes
With MR pin (Manual Reset)	No		Yes	No	
With SENSE pin	No			Yes	No
Remarks		C _D pin and C _{TW} pin are combined uses.		Operating Voltage Range 1.5V to 6.0V	Supply Current 11.5μA

BLOCK DIAGRAMS



PIN DESCRIPTIONS

• SOT-23-6



• SOT-23-6

Pin No.	Symbol	Description
1	SCK	Clock Input Pin from Microprocessor
2	C _{TW}	External Capacitor Pin for setting Reset and Watchdog Timer Timeout Period
3	V _{DD}	Power supply Pin
4	RESETB	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output "L" at detecting Detector Threshold and Watchdog Timer Reset.)
5	GND	Ground Pin
6	C _D	External Capacitor Pin for Setting delay time of Voltage Detector

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Symbol	Item		Rating	Unit
V _{DD}	Supply Voltage		-0.3 to 7.0	V
V _{CD}	Output Voltage	Voltage of C _D Pin	-0.3 to V _{DD} + 0.3	V
V _{CTW}		Voltage of C _{TW} Pin	-0.3 to V _{DD} + 0.3	V
V _{RESETB}		Voltage of RESETB Pin	-0.3 to 7.0	V
V _{SCK}	Input Voltage	Voltage of SCK Pin	-0.3 to 7.0	V
I _{RESETB}	Output Current	Current of RESETB Pin	20	mA
P _D	Power Dissipation ⁽¹⁾ (SOT-23-6, JEDEC STD. 51-7)		830	mW
T _j	Junction Temperature		-40 to 125	°C
T _{stg}	Storage Temperature Range		-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITONS

Symbol	Item		Rating	Unit
V _{DD}	Operating Voltage		0.9 to 6.0	V
Ta	Operating Temperature Range	R5105Nxx1x-TR-AE	-40 to 125	°C
		R5105Nxx1x-TR-JE	-40 to 105	°C

RECOMMENDED OPERATING RATINGS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

$V_{DD}=6.0V$, $C_{TW}=0.1\mu F$, $C_D=0.1\mu F$, In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of $100k\Omega$ (R5105Nxx1A), unless otherwise noted.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 125^{\circ}C$.

• R5105Nxx1A/C-TR-AE

($T_a = 25^{\circ}C$)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	$V_{DD} = -V_{DET} + 0.5V$, Clock pulse input		11	15	μA

• VD Part

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	$T_a = 25^{\circ}C$	$\times 0.990$		$\times 1.010$	V
		$-40^{\circ}C \leq T_a \leq 125^{\circ}C$	$\times 0.972$		$\times 1.015$	
V_{HYS}	Detector Threshold Hysteresis		$\frac{-V_{DET}}{\times 0.03}$	$\frac{-V_{DET}}{\times 0.05}$	$\frac{-V_{DET}}{\times 0.07}$	V
t_{PLH}	Output Delay Time	$C_D = 0.1\mu F$ ⁽¹⁾	340	370	485	ms
I_{RESETB}	Output Current (RESETB Output pin)	Nch $V_{DD} = 1.2V$ $V_{DS} = 0.1V$	0.36	0.8		mA
		Pch ⁽²⁾ $V_{DD} = 6.0V$ $V_{DS} = 0.5V$	0.63	0.9		mA

• WDT Part

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
t_{WD}	Watchdog Timeout period	$C_{TW} = 0.1\mu F$ ⁽¹⁾	230	310	450	ms
t_{WR}	Reset Hold Time of WDT	$C_{TW} = 0.1\mu F$ ⁽¹⁾	29	34	48	ms
V_{SCKH}	SCK Input "H"		$V_{DD} \times 0.8$		6.0	V
V_{SCKL}	SCK Input "L"		0		$V_{DD} \times 0.2$	V
t_{SCKW}	SCK Input Pulse Width	$V_{SCKL} = V_{DD} \times 0.2$ $V_{SCKH} = V_{DD} \times 0.8$	500			ns

As all of unit, all items in the above table are tested and specified under load conditions such that $T_j \approx T_a = 25^{\circ}C$.

⁽¹⁾ The specification does not contain the temperature characteristics of the external capacitor.

⁽²⁾ In case of CMOS type (R5105Nxx1C)

$V_{DD}=6.0V$, $C_{TW}=0.1\mu F$, $C_D=0.1\mu F$, In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of 100k Ω (R5105Nxx1A), unless otherwise noted.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 105^{\circ}C$.

● R5105Nxx1A/C-TR-JE

($T_a = 25^{\circ}C$)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	$V_{DD} = -V_{DET} + 0.5V$, Clock pulse input		11	15	μA

● VD Part

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	$T_a = 25^{\circ}C$	$\times 0.990$		$\times 1.010$	V
		$-40^{\circ}C \leq T_a \leq 105^{\circ}C$	$\times 0.972$		$\times 1.015$	
V_{HYS}	Detector Threshold Hysteresis		$\frac{-V_{DET}}{\times 0.03}$	$\frac{-V_{DET}}{\times 0.05}$	$\frac{-V_{DET}}{\times 0.07}$	V
t_{PLH}	Output Delay Time	$C_D = 0.1\mu F$ ⁽¹⁾	340	370	467	ms
I_{RESETB}	Output Current (RESETB Output pin)	Nch $V_{DD} = 1.2V$ $V_{DS} = 0.1V$	0.38	0.8		mA
		Pch ⁽²⁾ $V_{DD} = 6.0V$ $V_{DS} = 0.5V$	0.65	0.9		mA

● WDT Part

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
t_{WD}	Watchdog Timeout period	$C_{TW} = 0.1\mu F$ ⁽¹⁾	230	310	450	ms
t_{WR}	Reset Hold Time of WDT	$C_{TW} = 0.1\mu F$ ⁽¹⁾	29	34	48	ms
V_{SCKH}	SCK Input "H"		$V_{DD} \times 0.8$		6.0	V
V_{SCKL}	SCK Input "L"		0		$V_{DD} \times 0.2$	V
t_{SCKW}	SCK Input Pulse Width	$V_{SCKL} = V_{DD} \times 0.2$ $V_{SCKH} = V_{DD} \times 0.8$	500			ns

As all of unit, all items in the above table are tested and specified under load conditions such that $T_j \approx T_a = 25^{\circ}C$.

⁽¹⁾ The specification does not contain the temperature characteristics of the external capacitor.

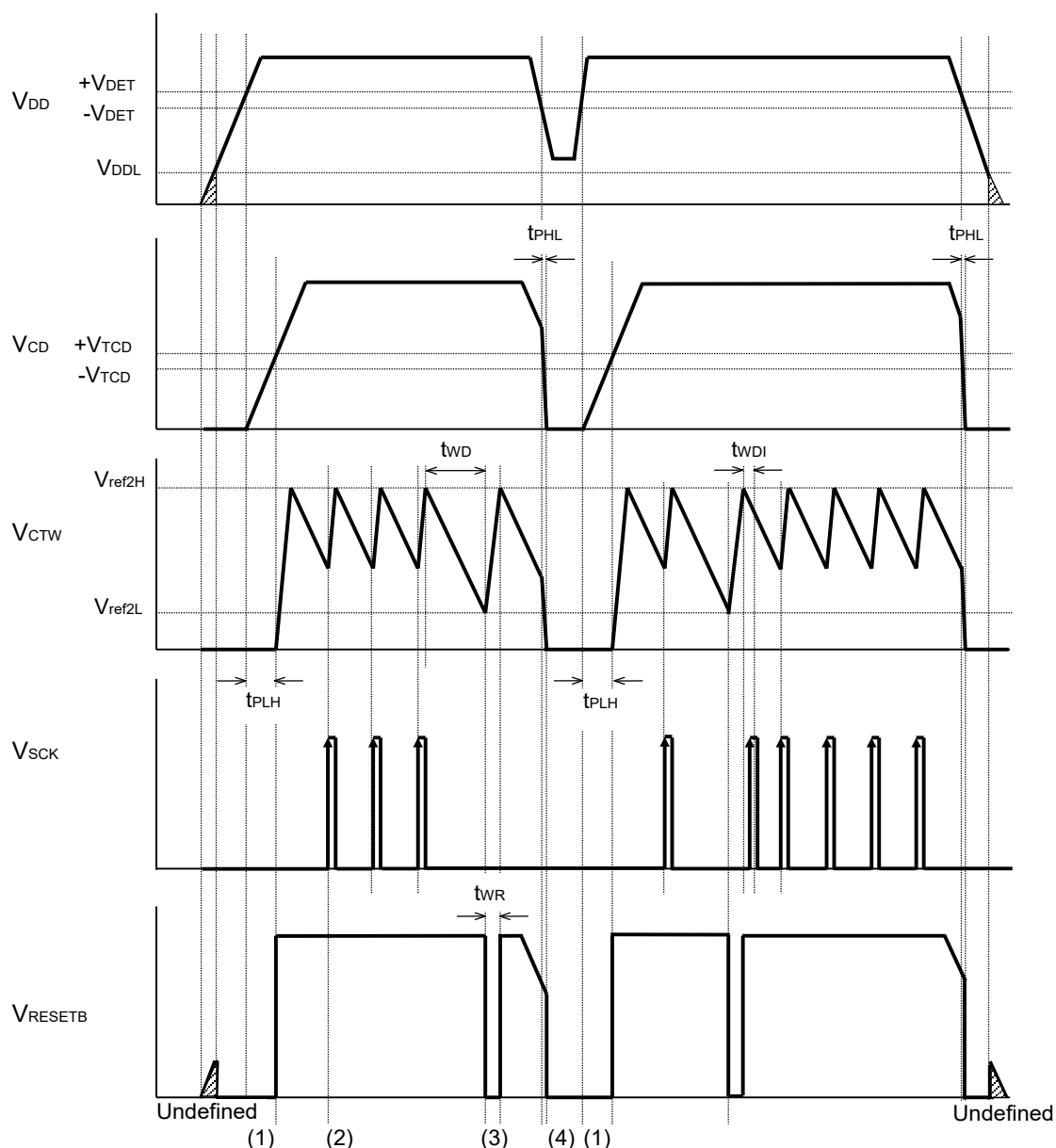
⁽²⁾ In case of CMOS type (R5105Nxx1C)

Product-specific Electrical Characteristics

Product Name	-V _{DET}						V _{HYS}		
	Ta = 25°C			-40°C ≤ Ta ≤ 125 °C/ -40°C ≤ Ta ≤ 105 °C					
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
R5105N151x	1.485	1.500	1.515	1.4580	1.500	1.5225	0.045	0.075	0.105
R5105N161x	1.584	1.600	1.616	1.5552	1.600	1.6240	0.048	0.080	0.112
R5105N171x	1.683	1.700	1.717	1.6524	1.700	1.7255	0.051	0.085	0.119
R5105N181x	1.782	1.800	1.818	1.7496	1.800	1.8270	0.054	0.090	0.126
R5105N191x	1.881	1.900	1.919	1.8468	1.900	1.9285	0.057	0.095	0.133
R5105N201x	1.980	2.000	2.020	1.9440	2.000	2.0300	0.060	0.100	0.140
R5105N211x	2.079	2.100	2.121	2.0412	2.100	2.1315	0.063	0.105	0.147
R5105N221x	2.178	2.200	2.222	2.1384	2.200	2.2330	0.066	0.110	0.154
R5105N231x	2.277	2.300	2.323	2.2356	2.300	2.3345	0.069	0.115	0.161
R5105N241x	2.376	2.400	2.424	2.3328	2.400	2.4360	0.072	0.120	0.168
R5105N251x	2.475	2.500	2.525	2.4300	2.500	2.5375	0.075	0.125	0.175
R5105N261x	2.574	2.600	2.626	2.5272	2.600	2.6390	0.078	0.130	0.182
R5105N271x	2.673	2.700	2.727	2.6244	2.700	2.7405	0.081	0.135	0.189
R5105N281x	2.772	2.800	2.828	2.7216	2.800	2.8420	0.084	0.140	0.196
R5105N291x	2.871	2.900	2.929	2.8188	2.900	2.9435	0.087	0.145	0.203
R5105N301x	2.970	3.000	3.030	2.9160	3.000	3.0450	0.090	0.150	0.210
R5105N311x	3.069	3.100	3.131	3.0132	3.100	3.1465	0.093	0.155	0.217
R5105N321x	3.168	3.200	3.232	3.1104	3.200	3.2480	0.096	0.160	0.224
R5105N331x	3.267	3.300	3.333	3.2076	3.300	3.3495	0.099	0.165	0.231
R5105N341x	3.366	3.400	3.434	3.3048	3.400	3.4510	0.102	0.170	0.238
R5105N351x	3.465	3.500	3.535	3.4020	3.500	3.5525	0.105	0.175	0.245
R5105N361x	3.564	3.600	3.636	3.4992	3.600	3.6540	0.108	0.180	0.252
R5105N371x	3.663	3.700	3.737	3.5964	3.700	3.7555	0.111	0.185	0.259
R5105N381x	3.762	3.800	3.838	3.6936	3.800	3.8570	0.114	0.190	0.266
R5105N391x	3.861	3.900	3.939	3.7908	3.900	3.9585	0.117	0.195	0.273
R5105N401x	3.960	4.000	4.040	3.8880	4.000	4.0600	0.120	0.200	0.280
R5105N411x	4.059	4.100	4.141	3.9852	4.100	4.1615	0.123	0.205	0.287
R5105N421x	4.158	4.200	4.242	4.0824	4.200	4.2630	0.126	0.210	0.294
R5105N431x	4.257	4.300	4.343	4.1796	4.300	4.3645	0.129	0.215	0.301
R5105N441x	4.356	4.400	4.444	4.2768	4.400	4.4660	0.132	0.220	0.308
R5105N451x	4.455	4.500	4.545	4.3740	4.500	4.5675	0.135	0.225	0.315
R5105N461x	4.554	4.600	4.646	4.4712	4.600	4.6690	0.138	0.230	0.322
R5105N471x	4.653	4.700	4.747	4.5684	4.700	4.7705	0.141	0.235	0.329
R5105N481x	4.752	4.800	4.848	4.6656	4.800	4.8720	0.144	0.240	0.336
R5105N491x	4.851	4.900	4.949	4.7628	4.900	4.9735	0.147	0.245	0.343
R5105N501x	4.950	5.000	5.050	4.8600	5.000	5.0750	0.150	0.250	0.350
R5105N511x	5.049	5.100	5.151	4.9572	5.100	5.1765	0.153	0.255	0.357
R5105N521x	5.148	5.200	5.252	5.0544	5.200	5.2780	0.156	0.260	0.364
R5105N531x	5.247	5.300	5.353	5.1516	5.300	5.3795	0.159	0.265	0.371
R5105N541x	5.346	5.400	5.454	5.2488	5.400	5.4810	0.162	0.270	0.378
R5105N551x	5.445	5.500	5.555	5.3460	5.500	5.5825	0.165	0.275	0.385

THEORY OF OPERATION

Timing Chart



*) V_{TCD} : Threshold voltage of C_D pin when a power-on reset pulse inverting.

*) V_{ref2H} : C_{TW} pin voltage at the end of WDT timeout period.

*) V_{ref2L} : C_{TW} pin voltage at the begin of WDT timeout period.

*) V_{DDL} : 0.9 V (Max.)

Operating Description

- (1) When the power supply, V_{DD} pin voltage becomes more than the released voltage ($+V_{DET}$), after the released delay time (or the power on reset time t_{PLH}), the output of RESETB becomes "H" level.
- (2) When the SCK pulse is input, the watchdog timer (WDT) is cleared, and C_{TW} pin mode changes from the discharge mode to the charge mode. When the C_{TW} pin voltage becomes higher than V_{refH} , the mode will change into the discharge mode, and next watchdog time count starts.

- (3) Unless the SCK pulse is input, WDT will not be cleared, and during the charging period of C_{TW} pin, RESETB="L".
- (4) When the V_{DD} pin becomes lower than the detector threshold voltage ($-V_{DET}$), RESETB outputs "L".

Watchdog Timeout period/Reset hold time

The watchdog timeout period and reset hold time can be set with an external capacitor to C_{TW} pin.

The next equations describe the relation between the watchdog timeout period and the external capacitor value, or the reset hold time and the external capacitor value.

$$t_{WD} (s) = 3.1 \times 10^6 \times C (F)$$

$$t_{WR} (s) = t_{WD}/9$$

The watchdog timer (WDT) timeout period is determined with the discharge time of the external capacitor.

During the watchdog timeout period, if the clock pulse from the system is detected, WDT is cleared and the capacitor is charged. When the charge of the capacitor completes, another watchdog timeout period starts again. During the watchdog timeout period, if the clock pulse from the system is not detected, during the next reset hold time RESETB pin outputs "L".

During the reset time, (while charging the external capacitor) and after starting the watchdog timeout period, (just after from the discharge of the external capacitor) even if the clock pulse is input during the time period " t_{WDI} ", the clock pulse is ignored.

$$t_{WDI} (s) = t_{WD}/10$$

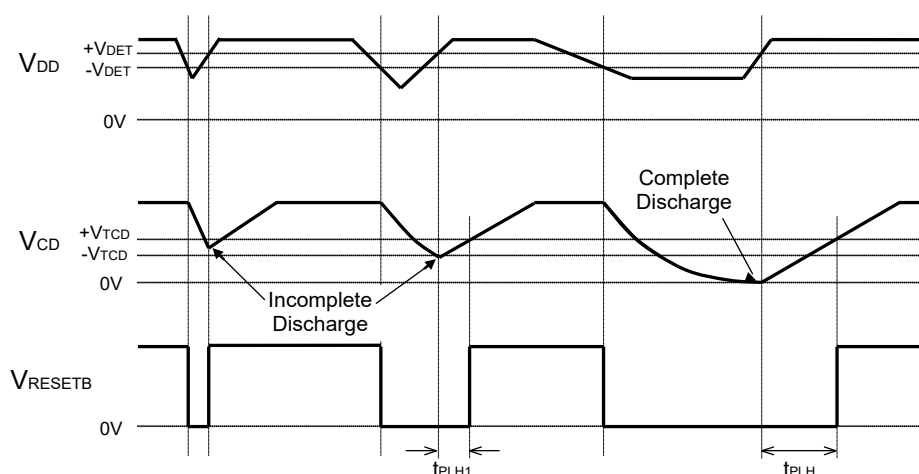
Released Delay Time (Power-on Reset delay time)

The released delay time can be set with an external capacitor connected to the C_D pin. The next equation describes the relation between the capacitance value and the released delay time (t_{PLH}).

$$t_{PLH} (s) = 3.7 \times 10^6 \times C (F)$$

When the V_{DD} voltage becomes equal or less than ($-V_{DET}$), discharge of the capacitor connected to the C_D pin starts. Therefore, if the discharge is not enough and V_{DD} voltage returns to ($+V_{DET}$) or more, thereafter the delay time will be shorter than t_{PLH} which is expected.

Power on Reset Operation against the input glitch ($t_{PLH1} < t_{PLH}$)



Minimum Operating Voltage

We specified the minimum operating voltage as the minimum input voltage in which the condition of RESETB pin being 0.1V or lower than 0.1V. (Herein, pull-up resistance is set as 100k Ω in the case of the Nch open-drain output type.)

RESETB Output

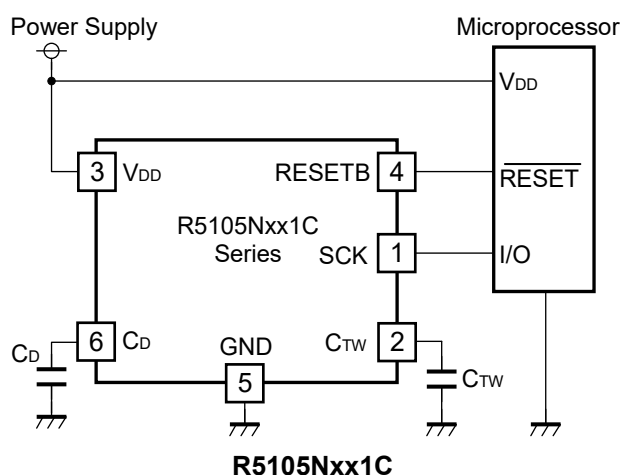
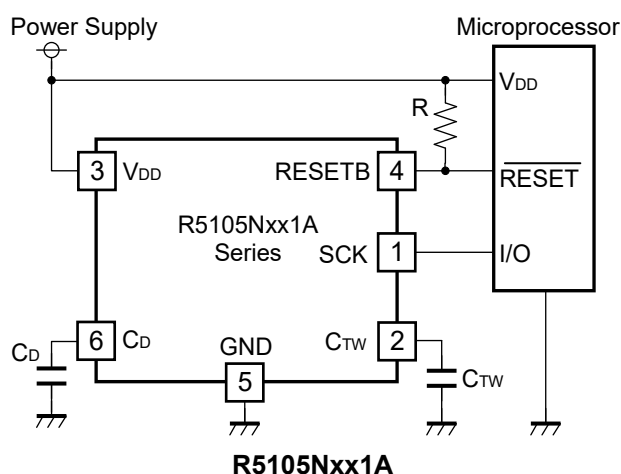
RESETB pin's output type is selectable either the Nch open-drain output or CMOS output. If the Nch open-drain type output is selected, the RESETB pin is pulled up with an external resistor to an appropriate voltage source.

Clock Pulse Input

Built-in watchdog timer is cleared with the SCK clock pulse within the watchdog timeout period.

APPLICATION INFORMATION

Typical Applications



TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current⁽¹⁾, which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100kΩ or less as a guide, and connect C_{IN}⁽²⁾ of 0.1μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As result, make sure that the cross conduction current has no problem.

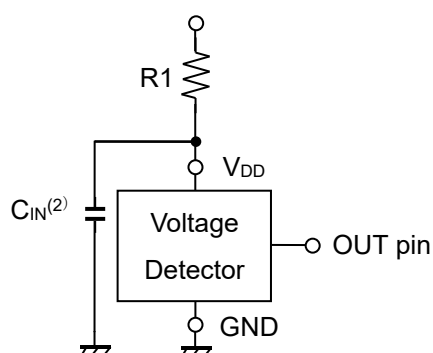


Figure A

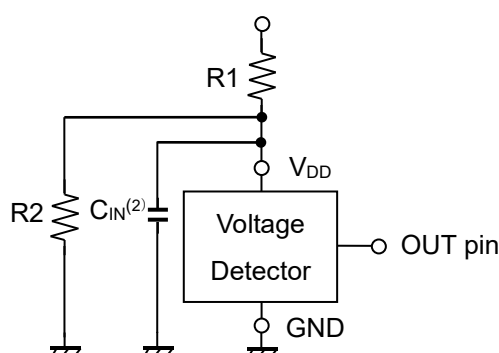


Figure B

⁽¹⁾ In the CMOS output type, a charging current for OUT pin is included.

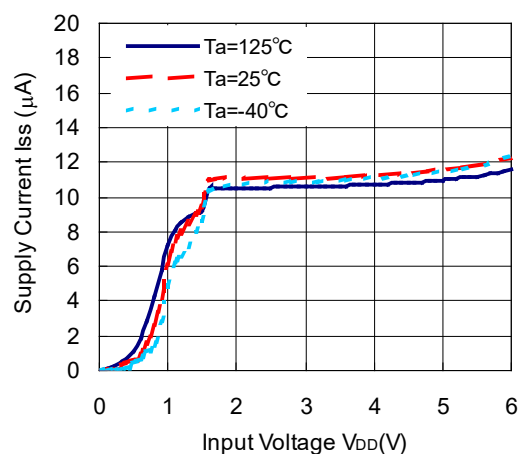
⁽²⁾ Note the bias dependence of capacitors.

TYPICAL CHARACTERISTICS

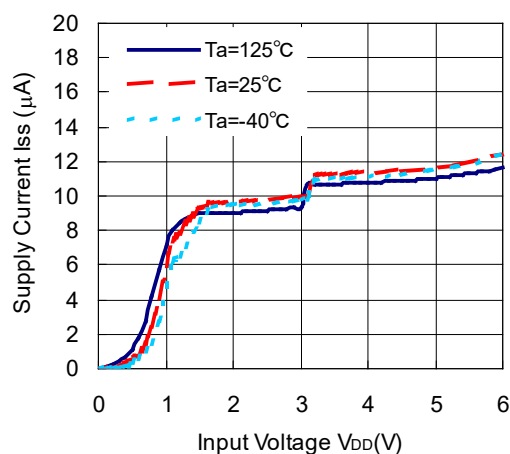
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Input Voltage

R510xx151x

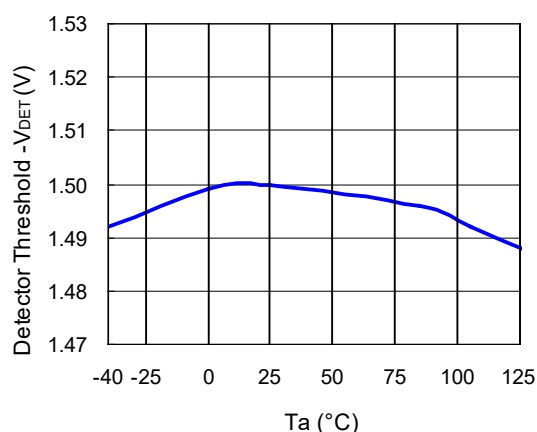


R510xx301x

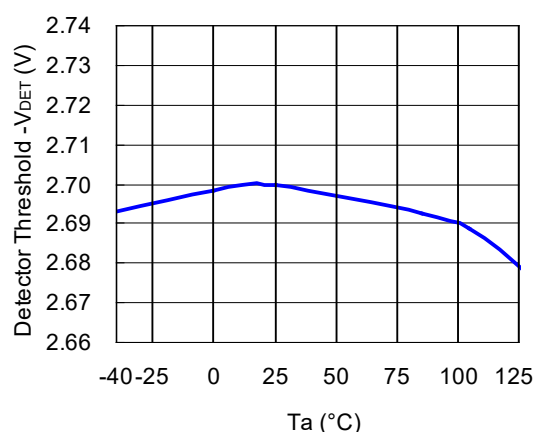


2) Detector Threshold vs. Temperature

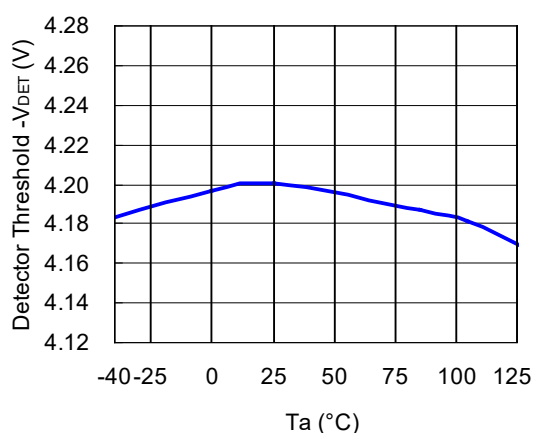
R510xx151x



R510xx271x

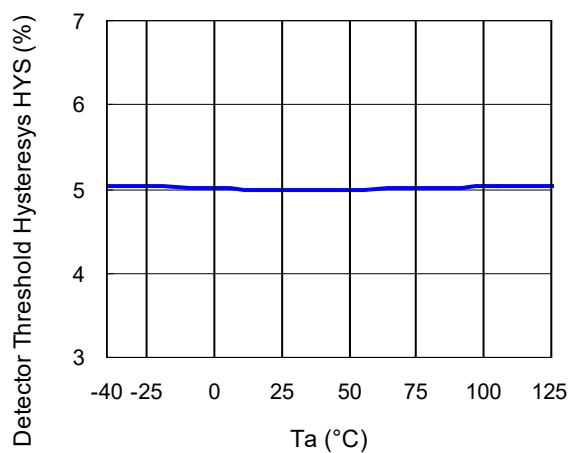


R510xx421x

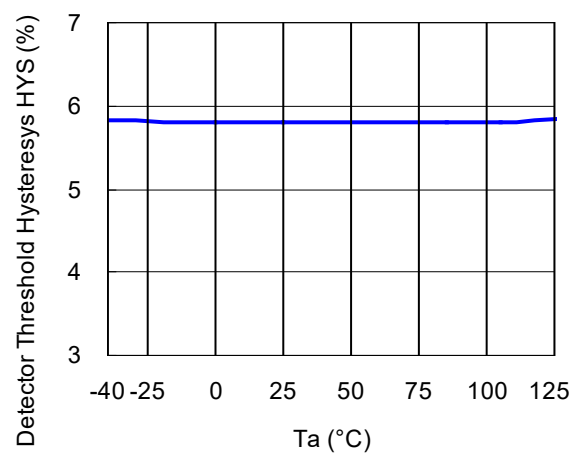


3) Detector Threshold Hysteresis vs. Temperature

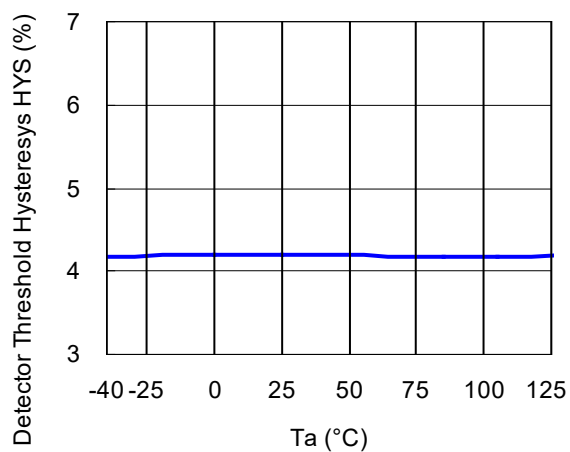
R510xx151x



R510xx271x

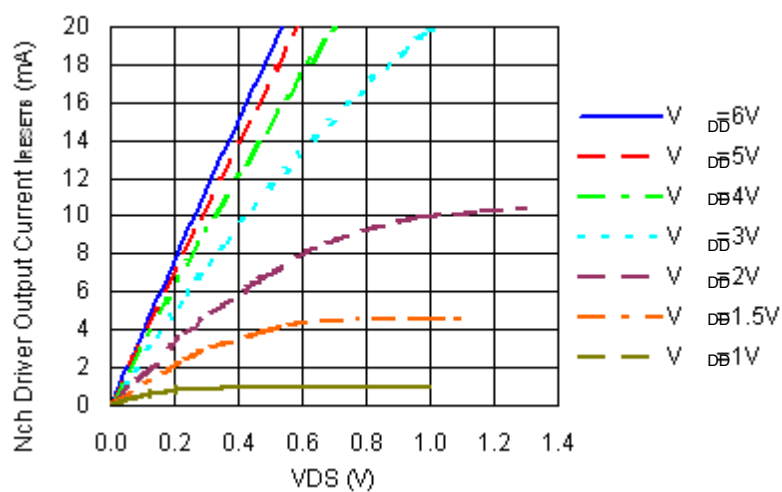


R510xx421x



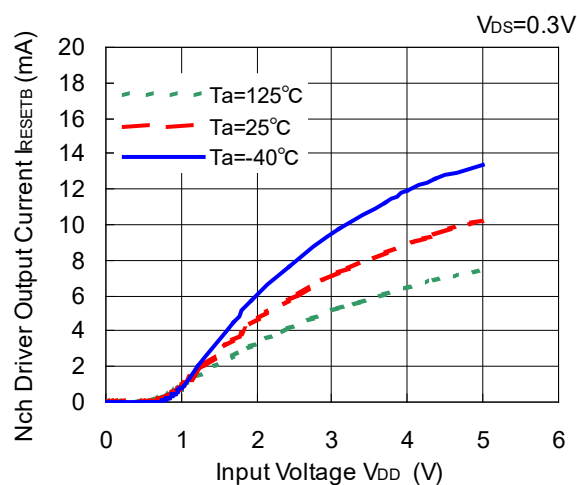
4) Nch Driver Output Current vs. Vds

R510xx

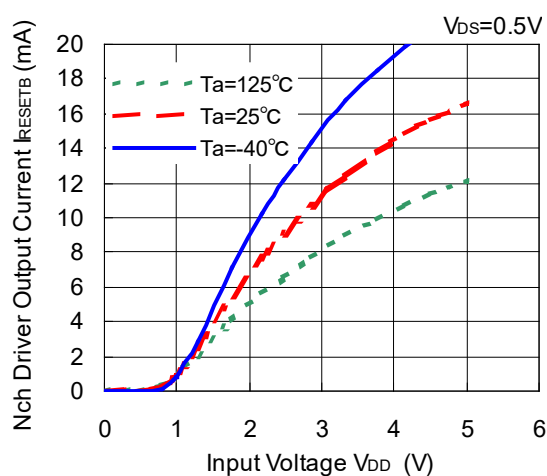


5) Nch Driver Output Current vs. Input Voltage

R510xx

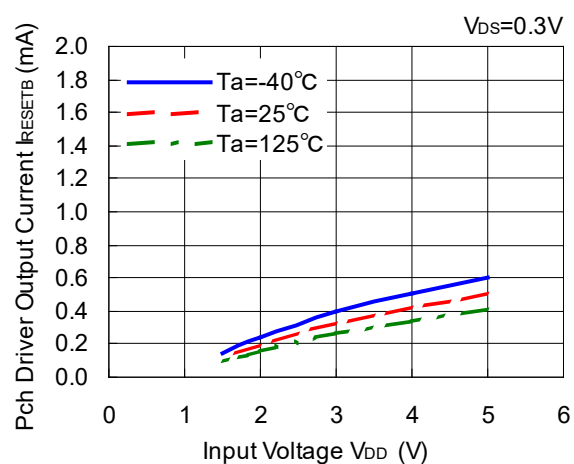


R510xx

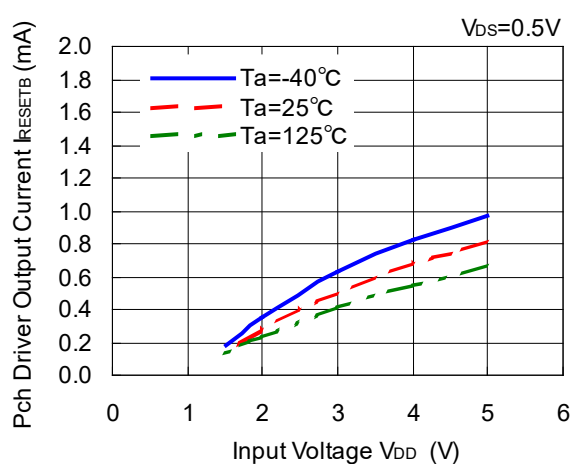


6) Pch Driver Output Current vs. Input Voltage

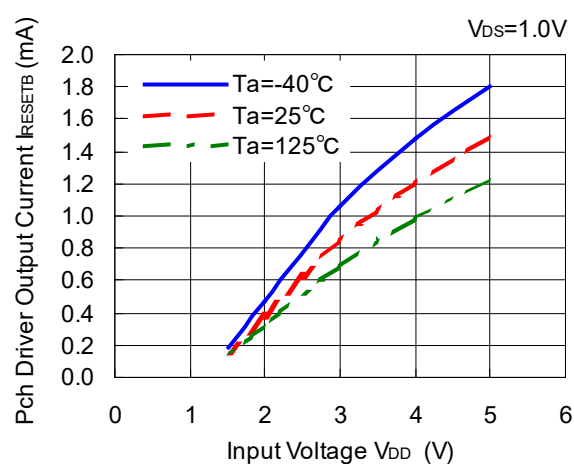
R510xx



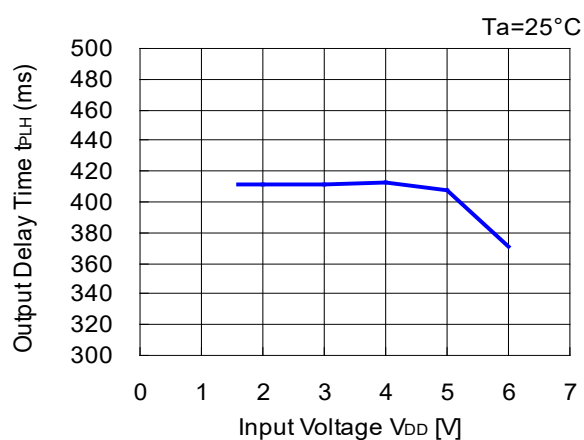
R510xx



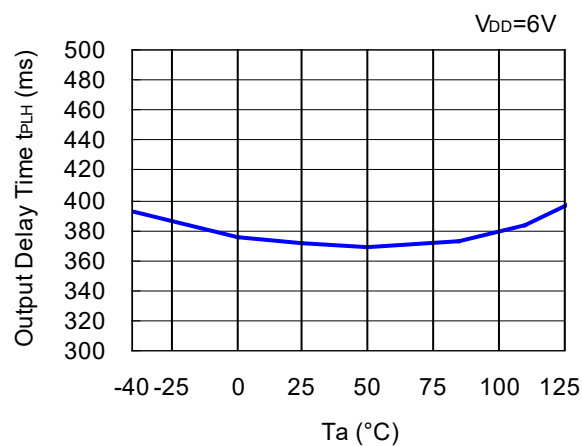
R510xx



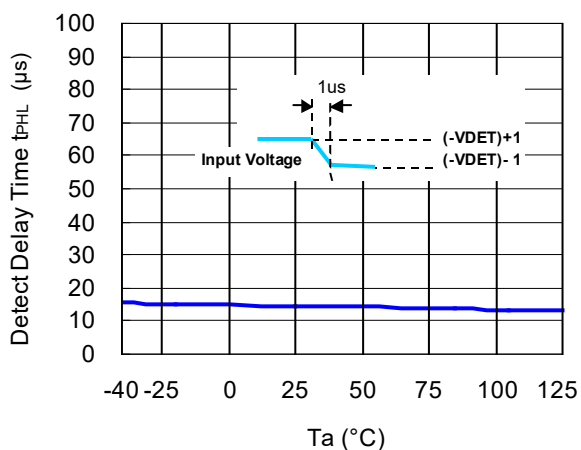
7) Released Delay Time vs. Input Voltage R510xx



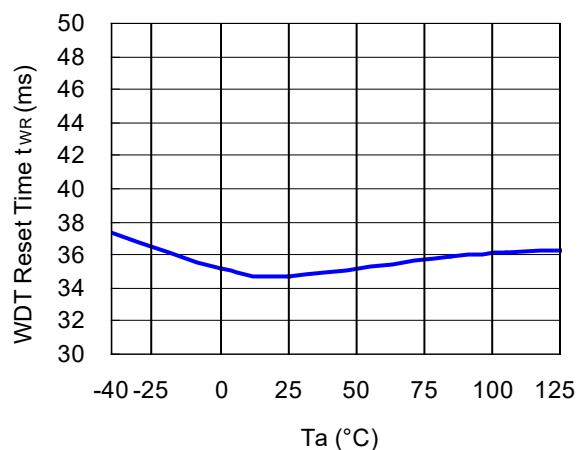
8) Released Delay Time vs. Temperature R510xx



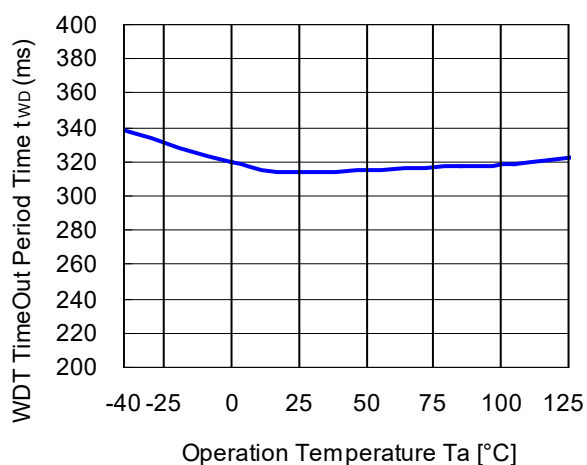
9) Detector Output Delay Time vs. Temperature R510xx



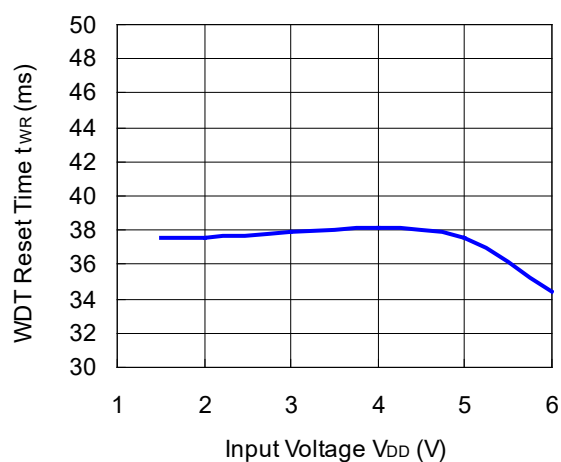
10) WDT Reset Timer vs. Temperature R510xx

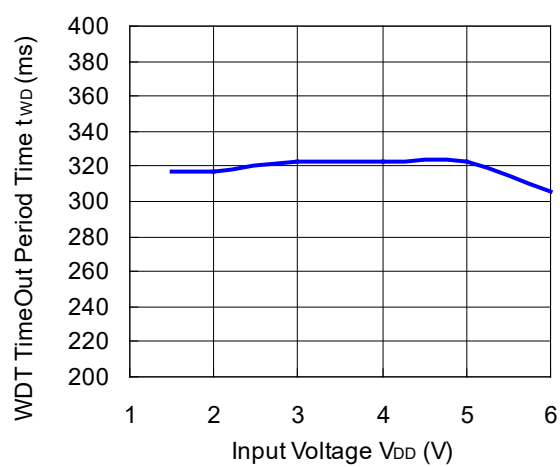
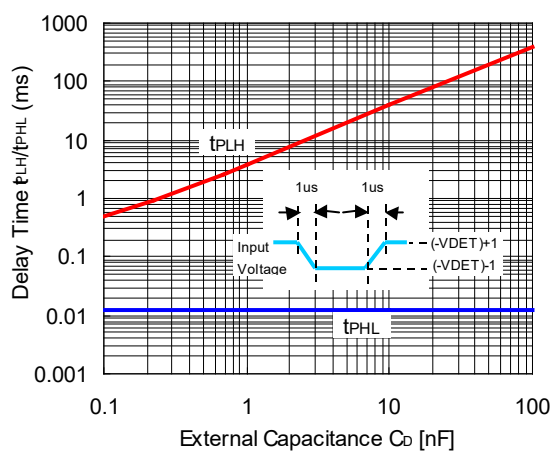


11) WDT Timeout Period vs. Temperature R510xx



12) WDT Reset Timer vs. Input Voltage R510xx



13) WDT Timeout Period vs. Input Voltage
R510xx**14) Output Delay Time vs. External Capacitance**
R510xx

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 7 pcs

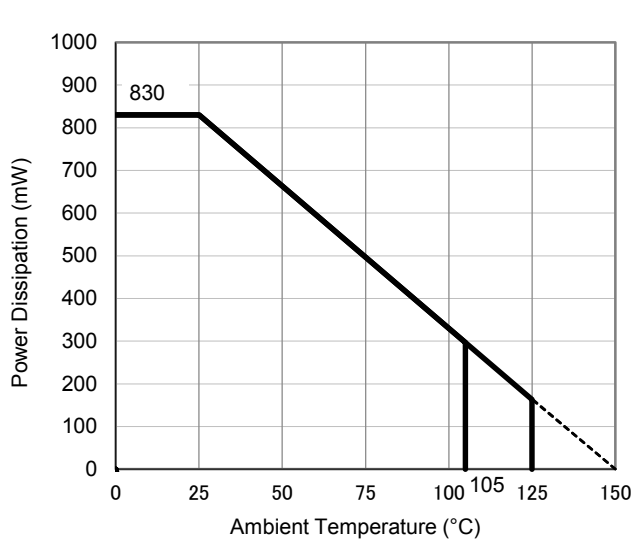
Measurement Result

(Ta = 25°C, Tjmax = 150°C)

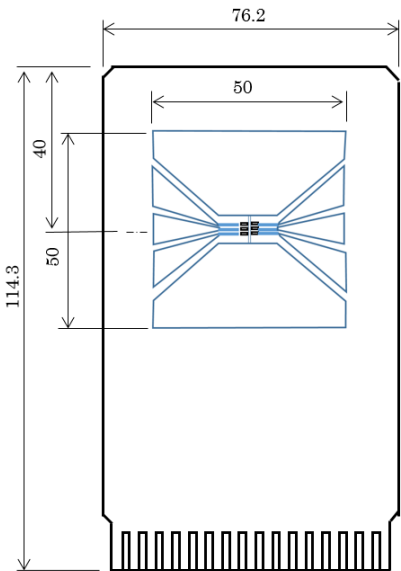
Item	Measurement Result
Power Dissipation	830 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 150^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 51^{\circ}\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

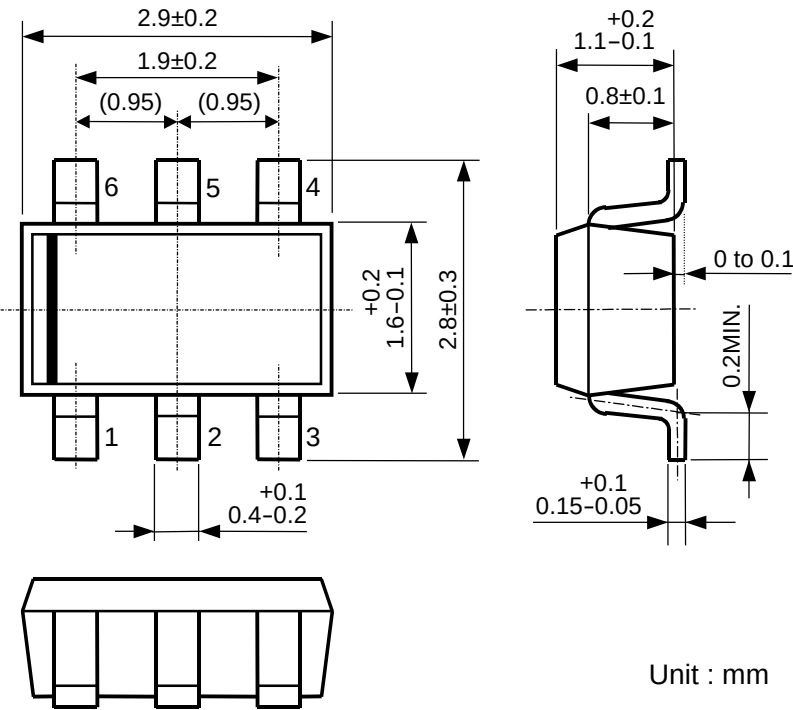
ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



SOT-23-6 Package Dimensions



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