pASIC 3 FPGA Family Data Sheet

Up to 60,000 Usable PLD Gate pASIC 3 FPGA Combining High Performance and High Density

Device Highlights

High Performance & High Density

- Up to 60,000 usable PLD gates with up to 316 I/Os
- 300 MHz 16-bit counters, 400 MHz datapaths
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use/Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V buses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O cells with individually controlled registered input path and output enables

Up to 316 I/O Pins

- Up to 308 bidirectional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- Up to eight high-drive input/distributed network pins

Up to Eight Low-Skew Distributed Networks

- Two array clock/control networks are available to the logic cell flip-flop; clock, set, and reset inputs — each can be driven by an input-only pin
- Up to six global clock/control networks are available to the logic cell; F1, clock, set, and reset inputs and the data input, I/O register clock, reset, and enable inputs as well as the output enable control — each can be driven by an input-only pin, I/O pin, any logic cell output, or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

Figure 1: Up to 1,584 pASIC 3 Logic Cells

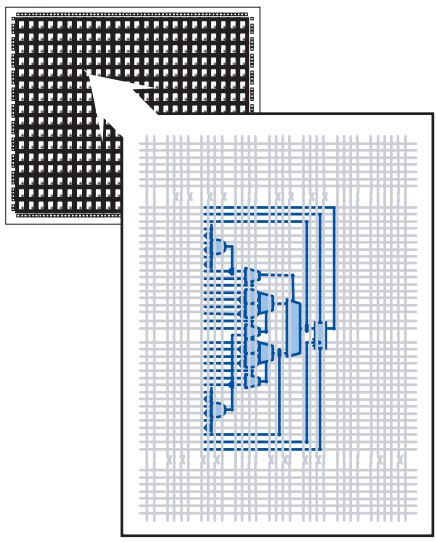


Table 1: pASIC 3 Product Family Members

		QL3004	QL3004E	QL3006	QL3012	QL3025	QL3040	QL3060
Max Gates		5,188	5,188	8,008	15,740	32,616	48,384	75,232
Logic Array		8 x 12	8 x 12	10 x 16	20 x 16	28 x 24	36 x 28	44 x 36
Logic Cells		96	96	160	320	672	1,008	1,584
Max Flip-Flops		178	178	322	438	876	1,260	1,900
Max I/O		74	74	74	110	196	244	308
Packages	PLCC	68	68	68	-	-	-	-
	PLCC	84	84	84	84	-	-	-
	TQFP	100	100	100	100	100	-	-
	TQFP	-	-	-	144	144	-	-
	PQFP	-	-	-	-	208	208	208
	PBGA	-	-	-	-	256	-	-
	PBGA	-	-	-	-	-	456	456

Table 2: Max I/O per Device/Package Combination

Device	68 PLCC	84 PLCC	100 TQFP	144 TQFP	208 PQFP	256PBGA	456 PBGA
QL3004	46	60	74	-	-	-	-
QL3004E	46	60	74	-	-	-	-
QL3006	46	60	74	-	-	-	-
QL3012	-	60	74	110	-	-	-
QL3025	-	-	74	110	166	196	-
QL3040	-	-	-	-	166	-	244
QL3060	-	-	-	-	166	-	308

Architecture Overview

The pASIC 3 family of devices have a range of 4,000 to 60,000 usable PLD gates. pASIC 3 FPGAs are fabricated on a 0.35 µm four-layer metal process using QuickLogic's" patented ViaLink" technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The pASIC 3 family of devices contain a range of 96 to 1,584 logic cells (see **Table 1**). With a range of 74 to 316 I/Os, the pASIC 3 family is available in many device/package combinations (see **Table 2**).

Software support for the complete pASIC 3 family is available through two basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools™ for Workstations package provides a solution for designers who use Cadence®, Exemplar™, Mentor®, Synopsys®, Synplicity®, Viewlogic™, Aldec™, or other third-party tools for design entry, synthesis, or simulation.

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 9** by the numbers provided in **Table 3** through **Table 7**.

Table 3: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay [b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time [b]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 9**.
b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 4: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 9**.

Table 5: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

Table 6: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

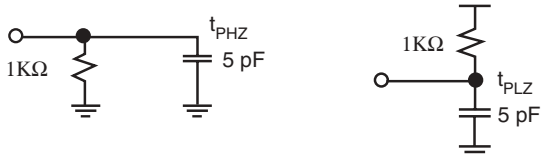
a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 9**.

Table 7: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State [a]	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State	1.2	-	-	-	-

a. The loads presented in **Figure 2** are used for t_{PXZ}:

Figure 2: Loads used for t_{PXZ}



DC Characteristics

The DC specifications are provided in **Table 8** through **Table 10**.

Table 8: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 9: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	-	-	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 10: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO}+0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	IOH = -12 mA	2.4	V_{CC}	V
		IOH = -500 µA	0.9 V_{CC}	V_{CC}	V
V_{OL}	Output LOW Voltage	IOL = 16 mA[a]		0.45	V
		IOL = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
I_{OS}	Output Short Circuit Current[c]	VO = GND	-15	-180	mA
		VO = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	VI, VIO = V_{CCIO} or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see "Contact Information" on page 49).

Kv and Kt Graphs

Figure 3: Voltage Factor vs. Supply Voltage

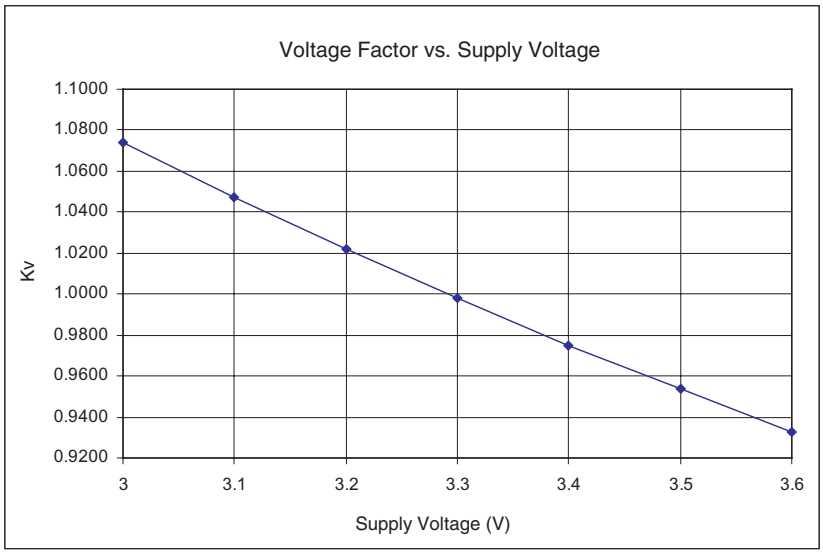
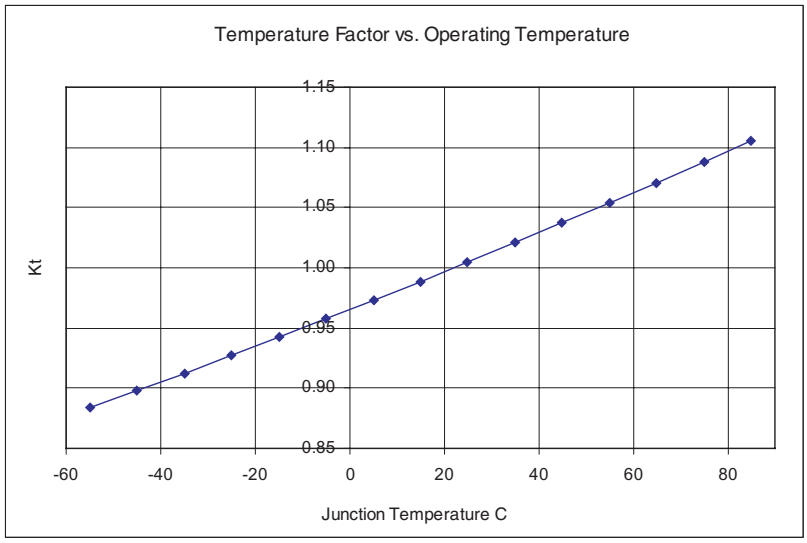
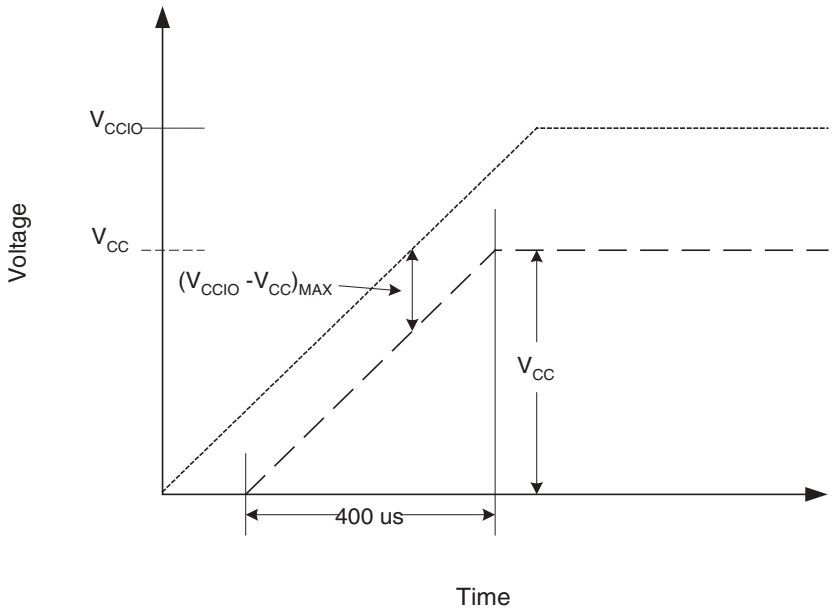


Figure 4: Temperature Factor vs. Operating Temperature



Power-Up Sequencing

Figure 5: Power-Up Requirements



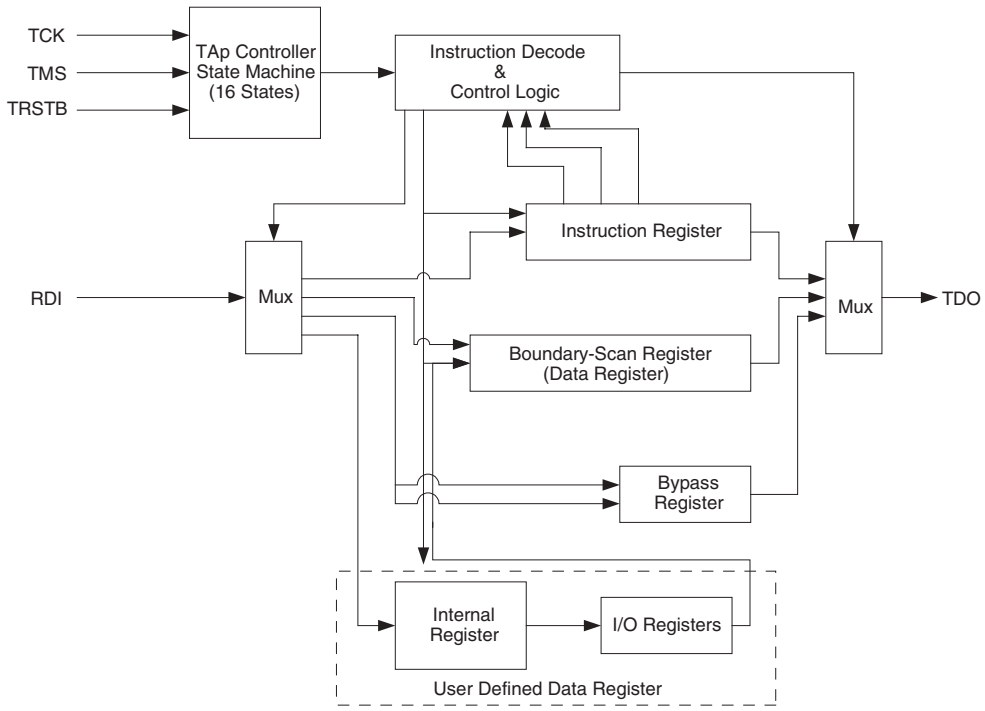
When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 µs or longer to reach the maximum value (refer to **Figure 5**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

JTAG

Figure 6: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.

- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

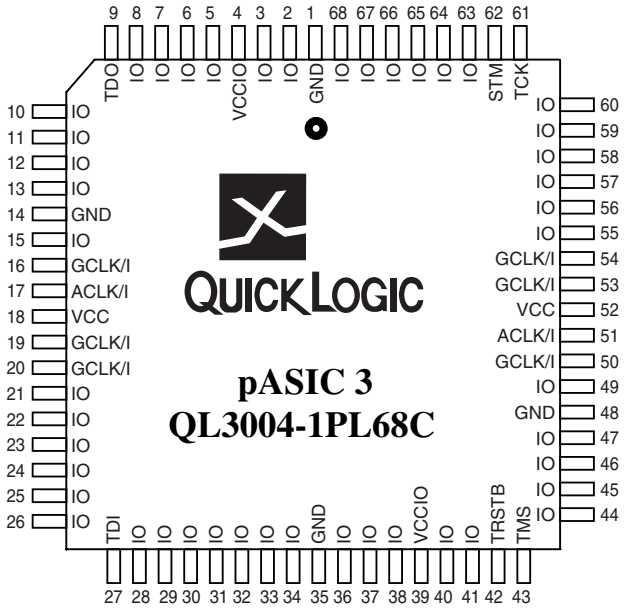
Pin Descriptions

Table 11: Pin Descriptions

Pin	Function	Description
TDI	Test data in for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TRSTB	Active low reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test mode select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TCK	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special test mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5.0 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.

QL3004 – 68 PLCC Pinout Diagram

Figure 7: QL3004 – 68 Pin PLCC (Top View)



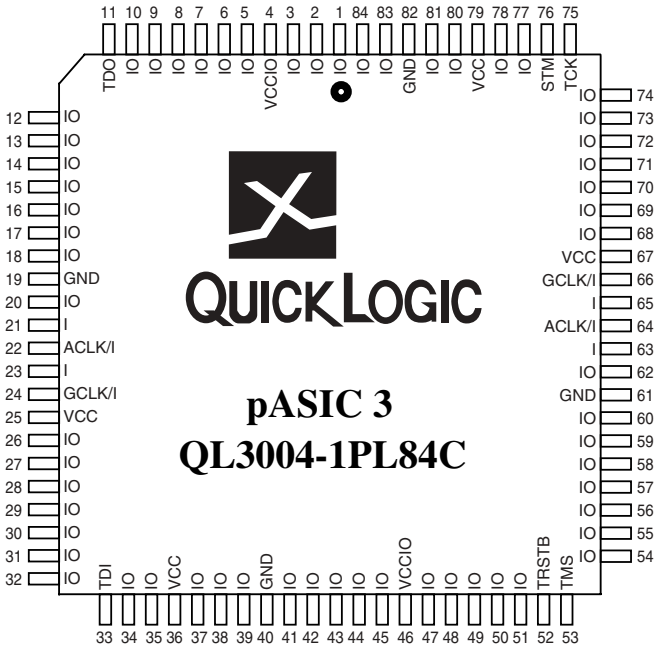
QL3004 – 68 PLCC Pinout Table

Table 12: QL3004 – 68 PLCC Pinout Table

68 PLCC	Function	68 PLCC	Function	68 PLCC	Function	68 PLCC	Function
1	GND	18	VCC	35	GND	52	VCC
2	I/O	19	GCLK/I	36	I/O	53	GCLK/I
3	I/O	20	GCLK/I	37	I/O	54	GCLK/I
4	VCCIO	21	I/O	38	I/O	55	I/O
5	I/O	22	I/O	39	VCCIO	56	I/O
6	I/O	23	I/O	40	I/O	57	I/O
7	I/O	24	I/O	41	I/O	58	I/O
8	I/O	25	I/O	42	TRSTB	58	I/O
9	TDO	26	I/O	43	TMS	60	I/O
10	I/O	27	TDI	44	I/O	61	TCK
11	I/O	28	I/O	45	I/O	62	STM
12	I/O	29	I/O	46	I/O	63	I/O
13	I/O	30	I/O	47	I/O	64	I/O
14	GND	31	I/O	48	GND	65	I/O
15	I/O	32	I/O	49	I/O	66	I/O
16	GCLK/I	33	I/O	50	GCLK/I	67	I/O
17	ACLK/I	34	I/O	51	ACLK/I	68	I/O

QL3004 – 84 PLCC Pinout Diagram

Figure 8: QL3004 – 84 Pin PLCC (Top View)



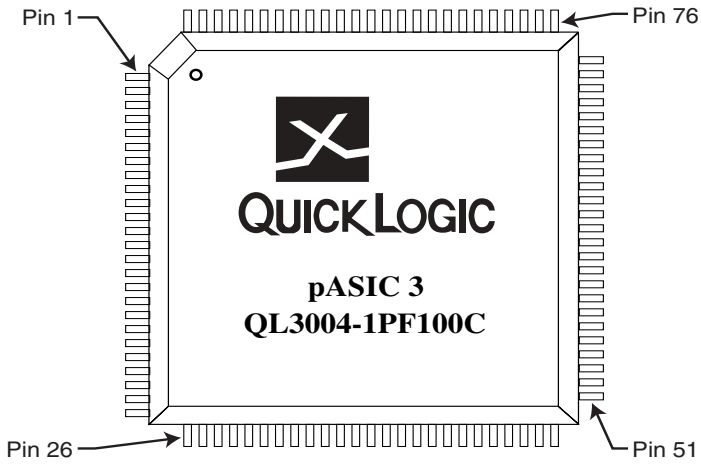
QL3004 – 84 PLCC Pinout Table

Table 13: QL3004 – 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

QL3004 – 100 TQFP Pinout Diagram

Figure 9: QL3004 – 100 Pin TQFP (Top View)



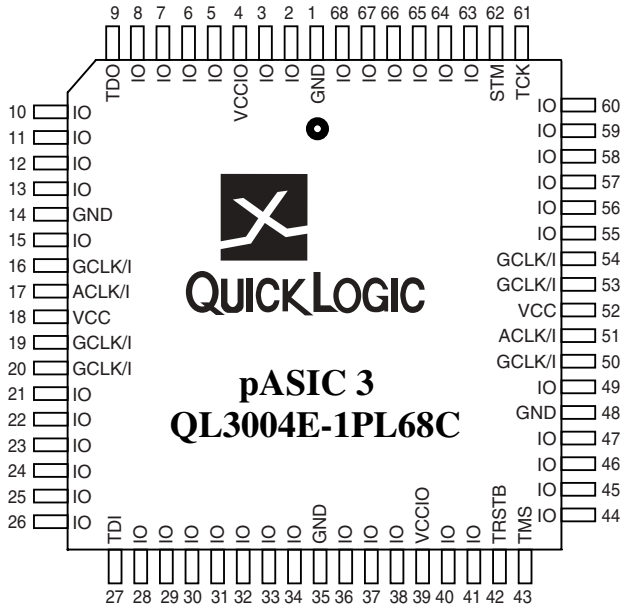
QL3004 – 100 TQFP Pinout Table

Table 14: QL3004 – 100 TQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	GCLK/I	36	I/O	61	GCLK/I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	GCLK/I	39	I/O	64	GCLK/I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

QL3004E – 68 PLCC Pinout Diagram

Figure 10: QL3004E – 68 Pin PLCC (Top View)



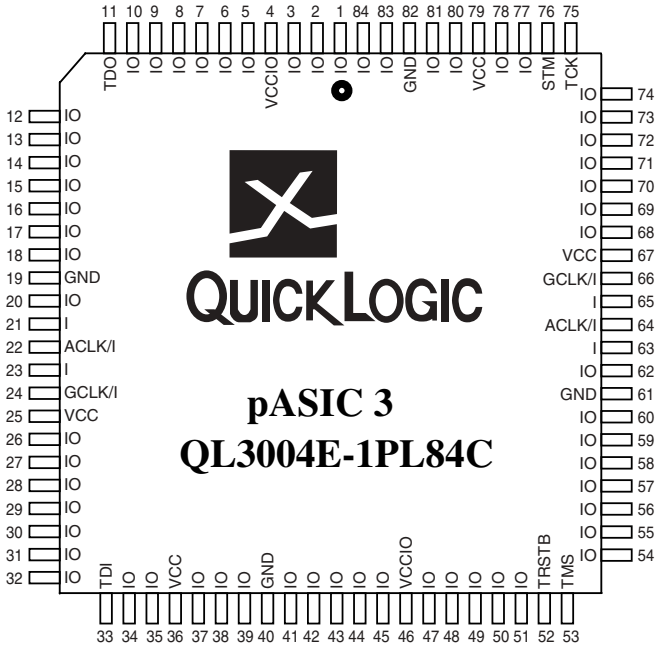
QL3004E – 68 PLCC Pinout Table

Table 15: QL3004E – 68 PLCC Pinout Table

68 PLCC	Function	68 PLCC	Function	68 PLCC	Function	68 PLCC	Function
1	GND	18	VCC	35	GND	52	VCC
2	I/O	19	I	36	I/O	53	I
3	I/O	20	GCLK/I	37	I/O	54	GCLK/I
4	VCCIO	21	I/O	38	I/O	55	I/O
5	I/O	22	I/O	39	VCCIO	56	I/O
6	I/O	23	I/O	40	I/O	57	I/O
7	I/O	24	I/O	41	I/O	58	I/O
8	I/O	25	I/O	42	TRSTB	58	I/O
9	TDO	26	I/O	43	TMS	60	I/O
10	I/O	27	TDI	44	I/O	61	TCK
11	I/O	28	I/O	45	I/O	62	STM
12	I/O	29	I/O	46	I/O	63	I/O
13	I/O	30	I/O	47	I/O	64	I/O
14	GND	31	I/O	48	GND	65	I/O
15	I/O	32	I/O	49	I/O	66	I/O
16	I	33	I/O	50	I	67	I/O
17	ACLK/I	34	I/O	51	ACLK/I	68	I/O

QL3004E – 84 PLCC Pinout Diagram

Figure 11: QL3004E – 84 Pin PLCC (Top View)



QL3004E – 84 PLCC Pinout Table

Table 16: QL3004E – 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

QL3004E – 100 TQFP Pinout Diagram

Figure 12: QL3004E – 100 Pin TQFP (Top View)

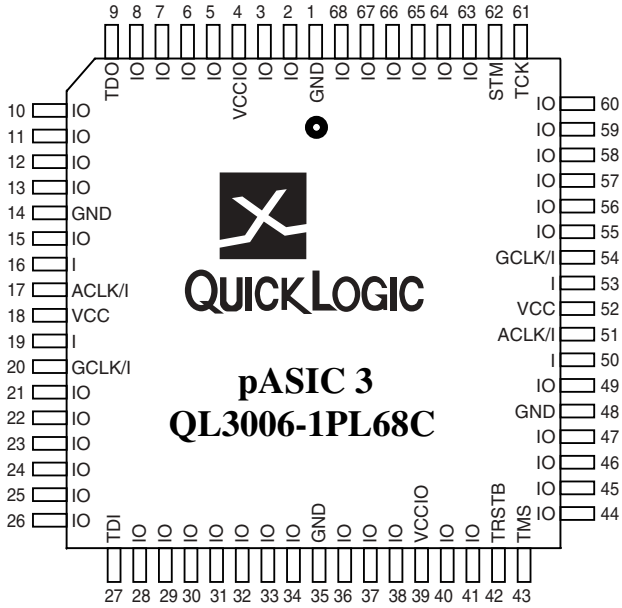
QL3004E – 100 TQFP Pinout Table

Table 17: QL3004E – 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

QL3006 – 68 PLCC Pinout Diagram

Figure 13: QL3006 – 68-pin PLCC (Top View)



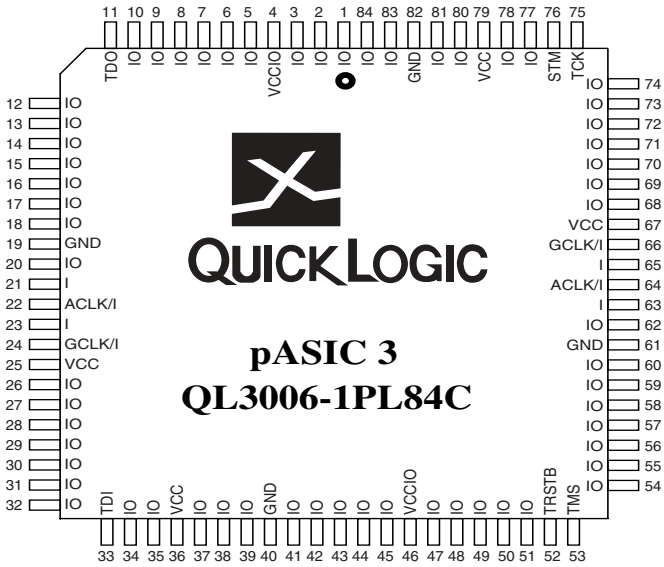
QL3006 – 68 PLCC Pinout Table

Table 18: QL3006 – 68 PLCC Pinout Table

68 PLCC	Function	68 PLCC	Function	68 PLCC	Function	68 PLCC	Function
1	GND	18	VCC	35	GND	52	VCC
2	I/O	19	I	36	I/O	53	I
3	I/O	20	GCLK/I	37	I/O	54	GCLK/I
4	VCCIO	21	I/O	38	I/O	55	I/O
5	I/O	22	I/O	39	VCCIO	56	I/O
6	I/O	23	I/O	40	I/O	57	I/O
7	I/O	24	I/O	41	I/O	58	I/O
8	I/O	25	I/O	42	TRSTB	58	I/O
9	TDO	26	I/O	43	TMS	60	I/O
10	I/O	27	TDI	44	I/O	61	TCK
11	I/O	28	I/O	45	I/O	62	STM
12	I/O	29	I/O	46	I/O	63	I/O
13	I/O	30	I/O	47	I/O	64	I/O
14	GND	31	I/O	48	GND	65	I/O
15	I/O	32	I/O	49	I/O	66	I/O
16	I	33	I/O	50	I	67	I/O
17	ACLK/I	34	I/O	51	ACLK/I	68	I/O

QL3006 – 84 PLCC Pinout Diagram

Figure 14: QL3006 – 84 Pin PLCC (Top View)



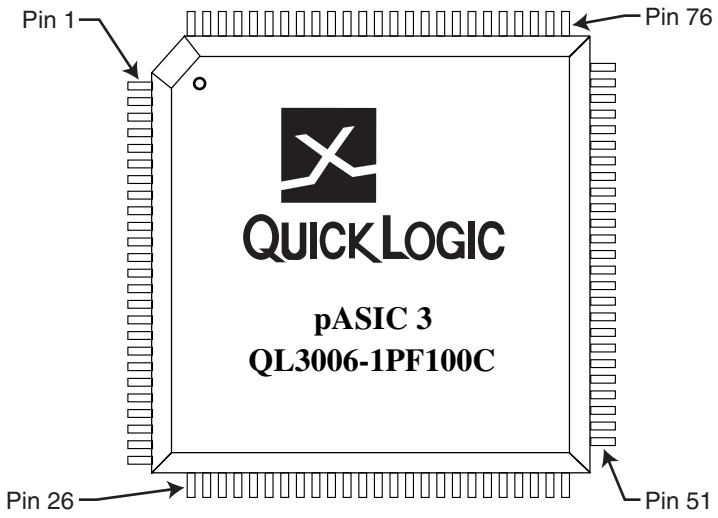
QL3006 – 84 PLCC Pinout Table

Table 19: QL3006 – 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

QL3006 – 100 TQFP Pinout Diagram

Figure 15: QL3006 – 100 Pin TQFP (Top View)



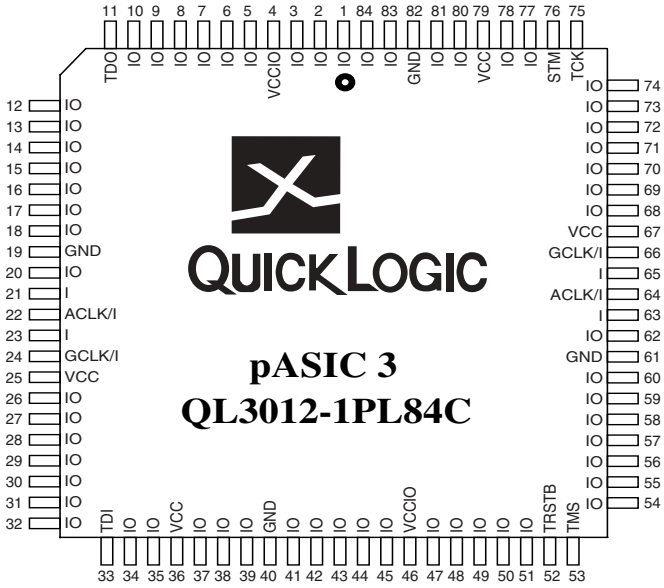
QL3006 – 100 TQFP Pinout Table

Table 20: QL3006 – 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

QL3012 – 84 PLCC Pinout Diagram

Figure 16: QL3012 – 84 Pin PLCC (Top View)



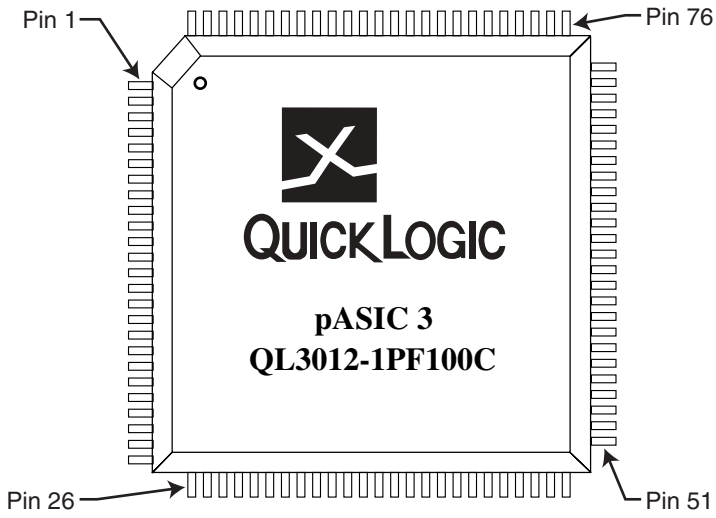
QL3012 – 84 PLCC Pinout Table

Table 21: QL3012 – 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

QL3012 – 100 TQFP Pinout Diagram

Figure 17: QL3012 – 100 Pin TQFP (Top View)



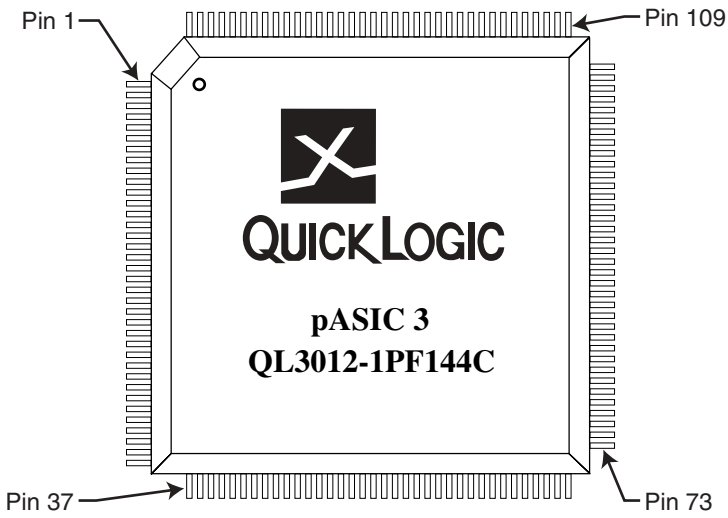
QL3012 – 100 TQFP Pinout Table

Table 22: QL3012 – 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

QL3012 – 144 TQFP Pinout Diagram

Figure 18: QL3012 – 144 Pin TQFP (Top View)



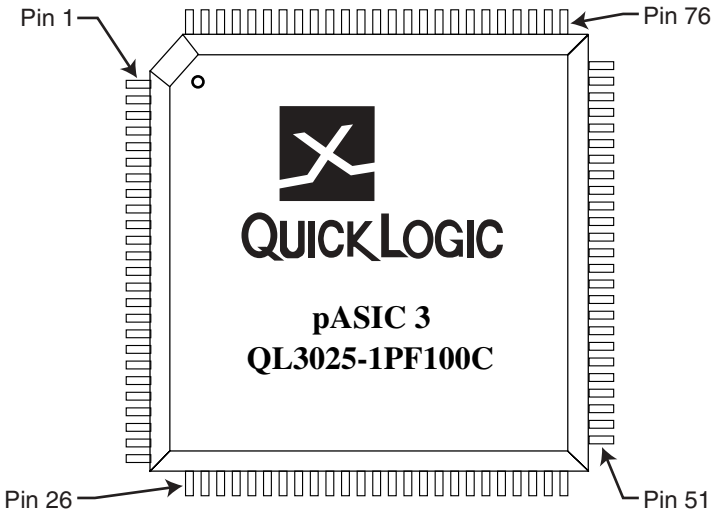
QL3012 – 144 TQFP Pinout Table

Table 23: QL3012 – 144 TQFP Pinout Table

144 TQFP	Function	144 TQFP	Function	144 TQFP	Function	144 TQFP	Function
1	I/O	38	TDI	75	I/O	111	I/O
2	I/O	39	I/O	76	I/O	112	I/O
3	I/O	40	I/O	77	I/O	113	I/O
4	I/O	41	I/O	78	I/O	114	VCC
5	I/O	42	VCC	79	VCC	115	I/O
6	I/O	43	I/O	80	I/O	116	I/O
7	VCC	44	I/O	81	I/O	117	I/O
8	I/O	45	I/O	82	I/O	118	I/O
9	I/O	46	I/O	83	I/O	119	I/O
10	I/O	47	I/O	84	I/O	120	I/O
11	I/O	48	I/O	85	I/O	121	I/O
12	I/O	49	I/O	86	I/O	122	GND
13	I/O	50	GND	87	GND	123	I/O
14	I/O	51	I/O	88	I/O	124	I/O
15	GND	52	I/O	89	I	125	I/O
16	I/O	53	I/O	90	ACLK/I	126	GND
17	I	54	GND	91	VCC	127	I/O
18	ACLK/I	55	I/O	92	I	128	I/O
19	VCC	56	I/O	93	GCLK/I	129	I/O
20	I	57	I/O	94	VCC	130	VCCIO
21	GCLK/I	58	VCCIO	95	I/O	131	I/O
22	VCC	59	I/O	96	I/O	132	I/O
23	I/O	60	I/O	NC	I/O	133	I/O
24	I/O	61	I/O	97	I/O	134	I/O
25	I/O	62	I/O	98	I/O	135	I/O
26	I/O	63	I/O	99	I/O	136	I/O
27	I/O	64	I/O	100	I/O	NC	I/O
28	I/O	65	I/O	101	I/O	137	I/O
29	I/O	66	GND	102	GND	138	GND
30	GND	67	I/O	103	I/O	139	I/O
31	I/O	68	I/O	104	I/O	140	I/O
32	I/O	69	I/O	105	I/O	141	I/O
33	I/O	70	I/O	106	I/O	142	I/O
34	I/O	71	TRSTB	107	I/O	143	TDO
35	I/O	72	TMS	108	I/O	144	I/O
36	I/O	73	I/O	109	TCK		
37	I/O	74	I/O	110	STM		

QL3025 – 100 TQFP Pinout Diagram

Figure 19: QL3025 – 100 Pin TQFP (Top View)



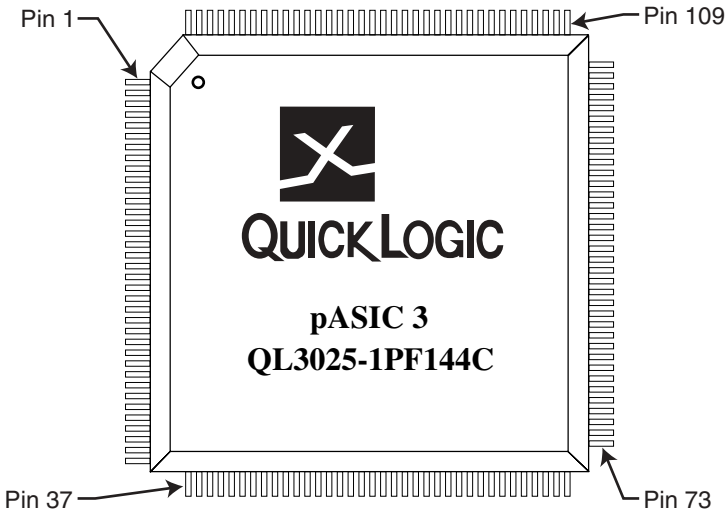
QL3025 – 100 TQFP Pinout Table

Table 24: QL3025 – 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

QL3025 – 144 TQFP Pinout Diagram

Figure 20: QL3025 – 144 Pin TQFP (Top View)



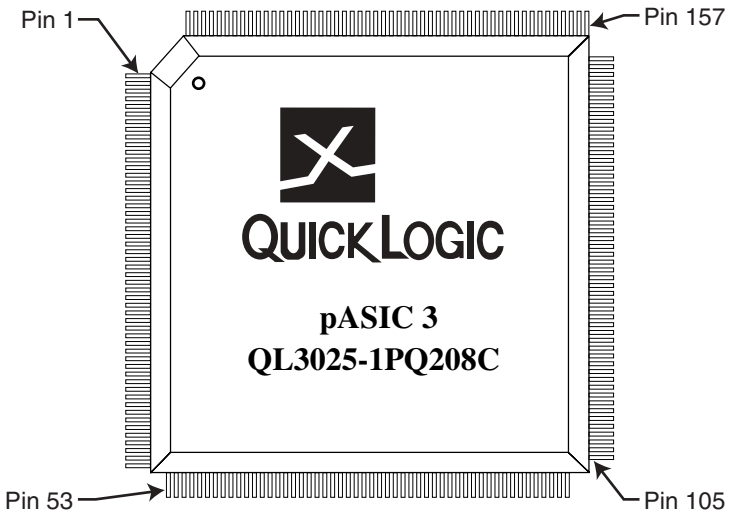
QL3025 – 144 TQFP Pinout Table

Table 25: QL3025 – 144 TQFP Pinout Table

144 TQFP	Function	144 TQFP	Function	144 TQFP	Function	144 TQFP	Function	144 TQFP	Function	144 TQFP	Function
1	I/O	25	I/O	49	I/O	73	I/O	97	I/O	121	I/O
2	I/O	26	I/O	50	GND	74	I/O	98	I/O	122	GND
3	I/O	27	I/O	51	I/O	75	I/O	99	I/O	123	I/O
4	I/O	28	I/O	52	I/O	76	I/O	100	I/O	124	I/O
5	I/O	29	I/O	53	I/O	77	I/O	101	I/O	125	I/O
6	I/O	30	GND	54	GND	78	I/O	102	GND	126	GND
7	VCC	31	I/O	55	I/O	79	VCC	103	I/O	127	I/O
8	I/O	32	I/O	56	I/O	80	I/O	104	I/O	128	I/O
9	I/O	33	I/O	57	I/O	81	I/O	105	I/O	129	I/O
10	I/O	34	I/O	58	VCCIO	82	I/O	106	I/O	130	VCCIO
11	I/O	35	I/O	59	I/O	83	I/O	107	I/O	131	I/O
12	I/O	36	I/O	60	I/O	84	I/O	108	I/O	132	I/O
13	I/O	37	I/O	61	I/O	85	I/O	109	TCK	133	I/O
14	I/O	38	TDI	62	I/O	86	I/O	110	STM	134	I/O
15	GND	39	I/O	63	I/O	87	GND	111	I/O	135	I/O
16	I/O	40	I/O	64	I/O	88	I/O	112	I/O	136	I/O
17	I	41	I/O	65	I/O	89	I	113	I/O	137	I/O
18	ACLK/I	42	VCC	66	GND	90	ACLK/I	114	V_{CC}	138	GND
19	VCC	43	I/O	67	I/O	91	VCC	115	I/O	139	I/O
20	I	44	I/O	68	I/O	92	I	116	I/O	140	I/O
21	GCLK/I	45	I/O	69	I/O	93	GCLK/I	117	I/O	141	I/O
22	VCC	46	I/O	70	I/O	94	VCC	118	I/O	142	I/O
23	I/O	47	I/O	71	TRSTB	95	I/O	119	I/O	143	TDO
24	I/O	48	I/O	72	TMS	96	I/O	120	I/O	144	I/O

QL3025 – 208 PQFP Pinout Diagram

Figure 21: QL3025 – 208 Pin PQFP (Top View)



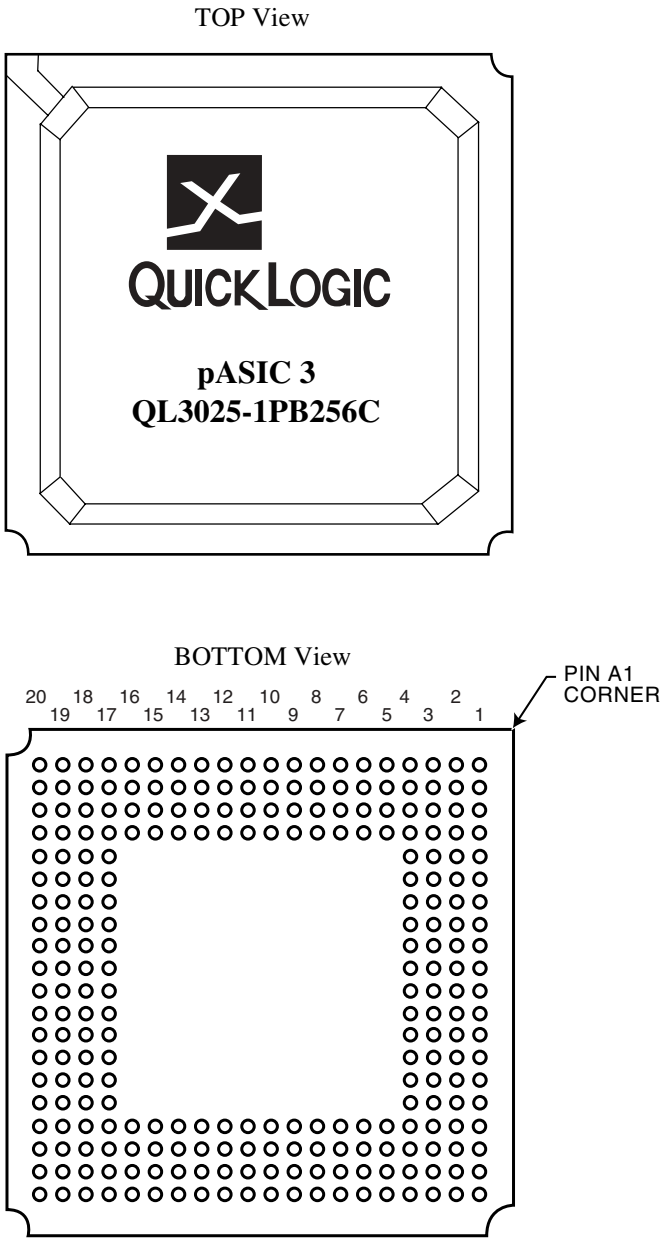
QL3025 – 208 PQFP Pinout Table

Table 26: QL3025 – 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	V_{CC}	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	VCC	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

QL3025 – 256 PBGA Pinout Diagram

Figure 22: QL3025 – 256-Pin PBGA Pinout Diagram



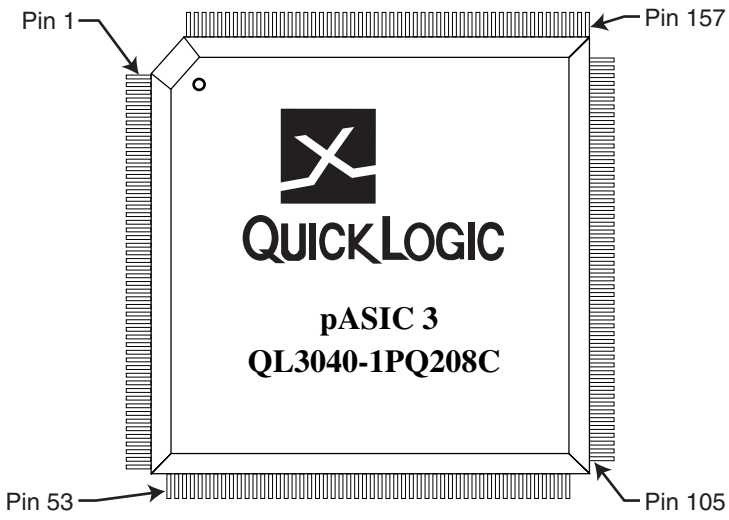
QL3025 – 256 PBGA Pinout Table

Table 27: QL3025 – 256 PBGA Pinout Table

256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function
A1	VSS	C4	I/O	E19	I/O	L2	ACLK/I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	I	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK/I	T19	NC	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	VCC	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	VCCIO	F4	VCC	L19	I/O	U2	I/O	W5	I/O
A7	I/O	C10	I/O	F17	VCC	L20	I/O	U3	I/O	W6	I/O
A8	I/O	C11	I/O	F18	NC	M1	I/O	U4	VSS	W7	I/O
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	I/O	W8	I/O
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	VCC	W9	I/O
A11	I/O	C14	I/O	G1	I/O	M4	NC	U7	I/O	W10	I/O
A12	I/O	C15	I/O	G2	NC	M17	NC	U8	VSS	W11	I/O
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	I/O	W12	I/O
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	VCC	W13	I/O
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	I/O
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	I/O
A17	I/O	C20	I/O	G19	NC	N2	I/O	U13	VSS	W16	I/O
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	I/O	W17	I/O
A19	TCK	D2	I/O	H1	I/O	N4	VSS	U15	VCC	W18	I/O
A20	I/O	D3	I/O	H2	I/O	N17	VSS	U16	I/O	W19	I/O
B1	TDO	D4	VSS	H3	I/O	N18	I/O	U17	VSS	W20	TRSTB
B2	I/O	D5	I/O	H4	VSS	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	VCC	H17	VSS	N20	I/O	U19	I/O	Y2	NC
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	VSS	H19	I/O	P2	I/O	V1	I/O	Y4	I/O
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	NC	Y5	I/O
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	I/O
B8	I/O	D11	VCC	J2	I/O	P17	I/O	V4	I/O	Y7	I/O
B9	I/O	D12	I/O	J3	NC	P18	I/O	V5	I/O	Y8	I/O
B10	I/O	D13	VSS	J4	I/O	P19	NC	V6	I/O	Y9	I/O
B11	I/O	D14	I/O	J17	NC	P20	I/O	V7	I/O	Y10	I/O
B12	I/O	D15	VCC	J18	I/O	R1	NC	V8	I/O	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	I/O	Y12	I/O
B14	I/O	D17	VSS	J20	GCLK/I	R3	I/O	V10	I/O	Y13	I/O
B15	I/O	D18	I/O	K1	I/O	R4	VCC	V11	I/O	Y14	I/O
B16	I/O	D19	I/O	K2	I/O	R17	VCC	V12	VCCIO	Y15	I/O
B17	NC	D20	I/O	K3	I/O	R18	I/O	V13	I/O	Y16	I/O
B18	STM	E1	NC	K4	VCC	R19	I/O	V14	I/O	Y17	I/O
B19	NC	E2	I/O	K17	I	R20	I/O	V15	I/O	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK/I	T1	NC	V16	I/O	Y19	I/O
C1	I/O	E4	I/O	K19	I	T2	I/O	V17	I/O	Y20	NC
C2	I/O	E17	I/O	K20	NC	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	I	T4	NC	V19	TMS		

QL3040 – 208 PQFP Pinout Diagram

Figure 23: QL3040 – 208 Pin PQFP (Top View)



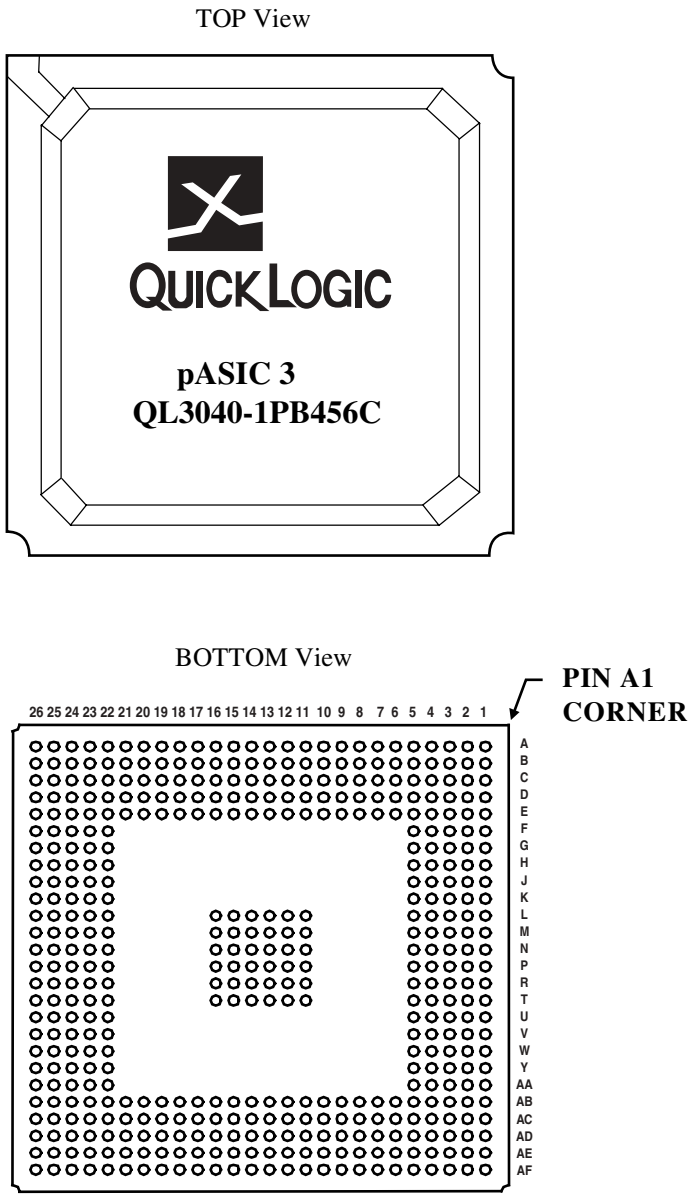
QL3040 – 208 PQFP Pinout Table

Table 28: QL3040 – 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	GCLK/I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	GCLK/I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	VCC	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	GCLK/I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	V_{CC}	69	I/O	111	I/O	153	I/O	195	I/O
28	GCLK/I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	V_{CC}	72	I/O	114	V_{CC}	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	V_{CC}
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	V_{CC}	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	V_{CC}	83	V_{CCIO}	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

QL3040 – 456 PBGA Pinout Diagram

Figure 24: QL3040 – 456-Pin PBGA Pinout Diagram



QL3040 – 456 PBGA Pinout Table

Table 29: QL3040 – 456 PBGA Pinout Table

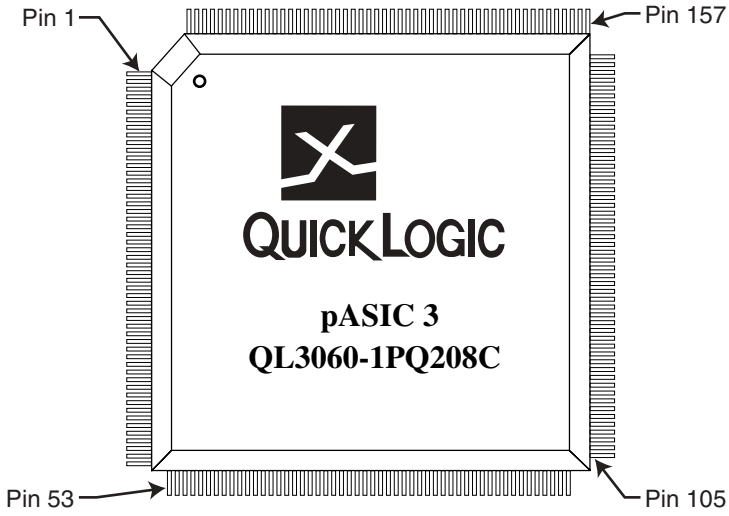
456	Function	456	Function	456	Function	456	Function	456	Function
A1	I/O	B26	STM	D25	I/O	H4	I/O	M14	GND/THERM
A2	I/O	C1	I/O	D26	I/O	H5	NC	M15	GND/THERM
A3	I/O	C2	I/O	E1	I/O	H22	NC	M16	GND/THERM
A4	I/O	C3	I/O	E2	I/O	H23	NC	M22	NC
A5	I/O	C4	TDO	E3	I/O	H24	I/O	M23	NC
A6	I/O	C5	I/O	E4	I/O	H25	NC	M24	I/O
A7	I/O	C6	I/O	E5	GND	H26	I/O	M25	I/O
A8	I/O	C7	I/O	E6	VCC	J1	I/O	M26	I/O
A9	NC	C8	I/O	E7	GND	J2	I/O	N1	GCLK/I
A10	I/O	C9	I/O	E8	NC	J3	I/O	N2	I/O
A11	I/O	C10	I/O	E9	GND	J4	NC	N3	I/O
A12	VCCIO	C11	I/O	E10	I/O	J5	GND	N4	GCLK/I
A13	I/O	C12	I/O	E11	GND	J22	NC	N5	VCC
A14	I/O	C13	I/O	E12	GND	J23	NC	N11	GND/THERM
A15	NC	C14	I/O	E13	VCC	J24	I/O	N12	GND/THERM
A16	I/O	C15	I/O	E14	GND	J25	I/O	N13	GND/THERM
A17	NC	C16	I/O	E15	GND	J26	I/O	N14	GND/THERM
A18	I/O	C17	NC	E16	GND	K1	NC	N15	GND/THERM
A19	I/O	C18	NC	E17	NC	K2	NC	N16	GND/THERM
A20	I/O	C19	I/O	E18	GND	K3	I/O	N22	GND
A21	NC	C20	I/O	E19	NC	K4	I/O	N23	I/O
A22	I/O	C21	I/O	E20	GND	K5	VCC	N24	I/O
A23	NC	C22	I/O	E21	VCC	K22	GND	N25	NC
A24	I/O	C23	I/O	E22	GND	K23	I/O	N26	I/O
A25	I/O	C24	I/O	E23	I/O	K24	I/O	P1	I/O
A26	I/O	C25	TCK	E24	I/O	K25	NC	P2	I/O
B1	I/O	C26	NC	E25	I/O	K26	I/O	P3	NC
B2	NC	D1	I/O	E26	I/O	L1	I/O	P4	I/O
B3	I/O	D2	I/O	F1	I/O	L2	I/O	P5	NC
B4	NC	D3	I/O	F2	I/O	L3	I/O	P11	GND/THERM
B5	NC	D4	GND	F3	NC	L4	I/O	P12	GND/THERM
B6	NC	D5	NC	F4	NC	L5	NC	P13	GND/THERM
B7	NC	D6	NC	F5	VCC	L11	GND/THERM	P14	GND/THERM
B8	NC	D7	I/O	F22	VCC	L12	GND/THERM	P15	GND/THERM
B9	I/O	D8	I/O	F23	NC	L13	GND/THERM	P16	GND/THERM
B10	NC	D9	GND	F24	I/O	L14	GND/THERM	P22	NC
B11	NC	D10	I/O	F25	I/O	L15	GND/THERM	P23	GCLK/I
B12	I/O	D11	I/O	F26	I/O	L16	GND/THERM	P24	GCLK/I
B13	I/O	D12	GND	G1	I/O	L22	NC	P25	NC
B14	NC	D13	I/O	G2	I/O	L23	I/O	P26	ACLK/I
B15	I/O	D14	I/O	G3	I/O	L24	I/O	R1	NC
B16	I/O	D15	GND	G4	I/O	L25	NC	R2	I/O
B17	I/O	D16	I/O	G5	NC	L26	I/O	R3	I/O
B18	I/O	D17	I/O	G22	GND	M1	ACLK/I	R4	NC
B19	I/O	D18	GND	G23	NC	M2	GCLK/I	R5	NC
B20	I/O	D19	I/O	G24	I/O	M3	I/O	R11	GND/THERM
B21	I/O	D20	NC	G25	I/O	M4	NC	R12	GND/THERM
B22	I/O	D21	NC	G26	I/O	M5	GND	R13	GND/THERM
B23	NC	D22	I/O	H1	NC	M11	GND/THERM	R14	GND/THERM
B24	I/O	D23	GND	H2	I/O	M12	GND/THERM	R15	GND/THERM
B25	I/O	D24	I/O	H3	NC	M13	GND/THERM	R16	GND/THERM

Table 29: QL3040 – 456 PBGA Pinout Table *(Continued)*

456	Function	456	Function	456	Function	456	Function	456	Function
R22	VCC	W1	I/O	AB12	NC	AD1	I/O	AE16	I/O
R23	NC	W2	I/O	AB13	I/O	AD2	NC	AE17	I/O
R24	NC	W3	I/O	AB14	GND	AD3	I/O	AE18	I/O
R25	I/O	W4	I/O	AB15	VCC	AD4	I/O	AE19	I/O
R26	GCLK/I	W5	NC	AB16	I/O	AD5	I/O	AE20	I/O
T1	I/O	W22	NC	AB17	NC	AD6	I/O	AE21	I/O
T2	I/O	W23	I/O	AB18	VCC	AD7	I/O	AE22	NC
T3	I/O	W24	I/O	AB19	GND	AD8	I/O	AE23	NC
T4	I/O	W25	I/O	AB20	NC	AD9	NC	AE24	TMS
T5	VCC	W26	NC	AB21	VCC	AD10	I/O	AE25	I/O
T11	GND/THERMAL	Y1	NC	AB22	GND	AD11	NC	AE26	I/O
T12	GND/THERMAL	Y2	I/O	AB23	I/O	AD12	I/O	AF1	I/O
T13	GND/THERMAL	Y3	NC	AB24	NC	AD13	I/O	AF2	NC
T14	GND/THERMAL	Y4	I/O	AB25	I/O	AD14	I/O	AF3	I/O
T15	GND/THERMAL	Y5	I/O	AB26	I/O	AD15	I/O	AF4	NC
T16	GND/THERMAL	Y22	GND	AC1	I/O	AD16	I/O	AF5	I/O
T22	GND	Y23	I/O	AC2	I/O	AD17	I/O	AF6	I/O
T23	I/O	Y24	NC	AC3	NC	AD18	I/O	AF7	I/O
T24	I/O	Y25	I/O	AC4	GND	AD19	NC	AF8	I/O
T25	NC	Y26	I/O	AC5	NC	AD20	NC	AF9	I/O
T26	I/O	AA1	I/O	AC6	NC	AD21	I/O	AF10	I/O
U1	NC	AA2	I/O	AC7	NC	AD22	I/O	AF11	NC
U2	I/O	AA3	NC	AC8	NC	AD23	TRSTB	AF12	I/O
U3	I/O	AA4	NC	AC9	NC	AD24	NC	AF13	I/O
U4	I/O	AA5	VCC	AC10	NC	AD25	I/O	AF14	NC
U5	GND	AA22	VCC	AC11	I/O	AD26	I/O	AF15	NC
U22	NC	AA23	NC	AC12	NC	AE1	TDI	AF16	I/O
U23	I/O	AA24	I/O	AC13	I/O	AE2	I/O	AF17	I/O
U24	I/O	AA25	I/O	AC14	VCCIO	AE3	I/O	AF18	I/O
U25	I/O	AA26	I/O	AC15	NC	AE4	I/O	AF19	NC
U26	I/O	AB1	NC	AC16	NC	AE5	I/O	AF20	I/O
V1	I/O	AB2	I/O	AC17	NC	AE6	I/O	AF21	I/O
V2	I/O	AB3	I/O	AC18	NC	AE7	I/O	AF22	I/O
V3	NC	AB4	I/O	AC19	I/O	AE8	I/O	AF23	I/O
V4	NC	AB5	GND	AC20	I/O	AE9	I/O	AF24	I/O
V5	NC	AB6	VCC	AC21	I/O	AE10	I/O	AF25	I/O
V22	GND	AB7	NC	AC22	NC	AE11	I/O	AF26	I/O
V23	NC	AB8	NC	AC23	GND	AE12	I/O		
V24	I/O	AB9	NC	AC24	NC	AE13	I/O		
V25	NC	AB10	VCC	AC25	I/O	AE14	I/O		
V26	I/O	AB11	GND	AC26	I/O	AE15	I/O		

QL3060 – 208 PQFP Pinout Diagram

Figure 25: QL3060 – 208 Pin PQFP (Top View)



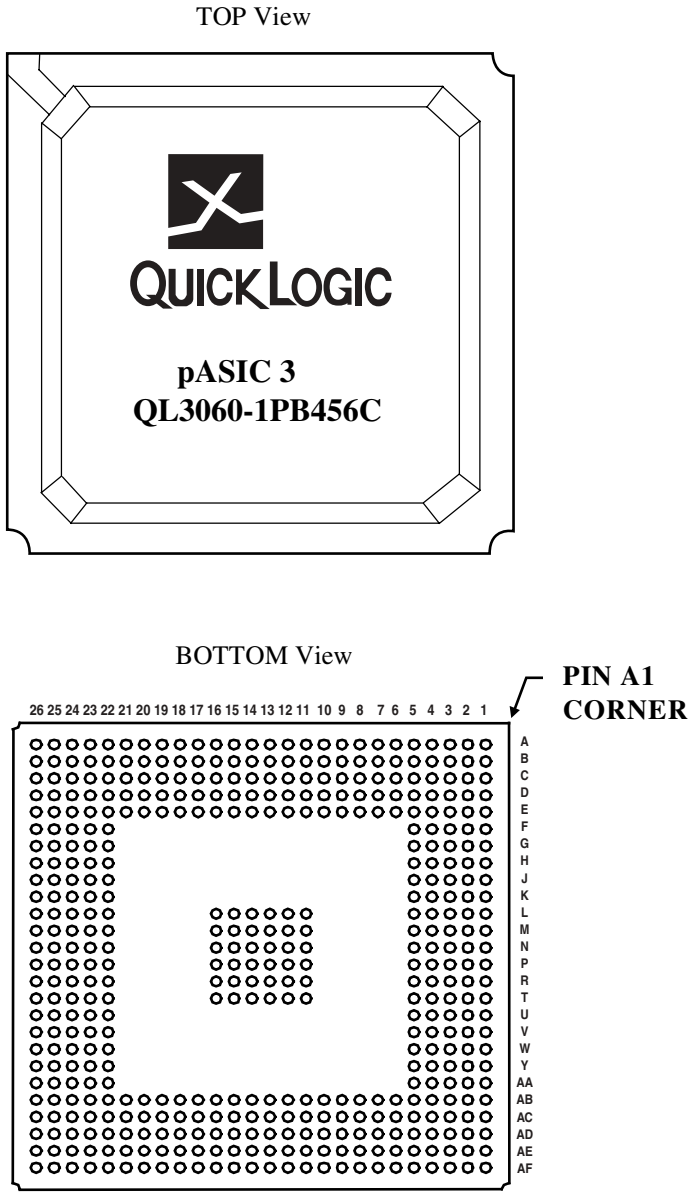
QL3060 – 208 PQFP Pinout Table

Table 30: QL3060 – 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	GCLK/I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK/I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	GCLK/I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	V_{CC}	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	GCLK/I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	GCLK/I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK/I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

QL3060 – 456 PBGA Pinout Diagram

Figure 26: QL3060 – 456-Pin PBGA Pinout Diagram



QL3060 – 456 PBGA Pinout Table

Table 31: QL3060 – 456 PBGA Pinout Table

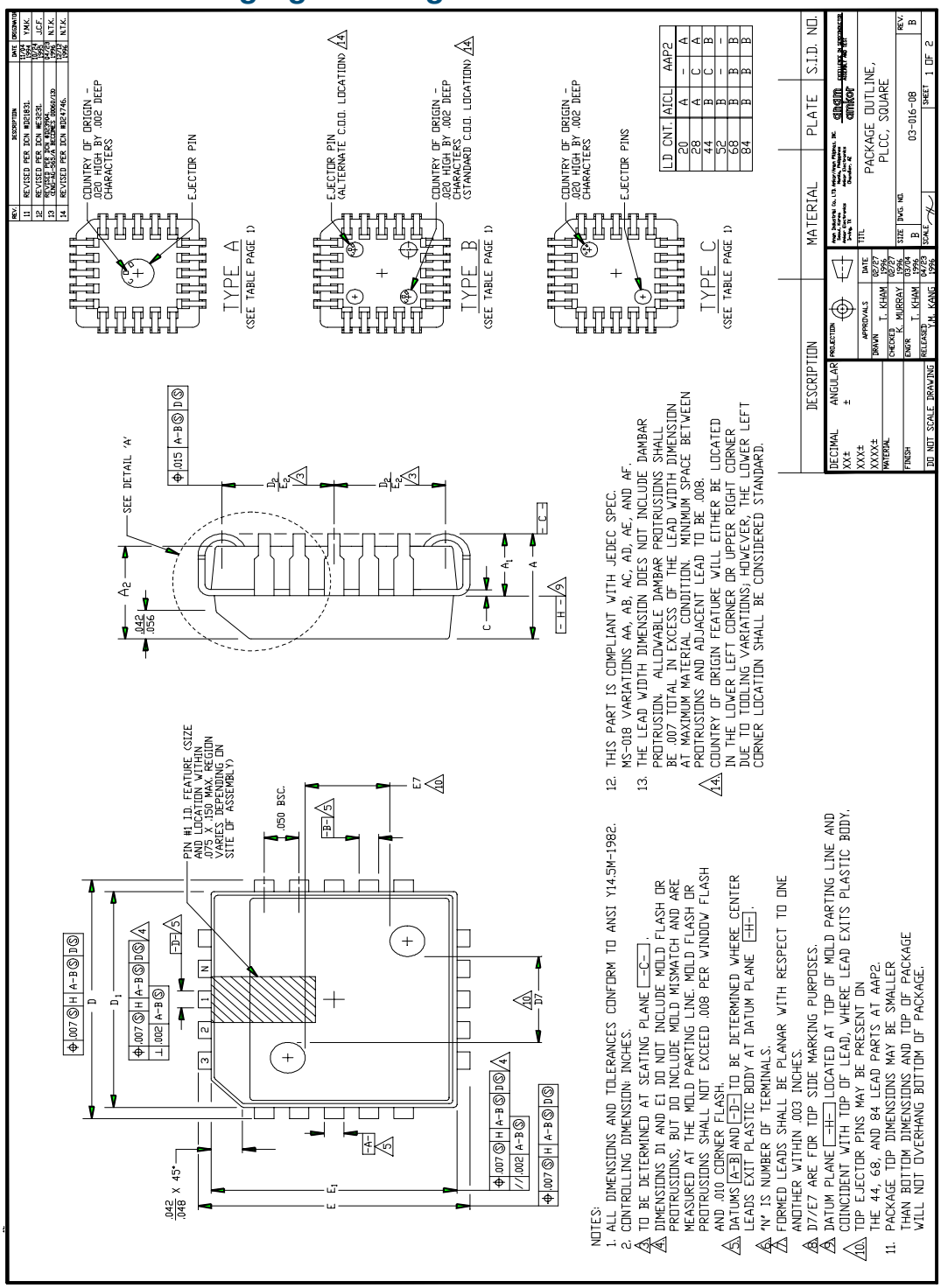
456	Function	456	Function	456	Function	456	Function	456	Function
A1	I/O	B26	STM	D25	I/O	H4	I/O	M14	GND/THERM
A2	I/O	C1	I/O	D26	I/O	H5	NC	M15	GND/THERM
A3	I/O	C2	I/O	E1	I/O	H22	NC	M16	GND/THERM
A4	I/O	C3	I/O	E2	I/O	H23	I/O	M22	NC
A5	I/O	C4	TDO	E3	I/O	H24	I/O	M23	NC
A6	I/O	C5	I/O	E4	I/O	H25	I/O	M24	I/O
A7	I/O	C6	I/O	E5	GND	H26	I/O	M25	I/O
A8	I/O	C7	I/O	E6	VCC	J1	I/O	M26	I/O
A9	I/O	C8	I/O	E7	GND	J2	I/O	N1	GCLK/I
A10	I/O	C9	I/O	E8	NC	J3	I/O	N2	I/O
A11	I/O	C10	I/O	E9	GND	J4	NC	N3	I/O
A12	VCCIO	C11	I/O	E10	I/O	J5	GND	N4	GCLK/I
A13	I/O	C12	I/O	E11	GND	J22	NC	N5	VCC
A14	I/O	C13	I/O	E12	GND	J23	NC	N11	GND/THERM
A15	I/O	C14	I/O	E13	VCC	J24	I/O	N12	GND/THERM
A16	I/O	C15	I/O	E14	GND	J25	I/O	N13	GND/THERM
A17	I/O	C16	I/O	E15	GND	J26	I/O	N14	GND/THERM
A18	I/O	C17	I/O	E16	GND	K1	I/O	N15	GND/THERM
A19	I/O	C18	I/O	E17	NC	K2	I/O	N16	GND/THERM
A20	I/O	C19	I/O	E18	GND	K3	I/O	N22	GND
A21	I/O	C20	I/O	E19	NC	K4	I/O	N23	I/O
A22	I/O	C21	I/O	E20	GND	K5	VCC	N24	I/O
A23	I/O	C22	I/O	E21	VCC	K22	GND	N25	I/O
A24	I/O	C23	I/O	E22	GND	K23	I/O	N26	I/O
A25	I/O	C24	I/O	E23	I/O	K24	I/O	P1	I/O
A26	I/O	C25	TCK	E24	I/O	K25	I/O	P2	I/O
B1	I/O	C26	I/O	E25	I/O	K26	I/O	P3	I/O
B2	I/O	D1	I/O	E26	I/O	L1	I/O	P4	I/O
B3	I/O	D2	I/O	F1	I/O	L2	I/O	P5	NC
B4	I/O	D3	I/O	F2	I/O	L3	I/O	P11	GND/THERM
B5	I/O	D4	GND	F3	I/O	L4	I/O	P12	GND/THERM
B6	I/O	D5	I/O	F4	NC	L5	NC	P13	GND/THERM
B7	I/O	D6	NC	F5	VCC	L11	GND/THERM	P14	GND/THERM
B8	I/O	D7	I/O	F22	VCC	L12	GND/THERM	P15	GND/THERM
B9	I/O	D8	I/O	F23	NC	L13	GND/THERM	P16	GND/THERM
B10	I/O	D9	GND	F24	I/O	L14	GND/THERM	P22	NC
B11	I/O	D10	I/O	F25	I/O	L15	GND/THERM	P23	GCLK/I
B12	I/O	D11	I/O	F26	I/O	L16	GND/THERM	P24	GCLK/I
B13	I/O	D12	GND	G1	I/O	L22	NC	P25	I/O
B14	I/O	D13	I/O	G2	I/O	L23	I/O	P26	ACLK/I
B15	I/O	D14	I/O	G3	I/O	L24	I/O	R1	I/O
B16	I/O	D15	GND	G4	I/O	L25	I/O	R2	I/O
B17	I/O	D16	I/O	G5	NC	L26	I/O	R3	I/O
B18	I/O	D17	I/O	G22	GND	M1	ACLK/I	R4	NC
B19	I/O	D18	GND	G23	I/O	M2	GCLK/I	R5	NC
B20	I/O	D19	I/O	G24	I/O	M3	I/O	R11	GND/THERM
B21	I/O	D20	I/O	G25	I/O	M4	NC	R12	GND/THERM
B22	I/O	D21	NC	G26	I/O	M5	GND	R13	GND/THERM
B23	I/O	D22	I/O	H1	I/O	M11	GND/THERM	R14	GND/THERM
B24	I/O	D23	GND	H2	I/O	M12	GND/THERM	R15	GND/THERM
B25	I/O	D24	I/O	H3	I/O	M13	GND/THERM	R16	GND/THERM

Table 31: QL3060 – 456 PBGA Pinout Table *(Continued)*

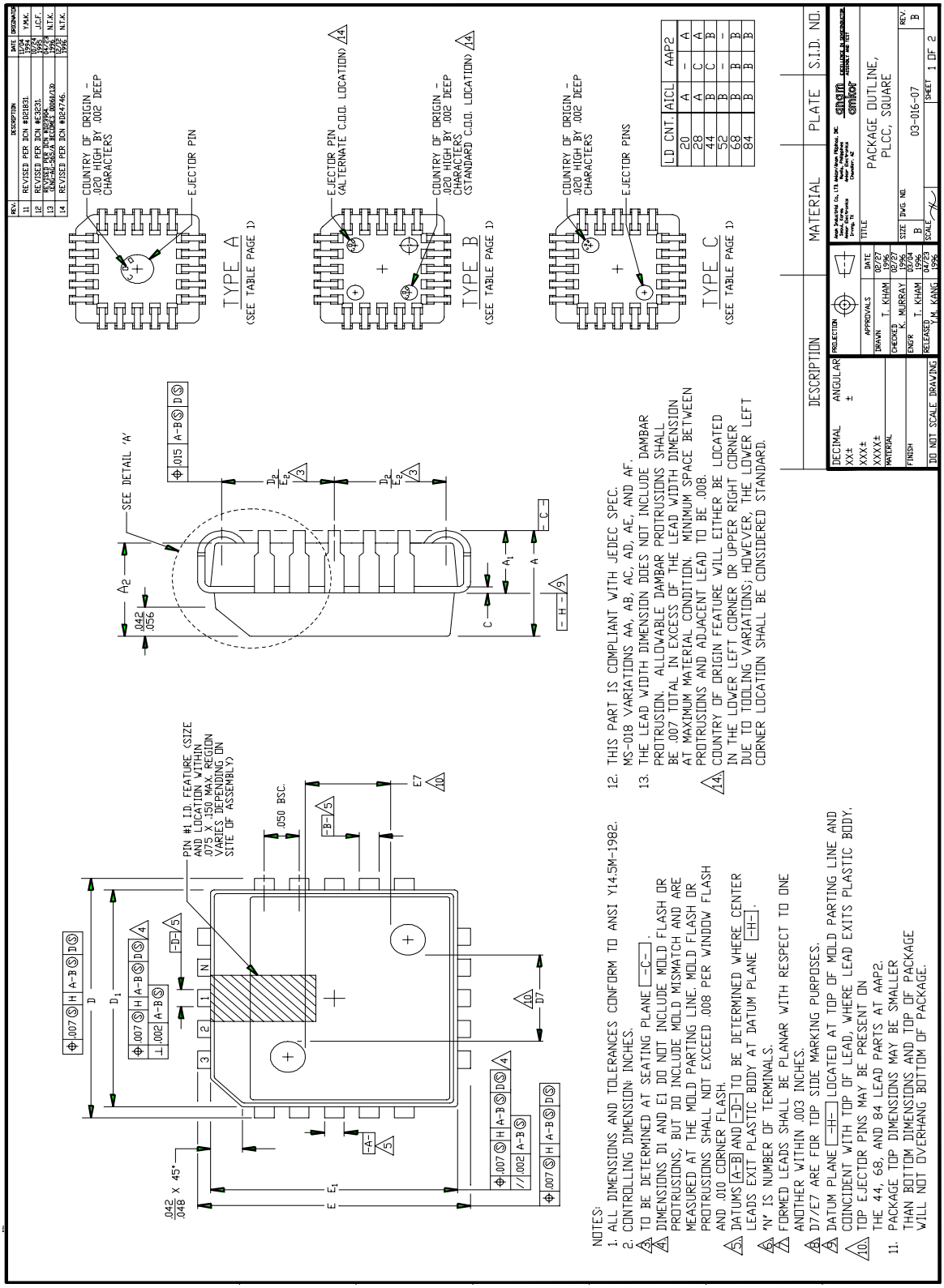
456	Function	456	Function	456	Function	456	Function	456	Function
R22	VCC	W1	I/O	AB12	NC	AD1	I/O	AE16	I/O
R23	NC	W2	I/O	AB13	I/O	AD2	NC	AE17	I/O
R24	I/O	W3	I/O	AB14	GND	AD3	I/O	AE18	I/O
R25	I/O	W4	I/O	AB15	VCC	AD4	I/O	AE19	I/O
R26	GCLK/I	W5	NC	AB16	I/O	AD5	I/O	AE20	I/O
T1	I/O	W22	NC	AB17	NC	AD6	I/O	AE21	I/O
T2	I/O	W23	I/O	AB18	VCC	AD7	I/O	AE22	I/O
T3	I/O	W24	I/O	AB19	GND	AD8	I/O	AE23	NC
T4	I/O	W25	I/O	AB20	NC	AD9	I/O	AE24	TMS
T5	VCC	W26	I/O	AB21	VCC	AD10	I/O	AE25	I/O
T11	GND/THERMAL	Y1	I/O	AB22	GND	AD11	I/O	AE26	I/O
T12	GND/THERMAL	Y2	I/O	AB23	I/O	AD12	I/O	AF1	I/O
T13	GND/THERMAL	Y3	I/O	AB24	I/O	AD13	I/O	AF2	I/O
T14	GND/THERMAL	Y4	I/O	AB25	I/O	AD14	I/O	AF3	I/O
T15	GND/THERMAL	Y5	I/O	AB26	I/O	AD15	I/O	AF4	I/O
T16	GND/THERMAL	Y22	GND	AC1	I/O	AD16	I/O	AF5	I/O
T22	GND	Y23	I/O	AC2	I/O	AD17	I/O	AF6	I/O
T23	I/O	Y24	I/O	AC3	NC	AD18	I/O	AF7	I/O
T24	I/O	Y25	I/O	AC4	GND	AD19	I/O	AF8	I/O
T25	I/O	Y26	I/O	AC5	I/O	AD20	I/O	AF9	I/O
T26	I/O	AA1	I/O	AC6	NC	AD21	I/O	AF10	I/O
U1	I/O	AA2	I/O	AC7	I/O	AD22	I/O	AF11	I/O
U2	I/O	AA3	NC	AC8	I/O	AD23	TRSTB	AF12	I/O
U3	I/O	AA4	NC	AC9	NC	AD24	I/O	AF13	I/O
U4	I/O	AA5	VCC	AC10	I/O	AD25	I/O	AF14	I/O
U5	GND	AA22	VCC	AC11	I/O	AD26	I/O	AF15	I/O
U22	NC	AA23	NC	AC12	NC	AE1	TDI	AF16	I/O
U23	I/O	AA24	I/O	AC13	I/O	AE2	I/O	AF17	I/O
U24	I/O	AA25	I/O	AC14	VCCIO	AE3	I/O	AF18	I/O
U25	I/O	AA26	I/O	AC15	NC	AE4	I/O	AF19	I/O
U26	I/O	AB1	I/O	AC16	I/O	AE5	I/O	AF20	I/O
V1	I/O	AB2	I/O	AC17	I/O	AE6	I/O	AF21	I/O
V2	I/O	AB3	I/O	AC18	NC	AE7	I/O	AF22	I/O
V3	I/O	AB4	I/O	AC19	I/O	AE8	I/O	AF23	I/O
V4	NC	AB5	GND	AC20	I/O	AE9	I/O	AF24	I/O
V5	NC	AB6	VCC	AC21	I/O	AE10	I/O	AF25	I/O
V22	GND	AB7	NC	AC22	NC	AE11	I/O	AF26	I/O
V23	NC	AB8	NC	AC23	GND	AE12	I/O		
V24	I/O	AB9	NC	AC24	I/O	AE13	I/O		
V25	I/O	AB10	VCC	AC25	I/O	AE14	I/O		
V26	I/O	AB11	GND	AC26	I/O	AE15	I/O		

Package Mechanical Drawings

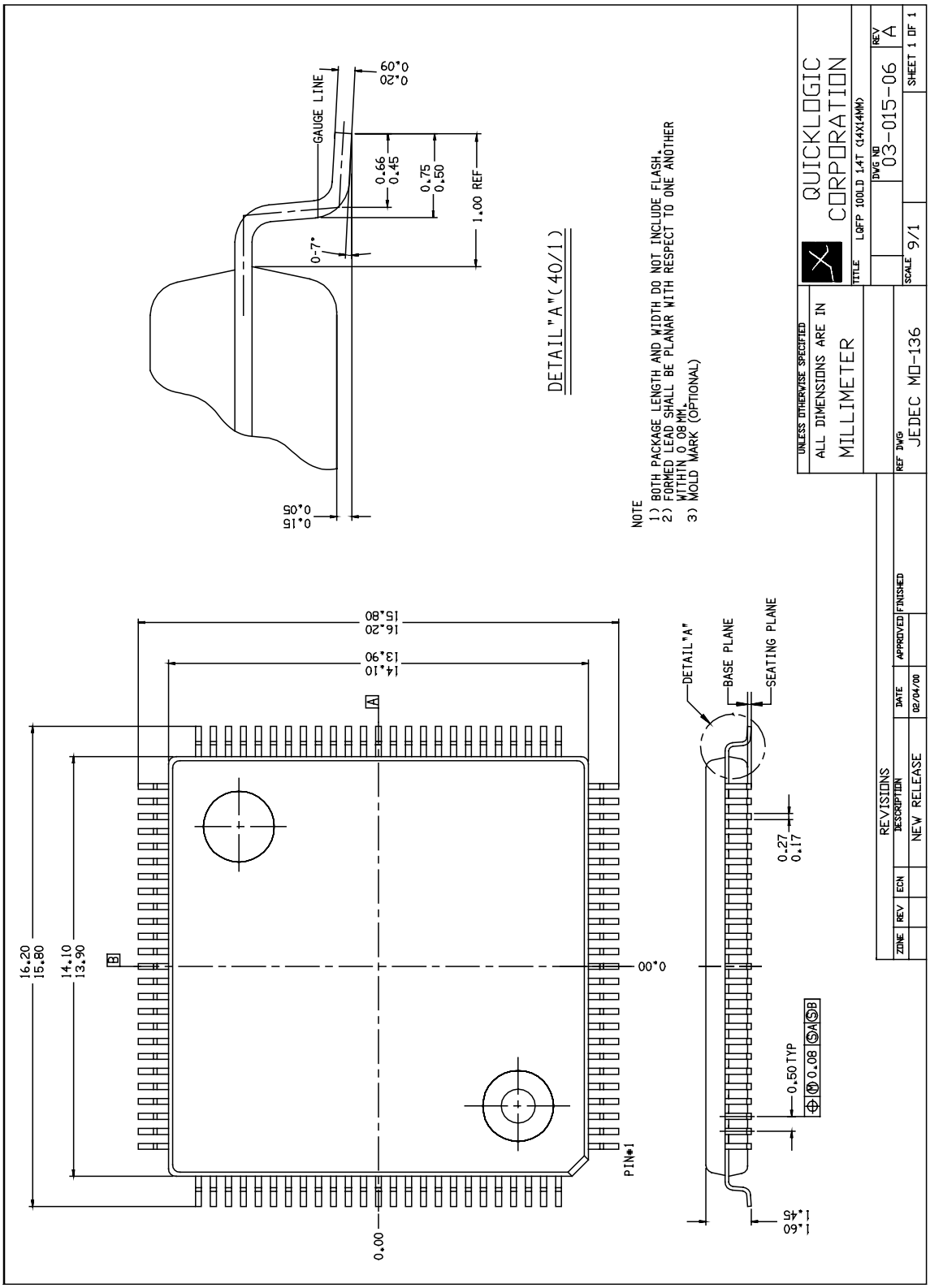
68 PLCC Packaging Drawing



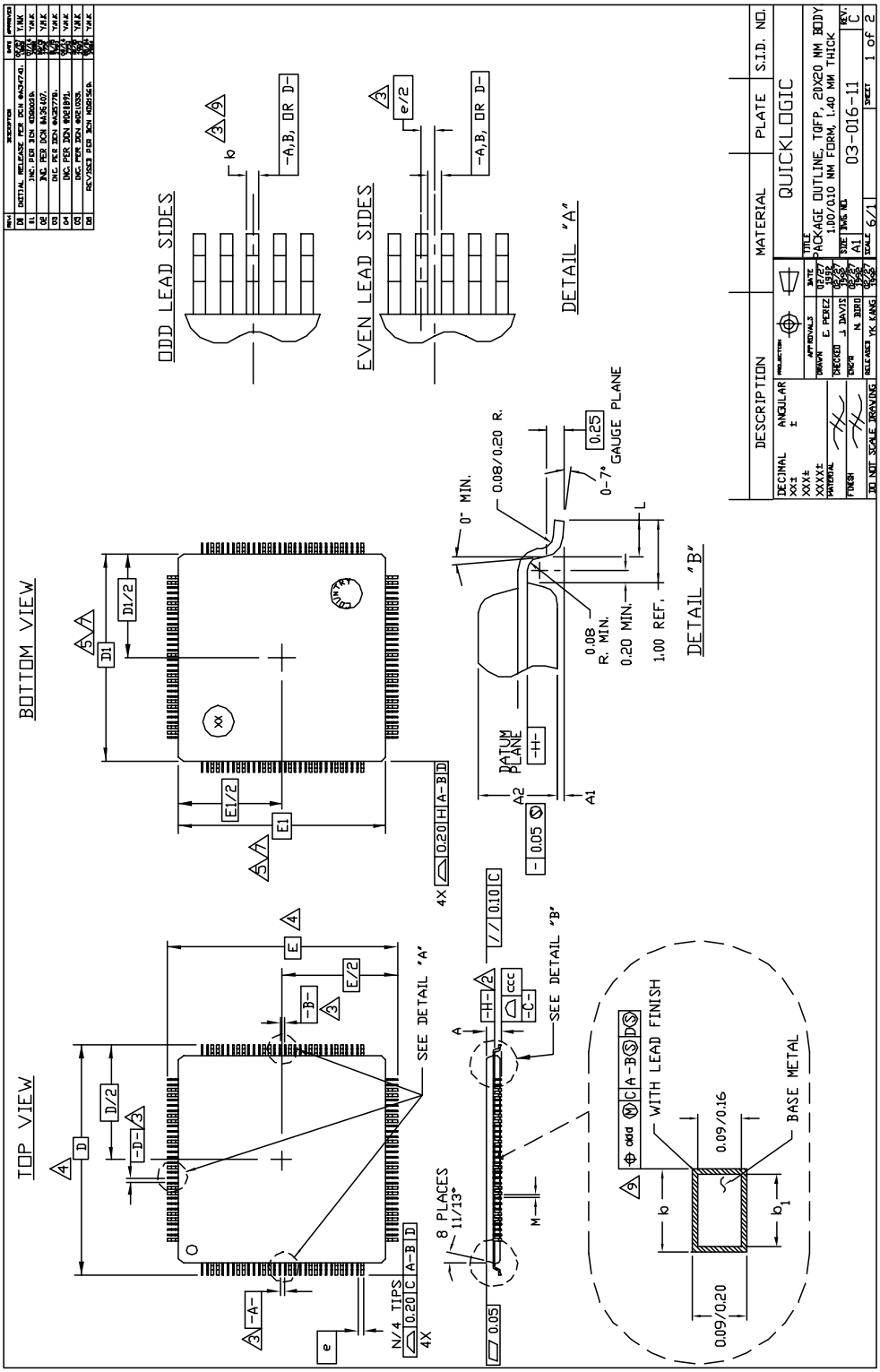
84 PLCC Packaging Drawing



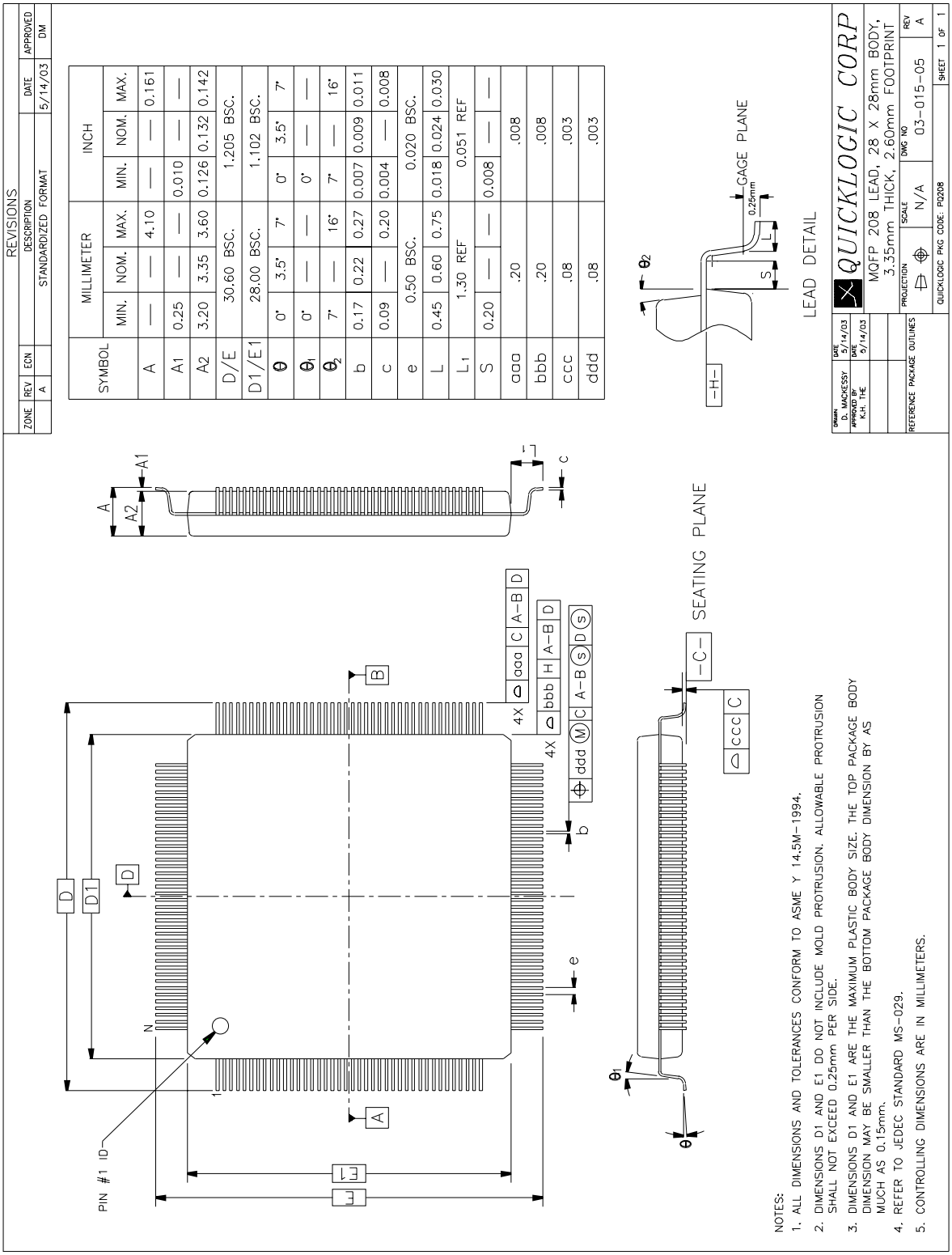
100 TQFP Mechanical Drawing



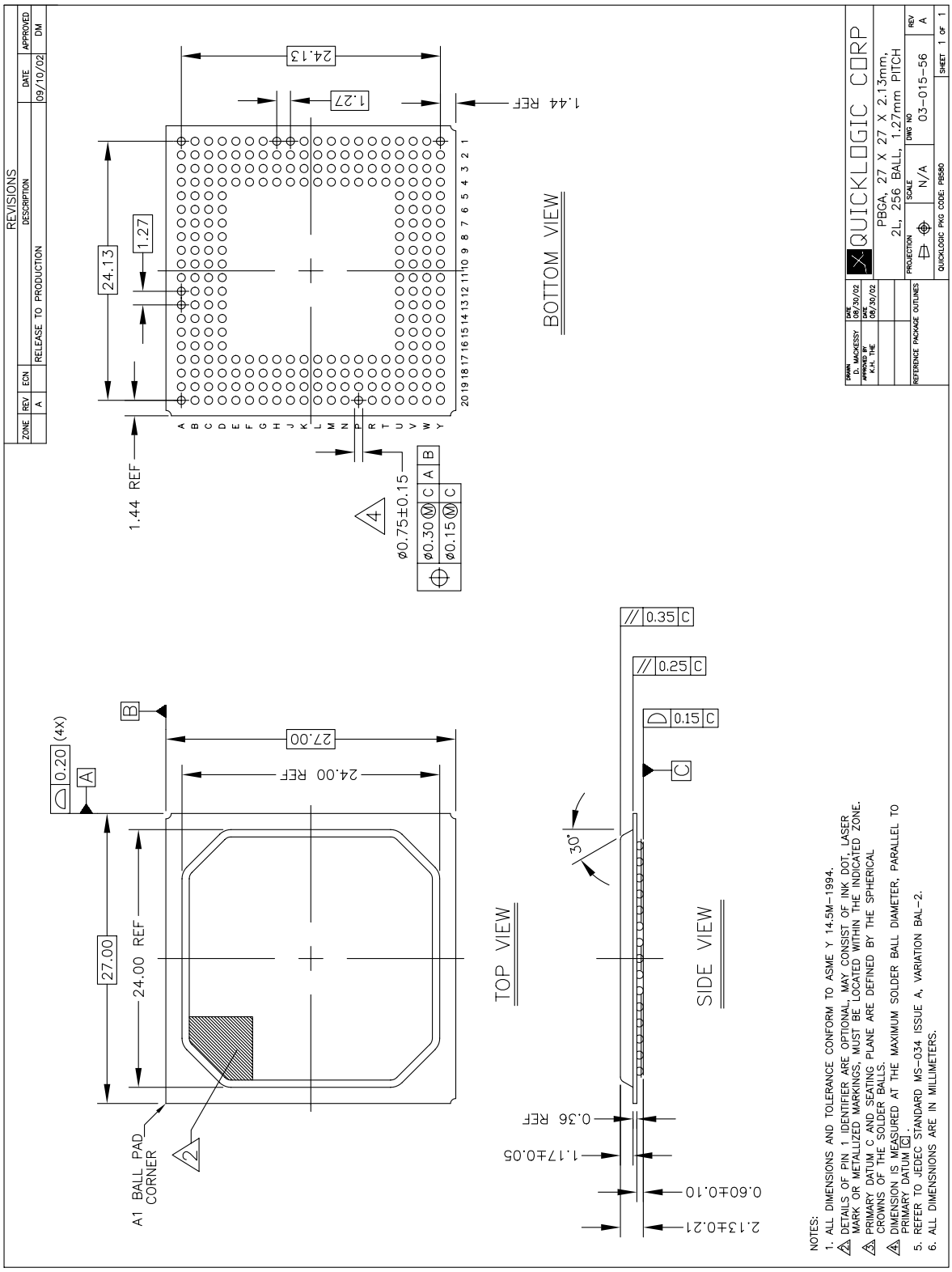
144 TQFP Mechanical Drawing



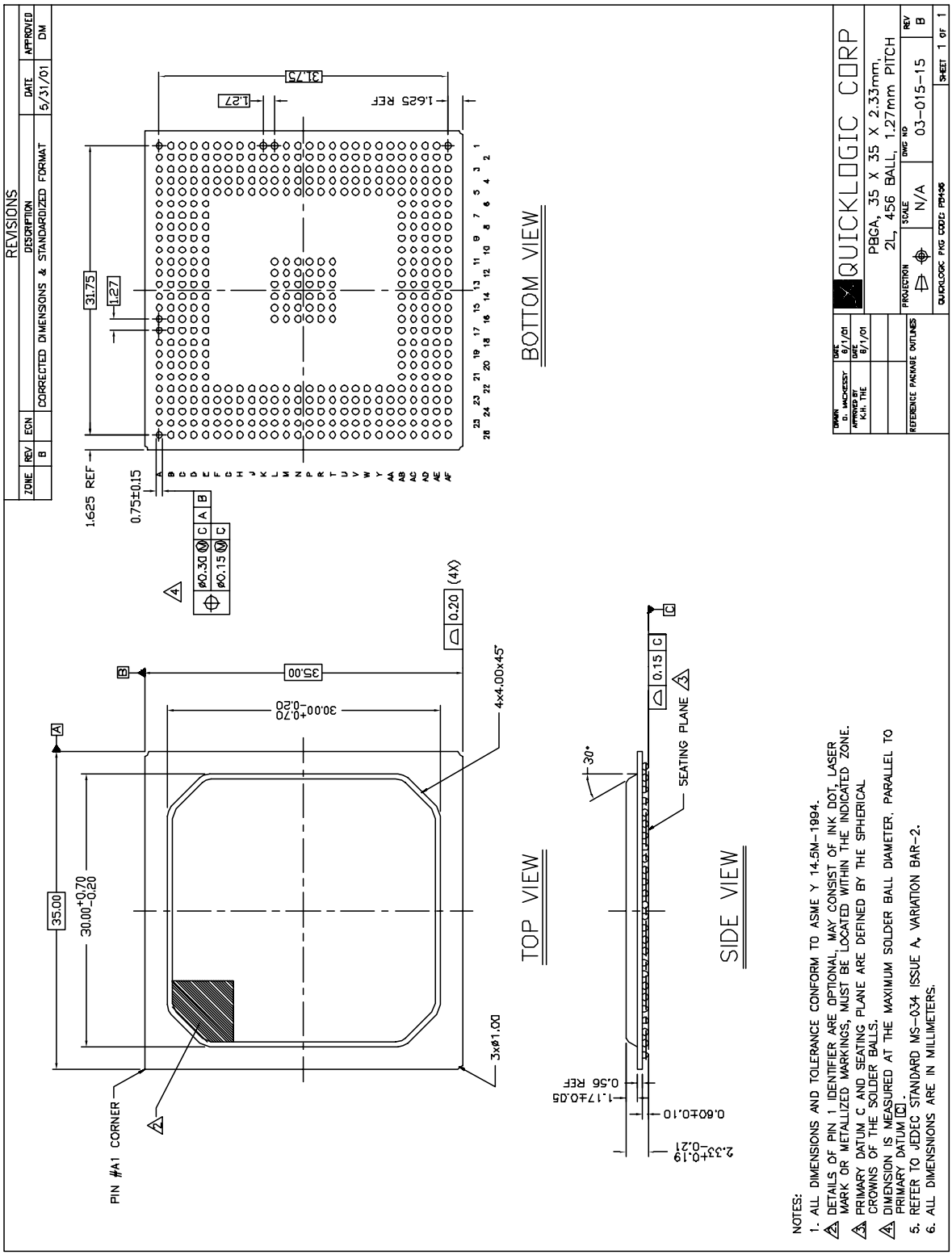
208 PQFP Packaging Drawing



256 PBGA Mechanical Drawing



456 PBGA Mechanical Drawing



Packaging Information

The pASIC 3 product family packaging information is presented in **Table 32**.

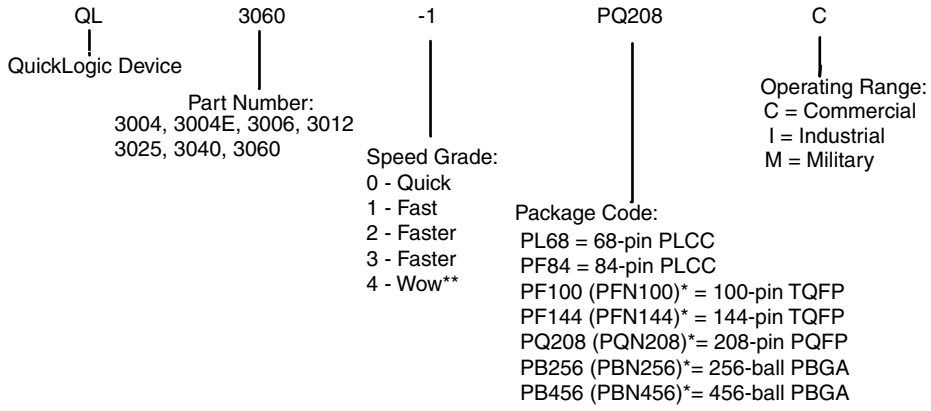
NOTE: Military temperature range plastic packages will be added as follow on products to the commercial and industrial products.

Table 32: Packaging Options

Device Information	Device													
	QL3004		QL3004E		QL3006		QL3012		QL3025		QL3040		QL3060	
	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pin	Pitch	Pin	Pitch	Pitch
Package Definitions[a]	68 PLCC	0.05 in.	68 PLCC	0.05 in.	68 PLCC	0.05 in.	84 PLCC	0.05 in.	100 TQFP	0.5 mm	208 PQFP	0.5 mm	208 PQFP	0.5 mm
	84 PLCC	0.05 in.	84 PLCC	0.05 in.	84 PLCC	0.05 in.	100 TQFP	0.5 mm	144 TQFP	0.5 mm	456 PBGA	1.27 mm	456 PBGA	1.27 mm
	100 TQFP	0.5 mm	100 TQFP	0.5 mm	100 TQFP	0.5 mm	144 TQFP	0.5 mm	208 PQFP	0.5 mm	-	-	-	-
	-	-	-	-	-	-	-	-	256 PBGA	1.27 mm	-	-	-	-

a. PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
PBGA = Plastic Ball Grid Array
TQFP = Thin Quad Flat Pack

Ordering Information



* Lead-free packaging is available, contact QuickLogic regarding availability (see Contact Information).
** Contact QuickLogic regarding availability (see Contact Information)

Contact Information

Phone: (408) 990-4000 (US)
(905) 940-4149 (Canada)
+(44) 1932 57 9011 (Europe – except Germany/Benelux)
+(49) 89 930 86 170 (Germany/Benelux)
+(86) 21 6867 0273 (Asia – except Japan)
+(81) 45 470 5525 (Japan)
E-mail: info@quicklogic.com
Sales: www.quicklogic.com/sales
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Comments
A	Not avail.	First Release
B	June 2002	Brian Faith and Andreea Rotaru
C	March 2005	Mehul Kochar and Kathleen Murchek
D	September 2005	Mehul Kochar and Kathleen Murchek Added lead free packaging information to Ordering Information section.

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