



High Speed CMOS QuickSwitch® 16 to 8 Multiplexer

QS3390
QS32390

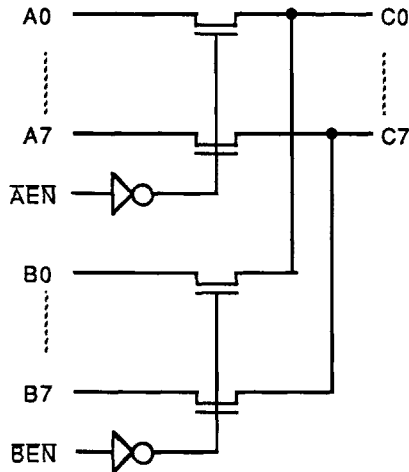
FEATURES/BENEFITS

- 16:8 multiplexer function with zero delay
- 5Ω switches connect inputs to outputs
- Zero propagation delay
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- Direct connection for mux, demux
- 32390 is 25Ω version for low noise
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 28-pin QSOP

DESCRIPTION

The QS3390 and 32390 each provide a 16 to 8 multiplexer logic switch. The low on resistance (5Ω) of the 3390 allows inputs to be connected to the output without adding propagation delay and without generating additional ground bounce noise. The 32390 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The select and enable inputs select and connect one of 8 inputs to the common I/O pin, respectively. The multiplexer function can be used to select and route logic signals for zero delay, isolate bus capacitance, form crossbar switches, etc.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
A0-7	I/O	Bus A
B0-7	I/O	Bus B
C0-7	I/O	Bus C
\overline{AEN} \overline{BEN}	I	Bus Switch Enable

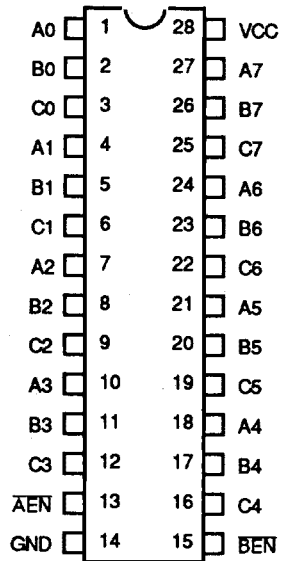
FUNCTION TABLE

\overline{AEN}	\overline{BEN}	A Sw	B Sw	Function
H	H	Off	Off	Disconnect
L	H	On	Off	A to AB
H	L	Off	On	B to AB
L	L	On	On	A, B to AB

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PIN CONFIGURATIONS

QSOP



ALL PINS TOP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
 DC Switch Voltage V_S -0.5V to $V_{CC} + 0.5V$
 DC Input Voltage V_I -0.5V to $V_{CC} + 0.5V$
 AC Input Voltage (for a pulse width ≤ 20 ns)..... -3.0V
 DC Input Diode Current with $V_I < 0$ -20 mA
 DC Output Current Max. sink current/pin..... 120 mA
 Maximum Power Dissipation..... 0.5 watts
 T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1$ MHz, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	QSOP	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0 V$	3	pF
Cin	A/B/C I/O Capacitance	$V_{in} = 0 V$	7	pF

Capacitance is guaranteed but not tested

QS3390, QS32390 Advanced Information

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

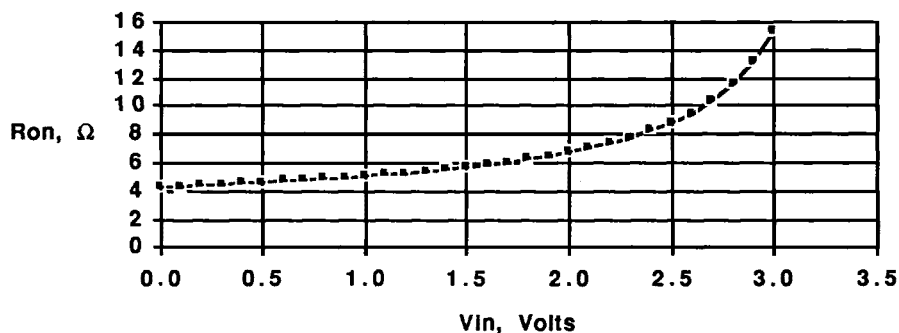
Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test	Min	Typ	Max	Unit	
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts	
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts	
iin	Input Leakage Current	0 ≤ Vin ≤ Vcc	-	-	5	μA	
ioz	Off State Current (Hi-Z)	0 ≤ A, B, AB ≤ Vcc	-	.001	5	μA	
ios	Short Circuit Current (2)	A,B (AB) = 0V, AB (A,B) = Vcc		300	-	mA	
Vic	Clamp Diode Voltage	Vcc = Min, iin = -18 mA	-	-0.7	-1.2	Volts	
Ron	Switch On Resistance (Notes: 3,4)	Vcc = Min, Vin = 0.0 Volts I _{on} = 30 mA	3390	-	5	7	Ω
			32390	20	28	40	Ω
		Vcc = Min, Vin = 2.4 Volts I _{on} = 15 mA	3390	-	10	15	Ω
			32390	20	35	48	Ω

Notes:

1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between A or B pins to AB pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.
4. 32390 Ron is a preliminary specification.

On Resistance vs Vin @ 4.75 Vcc (3390 Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, V _i = GND or V _{cc} , f = 0	-	-	5.0	mA
ΔI _{cc}	Pwr Supply Current, per Input High (2)	V _{cc} = MAX, Input = 3.4 V, f = 0 Per control input	-	-	3.5	mA
Q _{ccd}	Dynamic Pwr Supply Current per mHz (3)	V _{cc} = MAX, A, B, AB pins open, Control input toggling @ 50% duty cycle	-	-	.50	mA/ MHz
I _c	Total Power Supply Current (4,5)	V _{cc} = MAX, A, B, AB pins at 0.0V, Control inputs toggling @ 50% duty cycle V _{ih} = 3.4V, f clock = 10 MHz	-	-	11.8	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input (V_i=3.4V, control inputs only). A, B and AB pins do not contribute to I_{cc}.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, & AB I/Os generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_c = I_{\text{Quiescent}} + I_{\text{Inputs}} + I_{\text{Dynamic}}$
 $I_c = I_{cc} + \Delta I_{cc} Dh Nt + Q_{ccd} (f_i N_i)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for each TTL High input (V_i=3.4V, control inputs only)
 Dh = Duty Cycle for each TTL input that is High (control inputs only).
 Nt = Number of TTL inputs that are at DH (control inputs only).
 f_i = frequency that the inputs are toggled (control inputs only).
- Note that activity on A, B, or AB I/Os do not contribute to I_c if A, B, or AB I/Os are between gnd and V_{cc}. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_c will be equal to I_{cc} only regardless of activity on the A, B, or AB I/Os.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit	
			Min	Max	Min	Max		
† PLH † PHL	Data Propagation Delay A,B to/from AB	3390	2,3		0.25		0.25	ns
		32390	2,3,6		1.25		1.25	ns
† PZH † PZL	Switch Turn On Delay AEN/BEN to A,B, AB	3390	1	0.5	6.5	0.5	7.5	ns
		32390	1,6	0.5	7.5	0.5	8.5	ns
† PLZ † PHZ	Switch Turn Off Delay AEN/BEN to A,B, ABY	3390	1,2	0.5	5.5	0.5	6.5	ns
		32390	1,2,6					
Qcd	Charge Injection, Typical	3390	4,5		1.5		1.5	pC
		32390	4,6,6					

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pf load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A/B to AB, load = 50 pF in parallel with 10 meg scope probe, Vin at AEN/BEN = 0.0 volts.
- 5) Characterized parameter. Not 100% tested.
- 6) Preliminary data, subject to change.