



QPA2040D

20 – 40 GHz 2 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA2040D is a Ka-band power amplifier fabricated on Qorvo's 0.15um GaN on SiC process (QGaN15). Operating between 20 and 40 GHz, it achieves saturated output power of 2 W with power-added efficiency of 13%.

To simplify system integration, the QPA2040D is fully matched to 50 ohms with integrated DC blocking caps on both RF I/O ports. The RF input is DC blocked, and the RF output is a DC short.

The QPA2040D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.

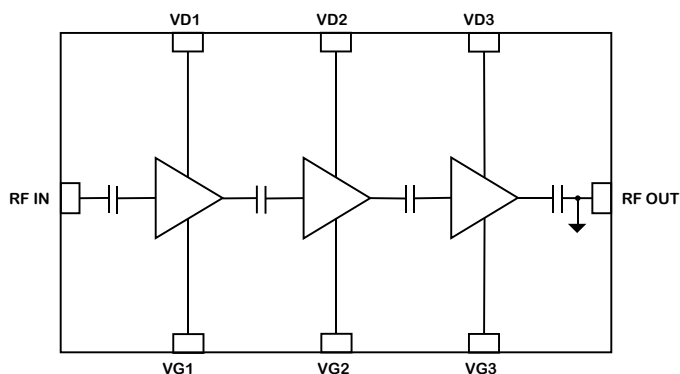


Key Features

- Frequency Range: 20 – 40 GHz
- P_{SAT} ($P_{IN}=21$ dBm): 33.5 dBm
- PAE ($P_{IN}=21$ dBm): 13 %
- Power Gain ($P_{IN}=21$ dBm): 12.5 dB
- Small Signal Gain: 24.3 dB
- Bias: $V_D = 18$ V, $I_{DQ} = 462$ mA
- Die Dimensions: 2.692 x 1.882 x 0.050 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Communications
- Radar
- Point-to-Point Radio
- Electronic Warfare

Ordering Information

Part No.	Description
QPA2040D	20–40 GHz 2 Watt GaN Amplifier
QPA2040DEVB01	Evaluation Board for QPA2040D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	–5 V to 0 V
Drain Current (I_{D1})	160 mA
Drain Current (I_{D2})	300 mA
Drain Current (I_{D3})	590 mA
Gate Current (I_G)	See plot pg. 18
Power Dissipation (P_{DISS}), 85 °C	17
Input Power (P_{IN}), 50 Ω , $V_D=18$ V, $I_{DQ} = 462$ mA, 85 °C	27 dBm
Input Power (P_{IN}), 3:1 VSWR, $V_D=18$ V, $I_{DQ} = 462$ mA, 85 °C	27 dBm
Soldering Temperature (30 s max.)	320 °C
Storage Temperature	–55 to +150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	18 V
Drain Current (I_{DQ})	462 mA
Operating Temperature	–40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

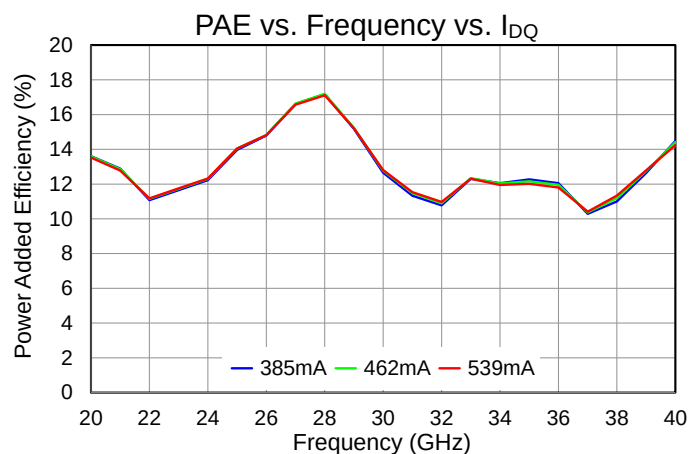
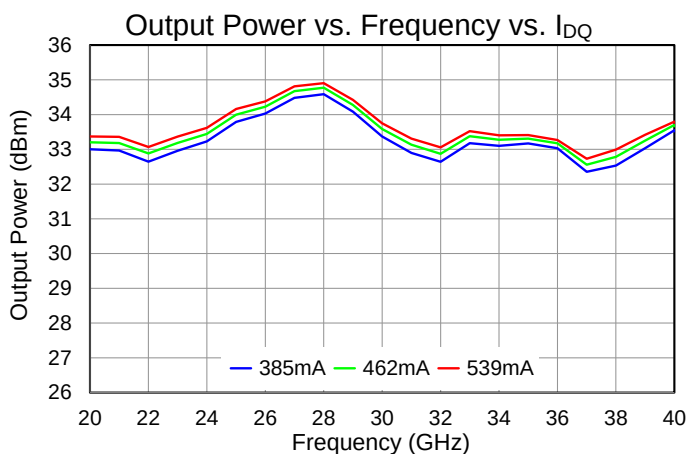
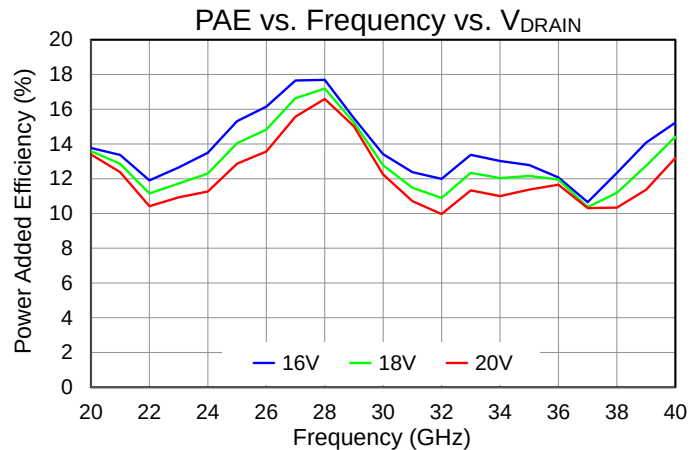
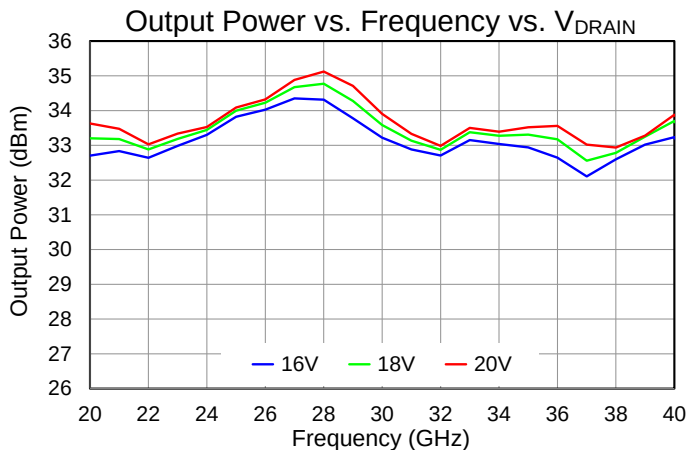
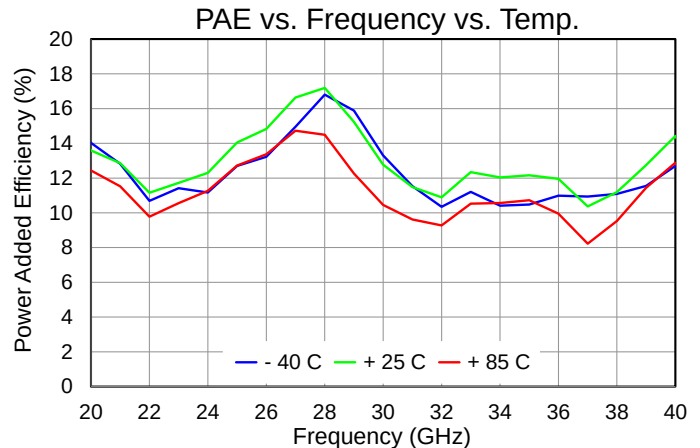
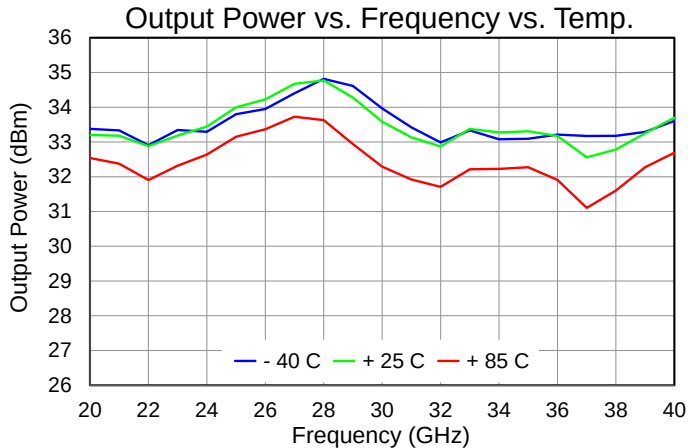
Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency	20		40	GHz
Output Power ($P_{IN}=21$ dBm)		33.5		dBm
Power Added Efficiency ($P_{IN}=21$ dBm)		13.0		%
Small Signal Gain		24.3		dB
Input Return Loss		14		dB
Output Return Loss		9		dB
P_{OUT} Temp. Coeff. (85 °C to –40 °C, $P_{IN} = 21$ dBm)		–0.009		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 °C to –40 °C)		–0.073		dB/°C

Test conditions, unless otherwise noted: $T = +25$ °C, $V_D = 18$ V, $I_{DQ} = 462$ mA

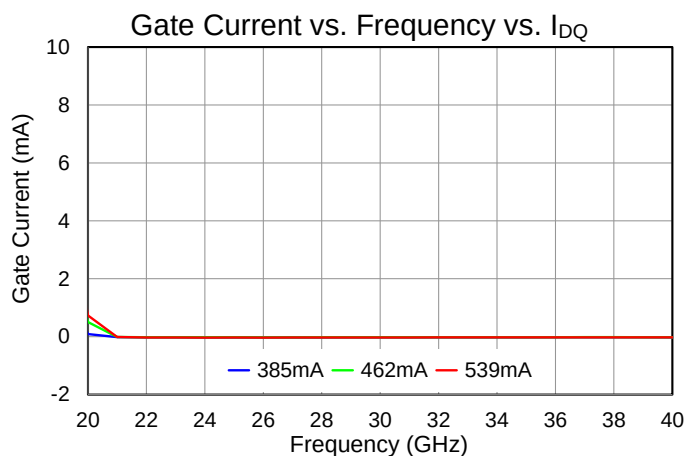
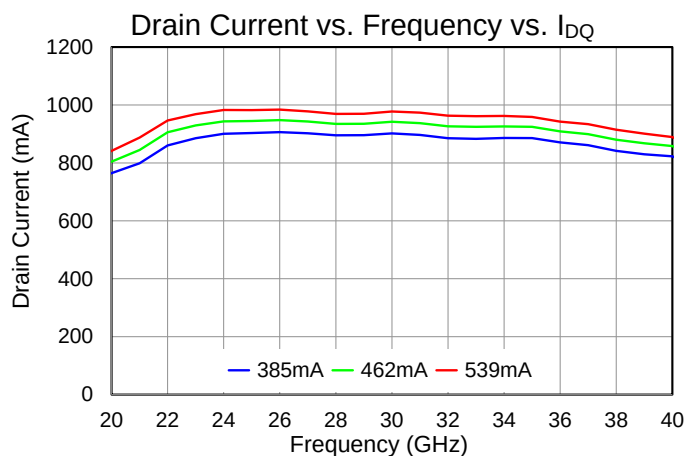
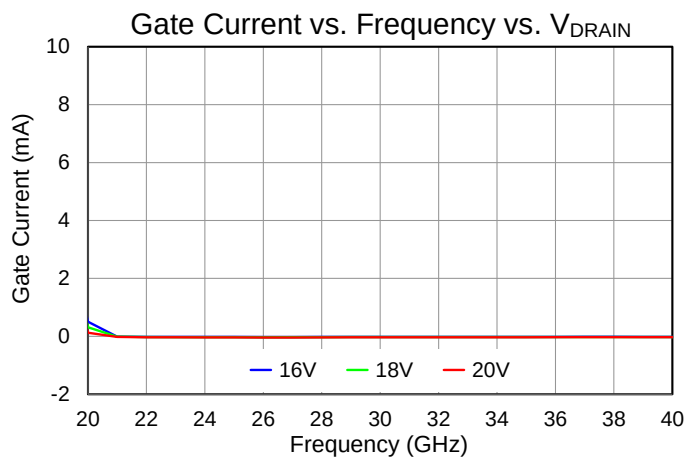
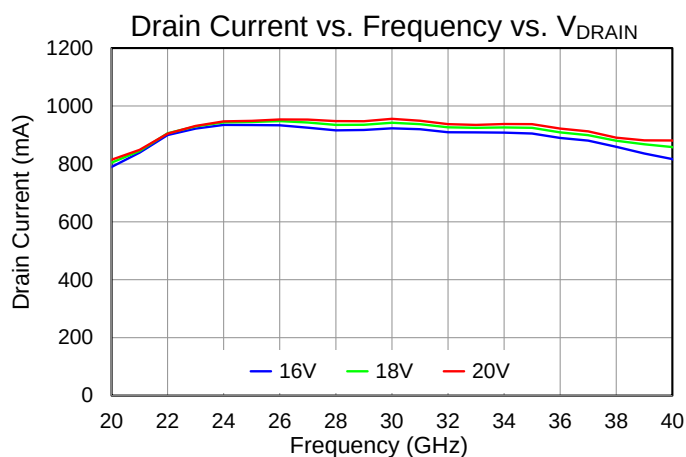
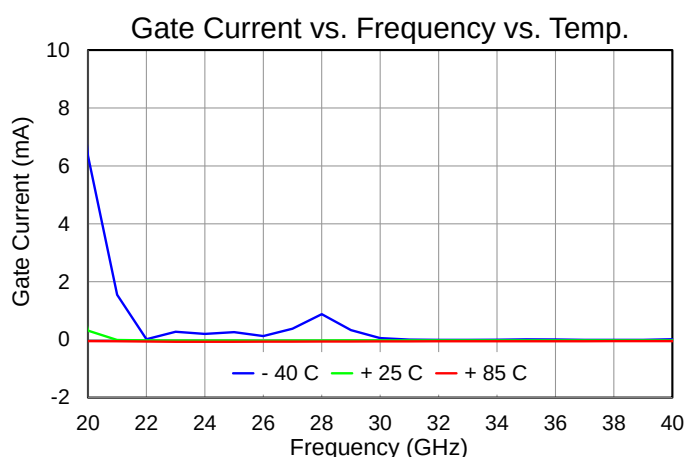
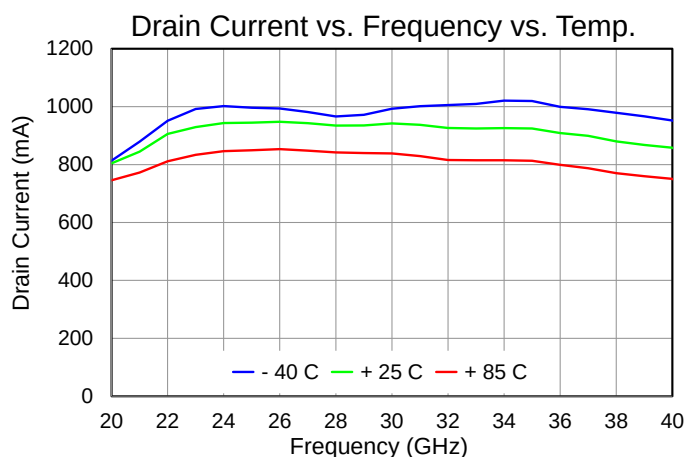
Performance Plots – Large Signal

Test conditions, unless otherwise noted: $V_D = 18\text{ V}$, $I_{DQ} = 462\text{ mA}$, $T = +25^\circ\text{C}$, $PIN = 21\text{ dBm}$



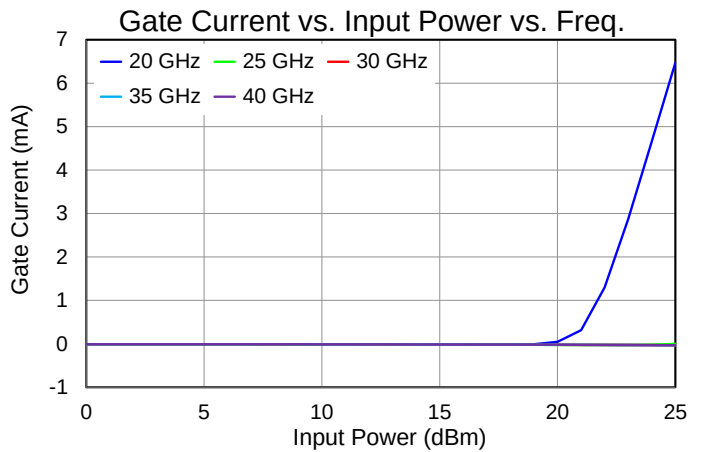
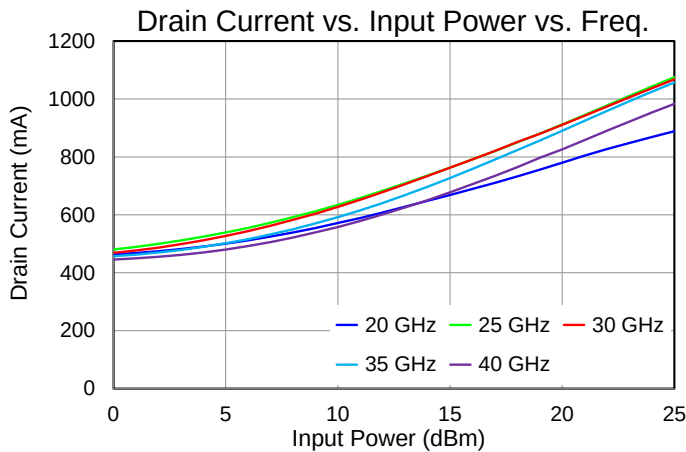
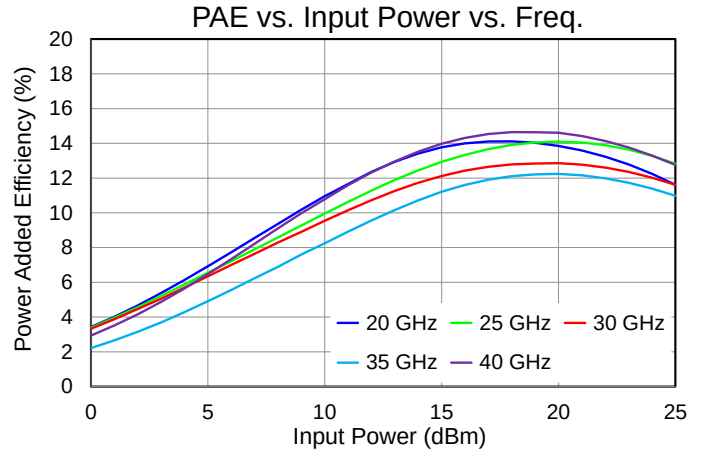
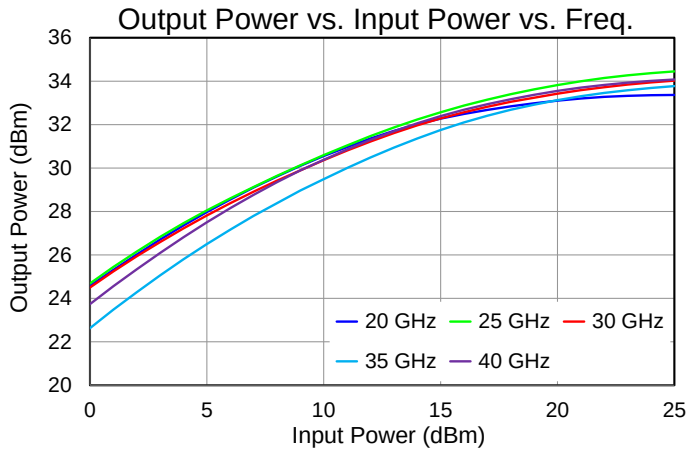
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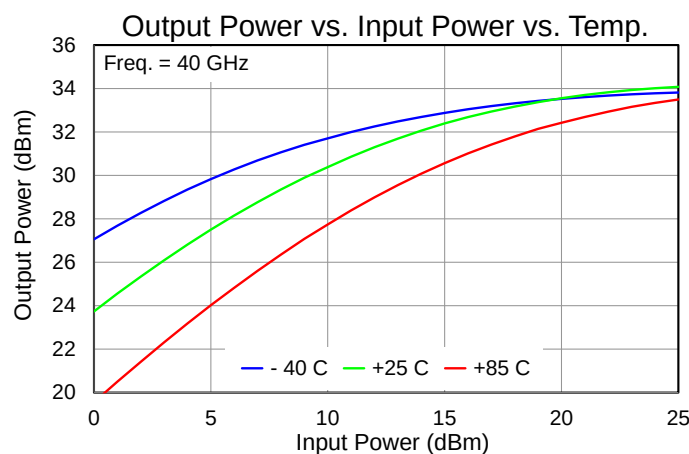
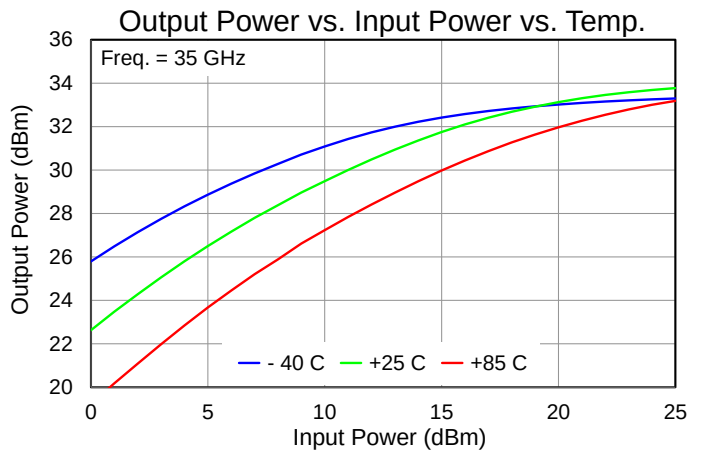
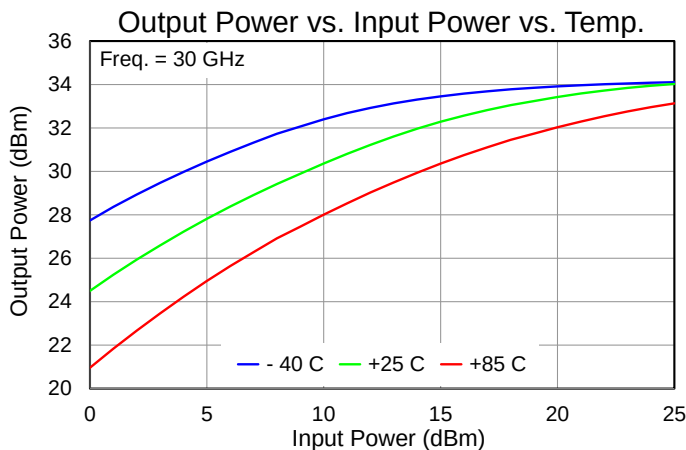
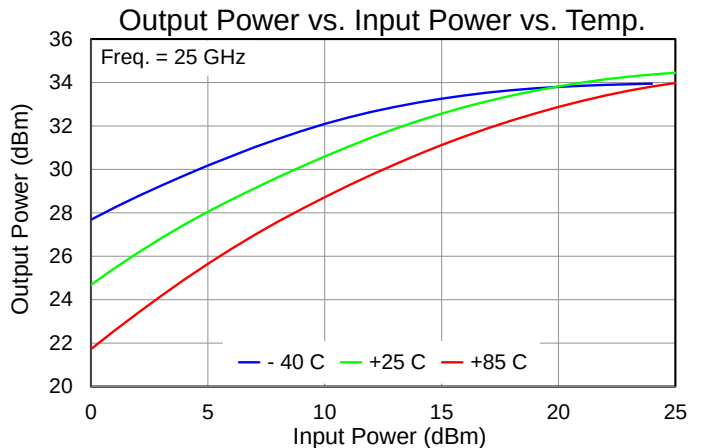
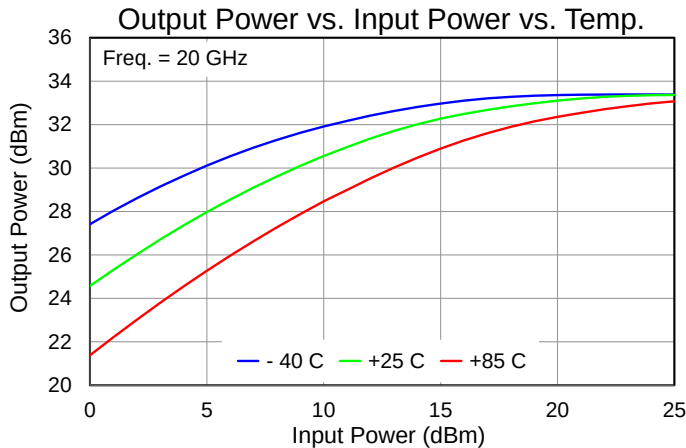
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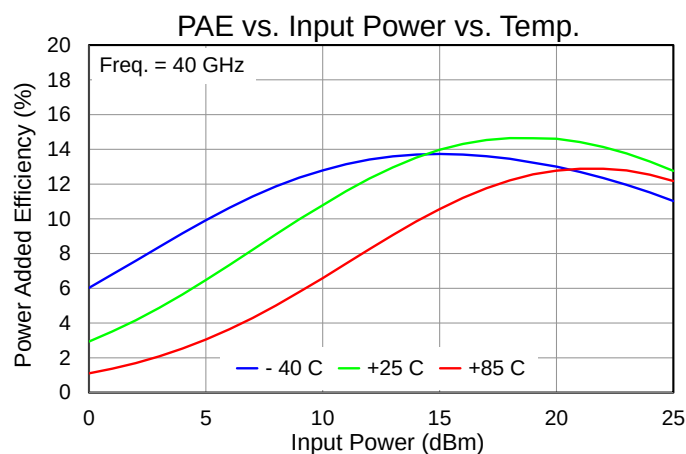
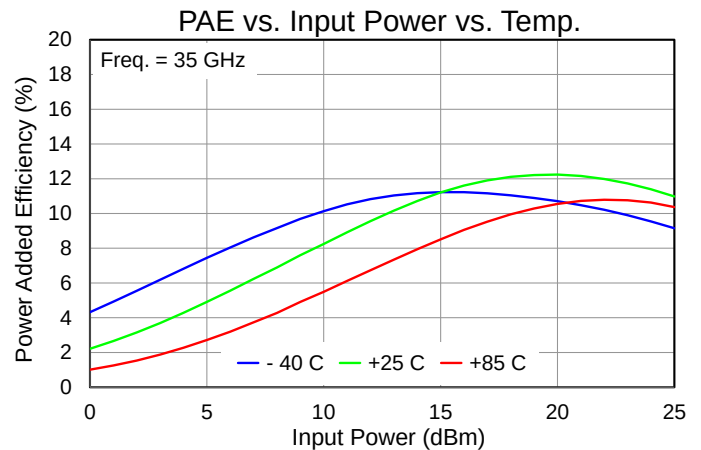
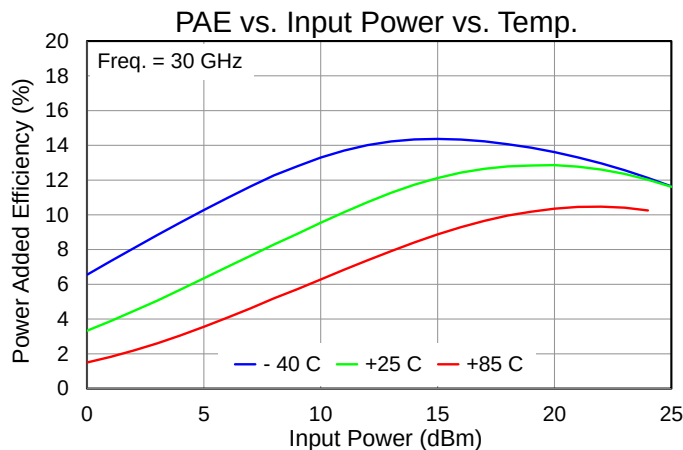
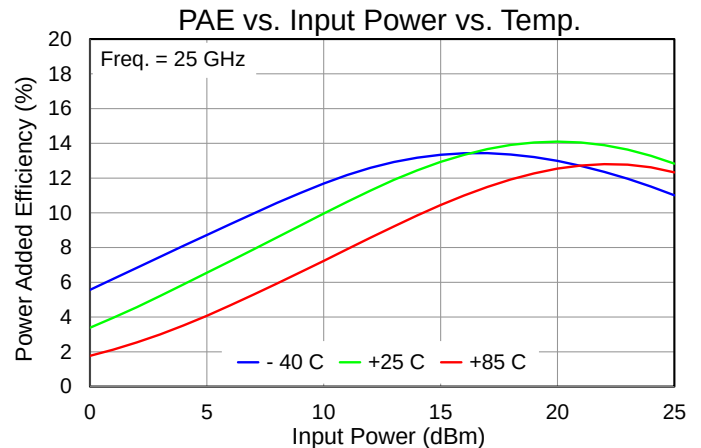
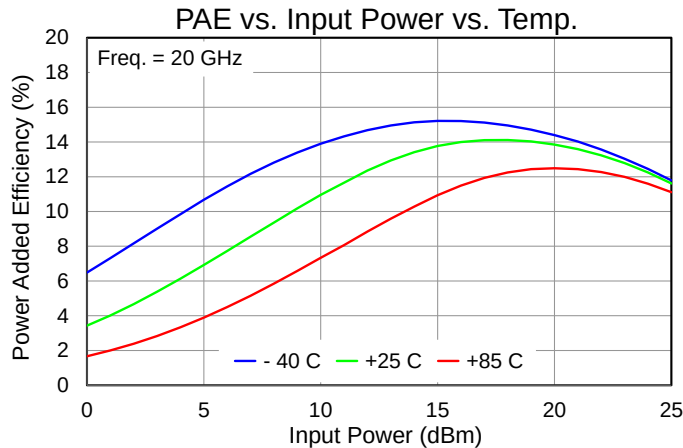
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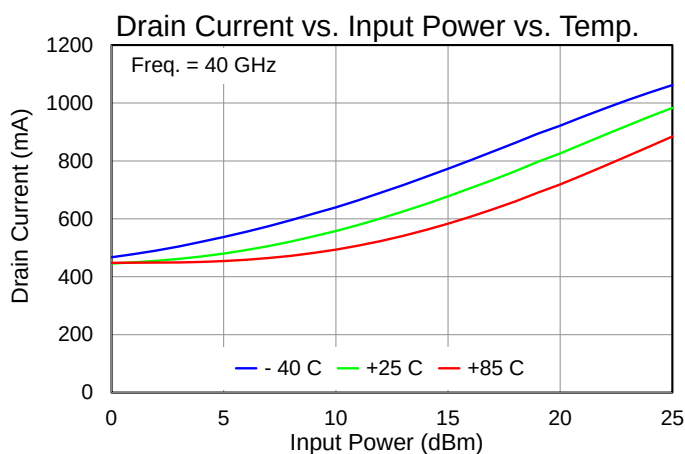
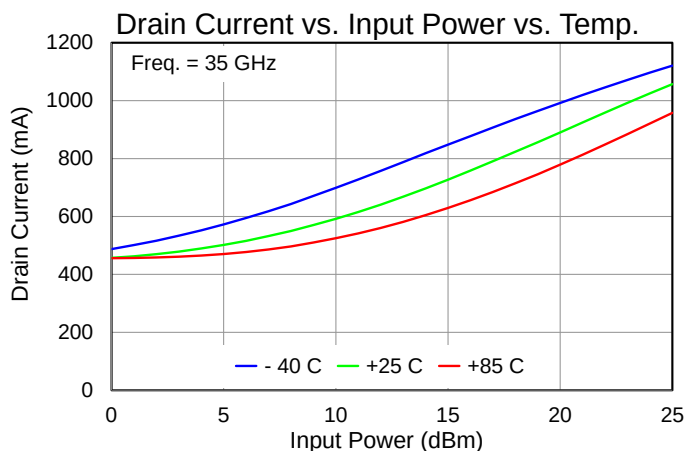
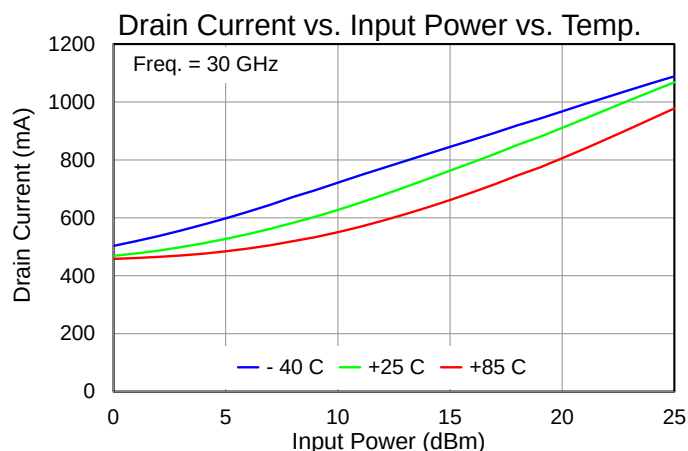
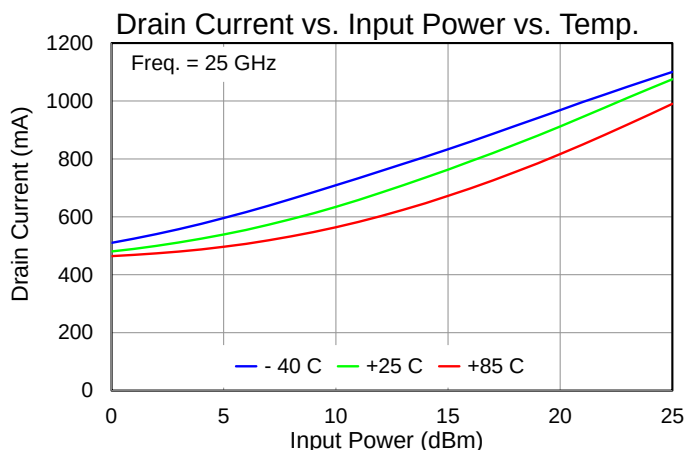
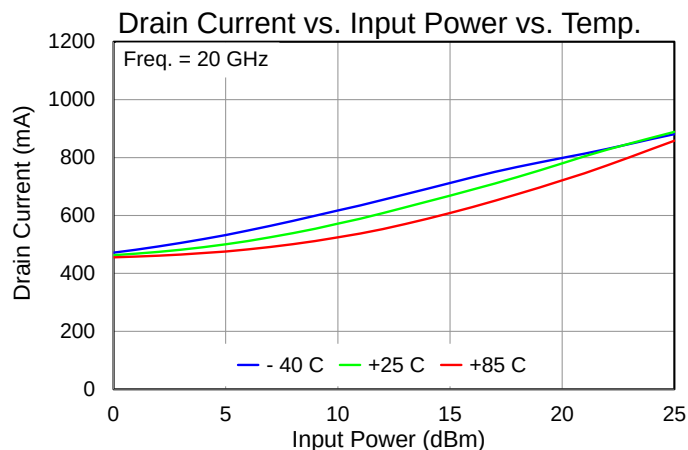
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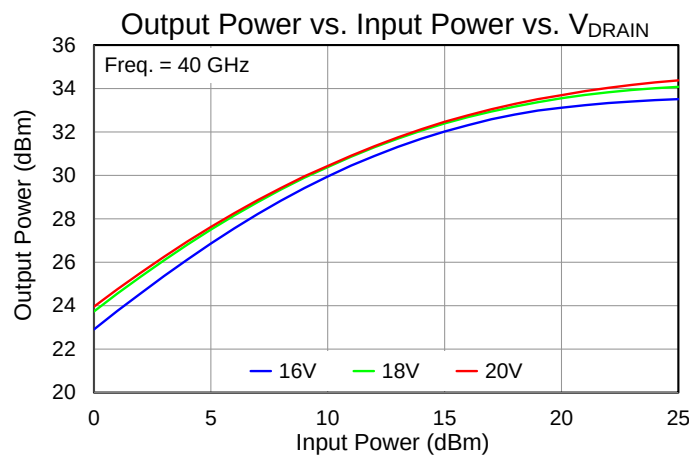
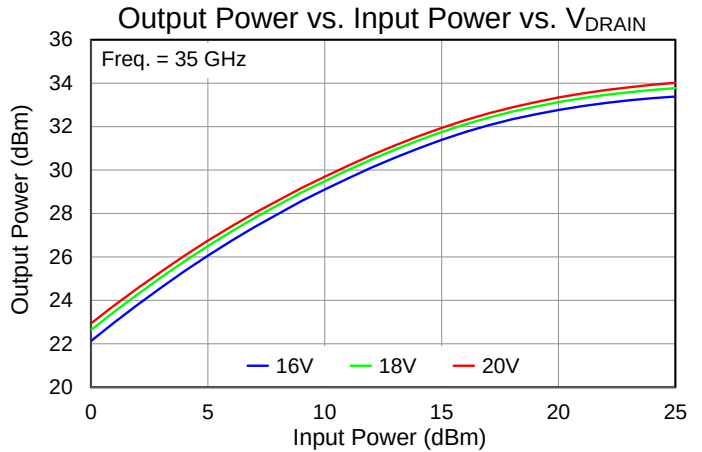
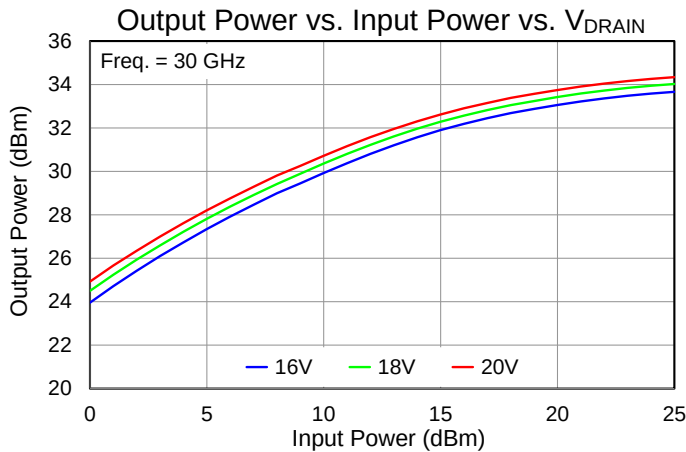
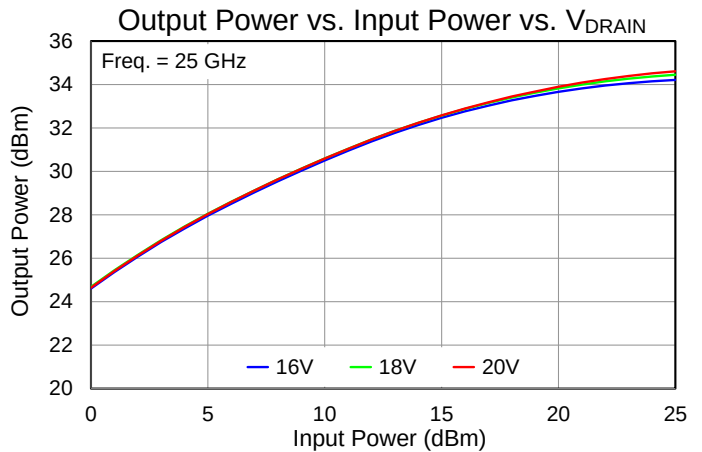
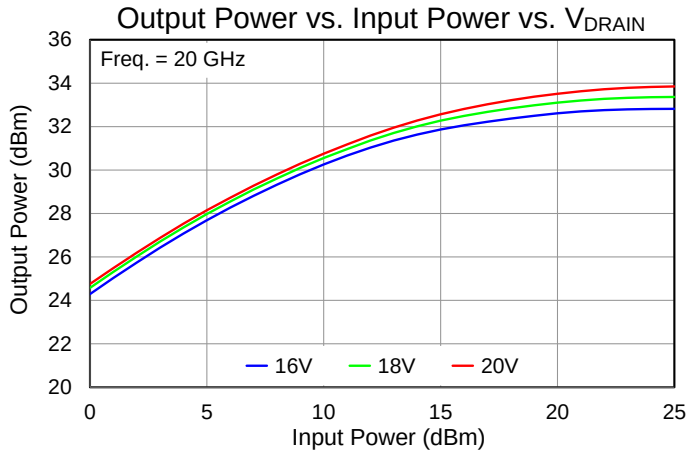
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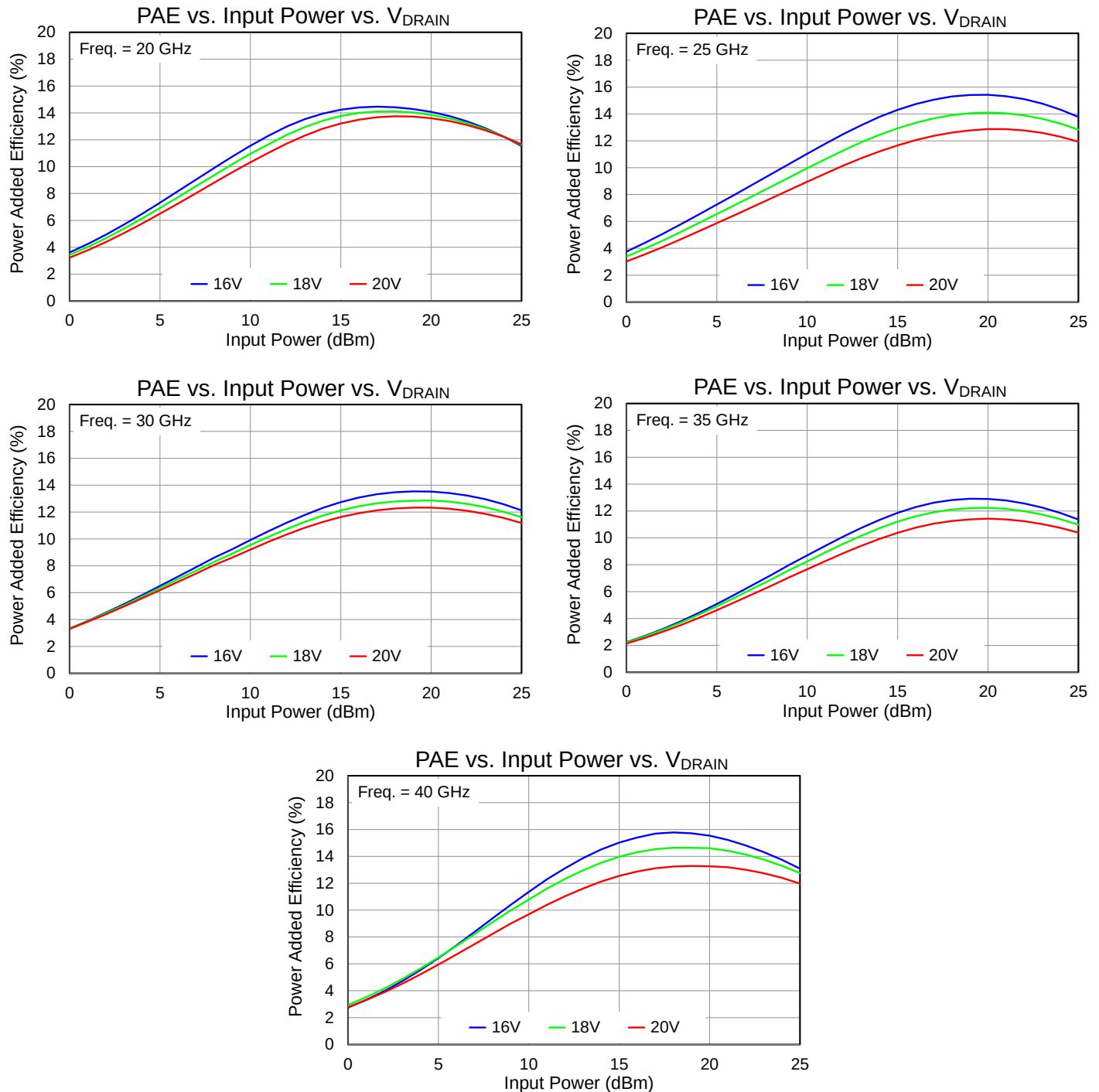
Performance Plots – Large Signal

Test conditions, unless otherwise noted: IDQ = 462 mA, T = +25 °C



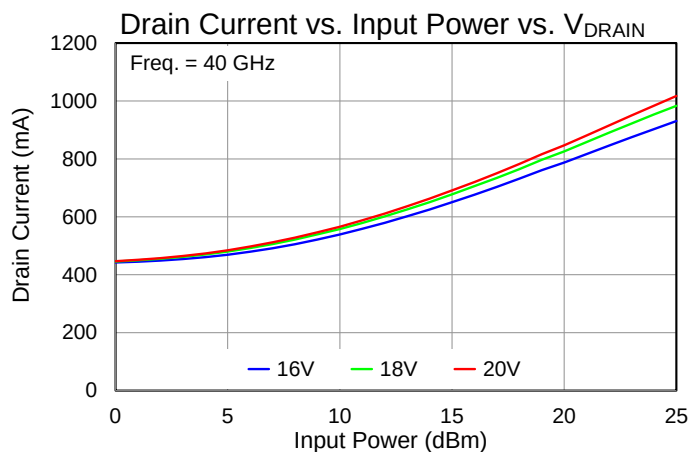
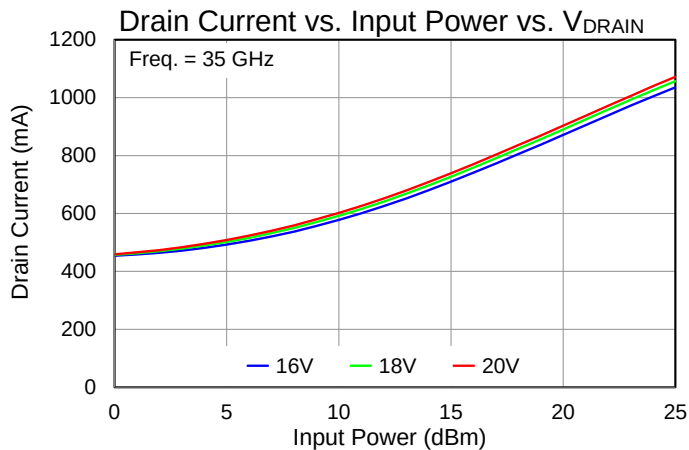
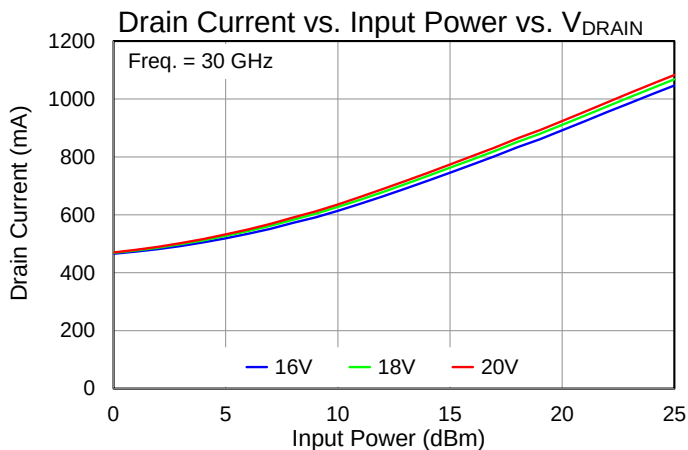
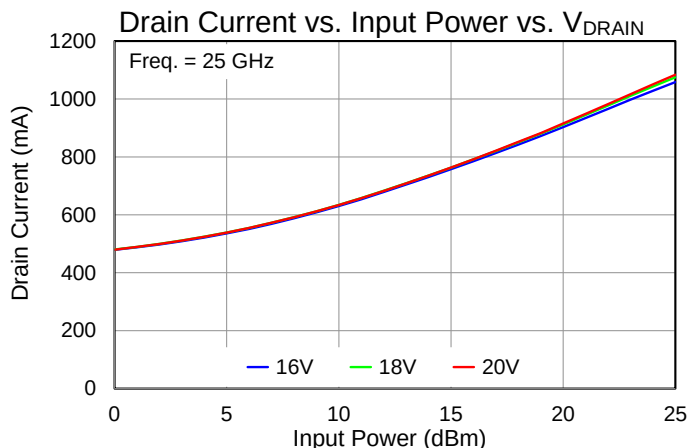
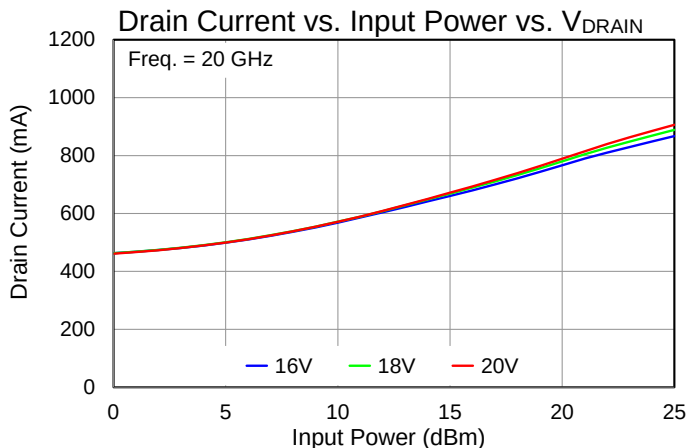
Performance Plots – Large Signal

Test conditions, unless otherwise noted: IDQ = 462 mA, T = +25 °C



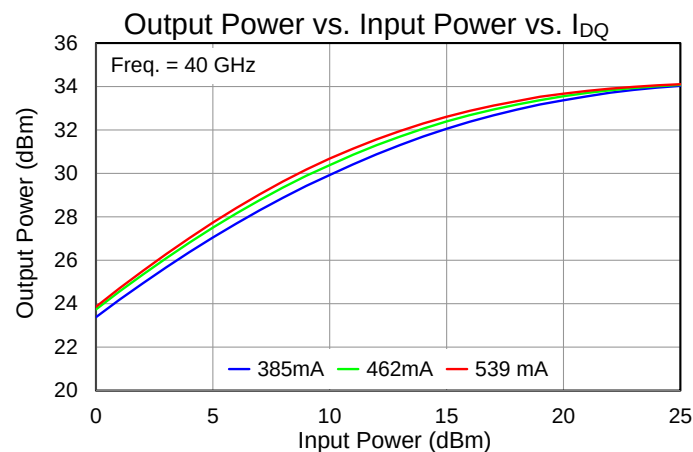
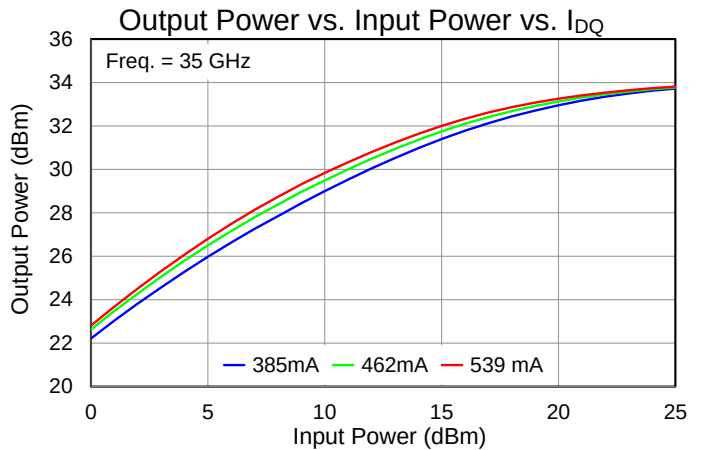
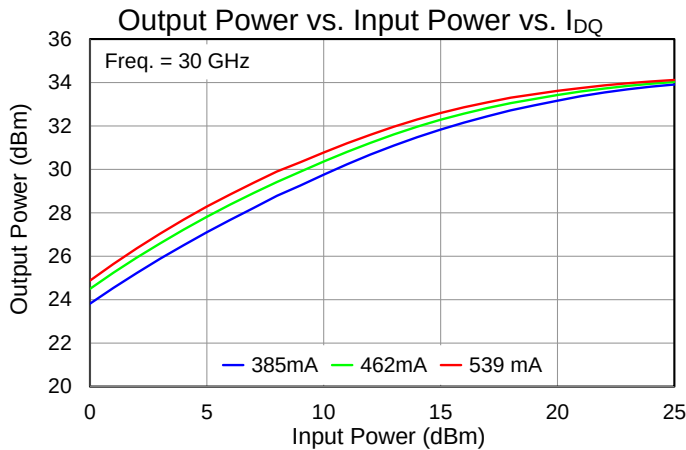
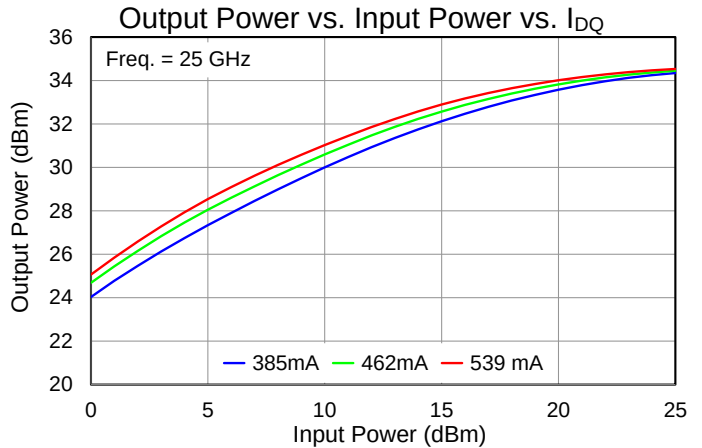
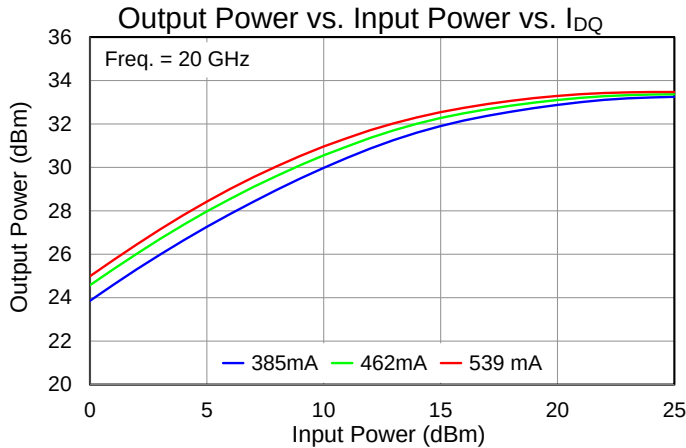
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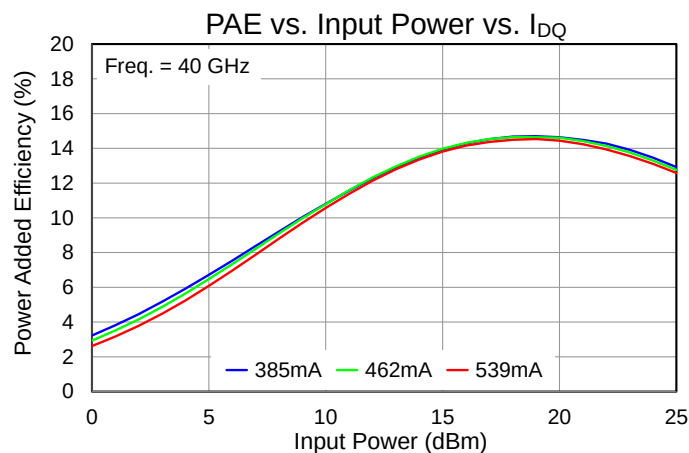
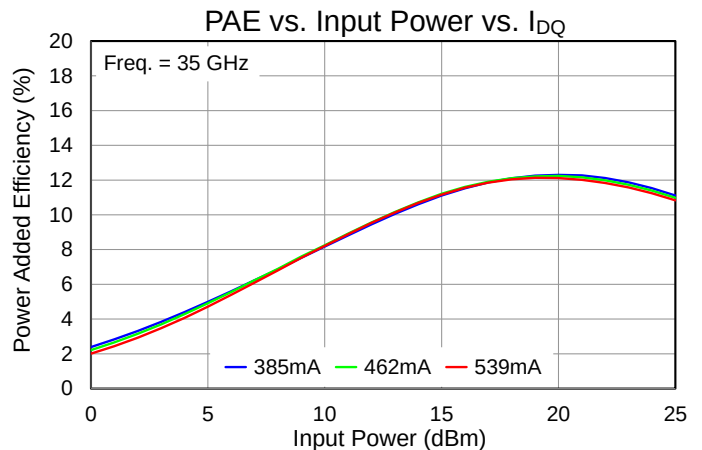
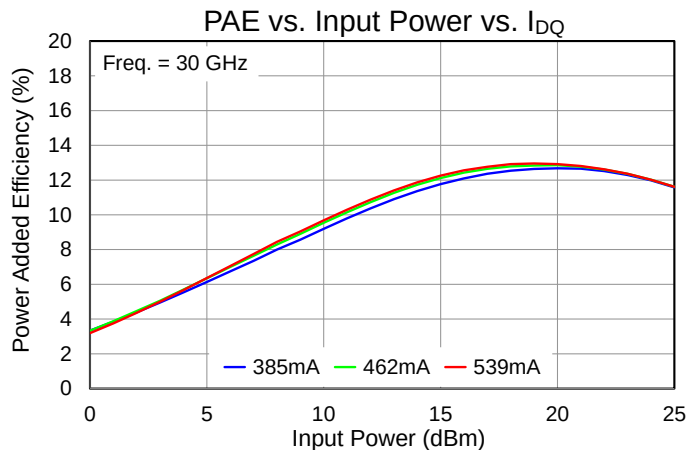
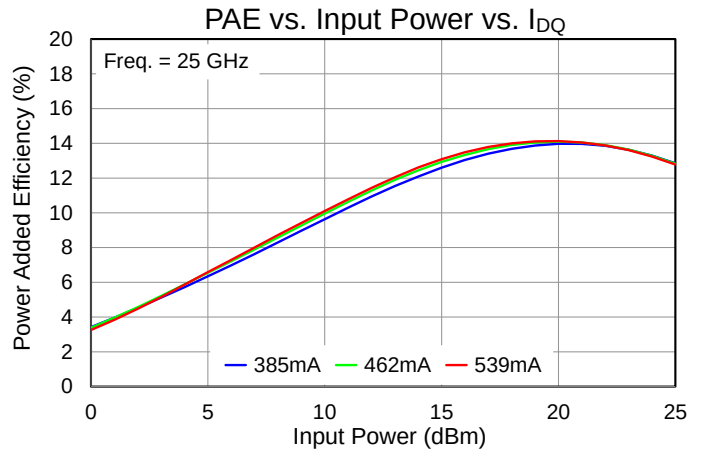
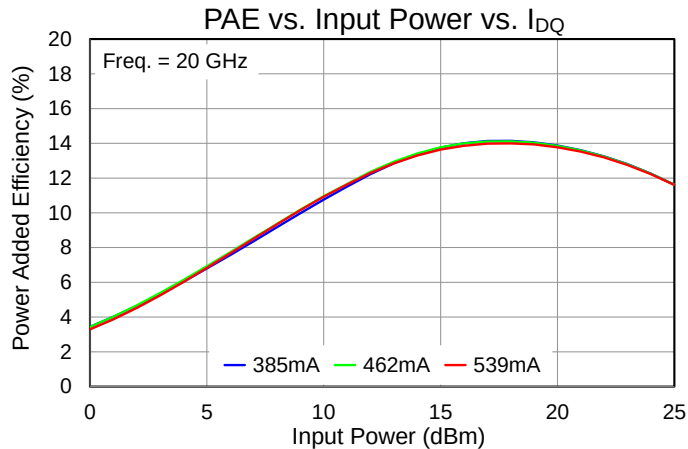
Performance Plots – Large Signal

Test conditions, unless otherwise noted: $V_D = 18\text{ V}$, $T = +25\text{ }^\circ\text{C}$



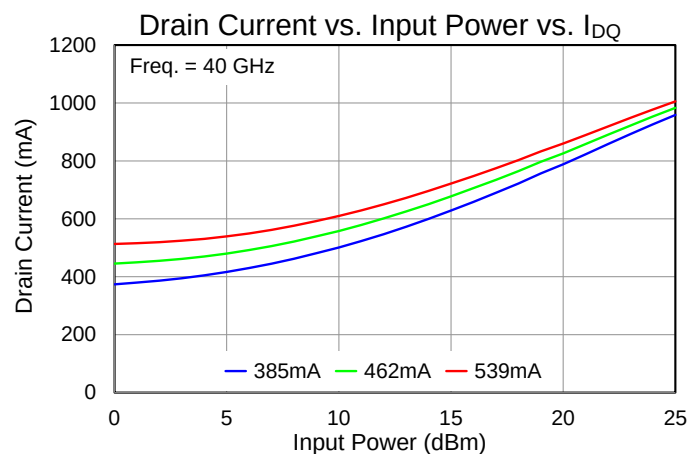
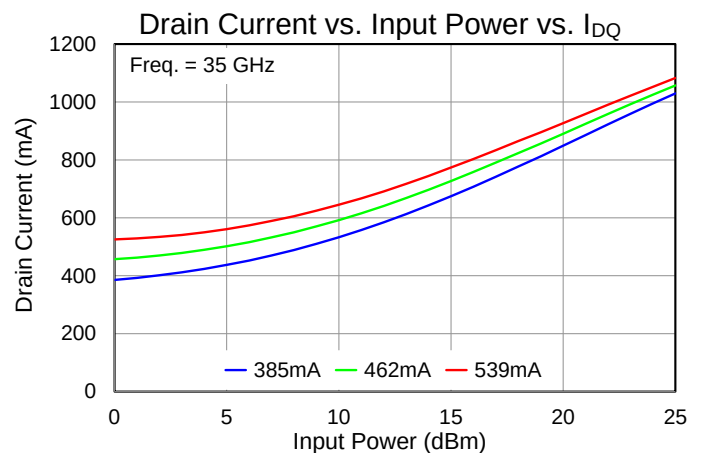
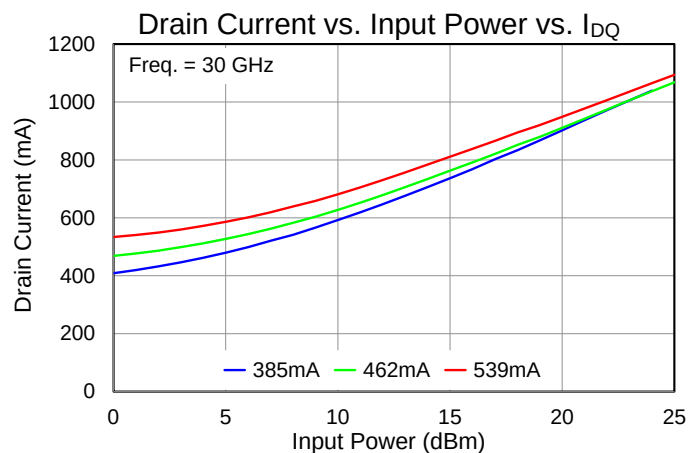
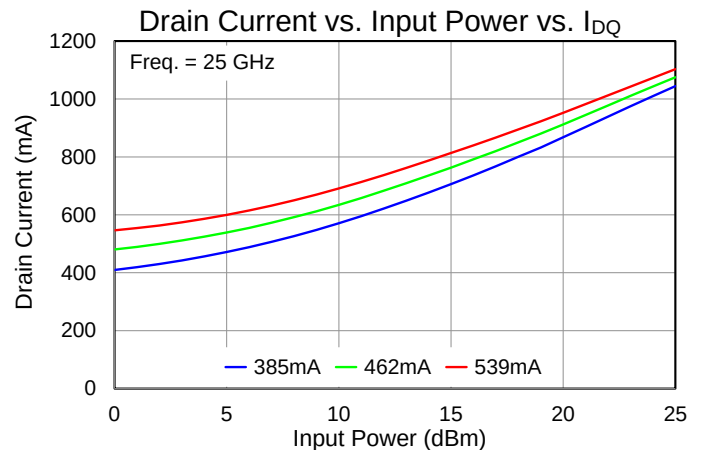
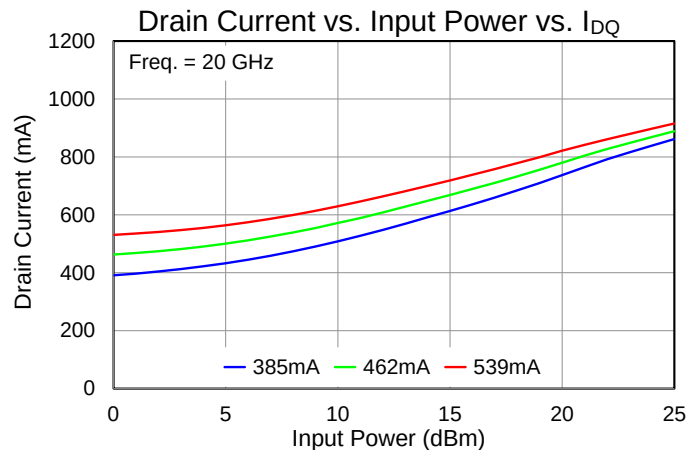
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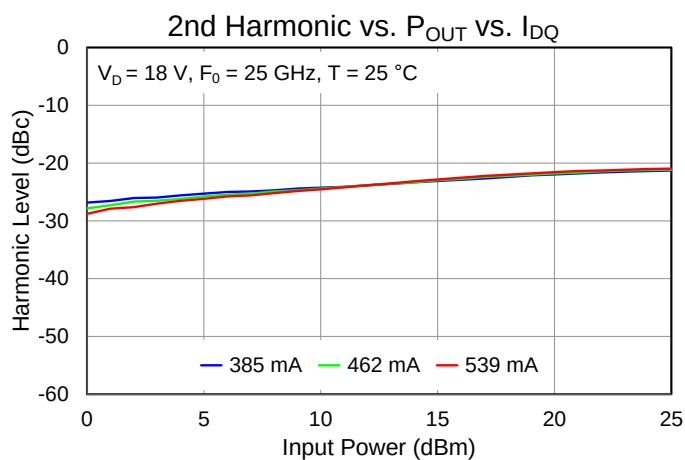
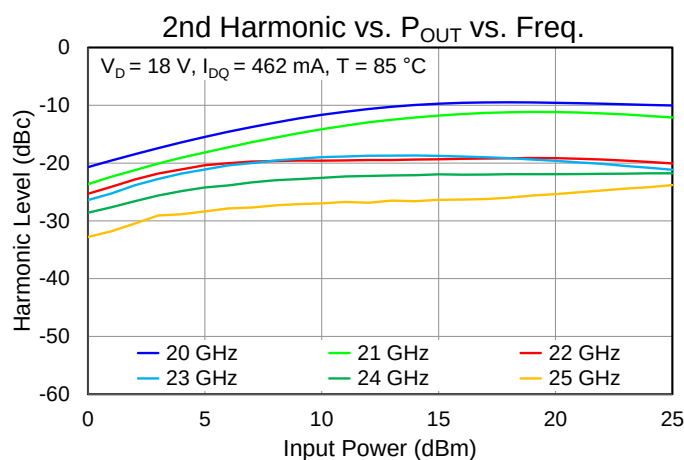
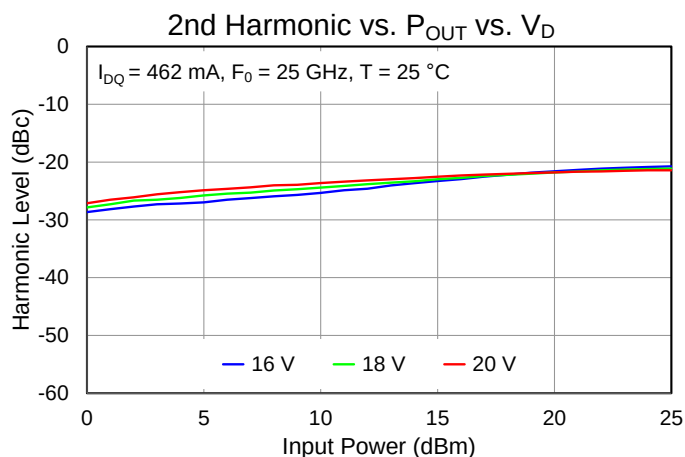
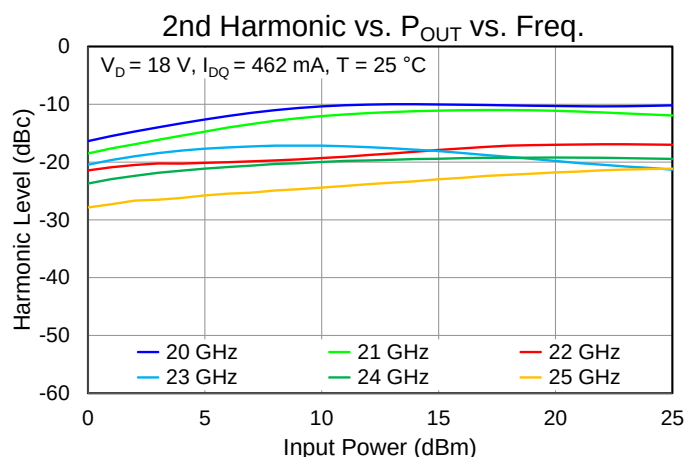
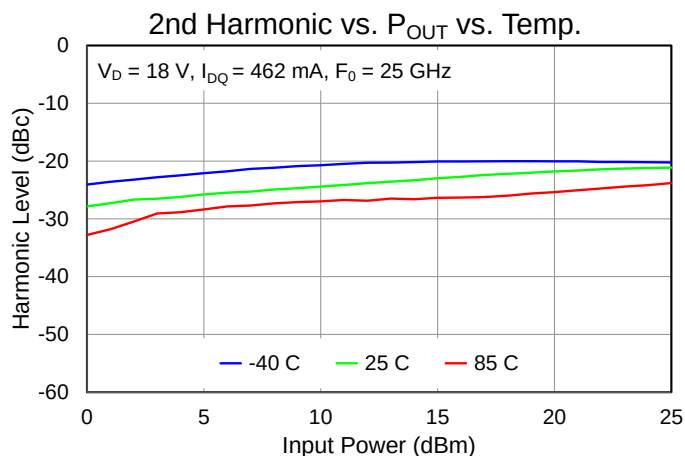
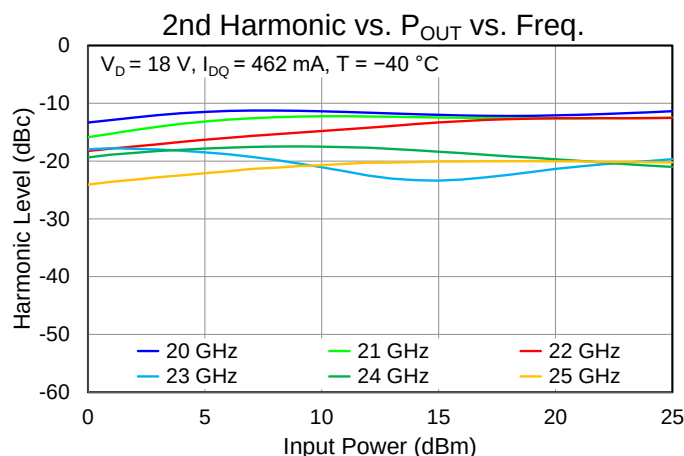
Performance Plots – Large Signal

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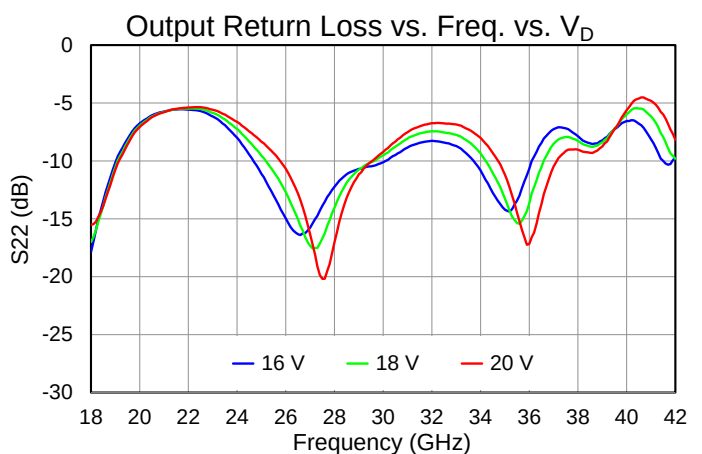
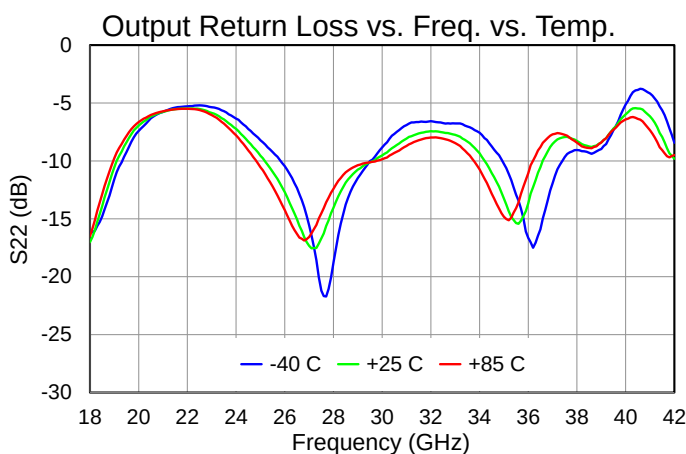
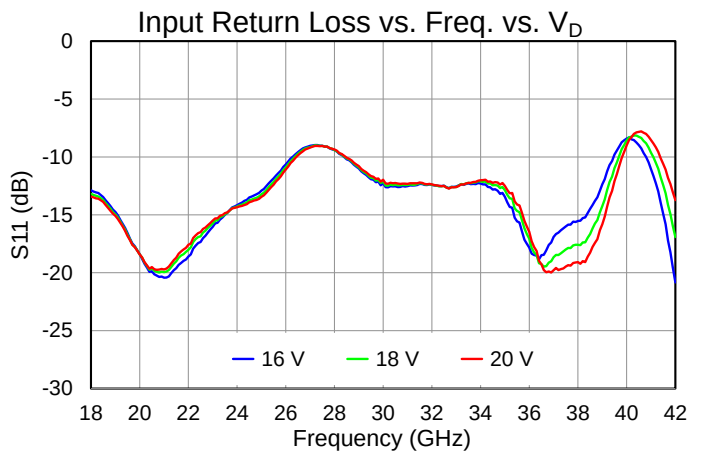
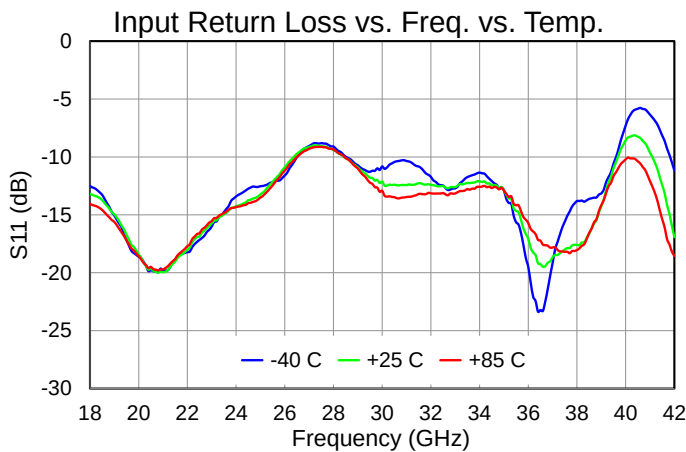
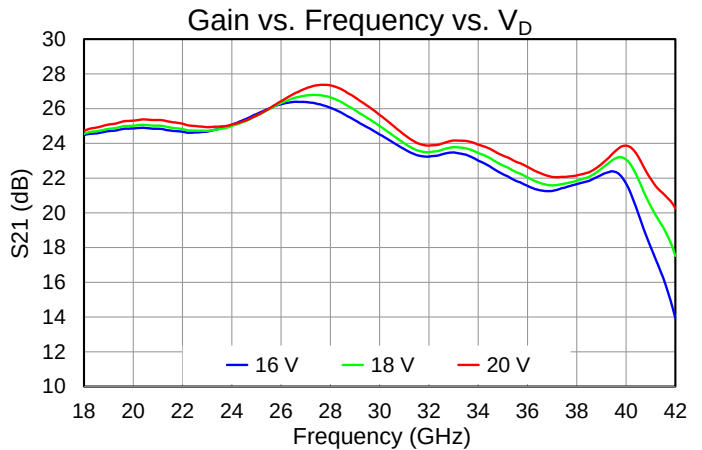
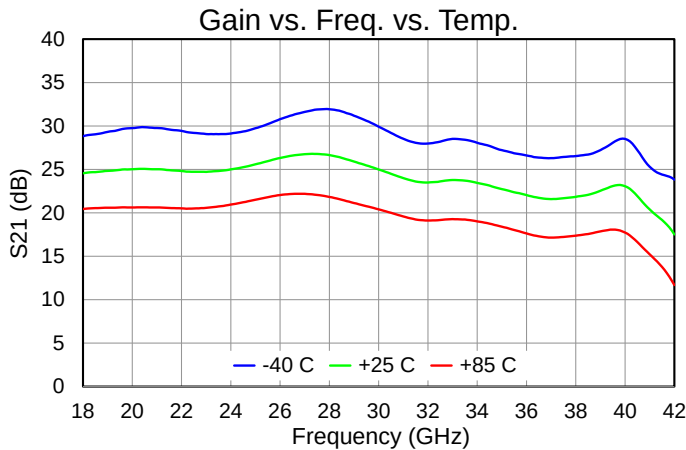
Performance Plots – Harmonics

Test conditions, unless otherwise noted: $V_D = 18\text{ V}$, $I_{DQ} = 462\text{ mA}$, $T = +25\text{ }^{\circ}\text{C}$



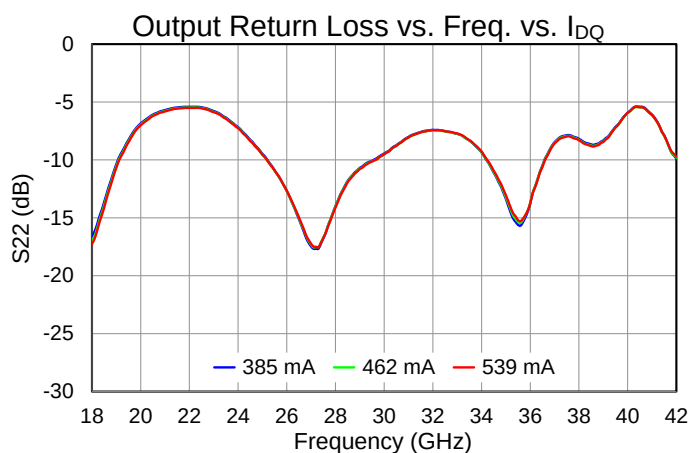
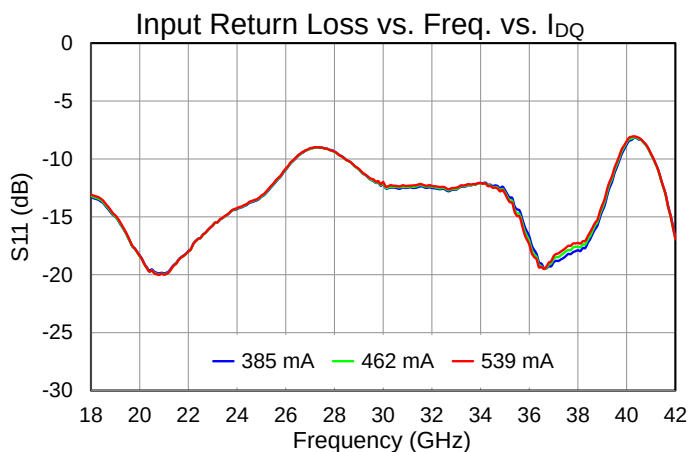
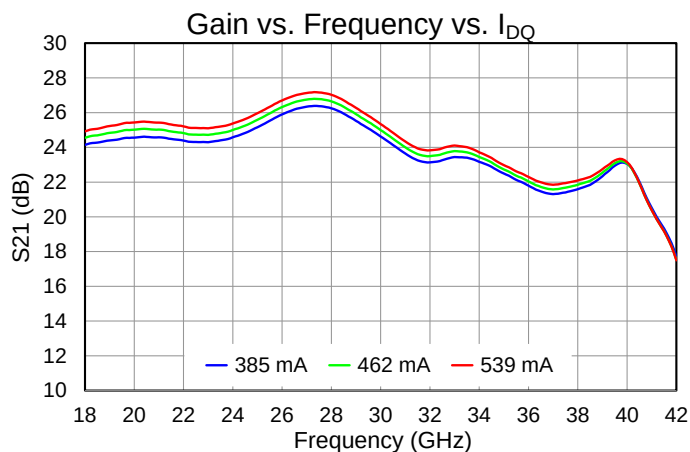
Performance Plots – Small Signal

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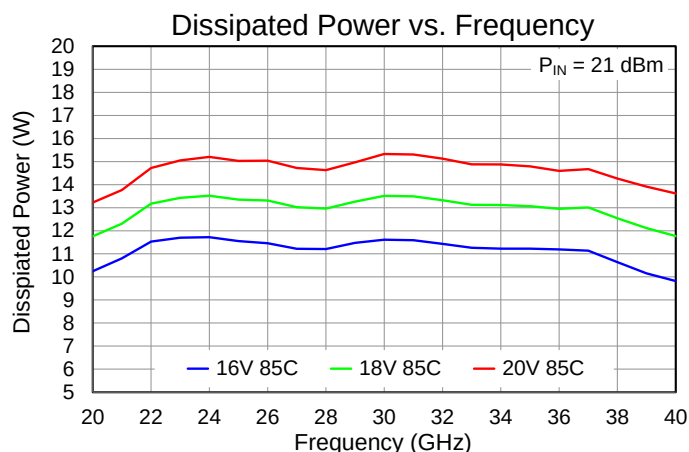
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85\text{ }^{\circ}\text{C}$, $V_D = 18\text{ V}$, $I_{DQ} = 462\text{ mA}$, $P_{DISS} = 8.316\text{ W}$, No RF (quiescent DC operation)	4.413	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH} (No RF) ⁽²⁾		121.7	$^{\circ}\text{C}$
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85\text{ }^{\circ}\text{C}$, $V_D = 18\text{ V}$, $I_{DQ} = 462\text{ mA}$, $\text{Freq} = 24\text{ GHz}$, $I_{D_Drive} = 846\text{ mA}$, $P_{IN} = 21\text{ dBm}$, $P_{OUT} = 32.6\text{ dBm}$, $P_{DISS} = 13.52\text{ W}$	5.644	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH} (Under RF) ⁽²⁾		161.3	$^{\circ}\text{C}$

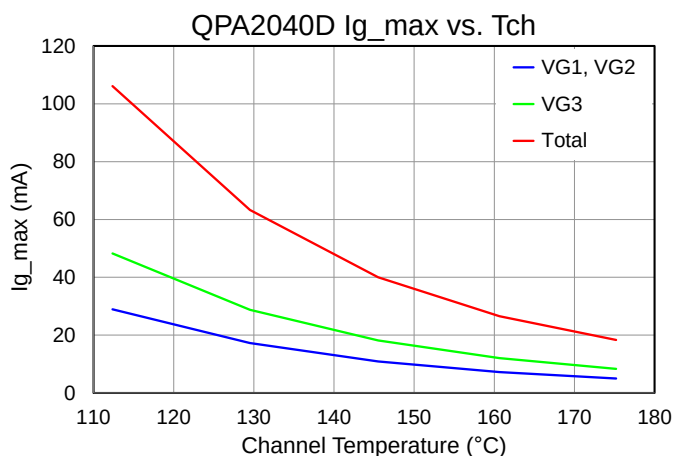
Notes:

1. Thermal resistance determined to the back of 20 mil CuMo carrier plate ($85\text{ }^{\circ}\text{C}$)
2. IR scan equivalent. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

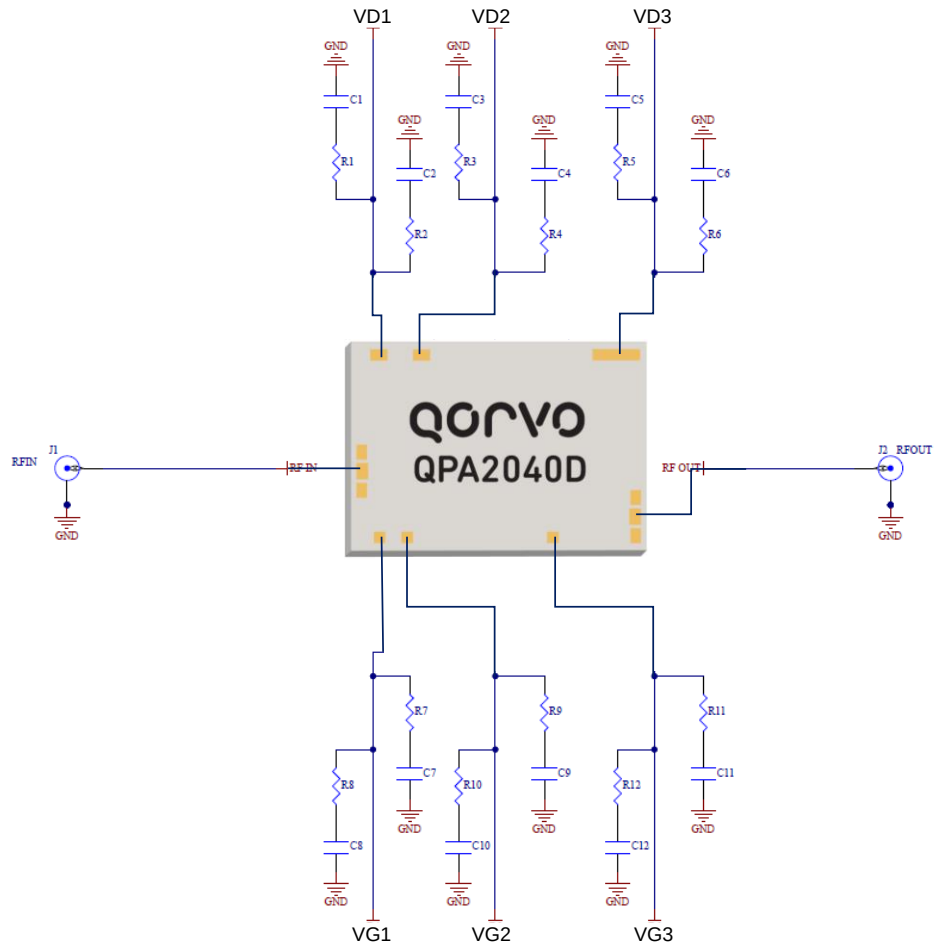
Dissipated Power and Maximum Gate Current



Test conditions unless otherwise noted:
 $I_{DQ} = 462\text{ mA}$, $T = +85\text{ }^{\circ}\text{C}$, $P_{IN} = 21\text{ dBm}$



Applications Information

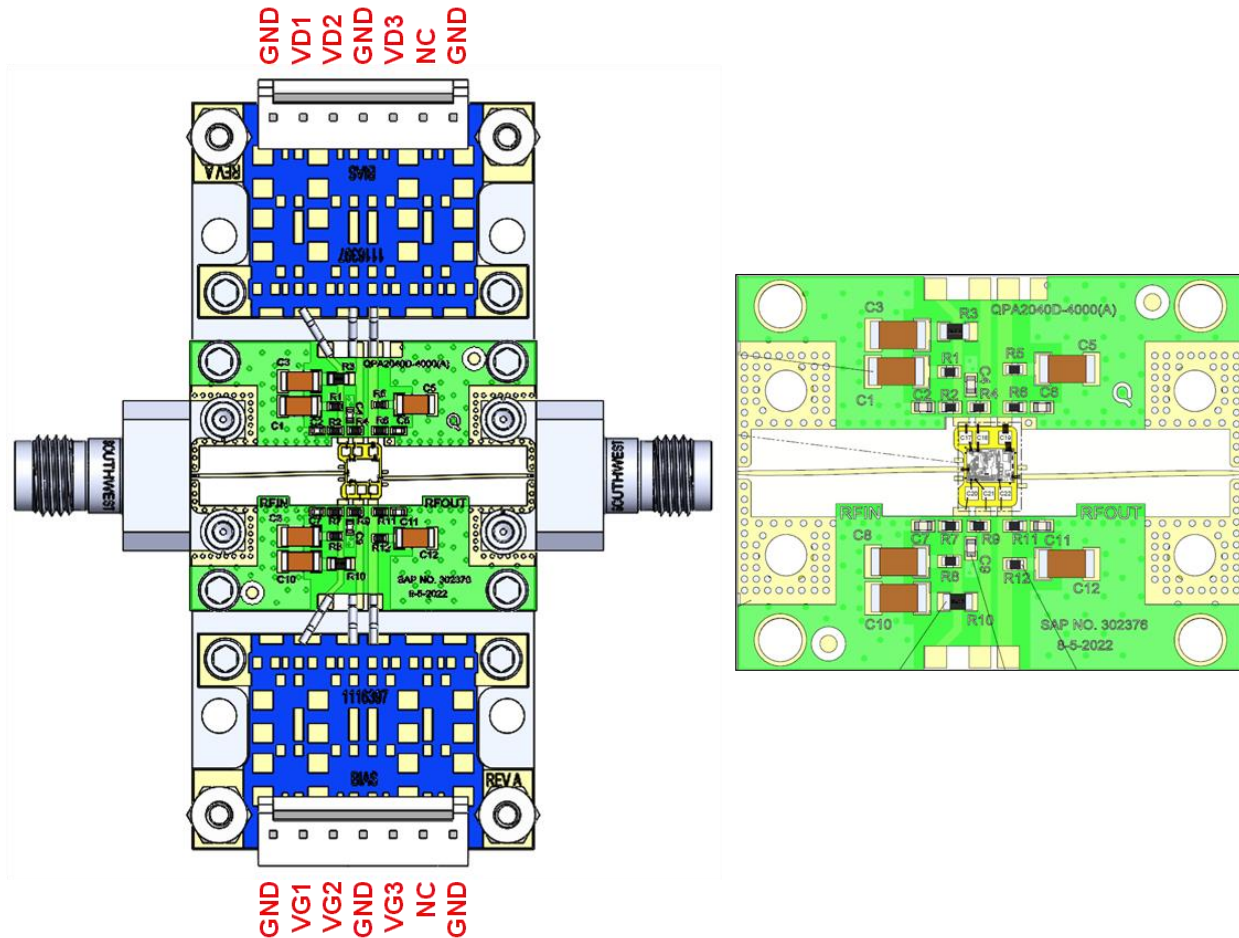


VG may be tied together, and VD may be tied together.
External bypassing is required.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1,C3,C5,C8,C10,C12	10 uF	CAP, 10uF, 20%, 50V, X5R, 1206		
C2,C4,C6,C7,C9,C11	10000 pF	CAP, 10000pF, ±10%, 50V, X7R, 0402		
C17,C18,C19,C20,C21,C22	10 nF	CAP, 10nF, 15%, 30V, 0303, SLC Si WP		
R1,R2,R4,R5,R6,R7,R8,R9,R11,R12	0 Ω	RES, 0 OHM, JMPR, 0402		
R3,R10	0 Ω	RES, 0 ohm, 1/10W, 0603		
J1, J2	2.4 mm	CONN, 2.4,SSENDW, F, PIN .005, DIEL .0295	Southwest Microwave	1492-04A-12

Evaluation Board (EVB) Layout Assembly



PCB is made from TACONICS TSM-DS3B dielectric, .005 inch thick, 0.5 oz. copper both sides.

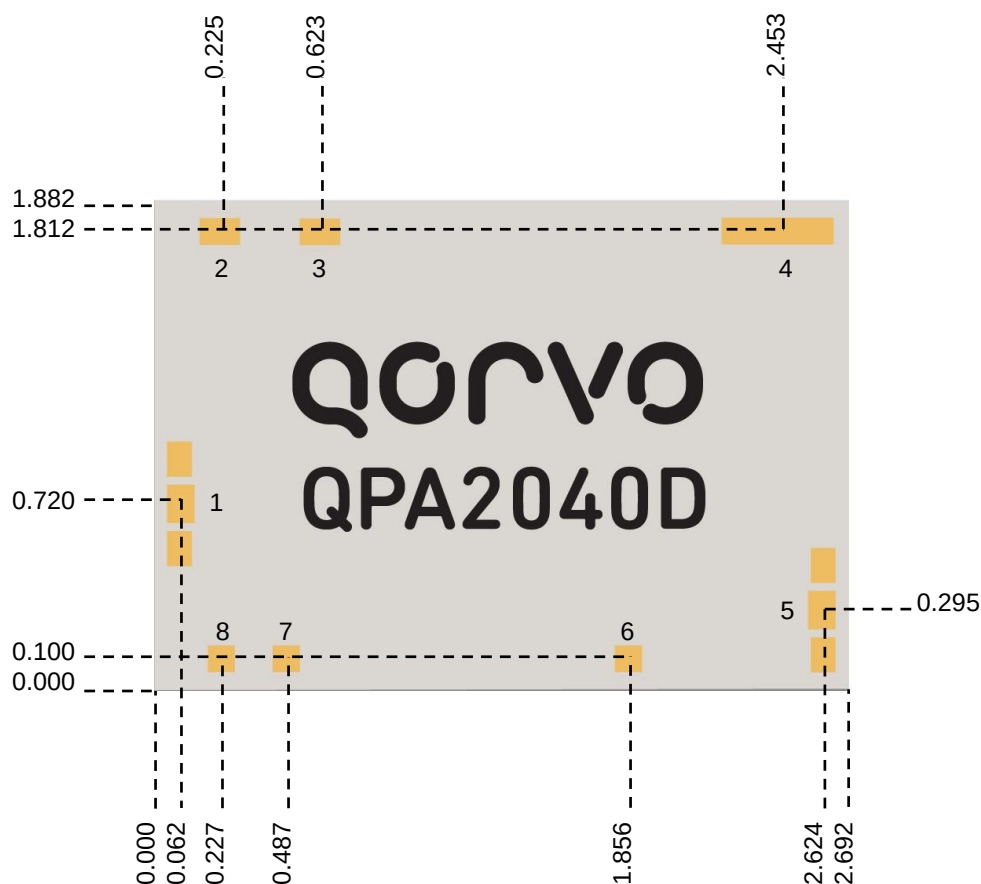
Bias-Up Procedure

1. Set I_D limit to 1200 mA, I_G limit to 20 mA
2. Set V_G to -5.0 V
3. Set V_D +18 V
4. Adjust V_G more positive until $I_{DQ} \approx 462$ mA
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure $I_{DQ} \sim 0$ mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Mechanical Information



Dimensions are in mm
Thickness: 0.050
Die x, y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (um)	Description
1	RF IN	88 x 132	RF input. 50 Ohms. DC blocked, DC grounded.
2	V _{D1}	142 x 92	Drain voltage stage 1. Bypass network required; refer to page 18.
3	V _{D2}	142 x 92	Drain voltage stage 2. Bypass network required; refer to page 18.
4	V _{D3}	430 x 92	Drain voltage stage 3. Bypass network required; refer to page 18.
5	RF OUT	88 x 132	RF output. 50 Ohms. DC blocked, DC grounded.
6	V _{G3}	92 x 92	Gate voltage stage 3. Bypass network required; refer to page 18.
7	V _{G2}	92 x 92	Gate voltage stage 2. Bypass network required; refer to page 18.
8	V _{G1}	92 x 92	Gate voltage stage 1. Bypass network required; refer to page 18.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	0B	ANSI/ESD/JEDEC JS-001



Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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