ACT88420

Advanced PMIC with 4 Bucks, 2 LDO, and Load Bypass Switches

BENEFITS and FEATURES

- **Wide Input Voltage Range**
  - Vin = 2.7V to 5.5V
- **Complete Integrated Power Solution**
  - Buck 1: 4A DC/DC Step-Down Regulator with Bypass Function
  - Buck 2: 2A DC/DC Step-Down Regulator
  - Buck 3: 4A DC/DC Step-Down Regulator Optimized for Low Voltage Output
  - Buck 4: 2A DC/DC Step-Down Regulator, can be Configured as 400mA LDO
  - LDO1: 400mA LDO or 1A Load Switch
  - LDO2: 400mA LDO or Load Switch
  - Current Mode Control for Buck1, COT Control for Buck 2, 3, and 4
- **Space Savings**
  - Fully Integrated
  - Works with 0.47µH Inductor
  - Integrated sequencing
- **Ultra-low Quiescent Current**
- **Excellent Efficiency at Very Light Load**
- **Easy System Level Design**
  - Configurable Sequencing
  - Multiple Wake up Triggers with GPIOs
  - Seamless Sequencing of External Supplies
  - 8 Programmable GPIOs
- **Buck 1 and LDO2 Bypass Mode for 3.3V system level compliance**
- **LDO1 Bypass Mode with Dedicated Input Pin, Support up to 1A Current**
- **Highly Configurable**
  - Regulator Operation Mode can be Configured by 3-Level GPIOs status
  - Configurable Platform ID with Different Power Up Delay Times
  - I²C Interface for Status Reporting and Controllability
  - Programmable Reset and Power Good GPIO's
  - Flexible Sequencing Options
  - Multiple Sleep Modes
  - Configurable Power Cycle and ActiveSafe™ ROM Mode through GPIO
- **I²C Interface – up to 3.4MHz**

APPLICATIONS

- Solid-State Drives (SSD)
- FPGA
- Computer Vision
- Portable Audio / Video

GENERAL DESCRIPTION

The ACT88420 PMIC is an integrated ActiveCiPS™ power management integrated circuit. It powers a wide range of processors, including solid-state drive applications, video processors, FPGA's, peripherals, and microcontrollers. The ACT88420 is highly flexible and can be reconfigured via I²C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. ACT88420 is programmed at the factory with a default configuration. These settings can be optimized for a specific design through the I²C interface. The ACT88420 is available in several default configuration. Contact the factory for specific default configurations.

The core of the device includes four DC/DC step down converters using integrated power FETs, two low-dropout regulators (LDO). Buck1 and two LDOs can be configured as a load switch, Buck 4 can be configured as LDO. Buck1 is a peak current mode, fixed frequency DC-DC step down converter that is optimized for output voltage closes to the input voltage. Buck1 switches at either 1.125MHz or 2.25MHz. Buck 2, 3, and 4 use an asynchronous constant on-time, ACOT, control architecture to optimize the load transient response with 0.47uH inductor and smaller output capacitors. The LDOs only require small ceramic capacitors. All outputs are highly configurable via the I²C interface.

ACT88420 has 8 configurable GPIOs. These GPIOs can be configured for multiple purposes like enable signal for external regulator, interrupt, PWREN, DVS control, ROM control, etc. In addition, some GPIOs support 3 states status that can be used to configure the regulators operation mode, default output voltage, and extra turn on delay times without the need for CMI changes.

The ACT88420 PMIC is available in a 2.693 x 2.693 mm 36 ball WLCSP package.

TYPICAL APPLICATION DIAGRAM

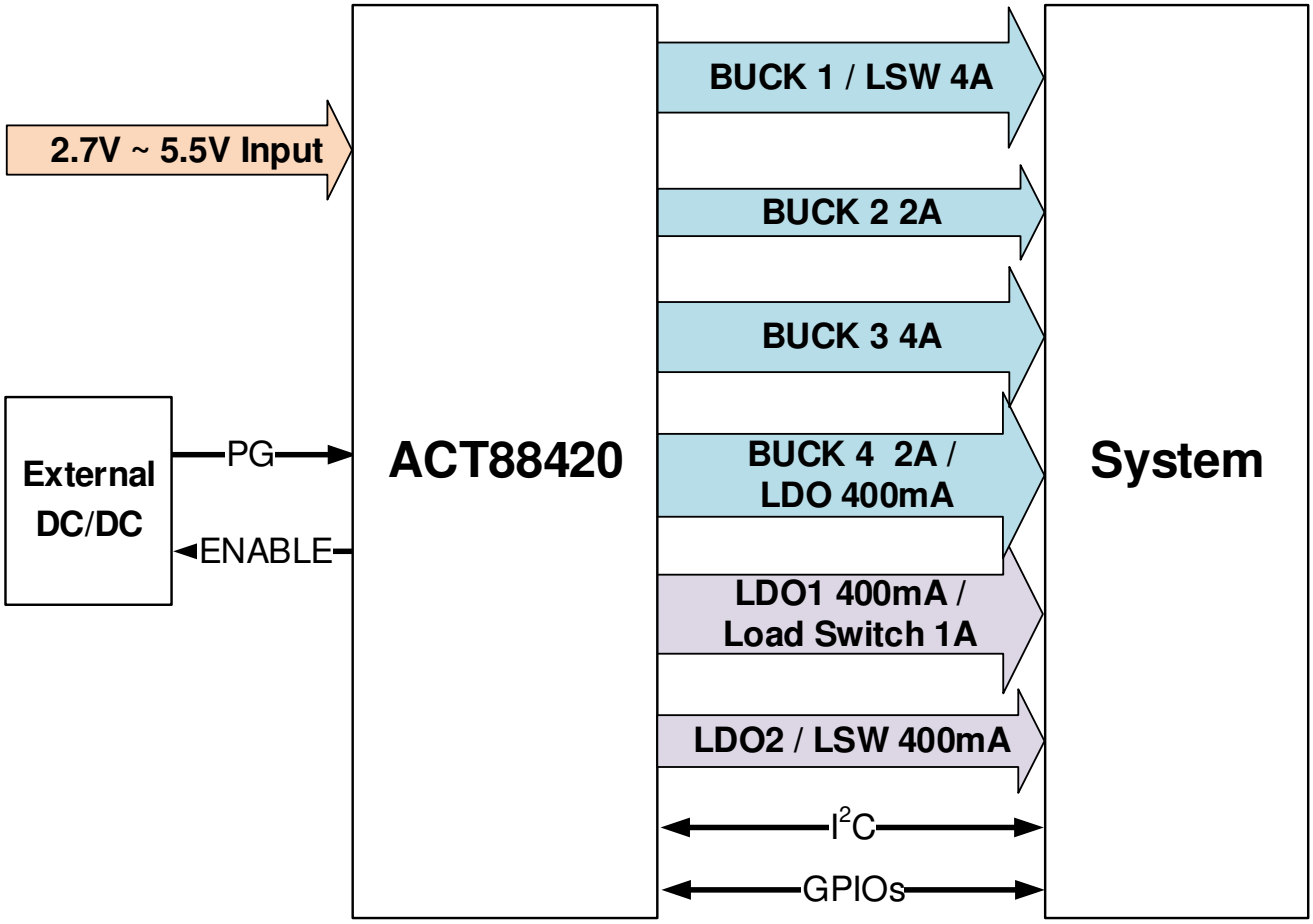


Figure 1: Typical Application Diagram

FUNCTIONAL BLOCK DIAGRAM

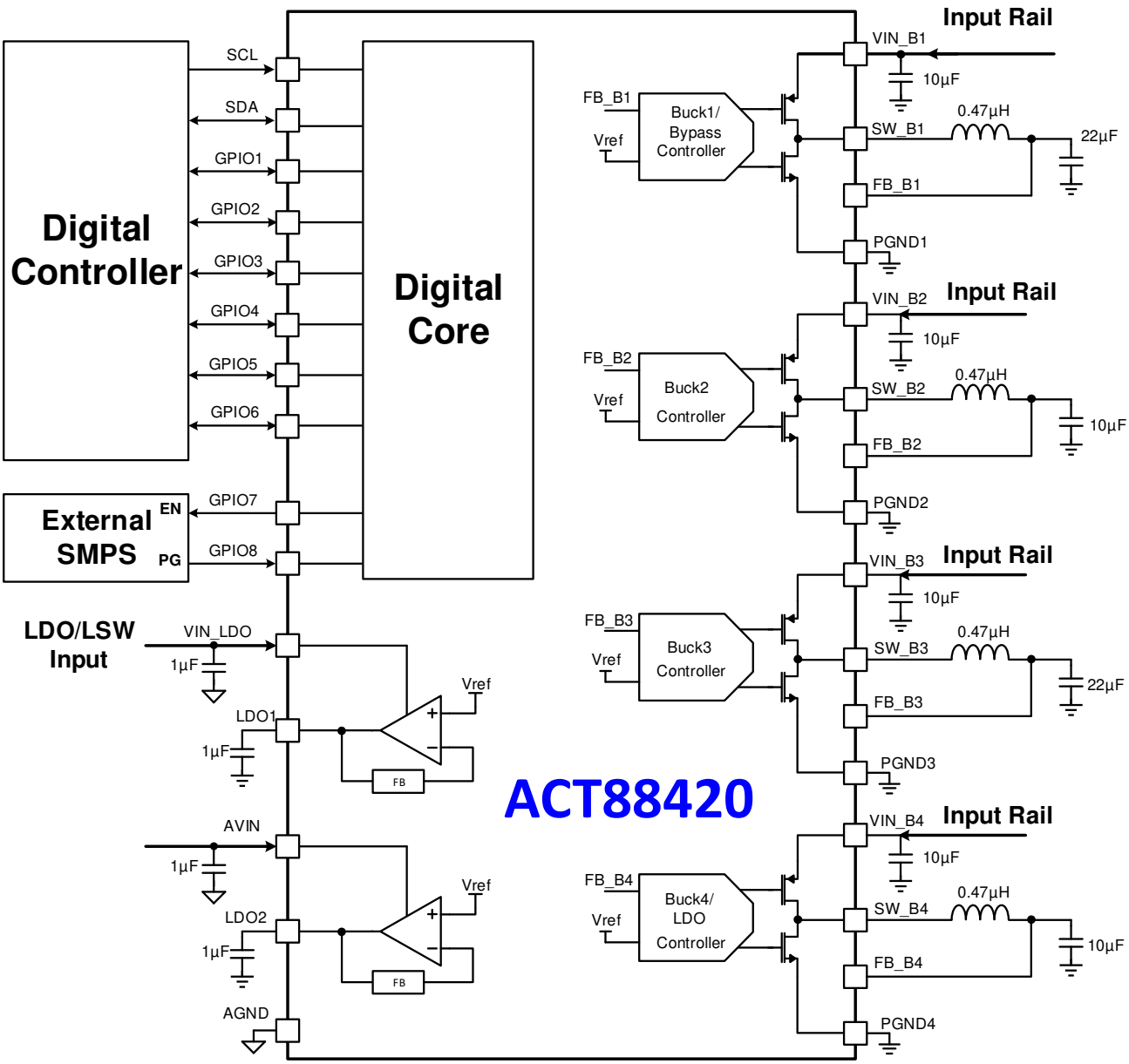
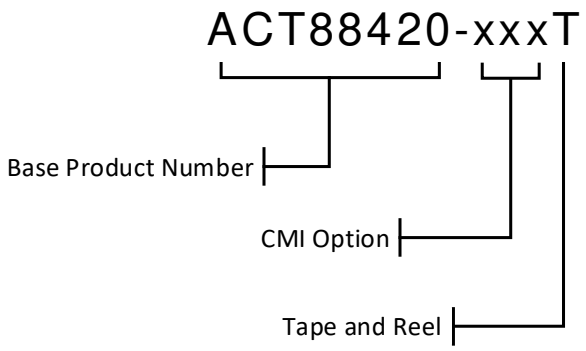


Figure 2: ACT88420 Block Diagram & Application Schematic

ORDERING INFORMATION

PART NUMBER	V_{IN}	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{LDO1}	V_{LDO2}	7-bit I^2C Address
ACT88420-101T	3.3V	2.5V	1.2V	0.8V	1.2V	LSW (3.3V)	1.8V	0x25h
ACT88420-102T	3.3V	2.5/2.9V	1.2/1.8V	0.83V/ 0.81V	1.1V	LSW (3.3V)	1.8V	0x25h
ACT88420-103T	3.3V	2.5/2.5V	1.2/1.2V	0.80V/ 0.81V	1.8V	LSW (3.3V)	1.8V	0x25h
ACT88420-104T	3.3V	2.5/2.9V	1.2/1.8V	0.8V	0.8V	1.8V	1.8V	0x25h



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION - WLCSP

	1	2	3	4	5	6
A	SW_B1	SW_B1	PGND12	SW_B2	VIN_B2	VIN_LDO1
B	VIN_B1	VIN_B1	PGND12	PGND12	FB_B2	LDO1
C	GPIO3	GPIO7	FB_B1	AGND	GPIO6	LDO2
D	GPIO2	SCL	SDA	GPIO5	FB_B3	AVIN
E	FB_B4	GPIO8	GPIO1	PGND34	GPIO4	VIN_B3
F	VIN_B4	SW_B4	PGND34	PGND34	SW_B3	SW_B3

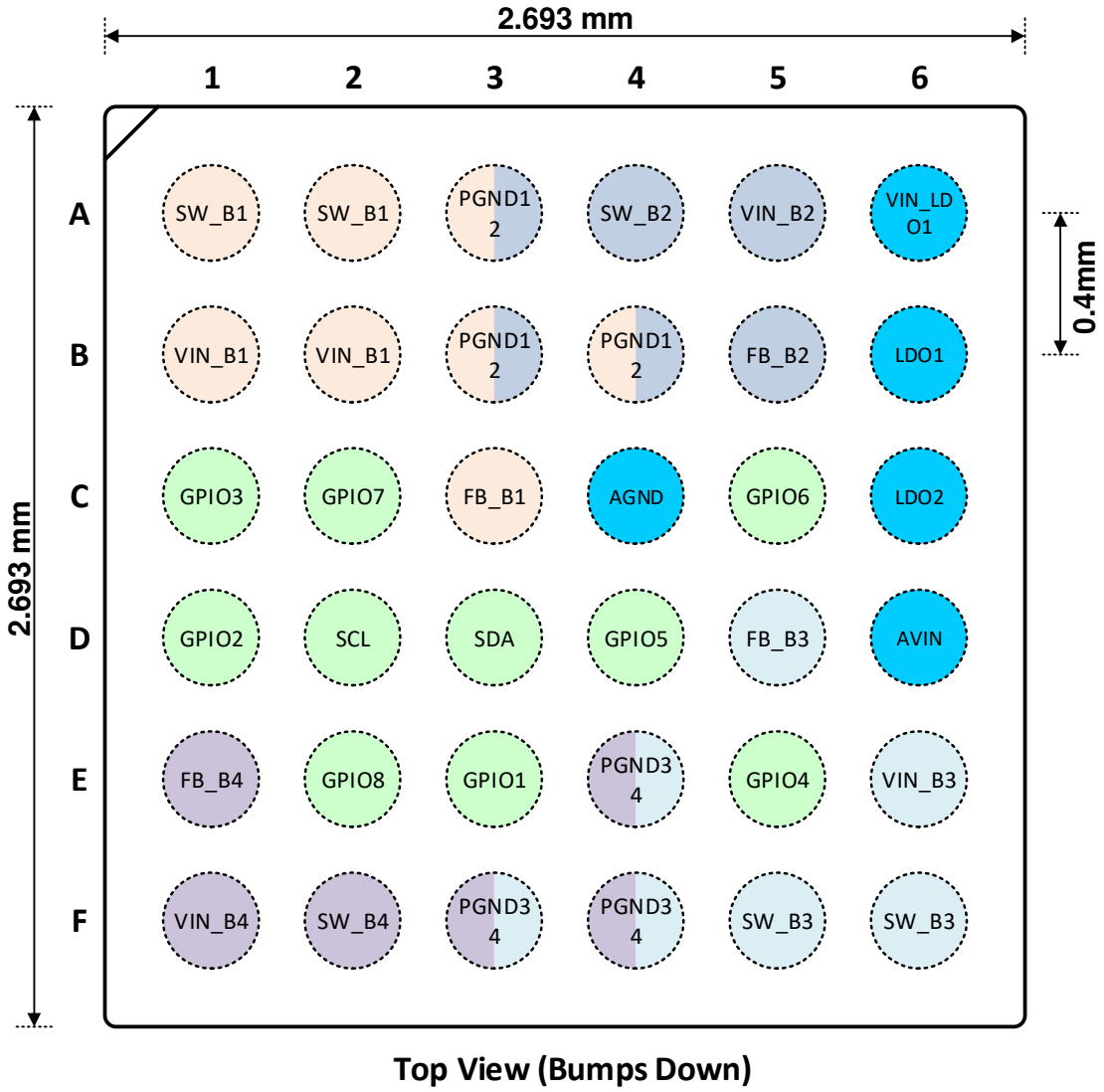


Figure 3: ACT88420 Pin Configuration – Top View (bumps down) – WLCSP- 36

PIN DESCRIPTIONS

Ball (CSP)	NAME	DESCRIPTION
A3, B3, B4	PGND12	Dedicated Power Ground for Buck1 and Buck2 Regulator.
E4, F3, F4	PGND34	Dedicated Power Ground for Buck3 and Buck4 Regulators
A1, A2	SW_B1	Switch Pin for Buck 1 Regulator.
B1, B2	VIN_B1	Dedicated VIN power input for Buck 1 Regulator.
C3	FB_B1	Feedback for Buck 1 Regulator. Connect to the Buck 1 output capacitor.
A4	SW_B2	Switch Pin for Buck 2 Regulator.
A5	VIN_B2	Dedicated VIN power input for Buck 2 Regulator.
B5	FB_B2	Feedback for Buck 2 Regulator. Connect to the Buck 2 output capacitor.

F5, F6	SW_B3	Switch Pin for Buck 3 Regulator.
E6	VIN_B3	Dedicated VIN power input for Buck 3 Regulator.
D5	FB_B3	Feedback for Buck 3 Regulator. Connect to the Buck 3 output capacitor.
F2	SW_B4	Switch Pin for Buck 4 Regulator.
F1	VIN_B4	Dedicated VIN power input for Buck 4 Regulator.
E1	FB_B4	Feedback for Buck 4 Regulator. Connect to the Buck 4 output capacitor.
B6	LDO1	Output for LDO1 Regulator (Leave unconnected if LDO is not used and disabled).
A6	VIN_LDO1	Dedicated VIN power input for LDO Regulator.
C6	LDO2	Output for LDO2 Regulator (Leave unconnected if LDO is not used and disabled).
D2	SCL	I^2C Clock Input.
D3	SDA	I^2C Data Input and Output.
C4	AGND	Analog Ground. Kelvin connects to the other ground pins on the IC.
E3	GPIO1	Configurable general-purpose input/open drain output.
D1	GPIO2	Configurable general-purpose input/open drain output.
C1	GPIO3	Configurable general-purpose input/open drain output.
E5	GPIO4	Configurable general-purpose input/open drain output.
D4	GPIO5	Configurable general-purpose input/open drain output.
C5	GPIO6	Configurable general-purpose input/open drain output.
C2	GPIO7	Configurable general-purpose input/open drain output.
E2	GPIO8	Configurable general-purpose input/open drain output.
D6	AVIN	Analog Input supply and power input for LDO2. This is also the pin that is monitored for VIN OV and UV.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

PARAMETER	VALUE	UNIT
All I/O and Power pins except PGND12, PGND34, AGND	-0.3 to 6	V
Grounds: Any PGND referenced to AGND	-0.3 to +0.3	V
SW_Bx to PGNDx	-1 to VIN_Bx + 1	V
FB_Bx to PGNDx	-0.3 to AVIN + 0.3	V
LDOx to AGND	-0.3 to VIN_LDO + 0.3	V
Junction to Ambient Thermal Resistance, CSP (Note2)	27.6	°C/W
Junction to Case Thermal Resistance, CSP (Note2)	4.7	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
HBM ESD (Note3)	1000	V
MSL Rating	1	

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.
Note2: Measured on Qorvo Evaluation Kit

Note3: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVIN, VIN_B1, VIN_B2, VIN_B3, VIN_B4 (Note1)		2.7		5.5	V
VIN_LDO1	LDO Mode	1.62		5.5	V
	NLSW Mode	0.4		Min of (AVIN-1 or 3.6V)	V
	PLSW Mode	1.62		AVIN	V
Operating Junction Temperature		-40		125	°C

Note1: AVIN must always be the highest input voltage to the IC.

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIOs Leakage Current	Output = 5V			1	µA
GPIOs Output Low (Open Drain)	IOL = 1mA			0.35	V
GPIOs Input Low (GPIO 2/3/4/5)				0.35	V
GPIOs Input Low (GPIO 1/6/7/8)				0.55	V
GPIOs Input High (All GPIOs)		1.25			V
GPIO 3-State Low (GPIO 2/3/4/5)				0.15	V
GPIOs 3-State High (GPIO 2/3/4/5)		1.65			V
GPIO Configurable Delay Times			0		ms
			0.25		
			0.5		
			0.75		
			1		
			2		
			4		
			8		
GPIOs Deglitch Time (GPIO 1/2/3/4/5/6/7)		10		40	µs
GPIOs Deglitch Time (GPIO 8)		1		40	µs
Minimum PWRDIS High Time	For GPIO that configured for PWRDIS. If PWRDIS < 100ms, NVM of Master tile is not reloaded		100		ms

PWRSYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Inputs Voltage Range: VIN_B1 referenced to PGND12 VIN_B2 referenced to PGND13 VIN_B3 referenced to PGND34 VIN_B4 referenced to PGND34		2.7		5.5	V
VIN_LDO1 referenced to AGND	LDO Mode	1.62		5.5	V
	NLSW Mode	0.4		Min of (AVIN-1 or 3.6V)	
	PLSW Mode	1.62		AVIN	
VIN UVLO Threshold Falling (Note 1)	Bit VIN_LVL=0	2.5	2.6	2.7	V
	Bit VIN_LVL=1	3.35	3.5	3.65	V
VIN UVLO Hysteresis (Note 1)	Bit VIN_LVL=0	50	100	150	mV
	Bit VIN_LVL=1	250	300	350	mV
VIN OV Threshold Rising – VIN_OV (Note 1)	Configurable from 3.7V to 5.8V with 0.3V steps. See details in VIN_OV table	-3.5	SET POINT	3.5	%
VIN OV Hysteresis (Note 1)		100	200	300	mV
VIN POK OV Interrupt Threshold Rising	Configurable from 3.5V to 5.6V with 0.3V steps. See details in POK_OV table	-3.5	SET POINT	3.5	%
VIN POK OV Interrupt Threshold Hysteresis		100	200	300	mV
VIN POK Deglitch Time OV or UV			5		µs
Operating Supply Current	All Regulators Disabled I²C is always available		12.5		µA
	Buck 3 is on, other Regulators Disabled		61		µA
	Buck 3 and Buck 4 (Buck mode) are on, other Regulators Disabled		78		µA
	Buck 3 and Buck 4 (LDO mode, ULPM) are on, other Regulators Disabled		66		µA
	Buck 3, LDO1(LDO mode, ULPM), and LDO2 (in LDO mode, ULPM) are on, other Regulators Disabled		74		µA
	Buck 3, Buck 4 (Buck mode), and LDO2 (in LSW mode) are on, other Regulators Disabled		82		µA
	Buck 3, Buck 4 (Buck), and LDO2 (in LDO mode, ULPM) are on, other Regulators Disabled		86		µA
	All Regulators Enabled – No load (not in ultra-low power mode)		250		µA
System Monitor (SYSMON) Programmable Range – Falling Threshold	In 25mV steps	2.725		3.1	V

VIN System Monitor (SYSMON) Accuracy		-2.5	SET POINT	2.5	%
VIN System Monitor (SYSMON) Hysteresis			50		mV
VIN System Warning (SYSWARN) Programmable Range– Falling Threshold	In 25mV steps	2.775		3.15	V
VIN System Warning (SYSWARN) Accuracy	In 25mV steps	-2.5	SET POINT	2.5	%
VIN System Monitor (SYSWARN) Hysteresis			50		mV
VIN Deglitch Time UV	Falling, enter UV		5		µs
VIN Deglitch Time UV	Rising, exit UV		100		µs
VIN UV Analog Debounce Time	Rising		5		µs
VIN Deglitch Time OV	Rising, enter OV		5		µs
VIN Deglitch Time OV	Falling, exit OV		200		µs
VIN OV Analog Debounce Time	Falling		10		µs
Thermal Shutdown Temperature TSD_SHUTDWN	Temperature rising		155		°C
Thermal Shutdown Hysteresis			30		°C
Thermal Interrupt Threshold, TWARN	Temperature rising - Referenced to TSD_SHUTDWN		TSD_SHUTDWN - 30		°C
Thermal Interrupt Hysteresis			20		°C
Load GPIO Configuration to Internal RAM	Start from VIN > UVLO		500		µs
Startup Delay after initial AVIN	Time from AVIN > UVLO threshold to start of first regulator turning On. (zero turn on delay setting)		1000	1500	µs
Transition time from Deep Sleep (DPSLP) State to Active State	Time from PWREN pin low to high transition to time when the first regulator turns ON (Start to ramp up) with minimum turn on delay configuration.		100	500	µs
	Using I^2C		100		µs
Transition time from Sleep State (SLEEP) to Active State	Time from I^2C command to clear sleep mode to time when the first regulator turns ON (Start to ramp up) with minimum turn on delay configuration.		100		µs
Time to first power rail turn off	Time from turn Off command to when the first power rail turns off with minimum turn off delay configuration		100		µs
OV/UV Retry Time	System retry time when one of the regulators exceeds an output OV or UV level at any time		200		ms
Startup Delay Programmable Range	ON_DELAY=000 ON_DELAY=001 ON_DELAY=010 ON_DELAY=011 ON_DELAY=100 ON_DELAY=101 ON_DELAY=110 ON_DELAY=111		Minimum 0.25 0.5 0.75 1 2 4 8		ms

Turn Off Delay Programmable Range	OFF_DELAY=000 OFF_DELAY=001 OFF_DELAY=010 OFF_DELAY=011 OFF_DELAY=100 OFF_DELAY=101 OFF_DELAY=110 OFF_DELAY=111	Minimum 0.25 0.5 0.75 1 2 4 8	ms
nRESET Programmable Range	TRST_DLY=000 TRST_DLY=001 TRST_DLY=010 TRST_DLY=011 TRST_DLY=100 TRST_DLY=101 TRST_DLY=110 TRST_DLY=111	0.5 1 2 4 8 16 32 64	ms
GPIOs Delay Programmable Range	IOx_DLY=000 IOx_DLY=001 IOx_DLY=010 IOx_DLY=011 IOx_DLY=100 IOx_DLY=101 IOx_DLY=110 IOx_DLY=111	Minimum 0.25 0.5 0.75 1 2 4 8	ms

Note1: All Under-voltage Lockout, Overvoltage measurements are referenced between AVIN and AGND pin.

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_B1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 25mV steps	0.6		3.775	V
Maximum Output Current (Note1)		4			A
Maximum Operation Duty Cycle		99			%
Supply Current, Standby	Low Power Mode Enabled Regulator Only, non-switching, V_{FB}=103*V_{SET}		50		µA
	ULPM Mode Enabled Regulator Only, non-switching, V_{FB}=103*V_{SET}, IC is in SLEEP or DEEP SLEEP Mode.		10		µA
Supply Current, Shutdown	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	7.5	uA
Output Voltage Accuracy – PWM (Note2)	Default output voltage +/- 200mV, I_{OUT} = 2A	-1	V_{NOM}	1	%
Output Voltage Accuracy – PWM	Default output voltage +/- 200mV, I_{OUT} = 2A	-1.5	V_{NOM}	1.5	%
Output Voltage Accuracy – PFM (Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}	1	%
Output Voltage Accuracy – PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1.5	V_{NOM}	1.5	%
Line Regulation	Default output voltage, V_{IN_B2} = 3.3V to 5.5V, CCM mode		0.05		%/V
Load Regulation	Default output voltage, CCM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B1} Rising	90	93	96	%V_{NOM}
Power Good Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B1} Rising	107	110	113	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Switching Frequency	HALF_FREQ = 0	2.00	2.25	2.4	MHz
	HALF_FREQ = 1	1.00	1.125	1.2	MHz
Soft-Start Period – Programmable	10% to 90% V_{NOM} B1_SST = 1 B1_SST = 0		250 500		µs
Soft-Start Period Tolerance	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET	B1_ILIM_SET=00 B1_ILIM_SET=01 B1_ILIM_SET=10 B1_ILIM_SET=11		4.0 5.0 6.2 7.8		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIM_SET	-25	ILIM_SET	25	%
	At other set points	-30	ILIM_SET	30	

Internal High Side Peak Current Limit, Shutdown Level	Above ILIM_SET settings	10	25	40	%
Low Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET (Note3)	B1_ILIM_SET=00 B1_ILIM_SET=01 B1_ILIM_SET=10 B1_ILIM_SET=11		5.0 6.2 7.8 10		A
OC Retry Time	Regulator retry time when it exceeds an output OC level		14		ms
PMOS On-Resistance	I_{SW} = -1A, VIN_B1 = 3.3V		30		mΩ
NMOS On-Resistance	I_{SW} = 1A, VIN_B1 = 3.3V		40		mΩ
SW Leakage Current – NMOS	V_{IN_B1} = 5V, V_{SW} = 5V (Note2)		0.1	1	µA
	V_{IN_B1} = 5V, V_{SW} = 5V		0.1	1.5	uA
SW Leakage Current – PMOS	V_{IN_B1} = 5V, V_{SW} = 0V (Note2)		0.1	2.5	µA
	V_{IN_B1} = 5V, V_{SW} = 0V		0.1	9.0	uA
Switching Rise / Fall Times	V_{IN_B1} = 5V B1_DRVADJ=00 B1_DRVADJ=01 B1_DRVADJ=10 B1_DRVADJ=11		2.2/2 1.9/1.9 1.7/1.8 1.6/1.7		ns
Output Pull Down Resistance	Enabled when regulator disabled		4.4		Ohms

Note1: There are two balls for VIN_B1 and SW_B1 which is good for 4A average lifetime rating at 105 deg C junction.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR: – BYPASS MODE OPTION

(VIN_B1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Bypass Mode					
Input Voltage Range for By-Pass Mode		2.7	3.3	3.7	V
PMOS On-Resistance	I_{SW} = -1A, VIN = 3.3V		30		mΩ
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	1.55	2.7	3.76	A
Internal PMOS Current Detection Deglitch Time			10		µs
Internal PMOS Current Shutdown (Note1)	Shuts down after deglitch time and stays off for Off Time	3.4	4.9	6.7	A
Internal PMOS Current Shutdown Deglitch Time			10		µs
Internal PMOS Current Shutdown Off time (hiccup time)			14		ms
Internal PMOS Softstart	VIN = 3.3V		6.6		mV/us
Overvoltage Protection Threshold			3.8		V
OV Deglitch Time			45		µs

Note1: There are two balls for VIN_B1 and SW_B1 which is good for 4A average lifetime rating at 105 deg C junction.

BUCK2 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B2 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 10mV steps	0.6		1.87	V
Maximum Output Current (Note1)		2			A
Supply Current, Standby	Ultra Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		11.5		µA
	Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		42		µA
Supply Current, Shutdown	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	4.5	µA
Output Voltage Accuracy – CCM (Note2)	Default output voltage +/-200mV, I_{OUT} = 1A	-1	V_{NOM}	1	%
Output Voltage Accuracy – CCM	Default output voltage +/-200mV, I_{OUT} = 1A	-2	V_{NOM}	2	%
Output Voltage Accuracy – DCM (Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}+ 3%	1	%
Output Voltage Accuracy – DCM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-2	V_{NOM}+ 3%	2	%
Line Regulation	Default output voltage, V_{IN_B3} = 3.3V to 5.5V, CCM mode		0.05		%/V
Load Regulation	Default output voltage, CCM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B2} Rising	92	94	96	%V_{NOM}
Power Good Hysteresis	V_{OUT_B2} Falling		4		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B2} Rising	111	114	117	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B2} Falling		4		%V_{NOM}
Emulated Switching Frequency	B2_FRE_SEL=00 B2_FRE_SEL =01 B2_FRE_SEL =10 B2_FRE_SEL =11		1.5 2.0 2.5 3.3		MHz
Soft-Start Period – Programmable Range	10% to 90% V_{NOM} B2_SST=000 B2_SST=001 B2_SST=010 B2_SST=011 B2_SST=100 B2_SST=101 B2_SST=110 B2_SST=111		 50 75 100 150 200 250 500 350		µs
Soft-Start Period Tolerance	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET	B2_ILIM_SET=0 B2_ILIM_SET=1		2.5 4.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIM_SET	-15	ILIM_SET	15	%
	At other set points	-20	ILIM_SET	20	%

Low Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET (Note3)	B2_ILIM_SET=0 B2_ILIM_SET=1	3 4.8		A
OC Retry Time	Regulator retry time when it exceeds an output OC level	14		ms
PMOS On-Resistance	I_{SW} = -500mA, VIN_B2 = 3.3V	75		mΩ
NMOS On-Resistance	I_{SW} = 500mA, VIN_B2 = 3.3V	40		mΩ
SW Leakage Current – NMOS	V_{IN_B2} = 5V, V_{SW} = 5V (Note2)	0.1	1	µA
	V_{IN_B2} = 5V, V_{SW} = 5V	0.1	2.5	µA
SW Leakage Current – PMOS	V_{IN_B2} = 5V, V_{SW} = 0V (Note2)	0.1	1	µA
	V_{IN_B2} = 5V, V_{SW} = 0V	0.1	7	µA
Switching Rise / Fall Times	V_{IN_B2} = 5V B2_DRVADJ=00 B2_DRVADJ=01 B2_DRVADJ=10 B2_DRVADJ=11	1.2/1.3 1.1/1.2 1.0/1.1 0.9/1.0		ns
Output Pull Down Resistance	Enabled when regulator disabled	9.40		Ohms

Note1: There is one ball for VIN_B2 and SW_B2 which is good for 2A average lifetime rating at 105 deg C junction.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK3 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B3 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 10mV steps	0.5		1.77	V
Maximum Output Current (Note1)		4			A
Supply Current, Standby	Ultra-Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		11.5		µA
	Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		42		µA
Supply Current, Shutdown	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	5.5	µA
Output Voltage Accuracy – CCM (Note2)	Default output voltage +/- 200mV, I_{OUT} = 1A	-1	V_{NOM}	1	%
Output Voltage Accuracy – CCM	Default output voltage +/- 200mV, I_{OUT} = 1A	-2	V_{NOM}	2	%
Output Voltage Accuracy – DCM(Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM} + 3%	1	%
Output Voltage Accuracy – DCM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage, Low Power Mode Enabled	-2	V_{NOM} + 3%	2	%
Line Regulation	Default output voltage, V_{IN_B3} = 3.3V to 5.5V, CCM mode		0.05		%/V
Load Regulation	Default output voltage, CCM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B3} Rising	92	94	96	%V_{NOM}
Power Good Hysteresis	V_{OUT_B3} Falling		4		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B3} Rising	111	114	117	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B3} Falling		4		%V_{NOM}
Emulated Switching Frequency	B3_FREQ_SEL =00 B3_FREQ_SEL =01 B3_FREQ_SEL =10 B3_FREQ_SEL =11		1.5 2.0 2.5 3.3		MHz
Soft-Start Period – Programmable	10% to 90% V_{NOM} B3_SST=000 B3_SST=001 B3_SST=010 B3_SST=011 B3_SST=100 B3_SST=101 B3_SST=110 B3_SST=111		 50 75 100 150 200 250 500 350		µs
Soft-Start Period Tolerance	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET	B3_ILIM_SET=00 B3_ILIM_SET=01 B3_ILIM_SET=10		4.0 5.0 6.2		A

	B3_ILIM_SET=11		7.8		
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIM_SET	-15	ILIM_SET	15	%
	At other set points	-20	ILIM_SET	20	%
Low Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET (Note3)	B3_ILIM_SET=00 B3_ILIM_SET=01 B3_ILIM_SET=10 B3_ILIM_SET=11		5.0 6.2 7.8 10		A
OC Retry Time	Regulator retry time when it exceeds an output OC level		14		ms
PMOS On-Resistance	I_{SW} = -500mA, VIN_B3 = 3.3V		40		mΩ
NMOS On-Resistance	I_{SW} = 500mA, VIN_B3 = 3.3V		20		mΩ
SW Leakage Current – NMOS	V_{IN_B3} = 5V, V_{SW} = 5V (Note2)		0.1	1	µA
	V_{IN_B3} = 5V, V_{SW} = 5V		0.1	4.3	µA
SW Leakage Current – PMOS	V_{IN_B3} = 5V, V_{SW} = 0V (Note2)		0.1	1.5	µA
	V_{IN_B3} = 5V, V_{SW} = 0V		0.1	6	µA
Dynamic Voltage Scaling Slew Rate	B3_ DVS_SET =00 B3_ DVS_SET =01 B3_ DVS_SET =10 B3_ DVS_SET =11		22.5 11.25 5.625 2.8125		mV/µs
Switching Rise / Fall Times	V_{IN_B3} = 5V B3_DRV_ADJ=00 B3_DRV_ADJ=01 B3_DRV_ADJ=10 B3_DRV_ADJ=11		1.4/1.4 1.2/1.3 1.1/1.2 1.0/1.1		ns
Output Pull Down Resistance	Enabled when regulator disabled		9.40		Ohms

Note1: There is one ball for VIN_B3 and two balls for SW_B3 which is good for 2A and 4A average lifetime rating at 105 deg C junction.
Note2: T_A = 25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK4 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B4 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 50mV steps	0.6		3.7	V
	Configured for 10mV steps	0.6		1.23	V
Maximum Output Current (Note1)		2			A
Supply Current, Standby	Ultra Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		11.5		µA
	Low Power Mode Enabled, Regulator Current Only, non-switching, V_{FB}=103*V_{SET}		42		µA
Supply Current, Shutdown	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	4.5	µA
Output Voltage Accuracy – CCM (Note2)	Default output voltage +/- 200mV, I_{OUT} = 1A	-1	V_{NOM}	1	%
Output Voltage Accuracy – CCM	Default output voltage +/- 200mV, I_{OUT} = 1A	-2	V_{NOM}	2	%
Output Voltage Accuracy – DCM (Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}+ 3%	1	%
Output Voltage Accuracy – DCM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-2	V_{NOM}+ 3%	2	%
Line Regulation	Default output voltage, V_{IN_B4} = 3.3V to 5.5V, CCM mode		0.05		%/V
Load Regulation	Default output voltage, CCM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B4} Rising	92	94	96	%V_{NOM}
Power Good Hysteresis	V_{OUT_B4} Falling		4		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B4} Rising	111	114	117	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B4} Falling		4		%V_{NOM}
Emulated Switching Frequency	B4_FREQ_SEL =00 B4_FREQ_SEL =01 B4_FREQ_SEL =10 B4_FREQ_SEL =11		1.5 2.0 2.5 3.3		MHz
Soft-Start Period – Programmable Range	10% to 90% V_{NOM} B4_SST=000 B4_SST=001 B3_SST=010 B3_SST=011 B3_SST=100 B3_SST=101 B3_SST=110 B3_SST=111		 50 75 100 150 200 250 500 350		µs
Soft-Start Period Tolerance	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET	B4_ILIM_SET=0 B4_ILIM_SET=1		2.0 3.5		A

Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIM_SET	-15	ILIM_SET	15	%
	At other set points	-20	ILIM_SET	20	%
Low Side Peak Current Limit (Cycle-by-Cycle) ILIM_SET (Note3)	B4_ILIM_SET=0 B4_ILIM_SET=1		2.4 4.25		A
OC Retry Time	Regulator retry time when it exceeds an output OC level		14		ms
PMOS On-Resistance	I_{SW} = -500mA, VIN_B4 = 3.3V		60		mΩ
NMOS On-Resistance	I_{SW} = 500mA, VIN_B4 = 3.3V		60		mΩ
SW Leakage Current – NMOS	V_{IN_B4} = 5V, V_{SW} = 5V (Note2)		0.1	1	µA
	V_{IN_B4} = 5V, V_{SW} = 5V		0.1	1.2	µA
SW Leakage Current – PMOS	V_{IN_B4} = 5V, V_{SW} = 0V (Note2)		0.1	1	µA
	V_{IN_B4} = 5V, V_{SW} = 0V		0.1	7	µA
Switching Rise / Fall Times	V_{IN_B3} = 5V B4_DRV_ADJ=00 B4_DRV_ADJ=01 B4_DRV_ADJ=10 B4_DRV_ADJ=11		 1.2/1.3 1.1/1.2 1.0/1.1 0.9/1.0		ns
Output Pull Down Resistance	Enabled when regulator disabled		9.40		Ohms

Note1: There is one ball for VIN_B4 and SW_B4 which is good for 2A average lifetime rating at 105 deg C junction.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK4 ELECTRICAL CHARACTERISTICS: – LDO MODE OPTION

(VIN_B4 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LDO Mode					
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configurable in 50mV steps	0.6		3.75	V
Output Current	VIN_B4 = 2.7V to 5.5V, B4_LDO_ILIM=1	0.4			A
Output Voltage Accuracy (Note 1)	At default output voltage setting VIN_B4 – $V_{B4\_LDO\_OUT}$ > 0.4V	-1	V_{SET}	1	%
Output Voltage Accuracy	At default output voltage setting VIN_B4 – $V_{B4\_LDO\_OUT}$ > 0.4V	-1.5	V_{SET}	1.5	%
Line Regulation	VIN_B4 – $V_{B4\_LDO\_OUT}$ > 0.4V VIN_B4 = 2.7V to 5.5V $I_{B4\_LDO\_OUT}$ = 1mA		0.01		% / V
Load Regulation	$I_{B4\_LDO\_OUT}$ = 1mA to 400mA, B4_LDO_ILIM=1 VIN_B4 – $V_{B4\_LDO\_OUT}$ > 0.4V		0. 8		% / A
Supply Current	Regulator Enabled, No Load, Ultra Low Power Mode		5.5		µA
	Regulator Enabled, No Load, Normal operation mode		10		µA
	Regulator Disabled		0	1	µA
Soft-Start Period – Programmable Range	10% to 90% V_{NOM} B4_SST_LDO=0 B4_SST_LDO=1		140 280		µs
Power Good Threshold	V_{OUT_B4} LDO Rising	90	93	96	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT_B4} LDO Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT_B4} LDO Rising	107	110	113	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT_B4} LDO Falling		3		$\%V_{NOM}$
Dropout Voltage	$I_{B4\_LDO\_OUT}$ = 150mA, VIN_B4 > 2.7V, B4_LDO_ILIM = 0			200	mV
	$I_{B4\_LDO\_OUT}$ = 300mA, VIN_B4 > 2.7V, B4_LDO_ILIM = 1			400	
Discharge Resistance	Enabled when regulator disabled		9.4		Ω
Output Current Limit	VIN_B4 = 2.7V to 5.5V, VIN_B4 – $V_{B4\_LDO\_OUT}$ > 0.4V B4_LDO_ILIM =0 B4_LDO_ILIM =1	300 400	450 550		mA
Short Output Foldback Current	Ratio of current limit when LDO output is short to GND to current limit setting value		25		%

Note1: T_A = 25°C

LDO1 ELECTRICAL CHARACTERISTICS

(VIN_LDO1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.62		5.5	V
Output Voltage Range	Configurable in 50mV steps	0.6		3.75	V
Output Current	VIN_LDO1 = 1.62V to 5.5V, LDO1_ILIM=1	0.4			A
Output Voltage Accuracy (Note1)	Default output voltage +/- 200mV V_{IN_LDO} - V_{LDO1} > 0.4V	-1	V_{NOM}	1	%
Output Voltage Accuracy	Default output voltage +/- 200mV V_{IN_LDO} - V_{LDO1} > 0.4V	-1.5	V_{NOM}	1.5	%
Line Regulation	V_{IN_LDO} - V_{LDO1} > 0.4V V_{IN_LDO} = 3V to 5V I_{LDO1} = 1mA		0.01		% / V
Load Regulation	I_{LDO1} = 1mA to 390mA, ILIM_SCL_LDO1=1 V_{IN_LDO} - V_{LDO1} > 0.4V		0.8		% / A
Supply Current	Regulator Enabled No Load, Ultra Low Power Mode (PMOS) (turn off OV & ILIM protection)		5.5		µA
	Regulator Enabled No Load, Normal Power Mode, (PMOS)		10		µA
	Regulator Disabled		0	1	µA
Soft-Start Period	10% to 90% LDO1_SST = 0. LDO1_SST = 1.		140 280		µs
Power Good Threshold	V_{LDO1} Rising	90	93	96	%V_{NOM}
Power Good Hysteresis	V_{LDO1} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{LDO1} Rising	107	110	113	%V_{NOM}
Overvoltage Fault Hysteresis	V_{LDO1} Falling		3		%V_{NOM}
Dropout Voltage	I_{LDO1} = 200mA, V_{IN_LDO} > 2.7V, LDO1_ILIM=0			200	mV
	I_{LDO1} = 400mA, V_{IN_LDO} > 2.7V, LDO1_ILIM=1			400	mV
	I_{LDO1} = 200mA, V_{IN_LDO} = 1.6V, LDO1_ILIM=0		225		mV
	I_{LDO1} = 400mA, V_{IN_LDO} = 1.6V, LDO1_ILIM=1		670		mV
Discharge Resistance	Enabled when regulator disabled	10	20	35	Ω
Output Current Limit	V_{IN_LDO} = 2.7V to 5.5V, V_{IN_LDO1} - V_{LDO1} > 0.4V LDO1_ILIM=0 LDO1_ILIM=1	300 400	450 550		mA
Short Output Foldback Current	Ratio of current limit when LDO output is short to GND to current limit setting value		25		%

Note1: T_A = 25°C

LDO1 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(VIN_LDO1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load Switch Operation Range	NLSW Mode, Input Voltage Range of VIN_LDO	0.4		Mini-mum of (AVIN-1 or 3.6V)	V
	PLSW Mode, Input Voltage Range of VIN_LDO	1.62		AVIN	V
Load Switch On-Resistance	NLSW Mode, V_{LDO1_IN} = 0.75V I_{LDO1} = 100mA		35		mΩ
	NLSW Mode, V_{LDO1_IN} = 3.3V I_{LDO1} = 100mA		80		mΩ
	PLSW Mode, V_{LDO1_IN} = 3.3V I_{LDO1} = 100mA		200		mΩ
Load Switch Supply Current	NLSW Mode. Load Switch Enabled. No Load, Ultra Low Power Mode (no current limit)		7.7		µA
	NLSW Mode. Load Switch Enabled. No Load, Normal Power Mode		15		
	PLSW Mode. Load Switch Enabled. No Load, Normal Power Mode (option no OV protection)		3.5		
	Load Switch Disabled		0	1	
Soft-Start Period	NLSW Mode		200		µs
Output Current Limit	NLSW Mode: NLSW1_ILIM = 0 NLSW Mode: NLSW1_ILIM = 1 PLSW Mode: @Current Foldback & VINL – VOUT = 0.7V, LDO1_ILIM = 0 PLSW Mode: @Current Foldback &VINL – VOUT = 0.7V, LDO1_ILIM = 1	0.49 0.84 0.3 0.40	0.65 1.1 0.45 0.55		A
Over Voltage Protection Threshold			3.8		V
OV Deglitch Time			45		µs

LDO2 ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configurable in 50mV steps	0.6		3.75	V
Output Current	AVIN = 2.7V to 5.5V, LDO2_ILIM=1	0.4			A
Output Voltage Accuracy (Note1)	At default output voltage setting AVIN - V_{LDO2_OUT} > 0.4V	-1	V_{SET}	1	%
Output Voltage Accuracy	At default output voltage setting AVIN - V_{LDO2_OUT} > 0.4V	-1.5	V_{SET}	1.5	%
Line Regulation	AVIN - V_{LDO2_OUT} > 0.4V AVIN = 2.7V to 5.5V I_{LDO2_OUT} = 1mA		0.01		% / V
Load Regulation	I_{LDO2_OUT} = 1mA to 400mA, LDO2_ILIM=1 AVIN - V_{LDO2_OUT} > 0.4V		0.8		% / A
Supply Current	Regulator Enabled, No Load, Ultra Low Power Mode (Turn off OV & ILIM protection)		5.5		µA
	Regulator Enabled, No Load, Normal Power Mode		10		µA
	Regulator Disabled		0	1	µA
Soft-Start Period	10% to 90% LDO2_SST = 0. LDO2_SST = 1.		140 280		µs
Power Good Threshold	V_{LDO2_OUT} Rising	90	93	96	$\%V_{NOM}$
Power Good Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{LDO2_OUT} Rising	107	110	113	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Dropout Voltage	I_{LDO2} = 200mA, AVIN > 2.7V, LDO2_ILIM=0			200	mV
	I_{LDO2} = 400mA, AVIN > 2.7V, LDO2_ILIM=1			400	
Discharge Resistance	Enabled when regulator disabled	10	20	35	Ω
Output Current Limit	AVIN = 2.7V to 5.5V, AVIN – V_{LDO1} > 0.4V LDO2_ILIM=0 LDO2_ILIM=1	300 400	450 550		mA
Short Output Foldback Current	Ratio of current limit when LDO output is short to GND to current limit setting value		25		%

Note1: T_A = 25°C

LDO2 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load Switch Operation Range	AVIN (Input Voltage) to the LDO2	2.7		5.5	V
PMOS On-Resistance	LDO2 only has PMOS		200		mΩ
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	330	500		mA
Internal PMOS Current Detection De-glitch Time			10		µs
Load Switch Supply Current	PLSW Mode. Load Switch Enabled. No Load, normal power mode (Option no OV protection)		3.5		µA
	Load Switch Disabled		0	1	
Output Current Limit	@Current Foldback & VINL – VOUT = 0.7V, LDO2_ILIM = 0 @Current Foldback & VINL – VOUT = 0.7V, LDO2_ILIM = 1	0.3 0.4	0.45 0.55		A
Internal PMOS Current Shutdown De-glitch Time			5		µs
Internal PMOS Current Shutdown Off time (Retry time)			14		ms
Internal PMOS Soft start	Only used with 3.3V Input, Cout = 1uF		10		mV/ µs
Over Voltage Protection Threshold			3.8		V
OV Deglitch Time			45		µs

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	AVIN = 3.3V			0.4	V
SCL, SDA Input High	AVIN = 3.3V	1.05			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		3400	kHz
SCL Low Period, t_{LOW}		0.125			µs
SCL High Period, t_{HIGH}		0.0625			µs
SDA Data Setup Time, t_{SU}		10			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	65			ns
Stop Setup Time, t_{SP}	For Stop Condition	65			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, T_r	Device requirement			30	ns
SDA Fall Time SDA, T_f	Device requirement			30	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 3.4MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering RESET, IDLE, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: Device Address is 7’h5A

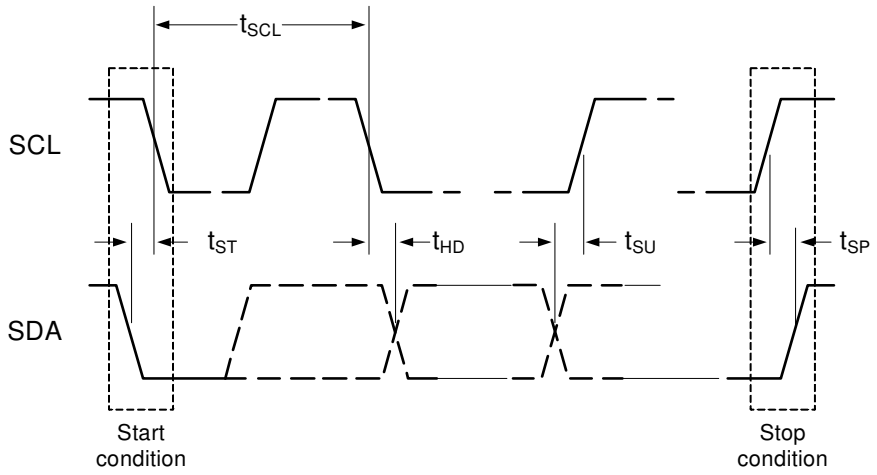


Figure 4: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88420 is a single-chip integrated power management solution designed to power many processors. It integrates four highly efficient buck regulators, and two LDOs. Its high integration and high switching frequency result in an extremely small footprint and low-cost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT88420 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can be masked, and fault levels and responses are configurable via I²C.

Many of the ACT88420 GPIOs and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The first part of the datasheet describes basic IC functionality and default pin functions. The last section of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@qorvo.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88420 uses standard I²C commands. The ACT88420 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Table 1: ACT88420 I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

I²C Registers

The ACT88420 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact Qorvo for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

The ACT88420 contains an internal state machine with five internal states.

RESET State

In the RESET, or "cold" state, the ACT88420 is waiting for the input voltage on AVIN to be within a valid range defined by the UVLO and VIN_OV thresholds. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to POWER SEQUENCE START when the input voltage enters the valid range. The IC transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

GPIO Status Check State

Before entering the power sequence start state, IC will check the GPIOs status to set the regulator operation mode and output voltages. ACT88420 has 4 3-state

GPIOs (GPIO2/3/4/5) that can configure regulator operation mode, default output voltage, and extra power up delay time for Buck4, LDO1, and LDO2.

Buck 1 has two different output voltage options for Buck operation, or it can be set at bypass mode as a load switch. Buck 3 has 3 different output options. Buck 4 has two different output voltage options for Buck operation, or it can be configured as LDO with another output voltage option. LDO 1 has two different output voltage options for LDO operation or set at bypass mode as a load switch.

Buck 2 output voltage can be selected by a 2-state GPIO. Pull high/low for VSET0 and VSET1.

LDO2 operation status can be configured by a 2-state GPIO. If the GPIO is pulled high, it operates at LDO mode; if the GPIO is pulled low, it operates at load switch mode. This feature can be used to automatic select the proper voltage for SoC I/O.

In addition, One GPIO can be used to configure Buck4, LDO1, and LDO2 extra power up delay time. Please see GPIO section for more details.

If the 3-state GPIOs are programmed to configure the regulator operation mode / default output voltages / extra delay time. They CANNOT be re-configured for other features through I²C.

For GPIO states that are used to configure the IC's operation mode, default output voltage, or extra delay time at power up, the ACT88420 only checks these inputs after AVIN is valid at power up. After power up, GPIO status is latched and can NOT be changed on the fly. The output voltages can be changed by I²C after power up. The sleep mode turn on/off sequence can also be changed by I²C after power up, but go back to the default setting if input power is cycled (power on reset = POR).

If the 3-state GPIOs are NOT programmed to configure the regulator operation mode / default output voltages / extra delay time, GPIO2/3/4/5 support change features through I²C command. But will back to default setting after POR.

All 2-state GPIOs (GPIO1/6/7/8) support change features through I²C command. But will back to default setting after POR.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The outputs are enabled and are starting up in this state. The IC immediately transitions to the POWER ON or SLEEP states when the regulators go into regulation. The ACT88420 fault mask bits ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 at startup, so if one regulator has a fault at startup, all other regulators will turn on. After a successful power up, these bits are cleared to 0 so that faults are detected. Any faults after this time result in standard hiccup mode functionality.

POWER ON (Active) State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. The IC only enters the ACTIVE State from the POWER SEQUENCE START State.

SLEEP State

The SLEEP state is a configurable low power state. Based on the system's low power operational requirements, the user can configure the SLEEP state by defining which internal and external regulators are kept on or turned off during the SLEEP state. Each individual regulator output can be programmed to be either on or off in the SLEEP state. Buck3 can also be programmed to regulate to its VSET0/1/2 voltage, or VSET3 voltage (DVS), or be turned off in the SLEEP state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state. The IC can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. **Figure 5** shows how the NVM SLEEP_MODE factory bit sets the I²C and GPIO requirements to enter and exit the SLEEP state.

When the I²C bit SLEEP_MODE = 0, the IC enters SLEEP State with the logical AND of the I²C SLEEP bit and the GPIOs. If more than one GPIO is configured as a SLEEP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the SLEEP State, then only the SLEEP bit controls SLEEP State entry and exit. The IC immediately exits the SLEEP State when the SLEEP bit or a GPIO is de-asserted.

When the I²C bit SLEEP_MODE = 1, the IC enters SLEEP State with the logical OR of the I²C SLEEP bit and the GPIOs. If no GPIOs are configured to control the SLEEP state, then only the SLEEP bit controls the SLEEP State. The IC exits SLEEP State when both I²C and GPIO are de-asserted.

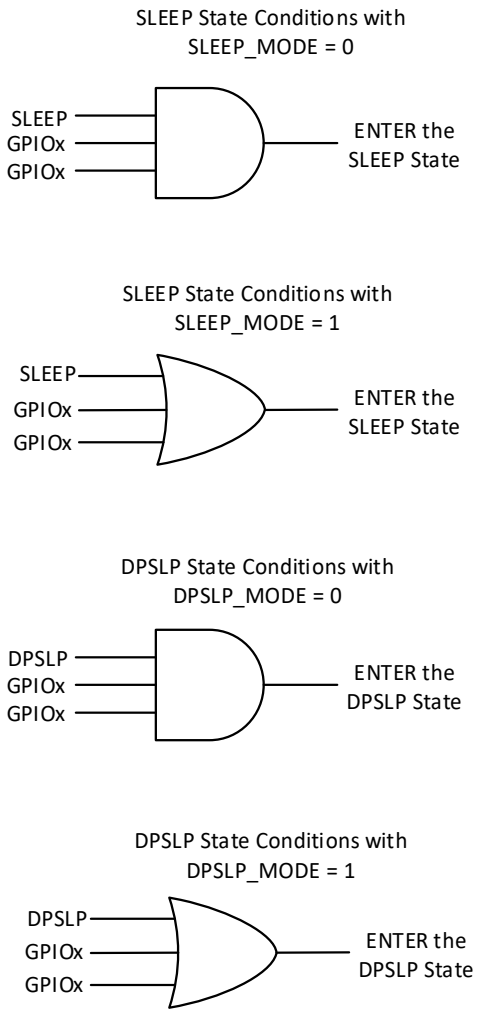


Figure 5: SLEEP and DPSLP State Truth Tables

DPSLP State

The DPSLP State is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP state. It is similar with the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can be programmed to be on or off in the DPSLP state. Buck 3 can also be programed to operate at its VSET0/1/2/3 voltages or be turned off. All outputs can be programmed to have different functionality between the SLEEP and DPSLP states. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state. The IC can enter DPSLP state via the I²C register DPSLP bit or by a GPIOs input. **Figure 5** shows how the NVM DPSLP factory bit sets the I²C and GPIO requirements to enter and exit the DPSLP state.

Any GPIO can be configured to control the DPSLP state without requiring any I²C command. This GPIO hardware function is called PWREN. When the IC is configured to enter DPSLP with the logical AND of the DPSLP I²C bit and a GPIO, the DPSLP state is enabled via I²C, but the IC does not enter the DPSLP state until there is a high to low transition on the PWREN GPIO inputs. When the PWREN input is toggled from low to high, the IC exits DPSLP state.

The PWREN function can be configured to be either edge triggered, or level triggered. The difference between these configurations only affects DPSLP Mode at power up.

Level triggered: If PWREN is low at startup, the IC enters DPSLP immediately after VIN goes above the UV threshold.

Edge triggered: If PWREN is low at startup, the IC ignores PWREN and starts up normally. PWREN must be pulled high and then pulled low to enter DPSLP Mode. If PWREN is high at startup, the IC immediately enters DPSLP Mode when PWREN is pulled low.

Like the SLEEP state, an NVM factory bit DPSLP_MODE sets the logic OR or AND logic between I²C and GPIOs for entering and exiting the DPSLP state.

When DPSLP_MODE = 0, the IC enters DPSLP State with the logical AND of the I²C DPSLP bit and the GPIOs. If more than one GPIO is configured as a DPSLP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the DPSLP State, then only the DPSLP bit controls DPSLP State entry and exit. The IC immediately exits the DPSLP State when the DPSLP bit or a GPIO is de-asserted.

When the I²C bit DPSLP_MODE = 1, the IC enters DPSLP State with the logical OR of the I²C DPSLP bit and the GPIOs. If no GPIOs are configured to control the DPSLP state, then only the DPSLP bit controls the DPSLP State. The IC exits DPSLP State when both I²C and GPIO are de-asserted.

GPIOs can also be programmed to individually turn one or multiple outputs on and off. This on/off GPIO functionality in addition to the PWREN functionality. It provides a wide range of configurability for setting different DPSLP on/off patterns. Note that the GPIOs have eight delay time options for both the rising and falling edges. These settings are 0ms, 0.25ms, 0.5ms, 0.75ms, 1ms, 2ms, 4ms, and 8ms.

For example, in SSD applications, the host can use these GPIOs as PWREN to enter different power save modes like PS3.5 and PS4.

In video applications, the GPIOs can be connected to sensor inputs to trigger the IC to exit the DPSLP mode when a sensor input triggers. The GPIO polarity can be programmed as active HIGH or LOW.

THERMAL State

In the THERMAL state, the IC has exceeded the thermal shutdown temperature. The IC shuts down all regulators and asserts the nRESET to protect the IC in this condition. The THERMAL state can be disabled by setting register 0x01h bit 5 (TMSK) = 1. Note that thermal shutdown fault bit, TWARN, still provides the thermal status even if TMSK = 1.

OVUVFLT State

If one of the regulators exceed an OV or UV level at any time after the soft start ramp has completed, the IC moves to UVOVFLT state. In this state, all regulators shutdown and the IC asserts the nRESET pin. After entering the OVUVFLT state, the IC stays there for 200ms and then goes back to the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state, the IC returns to the OVUVFLT state. The cycle continues until the OV or UV fault is removed, or the input power is removed. This state can only be enabled by clearing an output's OV_FLTMSK or UV_FLTMSK volatile bits to 0 and setting DIS_OVUV_SHD (0x09h[0])=0. The IC does not directly enter OVUVFLT in an overcurrent condition but does enter this state due to the resulting UV condition.

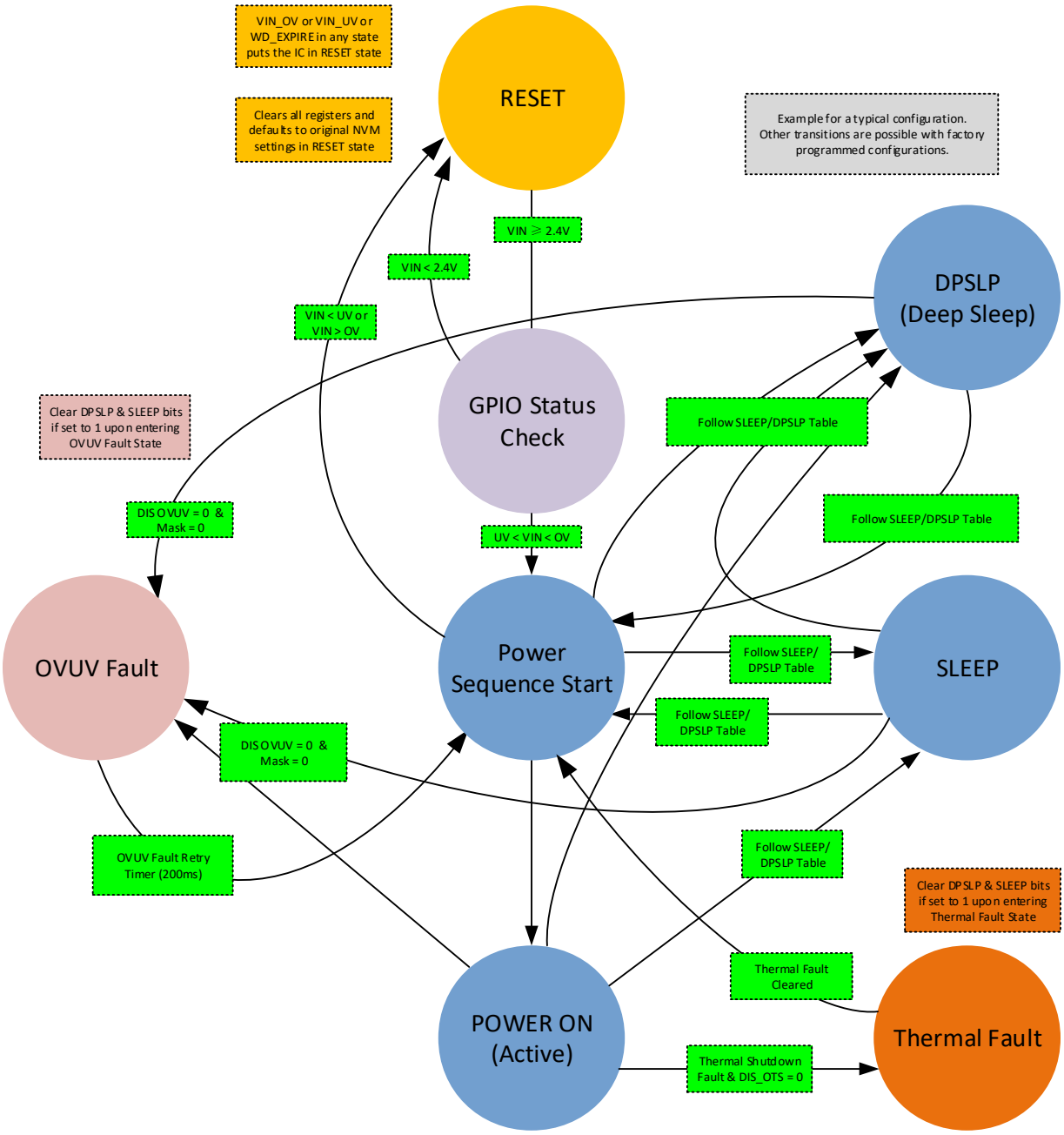


Figure 6: State Machine

Sequencing

The ACT88420 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the six outputs has five basic sequencing parameters: input trigger, turn-on delay, turn-off delay, softstart time, and output voltage. Each of these parameters is controlled via the ICs internal registers. Contact Qorvo for custom sequencing configurations. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Turn on and Turn off Options. The ACT88420 provides several options for enabling the IC. These include automatic power up when input power is applied as well as power up with a digital input signal to a GPIO. The GPIO can be configured to latch the IC on with an input pulse or to be level triggered. Once powered on, the IC can be turned off with either the GPIO or an I²C command.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to a GPIO. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can be changed with a custom CMI configuration. The GPIOs can be internally connected to a power supply's internal POK signal and used as an output to turn on external supplies in the overall sequencing scheme.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ON_DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

With SAVE_CURRENT[]=1, 230us delay time will be added to the regulator that have ON_DELAY=0ms.

Turn-off Delay. The turn-off delay is the time between the input trigger for SLEEP or DPSLP Mode being asserted and when each output starts to turn off. Each output's turn-off delay is configured via its I²C bit OFF_DELAY. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% to its programmed voltage. Each output's softstart time is configured separately via its I²C softstart bits. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Output Voltage. Each buck's output voltage is programmed via its I²C bits Bx_VSETx. Buck 1, Buck 2, and LDO1 have two VSEL options. Buck 3 has 4 VSEL options, Buck 4 has 3 VSEL options, and LDO2 only has one VSEL option. If have multiple output options, VSEL0 voltage setting can be higher or lower than VSEL1/x. For Buck3 regulates to its B3_VSET0/1/2 voltage in ACTIVE mode depends on GPIO configuration. It can be programmed to regulate to B3_VSET3 in DVS mode, SLEEP state or by a GPIO input. Buck3 can change between B3_VSET0/1/2 and B3_VSET3 on-the-fly. Buck1/2/4 cannot change between Bx_VSET0 and Bx_SET1/2 on-the-fly. Buck1/2/4 and LDO1 operate at the voltage configured by GPIO status. The configurable GPIO input must be set before the output is enabled and cannot be changed while the converter is running. The LDO2 only have a single register, LDO2_VSET, to set its output voltage.

Each output's Bx_VSETx voltage can be changed (by one LSB) via I²C after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. All bucks and LDOs output voltages can be changed on-the-fly by writing a new value into their I²C registers. Qorvo recommends minimizing the step size change to prevent the IC from detecting an instantaneous over or under voltage condition due to fault thresholds being immediately changed, but output voltage taking time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for Buck3 is available via the I²C interface. Note that Buck1/2/4 output voltage cannot be changed on-the-fly. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

The IC can be configured to enter DVS by I²C, by a GPIO pin, or when entering SLEEP/DPSLP mode. Entering DVS via I²C requires that the factory bit EN_DVS_BY_I2C be set to 1. To enter DVS, change I²C bit DVS_FROM_I2C from 000 to a different value. The required value is CMI specific. Entering DVS by a GPIO pin or when entering SLEEP/DPSLP are also CMI dependent, so contact Qorvo for details if this is required.

Input Voltage Monitoring (SYSMON)

The ACT88420 monitors the input voltage on the AVIN pin to ensure it is within specified limits for system level operation. The IC "wakes up" and allows I²C communication when AVIN rises above the UVLO threshold. UVLO can be set to either 2.6V or 3.5V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable. However, the outputs do not turn on until AVIN rises above the SYSMON threshold (falling threshold + hysteresis). SYSMON is programmable between 2.725V and 3.1V with 25mV steps. If AVIN drops below the SYSMON falling threshold, the outputs continue to operate normally as long as AVIN is still above UVLO. A GPIO can be programmed to output an active low SYSMON signal so the host can use it for system control purposes. In the meantime, the IC asserts the nIRQ interrupt when AVIN < SYSMON. The nIRQ interrupt can be masked by an NVM register bit. The SYSMON signal output is a real-time signal. The IC also has a real-time status bit, SYSMON, that follows the internal SYSMON signal. Note that the nIRQ output is latched until the SYSMON bit in register 0x00h is read via I²C. **Figure 7** shows the SYSMON details.

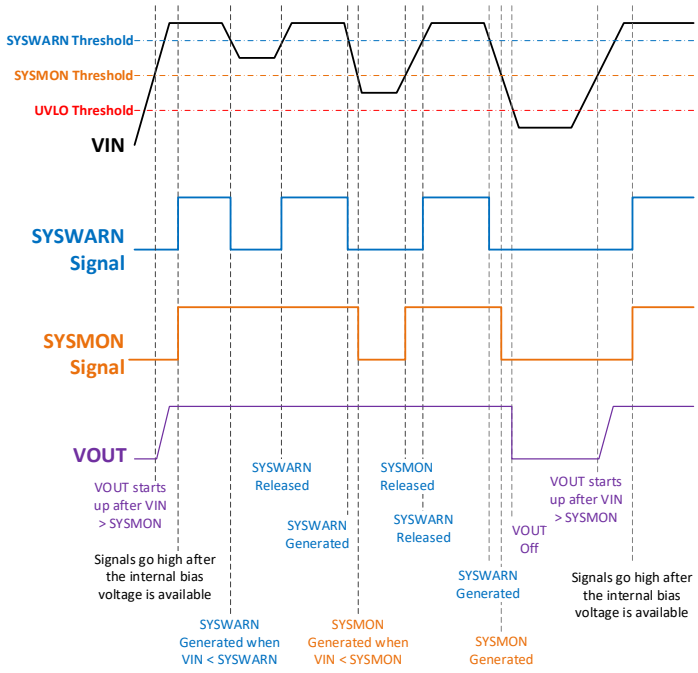


Figure 7: SYSMON and SYSWARN Signals

Input Voltage Warning (SYSWARN)

The ACT88420 also has a second level of input voltage monitoring, SYSWARN. SYSWARN provides another level of low input voltage warning to the host. It is programmable between 2.775V and 3.15V with 25mV steps by the SYSWARN bits. A GPIO can be programmed to output an active low SYSWARN signal so the host can use it for system control purposes when input voltage drops below SYSWARN falling threshold. In the meantime, the IC asserts the nIRQ interrupt when VIN < SYSWARN. The nIRQ interrupt can be masked in the NVM register bit. The SYSWARN signal output is a real-time signal. The IC also has a real-time status bit, SYSWARN, that follows the internal SYSWARN signal. Note that the nIRQ output is latched until the SYSWARN bit in register 0x00h is read via I²C.

Fault Protection

The ACT88420 contains several levels of fault protection, including the following:

Input Overvoltage

Input Undervoltage

Output Overvoltage

Output Undervoltage

Output Current Limit and Short Circuit

Thermal Warning

Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether that fault is masked. The fault bit is latched status bit and keep asserted until read by I²C. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Input Voltage UVLO

The ACT88420 monitors its input voltage at the AVIN pin for a UVLO condition. When the input voltage is below the UVLO threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is not enabled until AVIN goes above the UVLO threshold. When the input voltage goes above UVLO, the IC transitions to the ACTIVE state and starts up normally. The UVLO threshold can be set to either 2.6V or 3.5V by a factory programmable bit, VIN_LVL. Note that VIN_LVL is a Factory Bit and is not user adjustable.

Input Voltage OV

The ACT88420 monitors its input voltage at the AVIN pin for an OV condition. There are two overvoltage levels, POK_OV and VIN_OV. The first level is set by the POK_OV register, which is programmable between 3.5V and 5.6V in 300mV steps. When AVIN goes above the POK_OV threshold, an interrupt is generated on the nIRQ output, but all outputs stay on. If VIN_POK_OV_MASK = 0, the VIN_POK_OV register provides real-time status if. If VIN_POK_OV_MASK = 1, then VIN_POK_OV register is latched until read by I²C. The second level, VIN_OV, is programmable between 3.7V and 5.81V. When the input voltage is above the VIN_OV threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is still enabled while AVIN is above the VIN_OV threshold. When the input voltage goes below the VIN_OV threshold, the IC transitions back to the Power Sequence Start State and starts up normally.

Output Under/Over Voltage

When an output's OV_FLTMSK and UV_FLTMSK (volatile bits) = 0 and DIS_OVUV_SHD (0x09h[0])=0, the ACT88420 monitors the output voltages for under voltage and over voltage conditions. If one output enters an UV/OV fault condition, the IC enters the OVUV Fault State and shuts down all outputs for 200ms. It then enters the POWER START SEQUENCE State and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, just mask the appropriate fault bit. Note that all faults are masked by default. Even when the fault is masked, each output still provides its real-time UV/OV fault status via its fault flag. Masking an OV/UV fault just prevents the fault from being reported via the nIRQ pin. A UV/OV fault condition pulls the nRESET pins low. Note that then nRESET and nIRQ pins are configurable via CMI settings

Output Current Limit

The ACT88420 incorporates different overcurrent protection schemes for the bucks and LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. Buck1 has 3 level of overcurrent protection. The first protection level is when a buck converter's peak switch current reaches 80% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 200ms and restarts. The third level is when the peak switch current reaches 120% of the Cycle-by-Cycle current limit threshold for more than 2 switching cycles. This immediately shuts down the regulator and waits 14ms before restarting.

For Buck2/3/4, if the peak switch current reaches the programmed threshold for 16 consecutive switching cycles, the IC asserts the Buck2/3/4 ILIM bit and asserts nIRQ low. If the short circuit condition and cause UV fault, the IC immediately shuts down all supplies and restarts the system in 200ms with EN_ILIMSD=0, UV_FLT_MSK=0, DIS_OVUV_SHD=0. If Buck2/3/4's

EN_ILIMSD=1, ILIM_FLTMSK=0 and DIS_OVUV_SHD=1, and the short condition lasts for 32 consecutive switching cycles, the output automatically tries to restart in 14ms.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 200ms before restarting.

The overcurrent fault limits for each output are adjustable via I^2C. Overcurrent fault reporting can be masked via I^2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88420 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 155 deg C. A temperature fault moves the state machine to the Thermal Fault State and shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I^2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

GPIO CONFIGURATION

General Description

The ACT88420 has 8 configurable GPIOs. These GPIOs can be configured for many different features include: nRESET, interrupt, external enable, external power good, PWREN, sleep mode, operation mode selector, default output voltage selector, extra power up delay time selector, DVS control, VIN POK, regulator POK, input voltage monitoring, input voltage warning, I²C configurable output, LED drive, ROM mode input, ROM output, power recycle, and push button. These configurations are listed in

Table 2.

Four GPIOs (GPIO2/3/4/5) support 3-state inputs (high, float, and low) that can be used to configure the regulator operation mode, default output voltage, or power delay time. With NVM register configuration, Buck1 and Buck 2, LDO1 and Buck4 operation mode/default output can be controlled by one 3-state GPIO. Buck3 default voltage and Buck4/LDO1/LDO2 extra delay time can be configured by a 3-state GPIO.

The ACT88420 checks the 3-state GPIOs at power up and then latches the status. These GPIOs CANNOT be re-configured for other features through I²C.

3-state GPIOs are programmed to configure regulator extra power up delay time, regulator operation mode and default output voltage.

GPIO1/6/7/8 are standard 2-state GPIOs. After power up, these GPIO features can be reconfigured via I²C, go back to their default setting after a POR.

GPIO6 and GPIO7 support the Push Button functionality, and only GPIO8 supports the LED drive functionality.

GPIO1/6/7/8 can be configured with an internal 200kohm pull-up to VIO.

GPIO2/3/4/5 (the tri-state GPIOs) are automatically pulled up to half of the VIO voltage by an internal 300kOhm resistor at power up. After the GPIO input state is latched, the 300kohm resistor and VIO voltage are disconnected from the GPIO.

Table 2: Configurable GPIO Features

GPIO #	Default Assigned Function	Function																			Input Mode	Output Mode (Open Drain)	Input & Output Delay	Pull Up to Internal VIO or VIO/2	Miscellaneous
		Input Mode									Output Mode														
		3 State Mode Select	2 State Mode Select	PWREN	DVS	ENT_PG	SLEEP (DPSLP)	Push Button	ROM ISP IN	Power Recycle	nINT	ENT_EN	RESET	SYSMON	SYSWARN	ROM Output	LED Drive	VSYS_MON	VOUTx PG	I2C Control Output (Open Drain)					
GPIO1	RESET	No	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	200K	Configurable pull high or not
GPIO2	Buck 1/2 Mode	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	300k	Configurable pull high or not,Pulled up to VIO/2
GPIO3	Buck 3 Mode / Extra Delay Time	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	300k	Configurable pull high or not,Pulled up to VIO/2
GPIO4	LDO1 / Buck 4 Mode	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	300k	Configurable pull high or not,Pulled up to VIO/2
GPIO5	SLEEP / I2C Control Output	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	300k	Configurable pull high or not,Pulled up to VIO/2
GPIO6	LDO2 Mode	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	200K	Configurable pull high or not
GPIO7	PWREN / I2C Control Output	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	200K	Configurable pull high or not
GPIO8	EXT_EN / LED Drive	No	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	200K	Configurable pull high or not
SCL	SCL	No		No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	Yes	No	No	10K	Configurable pull high or not
SDA	SDA	No		No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	Yes	Yes	No	10K	Configurable pull high or not

PWREN

PWREN is a digital input that helps determine if the IC operates in POWER ON mode or DPSLP mode. Refer to the DPSLP State section for details. PWREN has a bidirectional filter to prevent noise from triggering this function. The PWREN signal must be asserted longer than 120µs to enter or exit DPSLP mode.

When PWREN is pulled low to enter the DPSLP state, Buck3 can be configured to regulate to the VSET0 ~ 3 voltages, or turn off. Buck1/2/4 and the LDOs can be configured to either stay on or turn off. This feature provides the system with a single digital input to reconfigure the outputs for a system level low power mode.

nIRQ

The ACT88420 interrupt pin informs the host of any unmasked IC faults. In general, anything with a status change asserts the nIRQ pin. The status changes can be masked by set the corresponding register bits. If interrupt bit is set, the fault must be read before it clears the interrupt bit. If the fault remains the interrupt bit remains set.

The following status changes assert nIRQ:

- Input over-voltage, under-voltage
- Input voltage drops below SYSMON
- Input voltage drops below SYSWARN
- Thermal warning
- Any buck regulator exceeding its warning current for 16 cycles after soft start or a UV/OV condition.
- Watch Dog timer expiring.
- GPIOs wake up mode high to low transition
- Enter ROM mode
- Power recycles

nIRQ can be re-configured to any GPIO pin.

nRESET

The nRESET pin is an open drain 5V compatible output used to issue the main reset to the system's CPU/controller. The output monitors the input voltage and valid regulator outputs to trigger a reset if the input voltage or regulator output voltages are not valid. The nRESET delay time is controlled by the TRST_DLY control bits. The delay time is programmable from 0.5ms to 64ms. nRESET is essentially the same as a Power Good (PG) function but with a fixed delay after all the supply rails go into regulation.

The nRESET output signal is typically tied to all regulators outputs that are necessary for the system controller and I/Os to function properly. Each regulator has a register bit, RST, that determines if that regulator's POK signal is used as an input to the nRESET output signal. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs with RST=1 is not okay, the nRESET output will be asserted low. The ACT88420 allows the user to determine how nRESET responds to a disabled regulator's POK bit. In general, a disabled regulator should not affect the nRESET signal, even if that regulator's POK signal is configured as an input to the nRESET output. This prevents a regulator's POK signal from triggering nRESET when the regulator is commanded by the user to turn off

EXT_EN

The EXT_EN is a GPIO output function that is used to enable an external power supply. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_EN output can be triggered by one of the regulator's POK signals. It can be programmed with a 0, 0.25, 0.5, 0.75, 1, 2, 4, or 8ms delay time using the GPIOx's I²C bits IOx_DLY in registers 0x0Bh ,0x0Ch, 0x27h and 0x28h.

EXT_PG

The EXT_PG is a GPIO input function that is used to determine that an external power supply has turned on and its output voltage is in regulation. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_PG output can be used as an input trigger to turn on one of the ACT88420 regulators.

POK

Any regulator's internal POK bit can be connected to a GPIO to provide an external POK signal. The POK function indicates that a regulator's output voltage is in regulation.

I2C Controlled Output

GPIO can be configured as the I²C controlled open drain output. The register bit can select HIGH or LOW output.

Extra Power Up Delay Options

A 3-state GPIO can be used to configure Buck4/LDO1/LDO2 power up delay time. Each of these three regulators has 4 options for extra power delay time: 0ms, 0.75ms, 1.5ms, and 2.25ms, which can be configured separated when GPIO is high, float, or low.

Table 3 shows an example for different options for extra power up delay. Notice that the actual delay time is the combination of regulator start up delay time and extra delay time. For example, if start up delay time is 0.75ms, extra delay time is 1.5ms, the actual delay time is 2.25ms.

In most of the case, when GPIO is float, all three regulators are all set at 0ms extra delay time. It is okay to have fixed 0ms for GPIO = Float.

It is acceptable to let Buck4, LDO1, and LDO2 have the same start up trigger signal, for instance, VIN UVLO.

Table 3: GPIO Configurable Extra Power Up Delay Time Example

GPIO Status	Regulator	Extra Delay Time
GPIO = LOW	Buck 4	2.25 ms
	LDO 1	0.75 ms
	LDO 2	0 ms
GPIO = Float	Buck 4	0ms
	LDO 1	0ms
	LDO 2	0ms
GPIO = HIGH	Buck 4	+ 2.25 ms
	LDO 1	+ 0.75 ms
	LDO 2	+ 0.75 ms

Regulator Mode & Output Voltage Selection

The 3-state GPIOs that can be configured to set Buck and LDO operation mode and default output voltages. Buck1 has two different output voltage options for Buck operation or can be set at bypass mode as a load switch. Buck3 has 3 different output options. Buck4 has two different output voltage options for Buck operation and one more output option for LDO mode. LDO1 has two different output voltage options for LDO operation or set at bypass mode as a load switch.

In addition, the Buck2 default output voltage can be selected by a 2-state GPIO. Pull high for VSET0, pull low for VSET1. The LDO2 operation status can be configured by a 2-state GPIO. If the GPIO is pulled high, it operates at LDO mode; if the GPIO is pulled low, it operates at load switch mode. This feature can be used to automatic select the proper voltage for multiple load voltage requirements.

The detailed configuration is shown in **Table 4**.

Table 4: Regulator Operation Mode & Default Output Voltage Options

Regulator	High	Floating	Low
Buck 1	LSW Mode	Buck Mode VSEL0	Buck Mode VSEL1
Buck 2	Buck Mode VSEL0	N/A	Buck Mode VSEL1
Buck 3	Buck Mode VSEL0	Buck Mode VSEL1	Buck Mode VSEL2
Buck 4	Buck Mode VSEL0	Buck Mode VSEL1	LDO Mode VSEL2
LDO1	LDO Mode VSEL0	LSW Mode	LDO Mode VSEL1
LDO2	LDO Mode	N/A	LSW Mode

VSELx voltages can be higher or lower or equal with each other. There is no limitation for the relative voltage levels between the VSETx registers.

To reduce the number of GPIOs required to configure the outputs, some factory bits can be set to configure a single GPIO to control Buck1 and Buck2, LDO1 and Buck4 operation modes and default voltage. Contact Qorvo for more detailed info if needed.

With NVM register bit B2_I2C_CF = 1, one GPIO can be used to configure both Buck1 and Buck2. NVM register bit BUCK2_VSET determines VSET value for Buck2 when GPIO high & float. NVM register bit B2VsetGPBK1_L determines VSET value for Buck2 when GPIO is low. GPIO determines Buck1 operation mode and VSET value.

Table 5: Regulator Operation Mode & Default Output Voltage Options for BUCK1/2 when B2_I2C_CF=1

	B2_I2C_CF=1		
GPIO Status	High	Float	Low
BUCK2_VSET = 0 & B2VsetGPBK1_L =0	Buck 1 = LSW	Buck 1 = Buck VSEL0	Buck 1 = Buck VSEL1
	Buck 2 = VSET 0	Buck 2 = VSET 0	Buck 2 = VSET0
BUCK2_VSET = 0 & B2VsetGPBK1_L =1	Buck 1 = LSW	Buck 1 = Buck VSEL0	Buck 1 = Buck VSEL1
	Buck 2 = VSET 0	Buck 2 = VSET 0	Buck 2 = VSET1
BUCK2_VSET = 1 & B2VsetGPBK1_L =0	Buck 1 = LSW	Buck 1 = Buck VSEL0	Buck 1 = Buck VSEL1
	Buck 2 = VSET 1	Buck 2 = VSET 1	Buck 2 = VSET0
BUCK2_VSET = 1 & B2VsetGPBK1_L =1	Buck 1 = LSW	Buck 1 = Buck VSEL0	Buck 1 = Buck VSEL1
	Buck 2 = VSET 1	Buck 2 = VSET 1	Buck 2 = VSET1

With NVM register bit B4_I2C_CF = 1, one GPIO can be used to configure both LDO1 and Buck 4. NVM register bit BUCK4_MODE determines Buck4 default operation in Buck or LDO.

Please note that when GPIO controls both LDO1 and Buck 4, Buck4 is always at Buck VSET0 mode when GPIO is HIGH or LOW, only different when GPIO is floating.

Table 6: Regulator Operation Mode & Default Output Voltage Options for BUCK4 &LDO1 when B4_I2C_CF=1

	B4_I2C_CF=1		
GPIO Status	High	Float	Low
BUCK4_Mode = 1	LDO 1 = LDO VSEL0	LDO 1 = LSW	LDO 1 = LDO VSEL1
	Buck 4 = Buck VSET0	Buck 4 = Buck VSET1	Buck 4 = Buck VSET0
BUCK4_Mode = 0	LDO 1 = LDO VSEL0	LDO 1 = LSW	LDO 1 = LDO VSEL1
	Buck 4 = Buck VSET0	Buck 4 = LDO VSET2	Buck 4 = Buck VSET0

ROM Mode

In SSD applications, there is a chance the firmware, which is stored in the flash, is not loaded properly. In this situation, the SSD fails to startup and work properly. The SSD core must be put back into ROM mode to attempt a restart. In some systems, this requires recycling power, removing and reinserting the SSD card, or manually shorting pins on the SSD module.

ACT88420 includes a ROM Mode feature that significantly simplifies this process at a system level. The ACT88420 ROM Mode forces the SSD core to stay in its ROM state if it does not power up properly.

Figure 8 shows how ROM Mode is implemented. One GPIO is configured as the input for the ISP Ready signal, which is an output from the SSD core after the system powers up. Another GPIO is configured as output for the ROM state signal. After the ACT88420 startup sequence completes, the ACT88420 deasserts its nRESET output and an internal watchdog timer starts monitoring the ISP Ready input signal (active high) to make sure system powers up successfully. If the ISP Ready input is not asserted within 7s (configurable to 7s or 20s), the ACT88420 starts the ROM mode. It turns off all regulator outputs, asserts nRESET low, and asserts the ROM_Only signal low. After a 200ms delay, the ACT88420 restarts the power up sequence. The ROM_Only output stays asserted low until nRESET is de-asserted high to make sure the SSD core stays in the ROM state when powered up.

ROM mode is only activated after nRESET is deasserted. I²C bit NVM ROM_EN enables ROM mode. If the SSD driver needs to enter a power save mode before the 7s watchdog timer expires, the host needs to disable ROM mode before entering the power save mode to avoid the potential risk of activating the ROM_Only and nRESET outputs.

The user can configure the IC to cycle power all outputs if the 7s watchdog timer expires. This solves a system level problem where the host firmware is locked up.

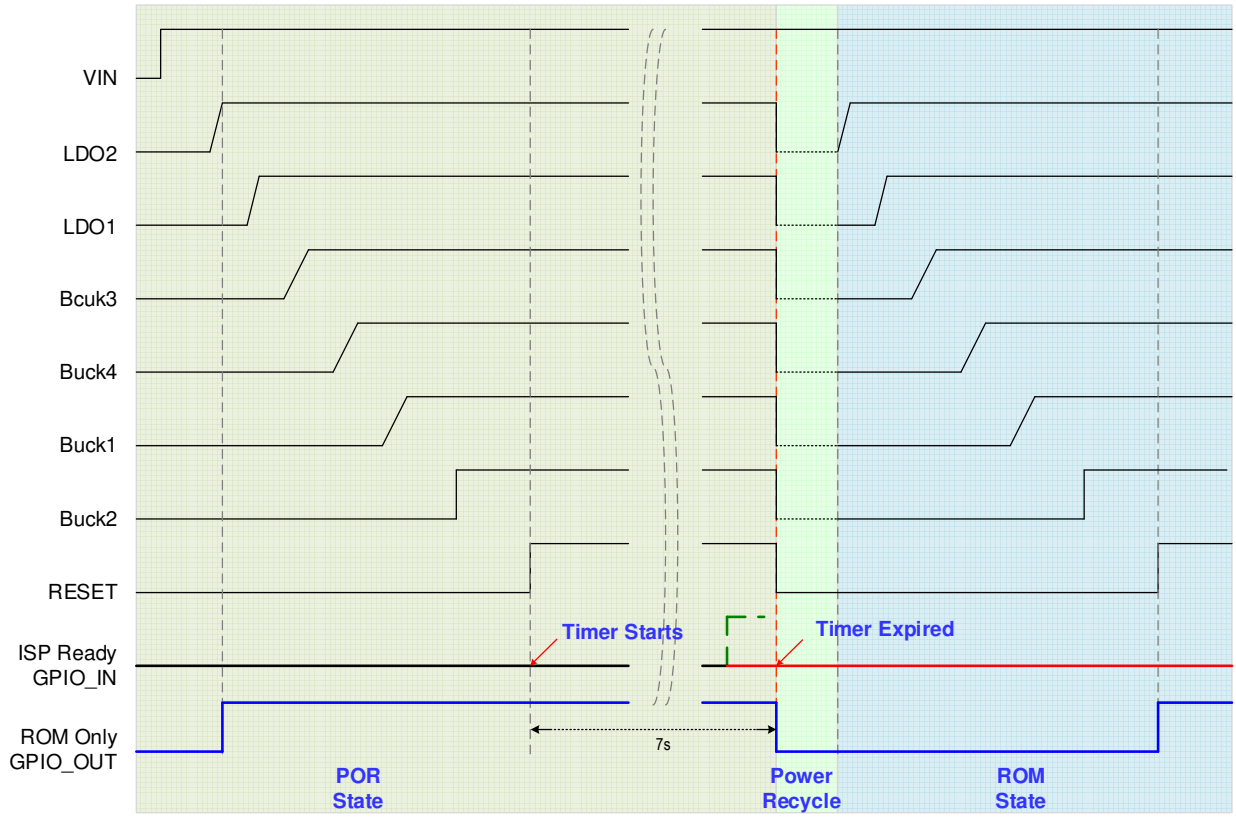


Figure 8: Enter ROM Mode Through GPIO

GPIO Wake up Mode

All GPIOs can be configured to force the IC into and out of DPSLP mode. Any number of GPIOs can be configured for this functionality. Please see the DPSLP State section for details.

Breath LED Drive

GPIO8 can be configured as the breath LED driver, as shown in **Figure 9**. This LED can be enabled or disabled through I²C command. The LED drive duty signal and time period can be configured in the register bits, as shown in **Table 5**, The LED drive current is set by external resistor, the maximum current is limited at 10mA.

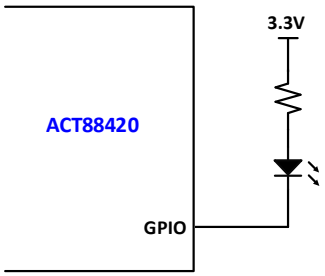


Figure 9: LED Driver Diagram

Table 5: LED Drive Setting

LED Time Register <2:0>	LED TIME PERIOD (s)	LED DUTY <3:0>	LED DUTY CYCLE (%)
000	0.466	000	12.5
001	0.932	001	25
010	1.864	010	37.5
011	2.796	011	50
100	3.728	100	62.5
101	5.59	101	75
110	7.45	110	87.5
111	11.184	111	100

With LED Time Register<2:0>=0b000, 0b001, 0b101, 0b100, 0b110, 0b111

LED DUTY <3:0>	LED DUTY CYCLE (%)
000	12.5
001	25
010	37.5
011	50
100	62.5
101	75
110	87.5
111	100

With LED Time Register<2:0>=0b011 and 0b101

LED DUTY <3:0>	LED DUTY CYCLE (%)
000	12.5
001	25
010	37.5
011	50
100	62.5
101	50
110	87.5
111	100

Push Button (nPB)

The ACT88420 GPIO6/7 can be configured as push button input. It can provide multiple system level functions based on its impedance to ground and "press" time. These functions include: Power On, Power Off, Power Cycle, and Generate Pulse.

Power On:

When PB is pressed for more than 50ms debounce time, IC always enters ACTIVE state from any previous state include SLEEP/DPSLP, UV/OV/OC protection, and POWER OFF states. The SLEEP/DPSLP bits got reset to "0". If the press time is less than 50ms, nothing will happen. Device stays in current state.

Pulse Generate:

If the PB is pressed for more than 50ms, and the EN_PB_PULSE = 1. Beside enters active state, IC also generate a pulse which last 100ms. In the meantime, the interrupt pin is also asserted if it is not masked in the register. This feature allows PB to control the system feature like taking photo every time it is pressed.

Power Off:

Device can be turned off by pressing PB if the EN_PB_OFF = 1 for more than 1s. IC will enter ACTIVE state first when PB is pressed, then enter PWER OFF state when PB is released or pressed for 8s or 12s depends on PB_OFF_Timer setting. There are 4 different options for the timer:

1. 00: 1s < Tpress < 4s, trigger at release
2. 01: 4s < Tpress < 8s, trigger at release
3. 10: Tpress = 8s, trigger at exact 8s
4. 11: Tpress = 12s, trigger at exact 12s

When device enter POWER OFF state, all the outputs are turned off following the turn off sequence.

Power Cycle:

In the case when system needs a complete reset, ACT88420 also provides a Power Cycle function through PB if EN_PB_CYCLE = 1. Similar with Power Off setting, the power cycle timer also has 4 options:

1. 00: 1s < Tpress < 4s, trigger at release
2. 01: 4s < Tpress < 8s, trigger at release
3. 10: Tpress = 8s, trigger at exact 8s
4. 11: Tpress = 12s, trigger at exact 12s

With different time settings, IC can achieve both Power Off and Power Cycle features. For example, set 4s < Tpress < 8s for Power Off and Tpress = 8s for Power Cycle.

Table 6 describes the functions available with the multi-purpose push button pin (nPB pin).

Table 6: Summary of nPB Functions

nPB FUNCTION SUMMARY			
Function	**nPB Time**	**nPB TIME Configuration**	**nPB Configuration**
Power On	t > 50ms		EN_PB_OFF = 0 EN_PB_CYCLE = 0
Generate Pulse	t > 50ms		EN_PB_PULSE = 1
Power Off	1s < t < 4s	PB_OFF_TIMER = 00	EN_PB_OFF = 1
	4s < t < 8s	PB_OFF_TIMER = 01	
	t = 8s	PB_OFF_TIMER = 10	
	t = 12s	PB_OFF_TIMER = 11	
Power Cycle	2s < t < 4s	PB_CYCLE_TIMER = 00	EN_PB_CYCLE = 1
	4s < t < 8s	PB_CYCLE_TIMER = 01	
	t = 8s	PB_CYCLE_TIMER = 10	
	t = 12s	PB_CYCLE_TIMER = 11	

PIN DESCRIPTIONS

The ACT88420 input and output pins are configurable via CMI configurations. The following descriptions refer to the basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

VIN_Bx
VIN_Bx pins are the dedicated input power pins to the buck converters. Each buck converter must be bypassed directly to its PGNDx pin on the top PCB layer with a high-quality ceramic capacitor. Refer to the Step-down DC/DC Converters section for more details.

AVIN
AVIN is the input power to LDO2. It also powers the IC's analog circuitry. AVIN must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

VIN_LDO1
This is the dedicated input power to the LDO1. VIN_LDO1 must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

GPIOx
The ACT88420 has 8 GPIO pins. The GPIOs allow a variety of functions to be implemented. They can be used as inputs or open drain outputs. The GPIOs do not have push-pull functionality. Their polarity can also be changed. These options allow implementation of a variety of system functions plus flexibility of functions tied to each pin. Examples of system functions that can be implemented are regulator mode and output voltage selector, nRESET, Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output from individual regulator power okay (POK) signals, digital output to control external regulators (EXT_EN), digital input to monitor power good signals from external regulators (EXT_PG), digital input to control power sequencing or regulator ON/Off control, control input used to enter or exit sleep (SLEEP) and deep sleep (DPSLP) modes, input to control Dynamic Voltage Scaling (DVS) in the Buck regulators, output for the SYSMON and SYMWARN functions, and an LED driver sink. All GPIOs are 5V compliant and can be pulled to 5V regardless of their bias supply.

SCL, SDA
These are the I^2C clock and data pins to the IC. They have standard I^2C functionality. The SCL and SDA pins have dedicated functionality and cannot be used for other functionality. If I^2C is not needed, these pins should be tied to either ground or to AVIN.

PGNDx
The PGNDx pins are the buck converter power ground pins. They connect directly to the buck converters' low side FETs.

SW_Bx
SWx are the switch nodes for the buck converters. They connect directly to the buck inductor on the top layer.

FB_Bx
These are the feedback pins for the buck regulators. They should be kelvin connected to the buck output capacitors.

LDOx
These are the LDO output pins. Each LDO output must be bypassed to AGND with a 1uF capacitor.

AGND
AGND is the ground pin for the IC's analog circuitry and LDOs. AGND must be connected to the IC's PGNDx pins. The connection between AGND and the PGNDx pins should not have high currents flowing through it.

STEP-DOWN DC/DC CONVERTERS

General Description

The ACT88420 contains four fully integrated step-down converters. Buck1/3 are 4A outputs, while Buck2/4 are 2A output. Buck1 is a fixed frequency, current mode controlled, synchronous PWM converter that achieves peak efficiencies of up to 96.5%. Buck1 switches at 1.125MHz or 2.25MHz. Buck2/3/4 are ACOT mode controlled. All bucks are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

Each buck converter has a dedicated input pin. Buck 1 and Buck 2 share the same PGND, and Buck 3 and Buck 4 share the same PGND. Each buck converter must have a dedicated input capacitor that is optimally placed to minimize its power routing loops. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

Buck1 is configurable as a bypass switch for systems with a 3.3V bus voltage. The bypass switch provides full sequencing capability by allowing the 3.3V bus to be used as the input to the other supplies and still be properly sequenced to the downstream load.

The ACT88420 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

DVS Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to Qorvo's Register Map Definition application note for full details on I²C functionality and programming ranges.

Operating Mode – Buck1

By default, Buck1 operates in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving Low Power Mode, LPM, at light loads to save power. LPM mode reduces conduction losses by preventing the inductor current from going negative.

To further optimize efficiency and reduce power losses at extremely light loads, an additional lower power mode, LPM, is available. LPM minimizes quiescent current in between switching cycles. This reduces input current to approximately 40µA in LPM mode. Light load output voltage ripple increases from approximately 5mV to 10mV when in LPM mode. Light load voltage droop when going from light load to heavier loads is only increased by 2-3mV when in LPM mode. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM.

BUCK1 ULPM

The ACT88420 incorporates an ultra-low power mode, ULPM, that provides significant efficiency improvements at very light loads. This improvement can be as much as 8% with a 2mA load. ULPM mode reduces the buck converters quiescent current from ~40µA to ~10µA. ULPM mode helps systems like SSDs achieve very low power loss at extremely light loads, which is a requirement in their standby modes. ULPM mode regulates the output voltage between 99% to 101% of the setpoint. When the output voltage increases to 101%, the buck converter shuts down to save quiescent current until the output voltage drops to 99%. It then turns back on and increases the output voltage to 101% again. ULPM mode should only be used when the load current is less than 50mA. With higher load currents, the output voltage drop can trigger UVLO before the converter can react. Using it with greater than 50mA results in much lower efficiencies than standard PWM or LPM mode operation.

Operating Mode – Buck2, Buck3, Buck4

By default, Buck2, Buck3, and Buck4 operate in adaptive constant on time (ACOT) mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads to save power.

To further optimize efficiency and reduce power losses at extremely light loads, an additional lower power mode, LPM, is available. LPM minimizes quiescent current in between switching cycles. This LPM mode reduces in-

put current to approximately 40µA at no load. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. Buck2, Buck3 and Buck4's LPM mode can be controlled independently.

BUCK2/3/4 ULPM

Buck2, Buck3, and Buck4 also have the capability to operate in ULPM. This is controlled by each regulator's EN_LPM bit. Setting EN_LPM = 1 enables ultra low power mode while setting EN_LPM = 0 disables it. ULPM provides significant efficiency improvements at very light loads. ULPM mode reduces the buck converters quiescent current from 40µA to ~10µA. ULPM mode helps systems like SSDs achieve very low power loss at extremely light loads, which is a requirement in their standby modes. ULPM mode regulates the output voltage between 101.5% to 102% of the setpoint. When the output voltage increases to 102%, the buck converter shuts down to save quiescent current until the output voltage drops to 101.5%. It then turns back on and increases the output voltage to 102% again. With higher load currents, the efficiency is lower than LPM or normal mode operation.

The ULPM can be figured by register bit. Ideally, Buck 3 and Buck4 can be set at ULPM by default, so when enter PS4 mode, these two Bucks operate in ULPM to minimize the standby current and save power dissipation.

Synchronous Rectification

Buck1/2/3/4 each feature integrated synchronous rectifiers (or LS FETs) to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is enabled via the I²C bit DIS_Pulldown.

Soft-Start

Each buck regulator contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition. The Buck1 softstart time is adjustable to either 250µs or 500µs via its I²C SST register. The Buck2/3/4 softstart time is adjustable to 50µs, 100µs, 250µs, or 500µs via its I²C SST bits.

Output Voltage Setting

Buck1/2/3/4 regulate to the voltage defined by I²C register VSETx.

For Buck1, the output voltage programming range is 0.6V to 3.775V in 25mV steps.

VBUCK1 = 0.6V + VSETx * 0.025V

Where VSETx is the decimal equivalent of the value in I²C VSETx register. The VSETx registers contain an unsigned 7-bit binary value.

For Buck2, the output voltage programming range is 0.6V to 1.87V in 10mV steps.

VBUCK2 = 0.6V + VSETx * 0.01V

For Buck3, the output voltage programming range is 0.6V to 1.87V in 10mV steps.

VBUCK3 = 0.5V + VSETx * 0.01V

For Buck4, the output voltage programming range is 0.6V to 3.75V in 50mV steps.

VBUCK4 = 0.6V + VSETx * 0.05V

Buck4 output voltage step can be configured for 10mV, the programming output voltage range is 0.6V to 1.23V.

VBUCK4 = 0.6V + VSETx * 0.01V

Qorvo recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

100% Duty Cycle Operation

Buck1 supports 100% duty cycle operation. This allows operating conditions where the output voltage is very close to the input voltage. During 100% duty cycle operation, the P-ch high-side power MOSFET is turned on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Because Buck2/3/4 operate in ACOT mode, they require a minimum off-time every switching cycle. The required off-time is 40ns. Buck4 has an additional option that allows almost 100% duty cycle when VIN is close to VOUT. This option, frequency foldback, starts in-

creasing the on-time when the input voltage drops below 125% of the programmed output voltage. This effectively reduces the switching frequency. As the input voltage drops, the on-time increases until it reaches the maximum allowable on-time of 3.5µs. This results in >98% duty cycle with a switching frequency of 285kHz, which supports very low dropout voltages. Enable this option by setting EN_FRQ_FB_HDTY=1.

Dynamic Voltage Scaling

Buck3 supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's operating frequency and input voltage when lower performance is acceptable. In normal operation, each output regulates to the voltage programmed in its I²C register VSET0/1/2. During DVS, the output regulates to VSET3. The output transitions from VSET0/1/2 to VSET3 at a rate determined by the output capacitance and the load current. The outputs transition between VSET3 and VSET0/1/2 by the rate determined by the I²C bits DVS_SET. VSET3 must always be set equal to or lower than VSET0/1/2.

The Buck1/2/4 output voltage can be changed on-the-fly, but the voltage transition is not slew rate controlled. Qorvo recommends changing the output voltage using multiple I²C writes that only change the output voltage one step at a time.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Optimizing Noise

The internal FET rise and fall times can be optimized to minimize switching noise at the cost of lower efficiency via the DRV_ADJ I²C bit.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits.

For Buck1, if the peak switch current reaches the programmed threshold for 16 consecutive switching cycles, the IC asserts the Buck1 ILIM_WARN bit and pulls nIRQ low. A short circuit condition that results in the peak switch current being 122% of the value set by ILIM_SET for more than 2 switching cycles immediately shuts down all supplies, asserts the ILIM bit, and restarts the system in 200ms when EN_ILIM2 (0x4Dh[5])=1, ILIM_FLTMSK=0 and DIS_OVUV_SHD=0. BUCK1 automatically tries to restart in 14ms if EN_ILIM2=1 and its faults are masked.

if Buck1 is configured in bypass mode, shorting VOUT to GND or overload at OUT1 will not trigger UV_FLT due to the Buck1 shutdowns quickly to protect from damaging so does not have enough time to report UV to the MSTR.

For Buck2/3/4, if the peak switch current reaches the programmed threshold for 16 consecutive switching cycles, the IC asserts the Buck2/3/4 ILIM bit and asserts nIRQ low. If the short circuit condition causes UV fault, the IC immediately shuts down all supplies and restarts the system in 200ms with EN_ILIMSD=0, UV_FLT_MSK=0, DIS_OVUV_SHD=0. If Buck2, Buck3, or Buck4's EN_ILIMSD=1, ILIM_FLTMSK=0 and DIS_OVUV_SHD=1, and the short condition lasts for 32 consecutive switching cycles, the output automatically tries to restart in 14ms.

Note that when Buck1 is configured in bypass mode, neither an overload or short circuit condition trigger a UV_FLT condition.

When an overcurrent condition is reported in the ILIM I²C registers, the contents of these registers are latched until read via I²C. Overcurrent and short circuit conditions can be masked via the I²C bit ILIM_FLTMSK. Note that ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 (masked) at power up. The user can un-mask faults by setting these bits to 0 via I²C.

After a buck converter starts up (internal POK=1), if its output voltage drops below the POK falling threshold longer than the blanking time (~28µs to 56µs), the converter enters foldback current mode. This reduces the current limit to 1.25A to reduce output voltage overshoot when the load current drops and the converter recovers from the short circuit condition.

When the on-time is less than 120ns, the high side FET overcurrent circuitry will not have enough time to react. All buck converters include a low-side current limit setting, to account for this condition. When this current limit threshold is reached, the low side FET stays on until the inductor current decays lower than the programmed current threshold. The high side FET cannot turn on again until the low side FET current drops below this value. The Buck1/3 have four low side overcurrent thresholds. The Buck2 low side overcurrent threshold is

3A when ILIM=0 and 4.8A when ILIM=1. The Buck4 low side overcurrent threshold is 2.4A when ILIM=0 and 4.25A when ILIM=1. This function also protects the inductor by preventing current runaway which could saturate the inductor.

Compensation

The buck converters utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Minimum On-Time

The ACT88420 Buck1 minimum on-time is 85ns and the Buck2/3 minimum on-time is 40ns. If the calculated on-time is less than the allowable minimum, then the user must configure the converter to switch at a lower frequency. The Buck1 switching frequency is typically set to 2.25MHz, but this can also be changed to 1.125MHz using a Factory bit. Contact Qorvo for this option. The Buck2/3 switching frequency can be set to 1.5MHz, 2.0MHz, 2.5MHz, or 3.3MHz using the I²C FREQ_SEL bits. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where V_{out} is the output voltage, V_{in} is the input voltage, and F_{SW} is the switching frequency.

BUCK1 Bypass Switch

The ACT88420 provides a bypass mode for 3.3V systems. This allows the 3.3V input voltage to power the ACT88420 regulators and be sequenced to the downstream loads. In bypass mode, the Buck1 P-ch FET acts as a switch and the N-ch FET is disabled. The bypass switch turns on the 3.3V rail with the programmed delay and soft start time.

In bypass mode, the ACT88420 Buck1 I²C registers are reconfigured to the following settings.

1. ILIM register bit is reconfigured to be the output of the internal PMOS Current Detection circuit. This is set to 4.5A typical. If the bypass current exceeds the Internal PMOS Current Detection current, ILIM triggers the nIRQ output and gets latched in the ILIM0 bit if IRQ_nMASK = 1 (not masked). Overcurrent can also be masked with the ILIM_FLTMSK register. Note that ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 (masked) at power up. The user can un-mask faults by setting these bits to 0 via I²C.
2. The POK register bit is reconfigured to the output of the Internal PMOS circuit. The voltage threshold is set to VIN_B1-200mV rising and VIN_B1-300mV falling. If the bypass switch output goes below this value, it triggers an undervoltage fault condition and moves the IC into the OVUVFLT state. This immediately shuts down all regulators including the bypass switch. The system restarts in 200ms, following the programmed startup sequencing. This fault is disabled by default but can be enabled by setting the I²C bit UV_FLTMSK = 0.

Note that in bypass mode, the overvoltage protection is set to 3.8V with a 10µs deglitch time. If AVIN goes above 3.8V, the bypass switch is turned off and retries after 200ms If OV_FLTMSK=0 and DIS_OVUV_SHD=0

Buck1 can be configured to enter bypass mode with a GPIO pin. With this configuration, the GPIO is called the MODE pin. Pulling MODE low puts Buck1 in Buck mode. Pulling MODE high puts Buck1 in bypass mode. Note that the MODE pin must be fixed either high or low at startup and that it cannot be changed on-the-fly.

Buck4 LDO Operation

Buck 4 also integrates a LDO with 400mA current capability. The Buck / LDO mode can be selected through CMI or GPIO. The output must be configured into either the Buck or the LDO mode before turning on the output. The mode cannot be changed on-the-fly while the output is turned on. The LDO output voltage is set in VSEL2. When operating in LDO mode, remove the Buck4 inductor and leave SW_B4 floating.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Note that even though each buck converter has separate input pins, all input pins must be connected to the same voltage potential. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input

capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VIN_Bx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The ACT88420 buck converters are optimized for operation with a 0.47µH inductor. They can also be used with 1µH inductors. Choose an inductor with a low DC resistance and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where VOUT is the output voltage, VIN is the input voltage, FSW is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The ACT88420 is designed to use small, low ESR, ceramic output capacitors. Bucks typically require a 22µF output capacitor. To ensure stability, the actual Buck1/3 capacitance must be greater than 12µF while Buck 2/4 must be greater than 6µF. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

LDO CONVERTERS

General Description

The ACT88420 contains two fully integrated low dropout linear regulators (LDO). LDO1 and LDO2 are 400mA outputs. The LDOs require only two small external components (Cin, Cout) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions. Both LDOs can also be configured for load switch mode.

LDO1 has a dedicated input pin, VIN_LDO, so it can operate from different input voltage than the Buck converters and from LDO2. LDO2 input voltage comes from the AVIN pin.

Enable / Disable Control

When power is applied to the IC, all LDOs automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C or GPIO. Each CMI version requires a different set of commands to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. Each LDO's discharge function is enabled via its I²C bit DIS_PULLDOWN_Lx.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up in a monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is adjustable to either 140µs or 280µs via its I²C bits SST_LDOx.

Output Voltage Setting

LDO1 has two default output voltage options, regulates the voltage defined by I²C registers LDO1_VSET0 and LDO1_VSEL1. LDO2 regulate to the voltage defined by I²C registers LDO2_VSET. Unlike the LDO1, the LDO2 only have one VSET register.

The LDO output voltage programming range is 0.6V to 3.75V in 50mV steps.

V_{LDOx} = 0.6V + LDOx_VSET * 0.05V

Where LDOx_VSETx is the decimal equivalent of the value in the register. LDOx_VSET contains an unsigned 6-bit binary value. As an example, if LDO1's LDO1_VSET register contains 011000b (24 decimal), the output voltage is 1.8V.

Qorvo recommends that an LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent and short circuit protection. The overcurrent threshold is set by their I²C bits. The LDO1 current limit is set to 0.4A or 0.5A by the ILIM_SCL_LDO1 I²C bit. The LDO2 current limit is set to 0.4A or 0.5A by the ILIM_SCL_LDO2 I²C bit.

In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. When the current limiting results in a drop-in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts nIRQ low, and enters the UVLOFLT state. The IC restarts in 200ms and starts up with default sequencing. Note that ILIM_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 (masked) at power up. The user can un-mask faults by setting these bits to 0 via I²C.

Input Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor. When LDOx_ILIM is set to 0.4A, a 1µF capacitor is typically suitable. The minimum allowable capacitance value is 0.7µF. When LDOx_ILIM is set to 0.5A, 2.2µF capacitor is typically suitable, with a minimum allowable capacitance value of 1.5µF. In both cases, the maximum allowable output capacitance is 100µF. The output capacitor should be a X5R, X7R, or similar dielectric.

LDO1 Load Switch Mode

LDO1 has the option to be used as a load switch. This option is only accessible via factory I²C bits and requires a custom CMI. When in load switch mode, LDO1 still retains overcurrent protection. Overvoltage and undervoltage protection are disabled.

In load switch mode, LDO1 has two operating options: NLSW and PLSW modes. In NLSW mode, the load switch is an n-ch FET. NLSW mode is used with an input voltage between 0.4V and AVIN-1V. Due to the lower n-ch FET Rdson, NLSW mode can operate with

up to 1A of bypass current while maintaining a low voltage drop. The NLSW current limit is set to 0.65A or 1.11A by the NLSW1_ILIM_SCL I²C bit.

In PLSW mode, the load switch is a p-ch FET. It can operate with an input voltage between 1.62V and AVIN. The PLSW current limit is set to 0.4A or 0.5A by the ILIM_SCL_LDO1 I²C bit.

NLSW and PLSW modes can only be fixed at the factory.

NLSW mode has a fixed 200µs softstart time. PLSW mode relies on the current limit setting for softstart.

NLSW mode does not have OV protection, PLSW has the OV protection.

The LDO1 POK is functional in Load Switch mode. The POK signal is asserted when the switch is enabled and is not in current limit. In bypass mode, the over voltage protection is set at 3.8V with a 10us deglitch time. If VIN_LDO goes above 3.8V, the load switch is turned off and retries after 200ms.

LDO2 Load Switch Mode

LDO2 has the option to be used as a load switch. When in load switch mode, LDO2 still retains overcurrent protection. Overvoltage and undervoltage protection are disabled.

LDO2 only has PLSW mode. In PLSW mode, the load switch is a p-ch FET. It can operate with an input voltage between 1.62V and AVIN. The PLSW current limit is set to 0.4A or 0.5A by the ILIM_SCL_LDO2 I²C bit.

Besides pre-programed in factory mode to set the LDO/LSW modes, one GPIO can be programmed as the MODE_LDO2 to set the LDO2 at LDO mode or load switch mode as well. Before power up, ACT88420 detects MODE_LDO2 input voltage. If the input is HIGH (> 1.2V), LDO2 will be set at LDO mode. If the input is LOW (<0.4V), LDO2 will be set at LSW mode and take AVIN as input. MODE_LDO2 pin has an internal 200k pull down resistor, so if no input at MODE_LDO2 pin, it is LOW and set at LSW mode. LDO2 does have OV protection.

The LDO2 POK is functional in Load Switch mode. The POK signal is asserted when the switch is enabled and is not in current limit. In bypass mode, the over voltage protection is set at 3.8V with a 10us deglitch time. If VIN_LDO goes above 3.8V, the load switch is turned off and retries after 200ms.

Ultra-Low Power Mode

LDO1 and LDO2 have the ultra-low power mode where the stand-by currents are minimized. It is helpful to meet system power dissipation requirements like PS4. Both LDO mode and LSW mode operation have ultra-low power mode. LDO1 and LDO2 have separated LPM NVM bits that enter ultra-low power mode when asserted. Ultra-low power can be entered/exited by I²C command.

Ultra-low power has some limitations like OV and ILIM protection will be disabled. NVM bits can configure whether ILIM is activated in LSW operation during ultra-low power mode.

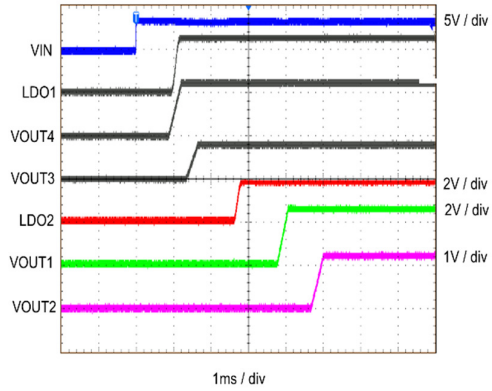
PC BOARD LAYOUT GUIDANCE

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT88420 PCB. Refer to the Qorvo ACT88420 Evaluation Kits for layout examples

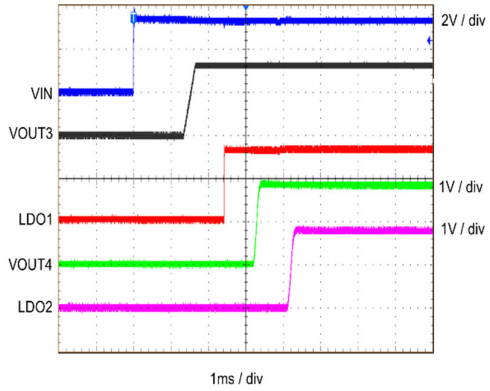
1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VIN_Bx input pin and PGNDx power ground pin on the same PCB layer as the IC. Avoid using vias.
2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. Place the LDO input capacitors close to their input pins. Connect their ground pins into the ground plane that connects the IC's PGNDx pins.
4. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
5. Connect the PGNDx ground pins and the AGND ground pin directly to the PGND under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
6. Connect the VIN input capacitor to the AGND ground pin.
7. Remember that all open drain outputs need pullup resistors.
8. Connect the PGND directly to the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations.

TYPICAL OPERATING CHARACTERISTICS

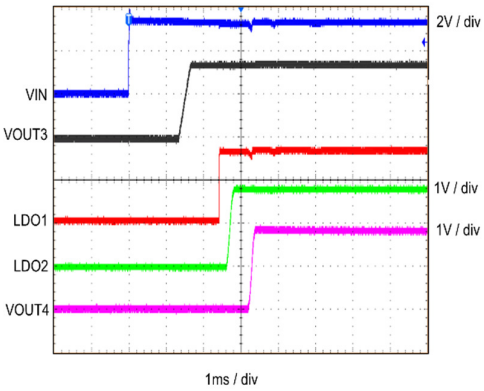
Start up with hot plug



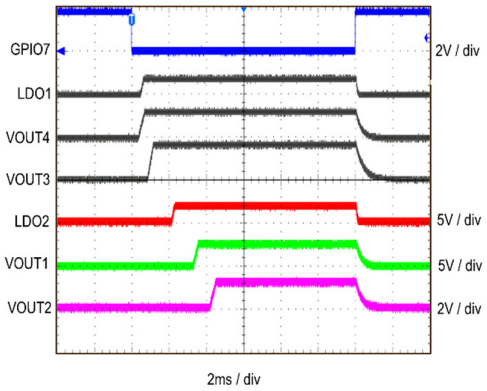
Start up with GPIO3=H



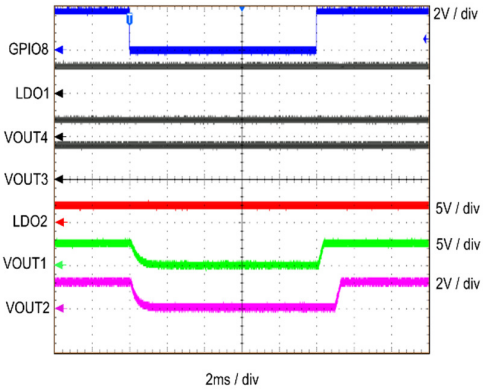
Start up with GPIO3=L

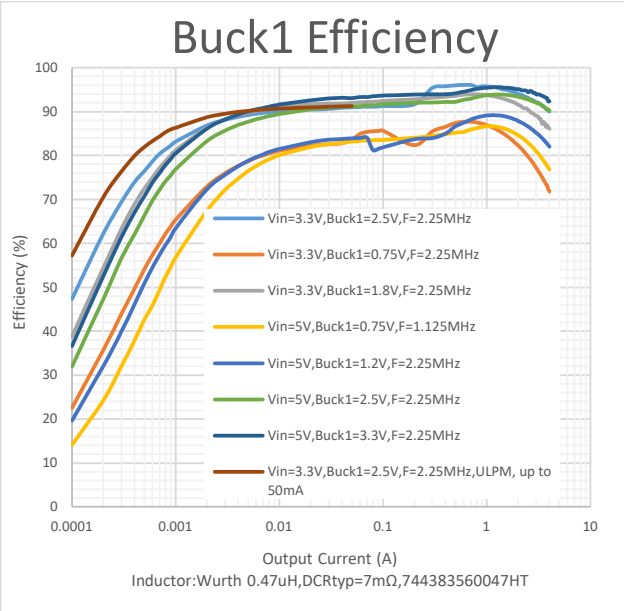


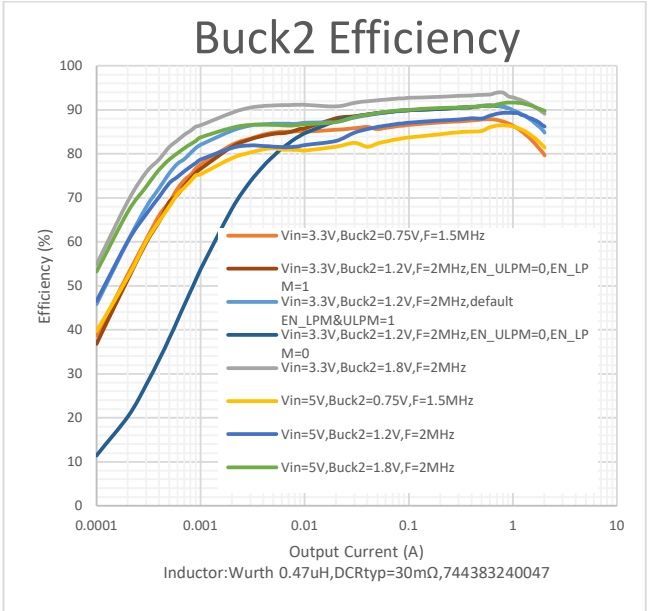
GPIO7-PWRDIS Function

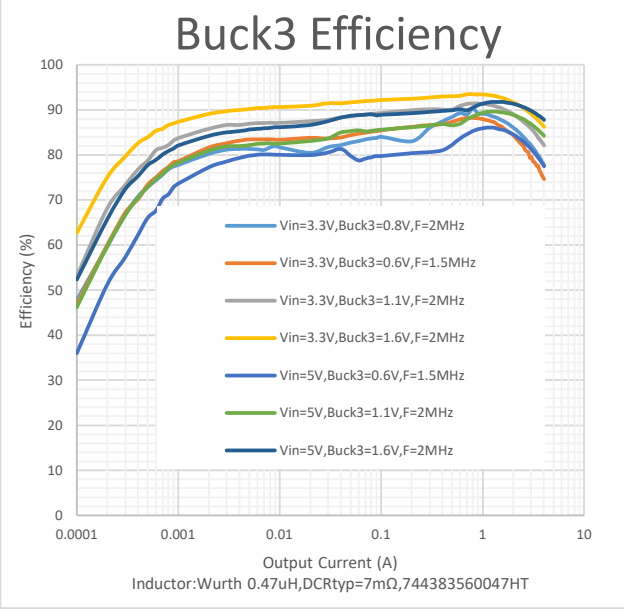


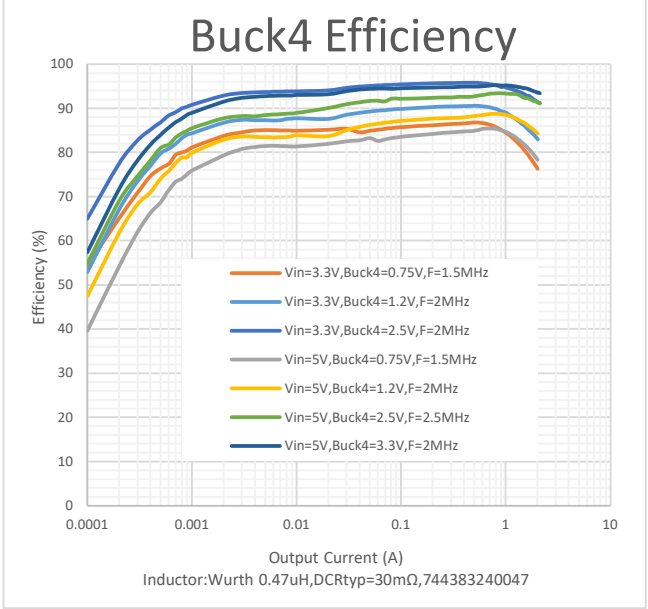
GPIO8 DPSLP Mode



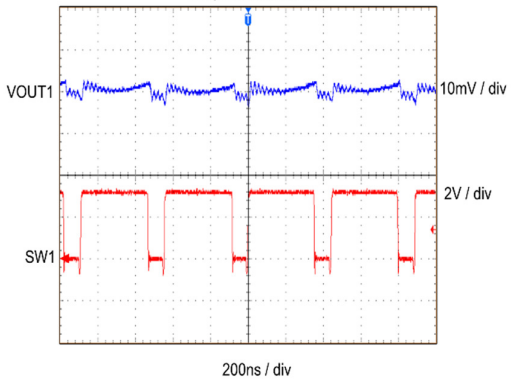

Buck1 Efficiency
Efficiency (%)
Output Current (A)
Inductor:Wurth 0.47uH,DCRtyp=7mΩ,744383560047HT
Vin=3.3V,Buck1=2.5V,F=2.25MHz
Vin=3.3V,Buck1=0.75V,F=2.25MHz
Vin=3.3V,Buck1=1.8V,F=2.25MHz
Vin=5V,Buck1=0.75V,F=1.125MHz
Vin=5V,Buck1=1.2V,F=2.25MHz
Vin=5V,Buck1=2.5V,F=2.25MHz
Vin=5V,Buck1=3.3V,F=2.25MHz
Vin=3.3V,Buck1=2.5V,F=2.25MHz,ULPM, up to 50mA


Buck2 Efficiency
Efficiency (%)
Output Current (A)
Inductor:Wurth 0.47uH,DCRtyp=30mΩ,744383240047
Vin=3.3V,Buck2=0.75V,F=1.5MHz
Vin=3.3V,Buck2=1.2V,F=2MHz,EN_ULPM=0,EN_LPM=1
Vin=3.3V,Buck2=1.2V,F=2MHz,default EN_LPM&ULPM=1
Vin=3.3V,Buck2=1.2V,F=2MHz,EN_ULPM=0,EN_LPM=0
Vin=3.3V,Buck2=1.8V,F=2MHz
Vin=5V,Buck2=0.75V,F=1.5MHz
Vin=5V,Buck2=1.2V,F=2MHz
Vin=5V,Buck2=1.8V,F=2MHz

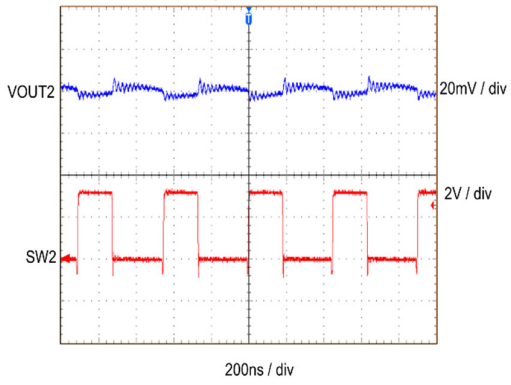

Buck3 Efficiency
Efficiency (%)
Output Current (A)
Inductor:Wurth 0.47uH,DCRtyp=7mΩ,744383560047HT
Vin=3.3V,Buck3=0.8V,F=2MHz
Vin=3.3V,Buck3=0.6V,F=1.5MHz
Vin=3.3V,Buck3=1.1V,F=2MHz
Vin=3.3V,Buck3=1.6V,F=2MHz
Vin=5V,Buck3=0.6V,F=1.5MHz
Vin=5V,Buck3=1.1V,F=2MHz
Vin=5V,Buck3=1.6V,F=2MHz


Buck4 Efficiency
Efficiency (%)
Output Current (A)
Inductor:Wurth 0.47uH,DCRtyp=30mΩ,744383240047
Vin=3.3V,Buck4=0.75V,F=1.5MHz
Vin=3.3V,Buck4=1.2V,F=2MHz
Vin=3.3V,Buck4=2.5V,F=2MHz
Vin=5V,Buck4=0.75V,F=1.5MHz
Vin=5V,Buck4=1.2V,F=2MHz
Vin=5V,Buck4=2.5V,F=2.5MHz
Vin=5V,Buck4=3.3V,F=2MHz

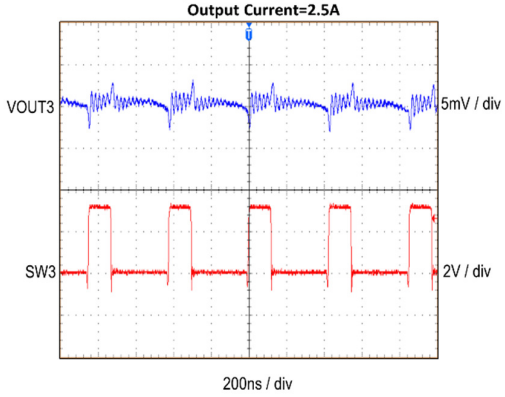
Output1 Voltage Ripple
Output Current=2A



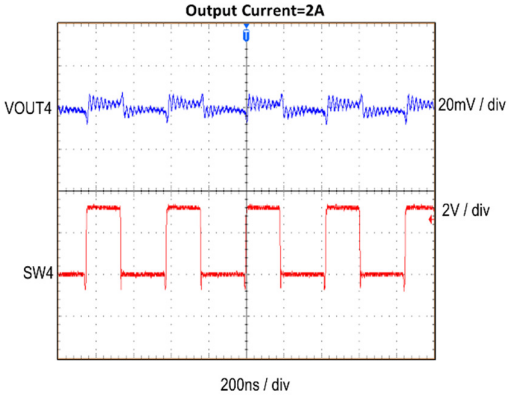
Output2 Voltage Ripple
Output Current=1.5A



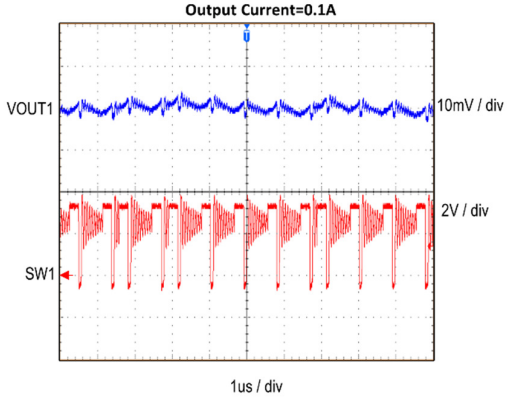
Output3 Voltage Ripple
Output Current=2.5A



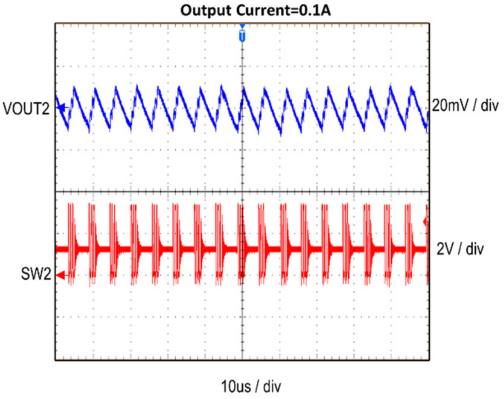
Output4 Voltage Ripple
Output Current=2A

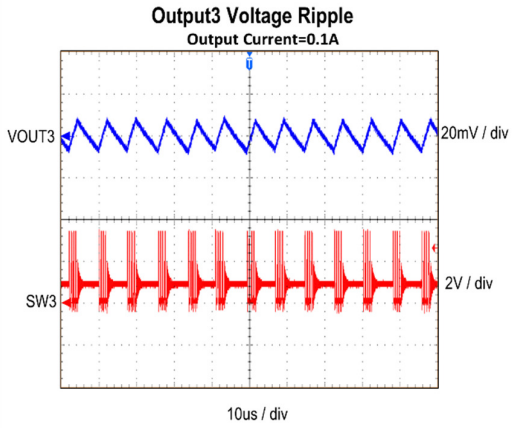


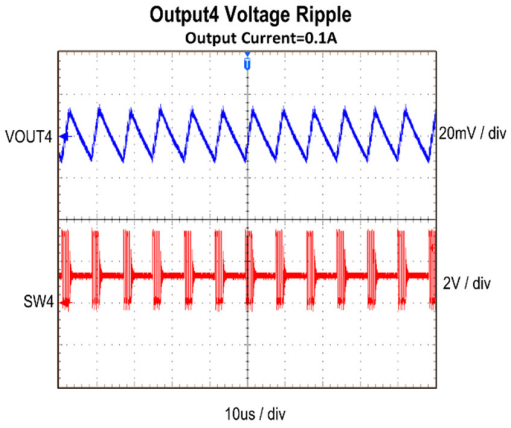
Output1 Voltage Ripple
Output Current=0.1A

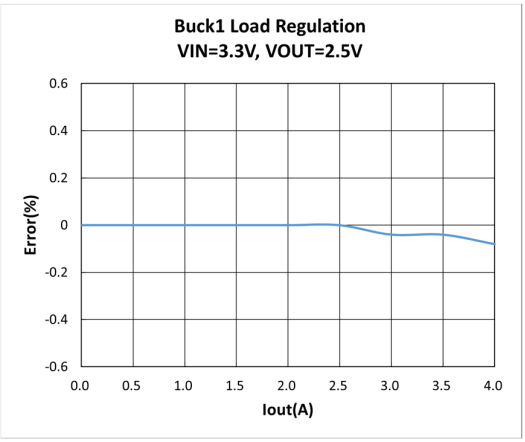


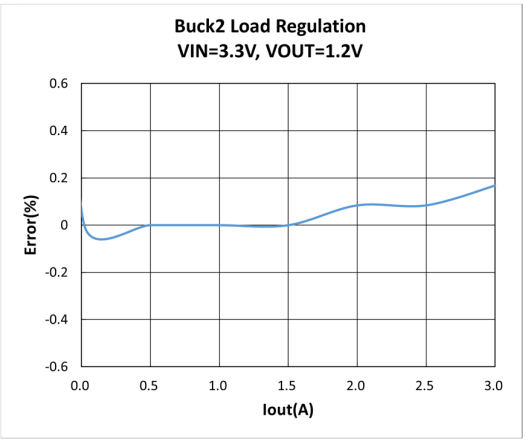
Output2 Voltage Ripple
Output Current=0.1A

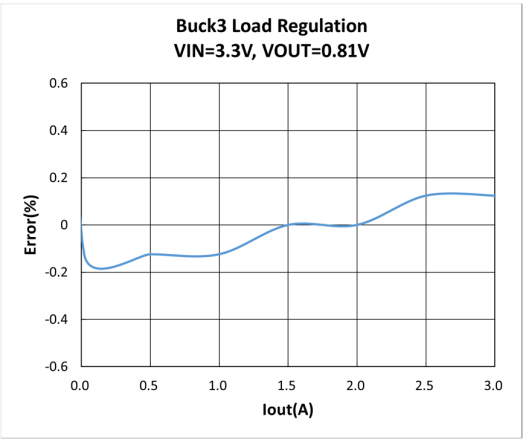


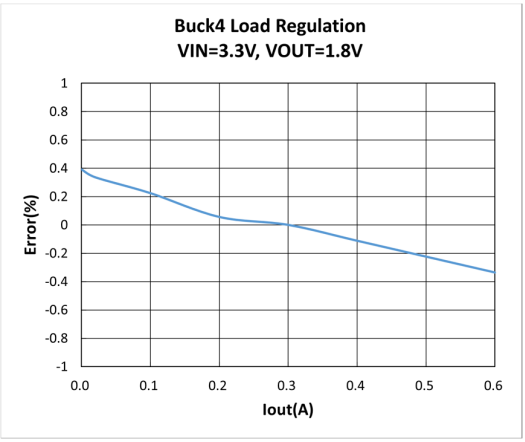

Output3 Voltage Ripple
Output Current=0.1A
VOUT3
20mV / div
SW3
2V / div
10us / div

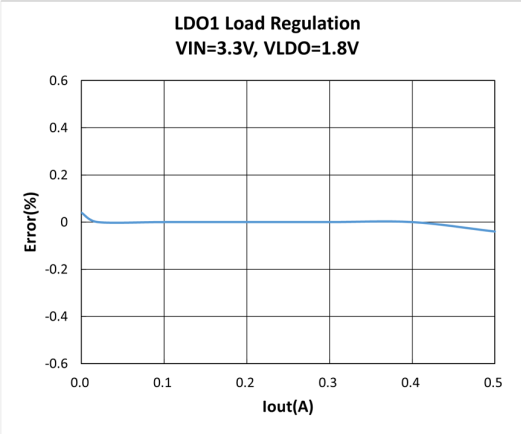

Output4 Voltage Ripple
Output Current=0.1A
VOUT4
20mV / div
SW4
2V / div
10us / div

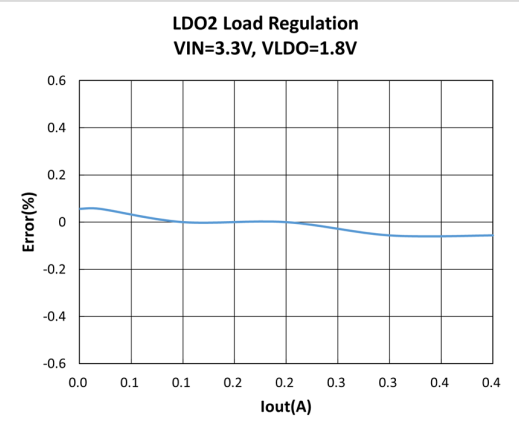

Buck1 Load Regulation
VIN=3.3V, VOUT=2.5V
Error(%)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
Iout(A)

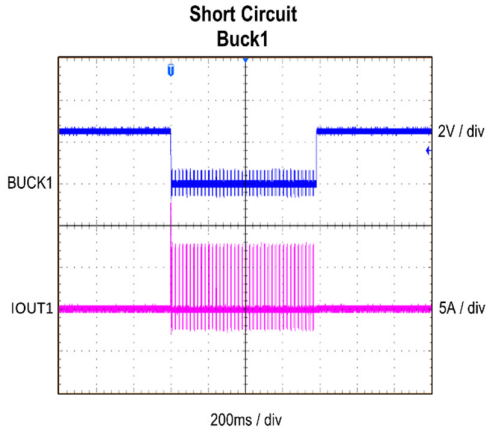

Buck2 Load Regulation
VIN=3.3V, VOUT=1.2V
Error(%)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.0 0.5 1.0 1.5 2.0 2.5 3.0
Iout(A)

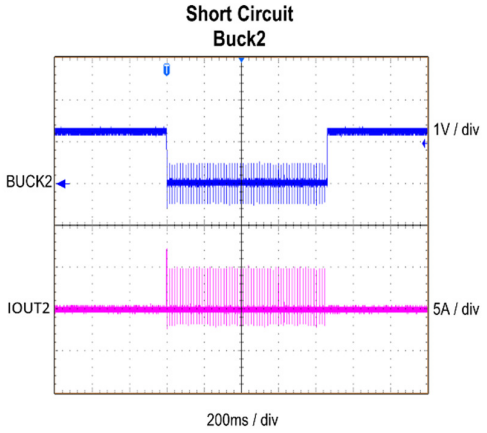

Buck3 Load Regulation
VIN=3.3V, VOUT=0.81V
Error(%)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.0 0.5 1.0 1.5 2.0 2.5 3.0
Iout(A)

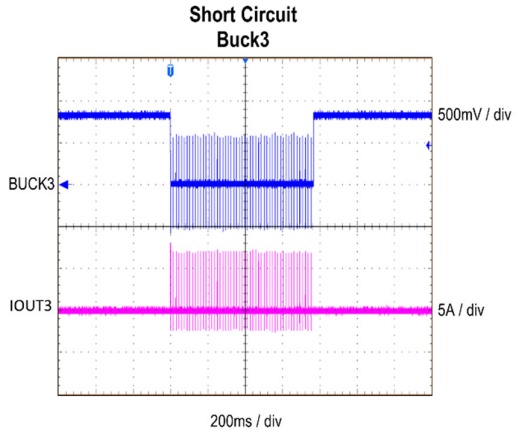

Buck4 Load Regulation
VIN=3.3V, VOUT=1.8V
Error(%)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.0 0.1 0.2 0.3 0.4 0.5 0.6
Iout(A)

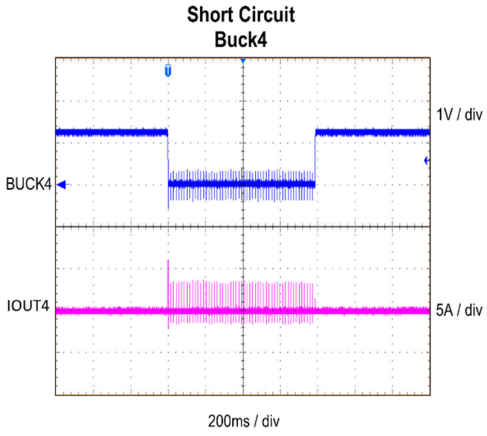

LDO1 Load Regulation
VIN=3.3V, VLDO=1.8V
Error(%)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.0
0.1
0.2
0.3
0.4
0.5
Iout(A)


LDO2 Load Regulation
VIN=3.3V, VLDO=1.8V
Error(%)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0.0
0.1
0.1
0.2
0.2
0.3
0.3
0.4
0.4
Iout(A)

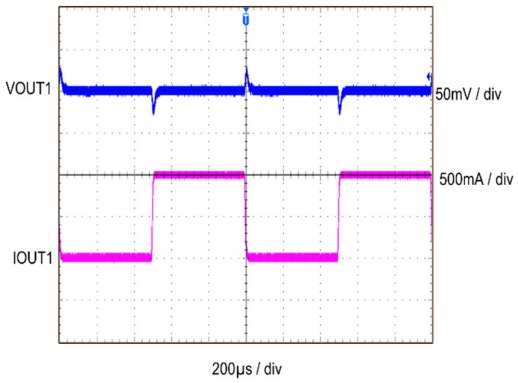

Short Circuit
Buck1
BUCK1
2V / div
IOUT1
5A / div
200ms / div


Short Circuit
Buck2
BUCK2
1V / div
IOUT2
5A / div
200ms / div

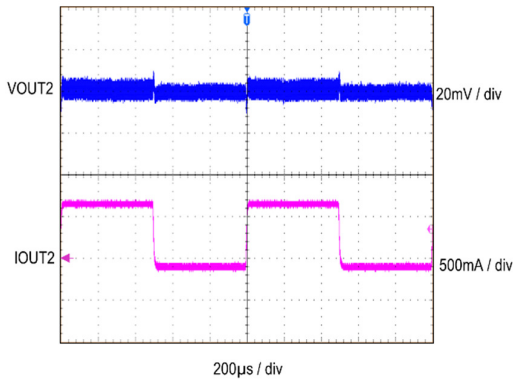

Short Circuit
Buck3
BUCK3
500mV / div
IOUT3
5A / div
200ms / div


Short Circuit
Buck4
BUCK4
1V / div
IOUT4
5A / div
200ms / div

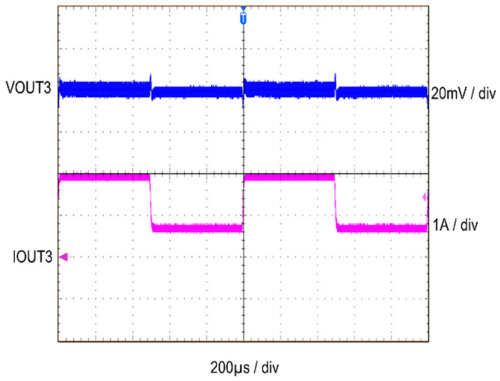
Load Transient
Buck1 Vout=2.5V
500mA to 1500mA



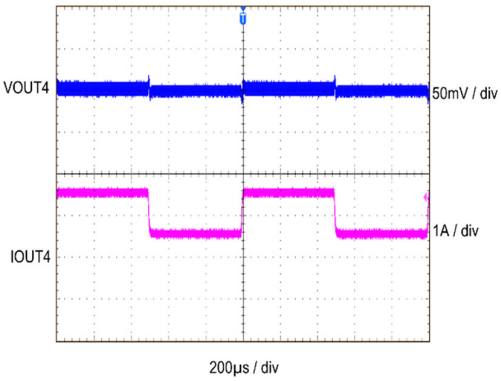
Load Transient
Buck2 Vout=1.2V
375mA to 1125mA



Load Transient
Buck3 Vout=0.81V
625mA to 1875mA



Load Transient
Buck4 Vout=1.2V
500mA to 1500mA



CMI OPTIONS

This section provides the basic default configuration settings for each available ACT88430 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 102: ACT88420-102T

The ACT88420-102 is a joint development between Qorvo and Solidigm, and is specifically designed to power the SM2269 Solid State Disk (SSD) controller. The ACT88420-102 is designed for a 3.3V input voltage. The output voltages and sequencing are directly compatible with the SM2269. Contact Qorvo for more details about this IC.

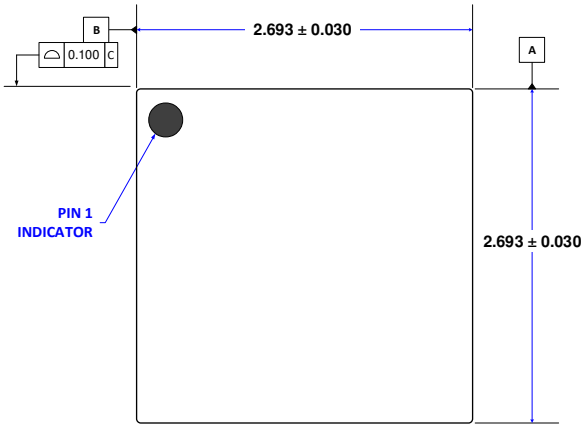
CMI 103: ACT88420-103T

The ACT88420-103 is a joint development between Qorvo and SSSTC, and is specifically designed to power the Phison PS5018 Solid State Disk (SSD) controller. The ACT88420-103 is designed for a 3.3V input voltage. The output voltages and sequencing are directly compatible with the PS5018. Contact Qorvo for more details about this IC.

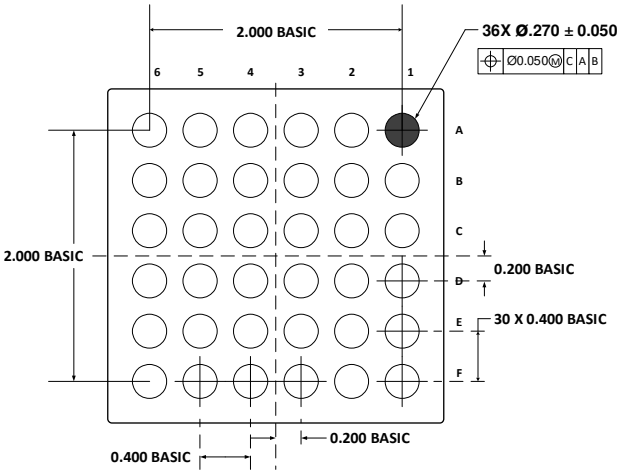
CMI 104: ACT88420-104T

The ACT88420-104 is a joint development between Qorvo and Tenafe, and is specifically designed to power Tenafe's TC2200 Solid State Disk (SSD) controller. The ACT88420-104 is designed for a 3.3V input voltage. The output voltages and sequencing are directly compatible with the TC2200. Contact Qorvo for more details about this IC.

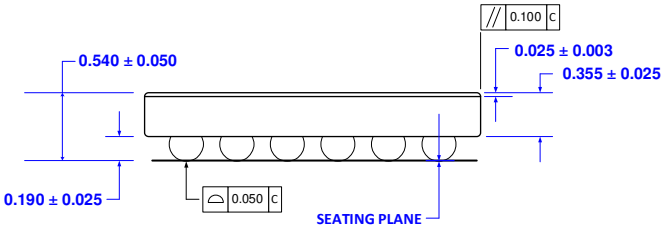
PACKAGE OUTLINE AND DIMENSIONS



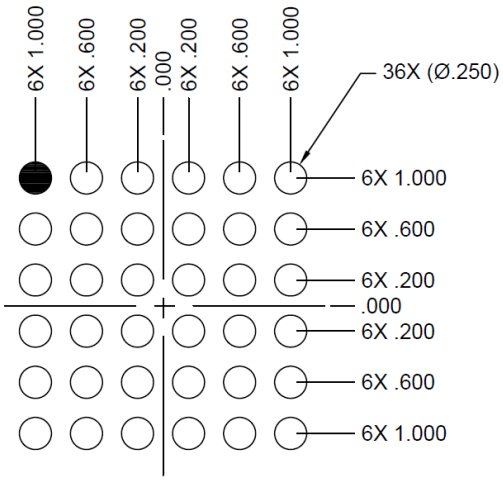
TOP VIEW (BUMPS DOWN)



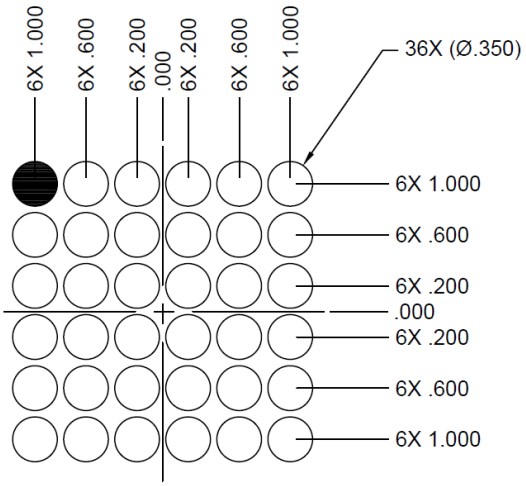
BOTTOM VIEW (BUMPS UP)



SIDE VIEW



RECOMMENDED PCB METAL TOP VIEW



RECOMMENDED SOLDERMASK TOP VIEW

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br402) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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