RFMD + TriQuint = Qorvo

TAT6254C

Fiber To The Home FR Amplifier 47–1000 MHz

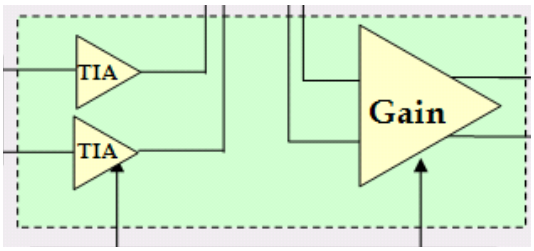
Product Description

The TriQuint TAT6254C FTTP SFU Video Receiver provides a low noise analog interface to CATV receivers and optical triplexers. The TAT6254C is intended for use in single family unit (SFU) analog video fiber to the premise (FTTP) applications.

The TAT6254C exhibits low input noise and distortion that provides performance margin critical to meeting stringent FTTP link requirements. It runs on either a single +12 V or +5 V supply, eliminating the need for an extra ONU power supply. The TAT6254C provides automatic gain control (AGC) to maintain a constant +19 dBmV/ch output (+23 dBmV in high output mode) to ensure consistent video quality and ease of design. The TAT6254C is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost.

The TAT6254C has the flexibility to be designed for a range of RF outputs and supply voltages. This datasheet discusses four configurations; standard RF output and high RF output with both +5 V and +12 V supplies.

Functional Block Diagram



Product Features

- Operating Frequency Range: DC to 4 GHz
- Single +12 V or +5 V configuration
- Low Noise 3.9 pA/rtHz Equivalent Input Noise
- 19 or 23 dBmV/channel RF output, at 55.25 MHz
- 33 dB AGC range, for −10 to +2 dBm optical inputs
- Low power consumption, 1.3 Watts at +12 V and 1.0 Watt at +5 V
- Potentially eliminates the need for costly balun and directional coupler
- Linearity better than −63 dBc CSO and CTB

Applications

- High dynamic range FTTH
- GPON FTTH
- Multi Dwelling Unit TIA
- Mini-node

Ordering Information

Part No.	Description
TAT6254C	CATV FTTH pHEMT amplifier
TAT6254C–EB	Evaluation Board
Standard T / R size = 2500 pieces on a 13” reel	

Absolute Maximum Ratings

Parameter	Range / Value	Units
Storage Temperature	−60 to +150	°C
Operating Temperature	−40 to +85	°C
Device Voltage,VDD	+15	V
Thermal Resistance (jnc. to case) θ_{jc}	17	°C / W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}	–	12	–	V
T_J (for > 10^6 hours MTTF)	–	–	150	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Ran	–	47	–	1000	MHz
RF Gain at 553.25 MHZ	See Note 1	–	33	–	dB
Gain Flatness	–	–	1.0	–	dB
Tilt	See Note 2	–	3	–	dB
Equivalent Input Noise	–	–	3.9	–	pA / rtHz
RF Output Level @ 55.25 MHz, Standard Output	See Note 3	18	19	–	dBmV / ch
RF Output Level @55.25 MHz, High Output	See Note 3 & 5	22	23	–	dBmV / ch
Output Return Loss	–	–	16	–	dB
CSO	See Note 4	–	−63	–	dB
CTB	See Note 4	–	−63	–	dB
Gain Control Range	See Note 6	–	33	–	dB
Power Supply Current @ +12 V	–	–	120	–	mA
Power Supply Current @ +5 V	–	–	200	–	mA

Notes:
1. Gain = 20*log (Z/75)
2. From 54 MHz to 870 MHz; higher tilt possible
3. AGC using 3.3 % / ch output level fixed by external AGC
4. 80 channels analog NTSC
5. Uses output transformer
6. With suggested application circuit
7. Per Applications Circuit Herein

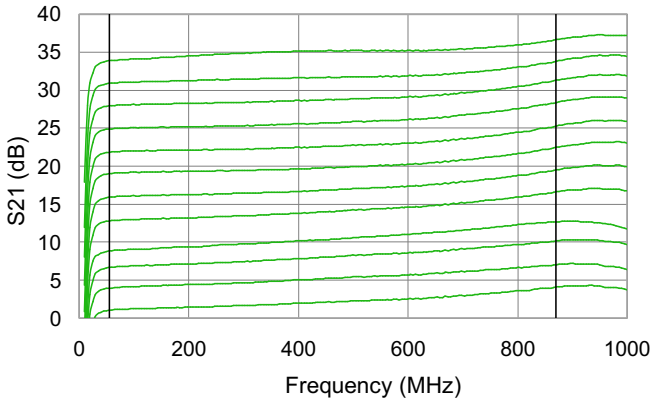
Optical Input and Triplexer Requirements

Parameter	Conditions (1)	Min	Typ	Max	Units
Optical Input Power	–	−10	–	2	dBm
Optical Modulation Index	–	–	3.3	–	% / ch
Triplexer 1550 mm PIN Responsivity	–	–	–	0.9	mA / mW
Triplexer 1550 mm PIN Capacitance	–	–	–	0.9	pF

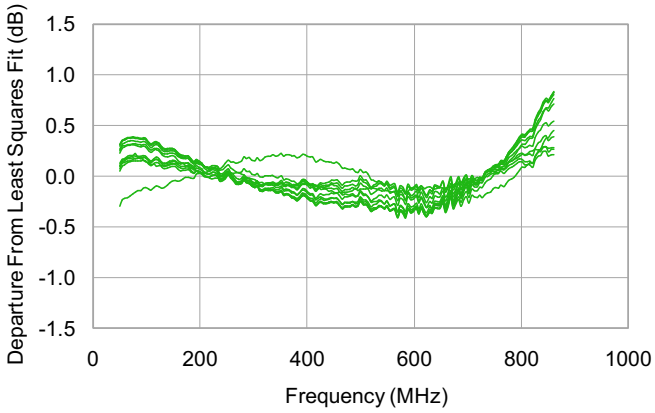
12 V Standard Output Application Board Typical Performance

DD = +12 V, IDD = 120 mA , Temperatures are ambient

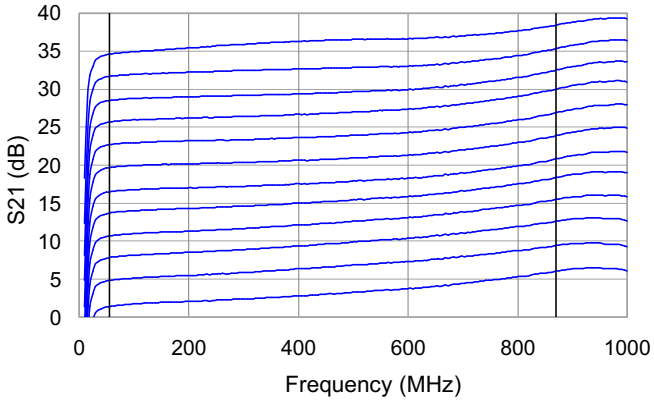
Gain over AGC Setting, +25 C



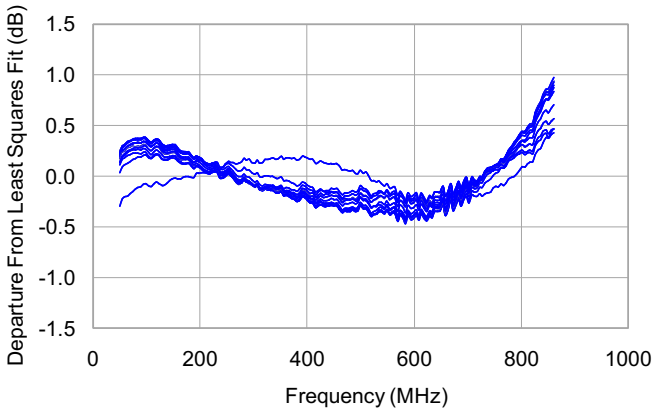
Gain Flatness, +25 C



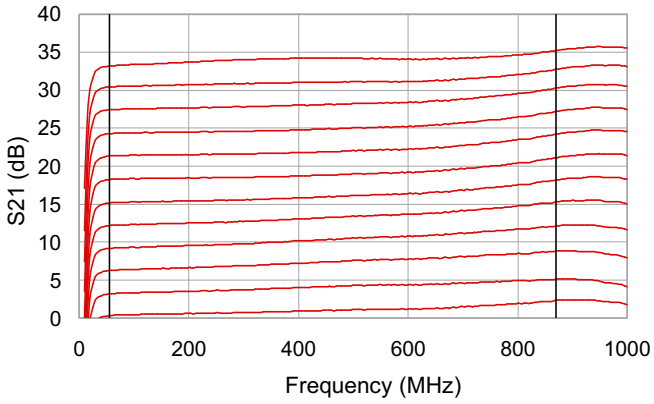
Gain over AGC Setting, -40 C



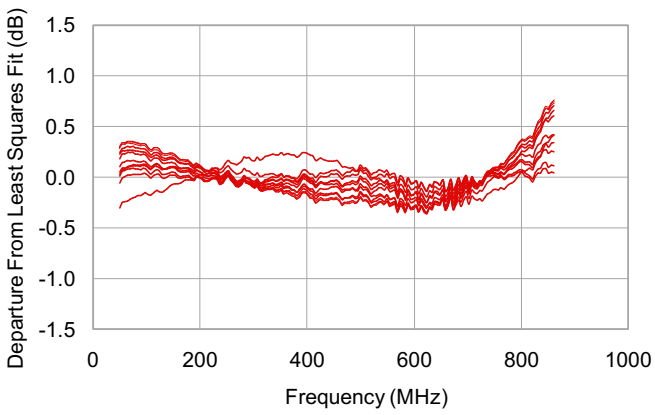
Gain Flatness, -40 C



Gain over AGC Setting, +85 C

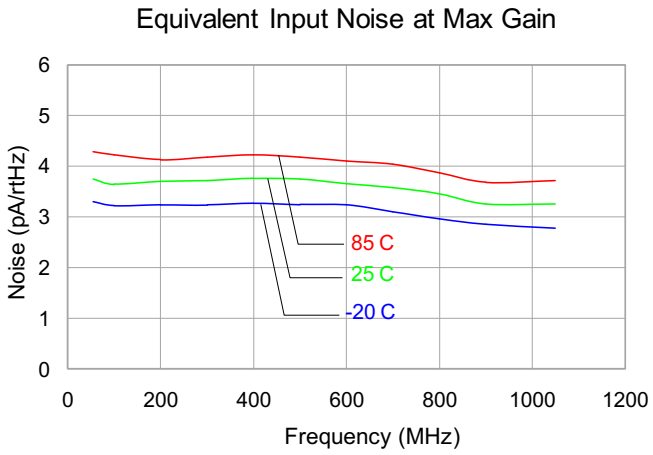


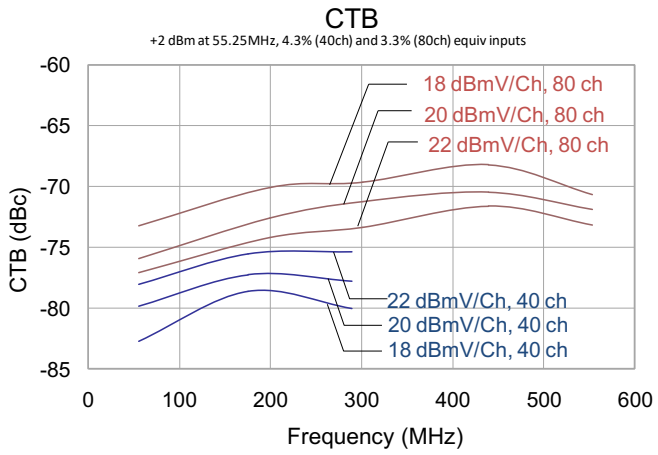
Gain Flatness, +85 C



12 V Standard Output Application Board Typical Performance (cont'd)

V_{DD} = +12 V, I_{DD} = 120 mA, 25 °C unless otherwise stated, Temperatures are ambient





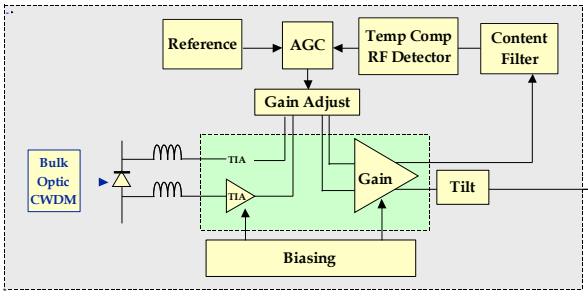
For performance data using 5 V Output, please email sjcapplication.engineering@tqs.com

12 V Standard Output Application Board Typical Performance (cont'd)

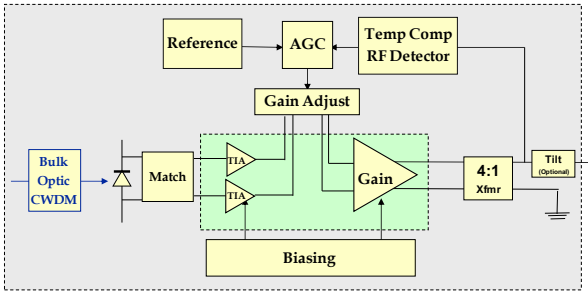
The TAT6254C integrates two low noise high gain trans-impedance amplifiers in a differential configuration followed by an output amplifier. It provides a low input impedance to minimize the effects of photodiode capacitances and stray impedance affects on gain flatness.

The TAT6254C is fabricated using high gain Gallium Arsenide pHEMT technology developed for high-volume commercial markets. It provides improved gain and noise compared to older MESFET technologies and lower gain pHEMT technologies.

The TAT6254C was designed as a general purpose FTTP receiver. While it eliminates the need for costly hand-wound parts such as baluns and directional couplers, it allows users wide flexibility in setting gain, tilt, and bias levels to best meet the requirements posed by different operators and architectures. The TAT6254C provides the flexibility to address high levels of gain required by GPON architectures. Designers can easily modify external circuit values to enable wider optical input ranges, such as needed in newer GPON architectures.



RF AGC Solution



RF AGC High Output Option

12 V Standard Output Application Board Typical Performance (cont'd)

The TAT6254C provides two high level outputs. One output drives an optical tilt network while the other drives a content filter and an RF detection circuit. The TAT6254C does not require an output balun. Because the two equal outputs have a high level of isolation; the TAT6254C effectively provides an integrated directional coupler with extra gain to drive the RF detection circuit at a high level. This eases offset voltage requirements on operational amplifiers used in the AGC block. Gain control is accommodated with a low cost external PIN diode circuit placed between the input trans-impedance amplifier and the output amplifier. This helps reduce the die size of the TAT6254C and provides for excellent PIN diode distortion characteristics over a continuous control range.

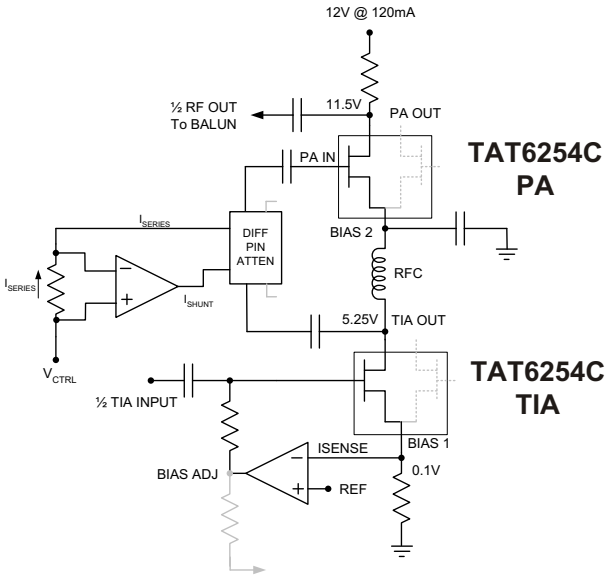
Up to 33 dB of gain control is possible using the recommended +12 V standard output application circuit.

The application circuits are optimized for 870 MHz performance with slight rolloff for use in combination with a post filter for applications such as MoCA. For optimized performance at 1 GHz and beyond, it is recommended that a low capacitance photodiode be used with a change in value of the peaking inductors L1 and L2. For further guidance, please contact TriQuint Semiconductor Application Engineering.

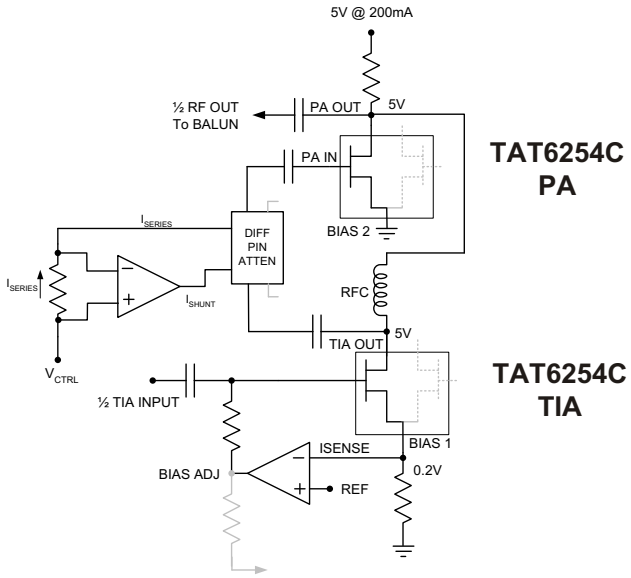
For high output operation, refer to the appropriate +5 V high output application circuit. This option uses a 4:1 transformer to combine the outputs of the second stage.

For further information email sjcapplication.engineering@tqs.com

12V EVB Functional Schematic



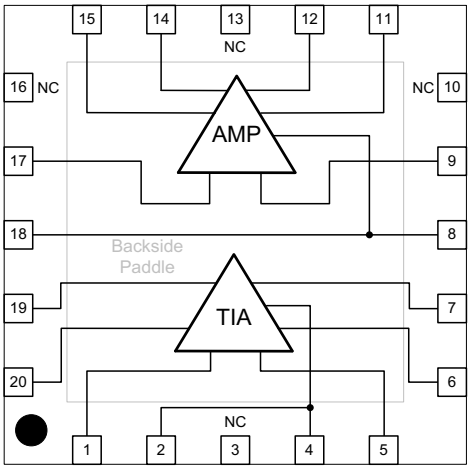
5V EVB Functional Schematic



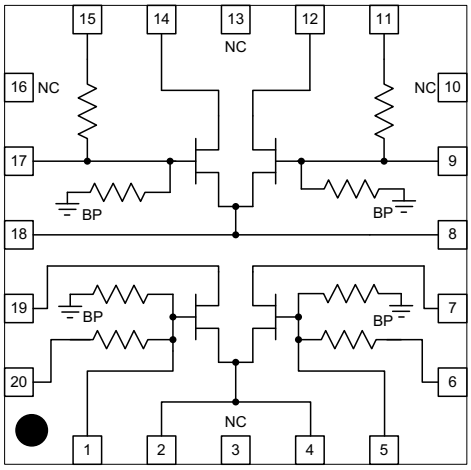
Pin Configuration and Description

TAT6254C

Functional Block

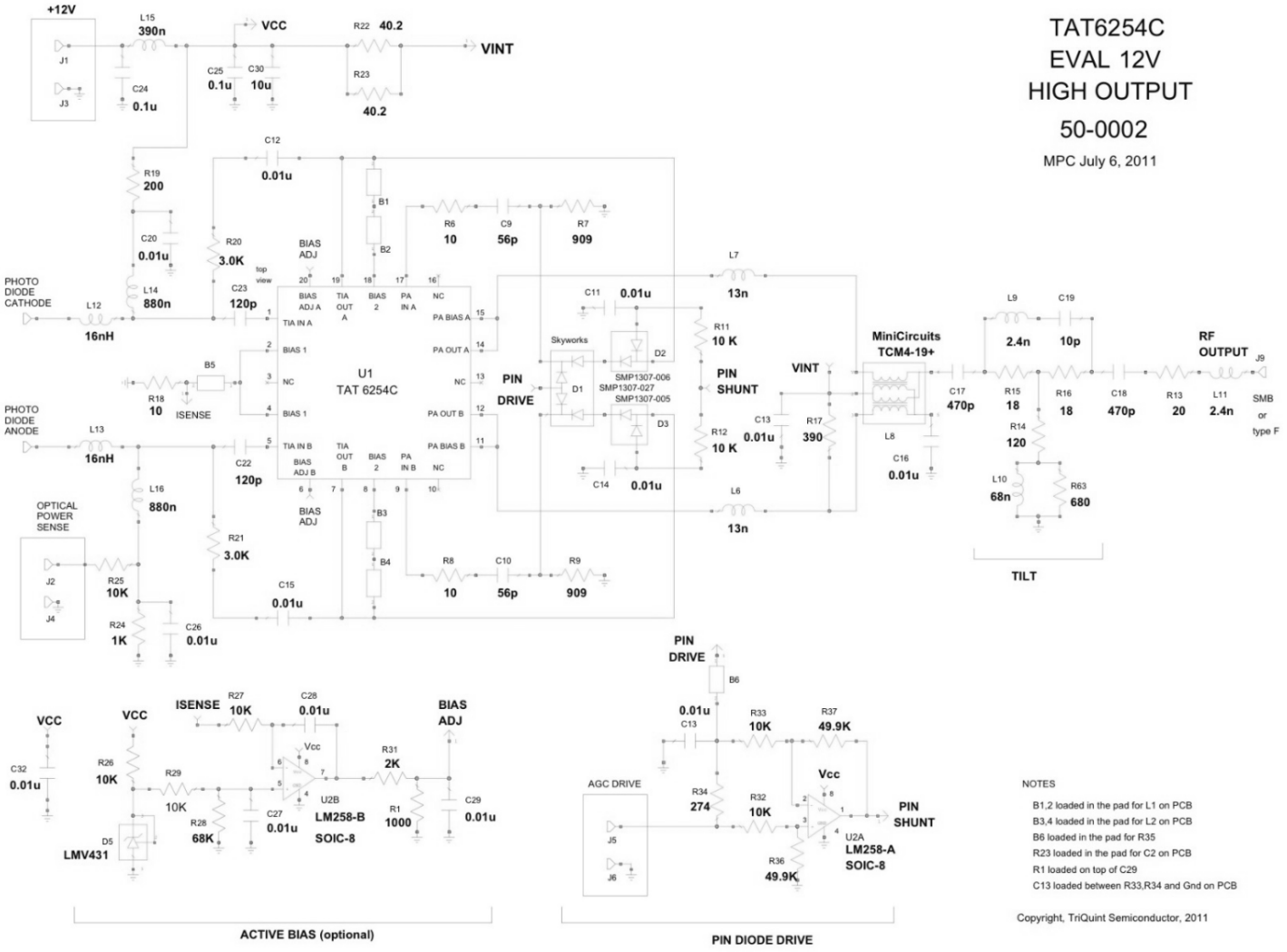


Simplified Schematic

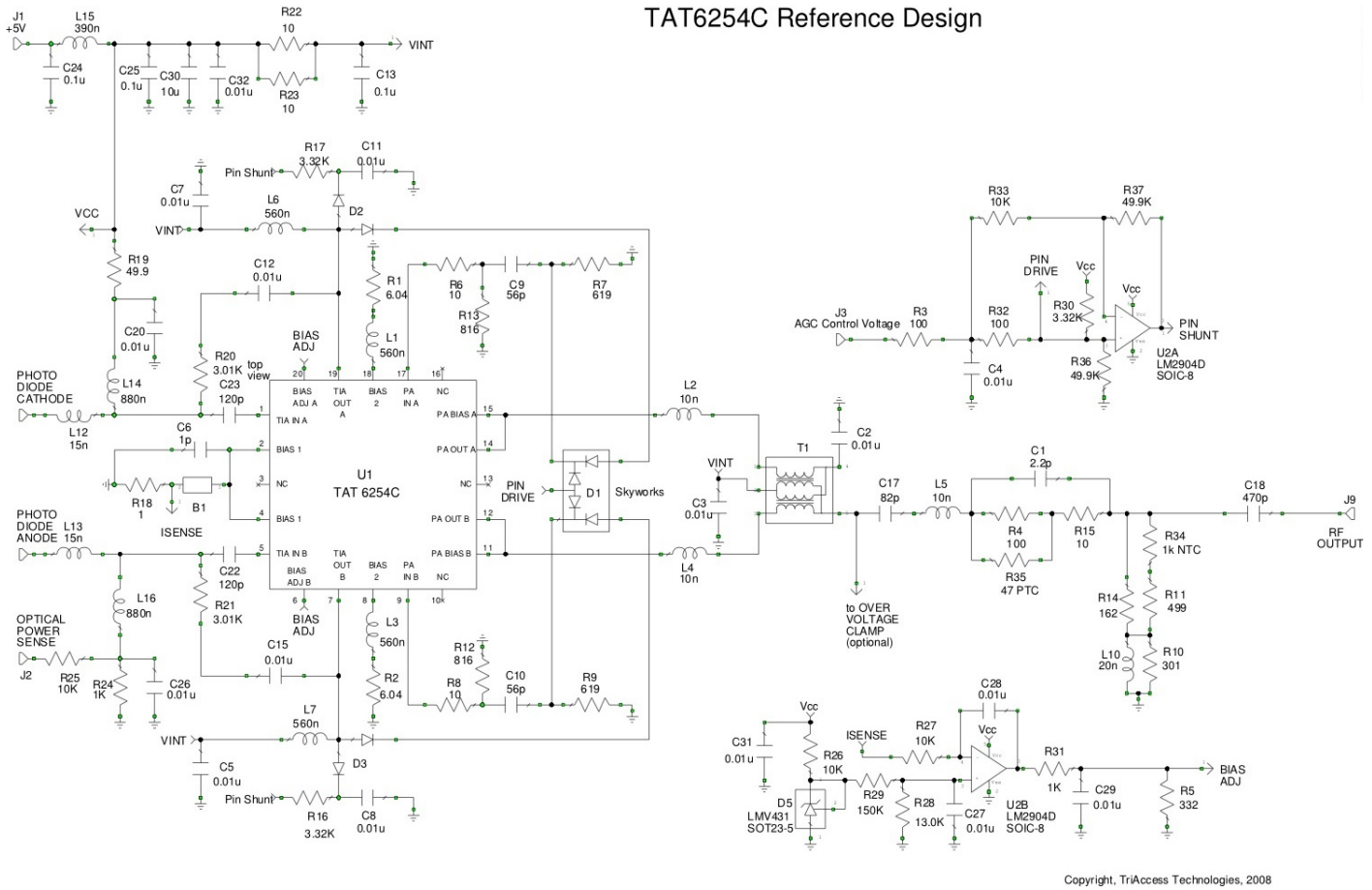


Pin No.	Label	Description
1	TIA IN A	Input to TIA A
2, 4	BIAS 1	Source of TIA differential pair
3, 10, 13, 16	NC	No Connect
5	TIA IN B	Input to TIA B
6	BIAS ADJ B	Bias adjustment for TIA B
7	TIA OUT B	Output of TIA B
8, 18	BIAS 2	Source of post amplifier (ground or used for recycling current of TIA)
9	PA IN B	Input to post-amplifier B
11, 15	PA BIAS B, A	Bias & Feedback of PA B and A
12, 14	PA OUT B, A	Output of post amplifier B and A
17	PA IN A	Input to post amplifier A
19	TIA OUT A	Output of TIA A
20	BIAS ADJ A	Bias adjustment for TIA A
BP	GND	Backside paddle, thermal and bias ground

12 V High Output Schematic

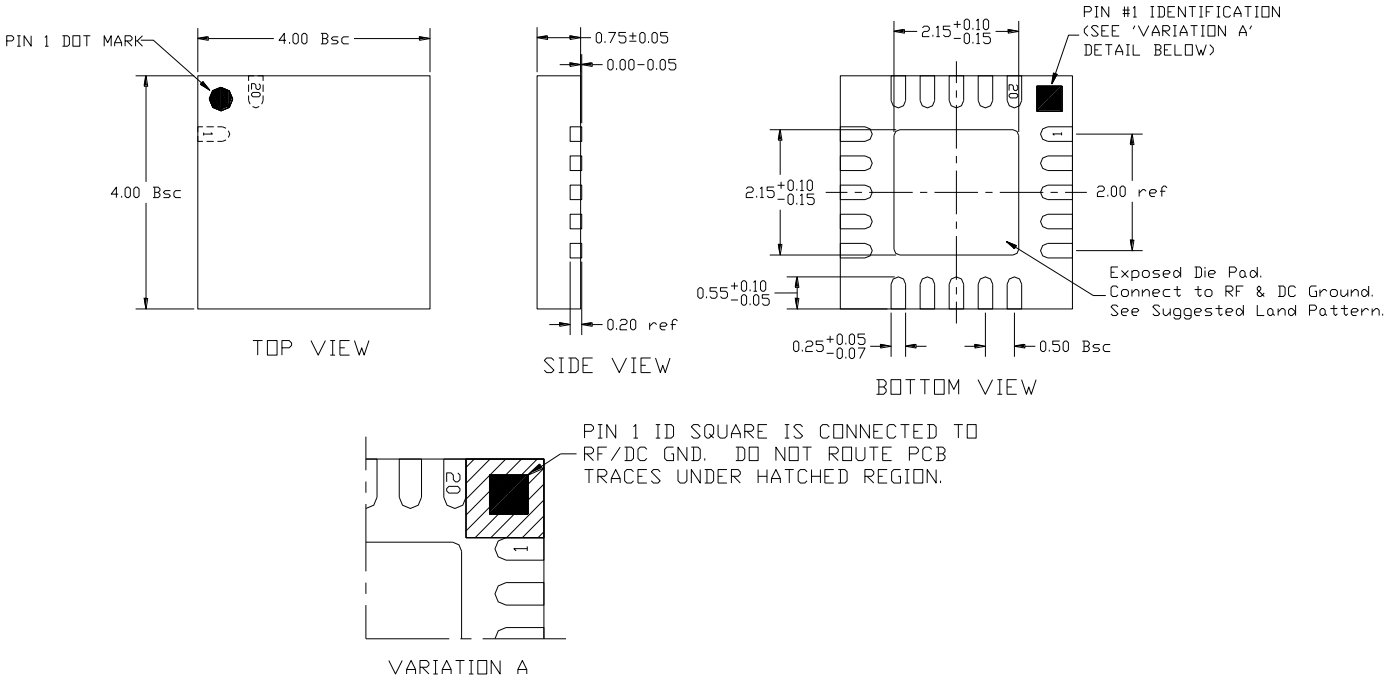


5 V High Output Schematic



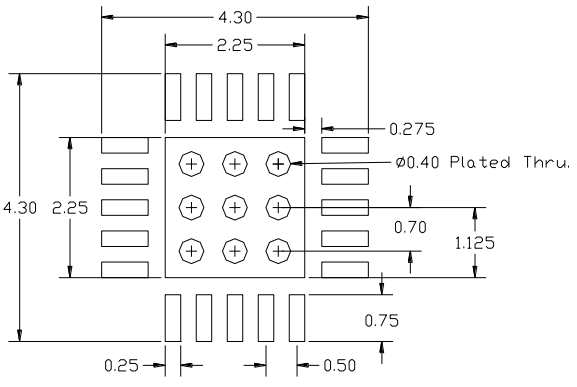
Package Information and Dimensions

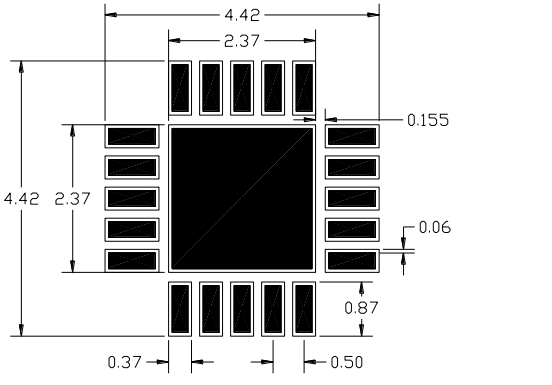
This package is lead-free / RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.



Mounting Configuration

All dimensions are in millimeters. Angles are in degrees.





Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0	JEDEC JESD22-A114
ESD – Charged Device Model (CDM)	Class IV	–
MSL	Level 3	JEDEC IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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For technical questions and application information:

Email: sjcapplication.engineering@tqs.com

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