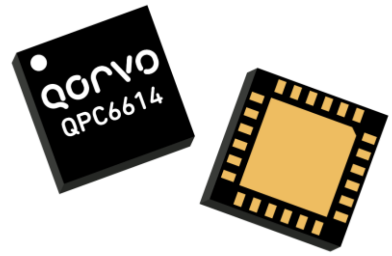
QPC6614

5 MHz to 6000 MHz Digital Step Attenuator

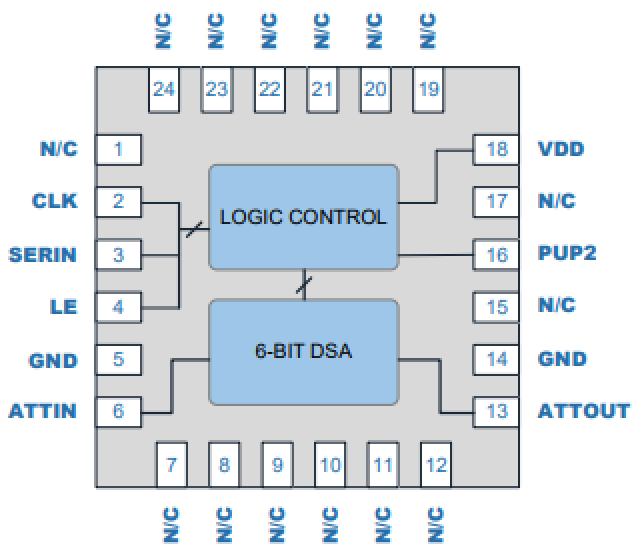


24-pin 4.2 mm x 4.2 mm x 0.975 mm

Product Description

The QPC6614 is a 6-bit digital step attenuator (DSA) that features high linearity over the entire 31.5 dB gain control range with 0.5 dB steps. The QPC6614 uses serial control interface. The QPC6614 has a low insertion loss of 1.4 dB at 2 GHz. Patented circuit architecture provides overshoot-free transient switching performance.

Functional Block Diagram



Top View

Key Features

- 6-Bit, 31.5 dB, 0.5dB Step
- Patented Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 5 MHz to 6000 MHz
- High Linearity, IIP3 >+55 dBm
- Serial Control Interface
- Fast Switching Speed,
- Single Supply 3 V to 5 V Operation
- RF Pins Have No DC Voltage, can be DC Grounded Externally
- Power-up attenuation state programmable

Applications

- 2G through 4G Base Stations
- Point-to-Point
- Wi-Fi
- Test Equipment

Ordering Information

Part No.	Description
QPC6614TR13	2500 pcs on 13" reel
QPC6614PCK401	5-600MHz PCBA w/5pcs sample bag

Absolute Maximum Ratings [1]

Parameter	Rating
Storage Temperature	−40 to +150 °C
Supply Voltage (V_{DD})	−0.5 to +6.0 V
Signal level applied to logic pins (when V_{DD} is applied prior to any other pin voltages)	−0.5 to V_{DD}
Signal level applied to logic pins (when V_{DD} is not applied prior to any other Pin Voltages) [2]	-0.5 to +4.0 V
Input Power (RFIN Pin, +85°C Case Temp.)	+30 dBm
Input Power (RFOUT Pin, +85°C Case Temp.)	+27 dBm

Notes:
1. Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.
2. If signal level applied to logic pins is 4 - 5 V, use series 1k Ohm resistor at the input of CLK, SERIN, LE and PUP2.

Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD}) [2]	+2.7	+5	+5.5	V
Case Temperature	−40		+105	°C
Operating Junction Temp.			+125	°C

Notes:
1. Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2. It is recommended to apply V_{DD} before applying any signal to logic pins.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		5		6000	MHz
Insertion Loss	0 dB Attenuation Setting		1.4	2.4	dB
Attenuation Range			31.5		dB
Attenuation Step			0.5		dB
Attenuation Accuracy		± (0.3 + 3% of Atten. Setting)			dB
Input IP3			+55		dBm
Input P0.1dB			+30		dBm
RF Input Power to RFIN Pin				+27	dBm
RF Input Power to RFOUT Pin				+20	dBm
Return Loss			15		dB
Switching time	50% CTL to 10% / 90% RF		50		ns
Successive Step Phase Delta	2000 MHz		2		Deg.
Supply Current, I_{DD}	Steady state operation [2]		180		µA
Thermal Resistance	At maximum attenuation state with RF power applied to the ATTIN pin		60		°C/W

Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq = 2GHz, 50 Ω system.
2. Current draw during attenuation state transitions is higher.

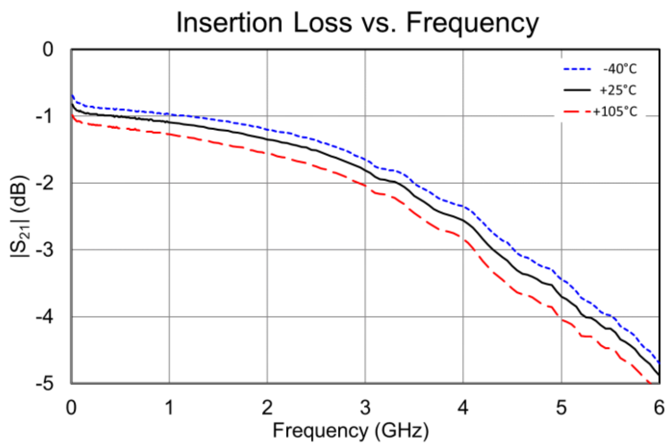
Control Logic Requirements

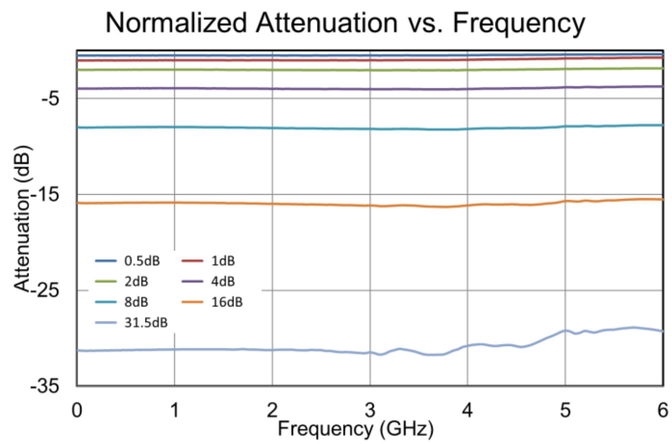
Parameter	Conditions	Min	Typ	Max	Units
Low State Input Voltage		0		+0.63	V
High State Input Voltage		+1.17		V_{DD}	V

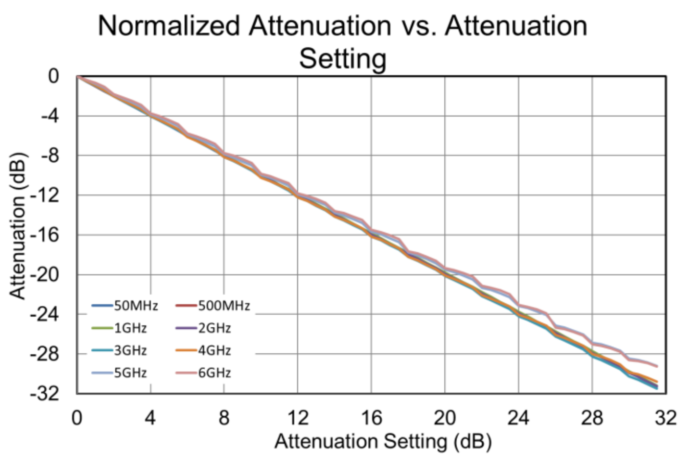
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq.=2GHz, 50 Ω system.

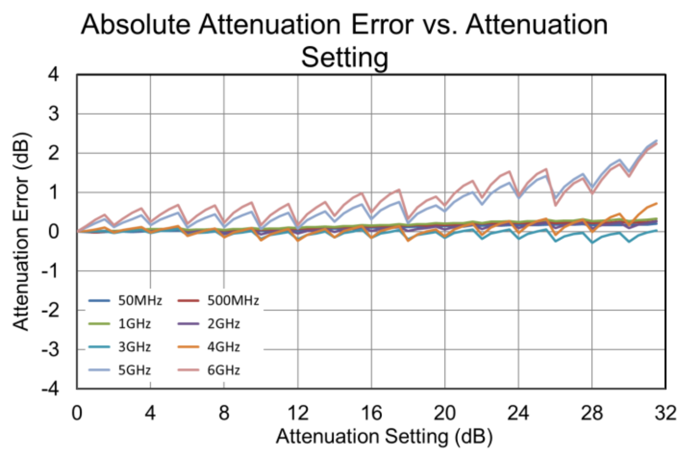
Performance Plots – QPC6614

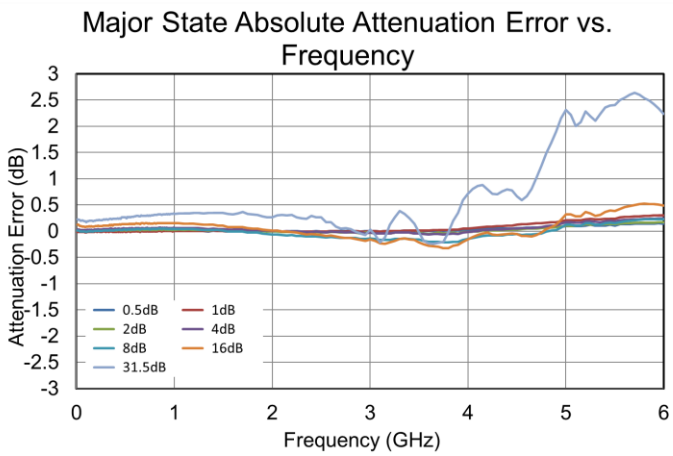
Test conditions unless otherwise noted: V_{DD} = +5.0 V, 50 Ω system, Temp = 25°C

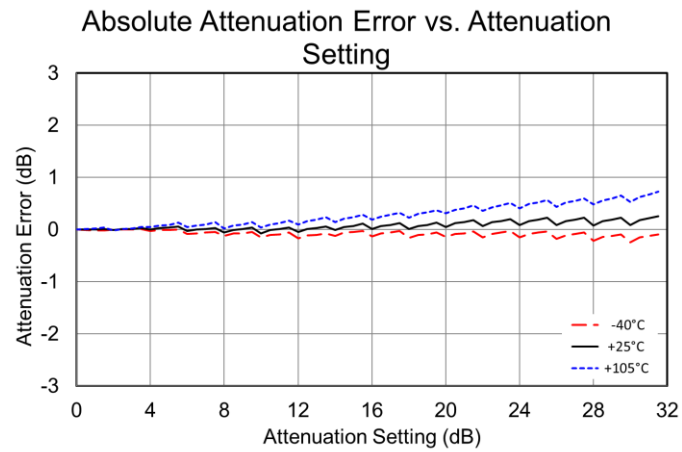






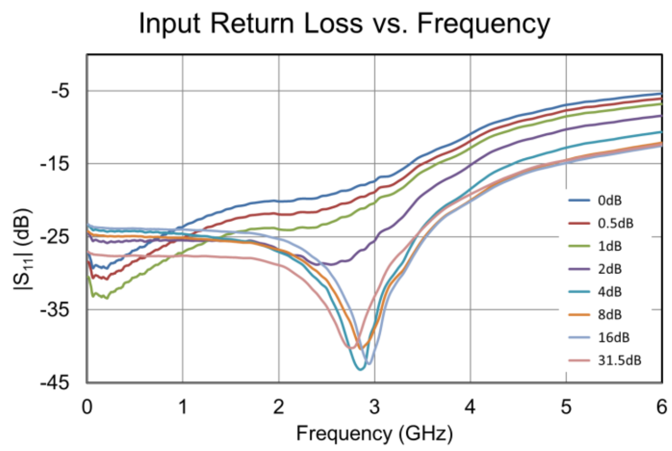


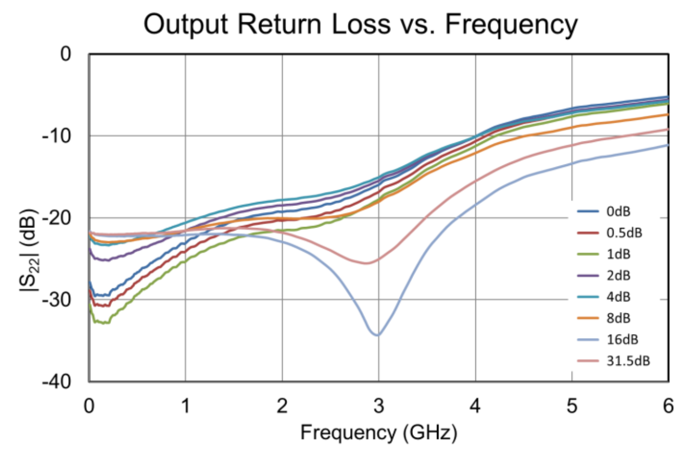


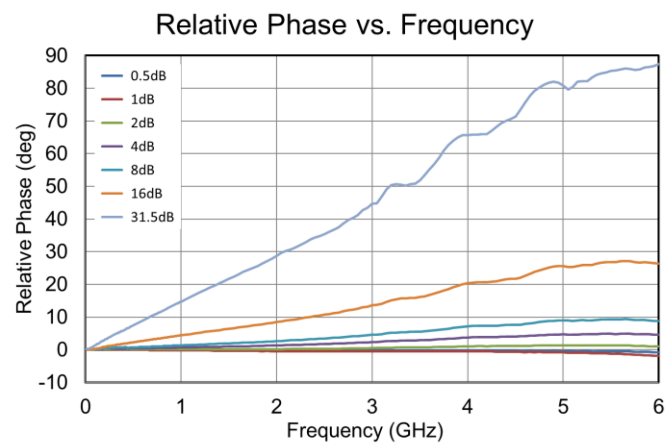


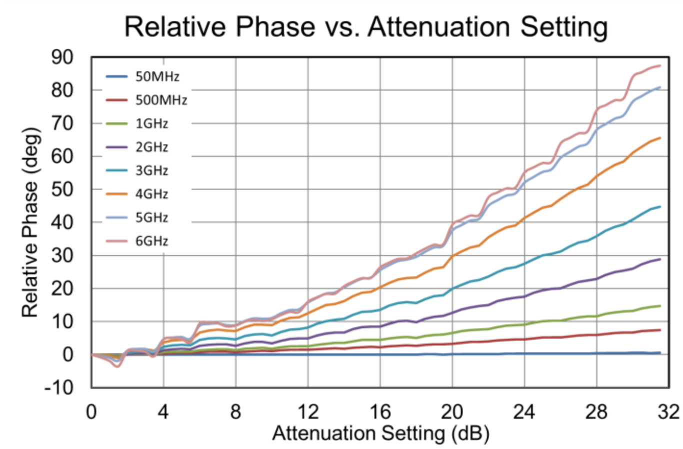
Performance Plots – QPC6614 (Continued)

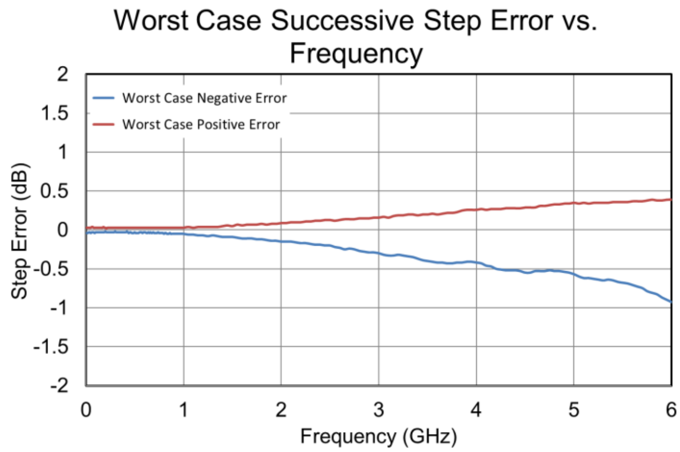
Test conditions unless otherwise noted: V_{DD} = +5.0 V, 50 Ω system, Temp = 25°C

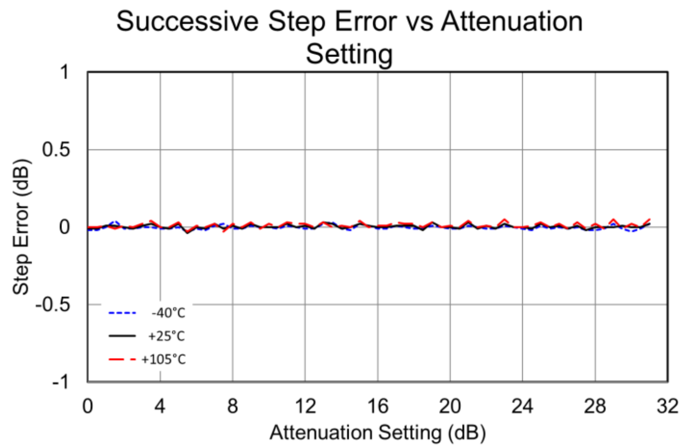






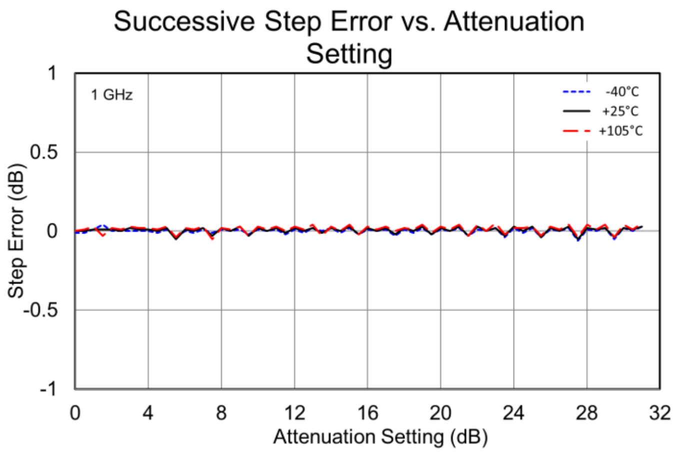


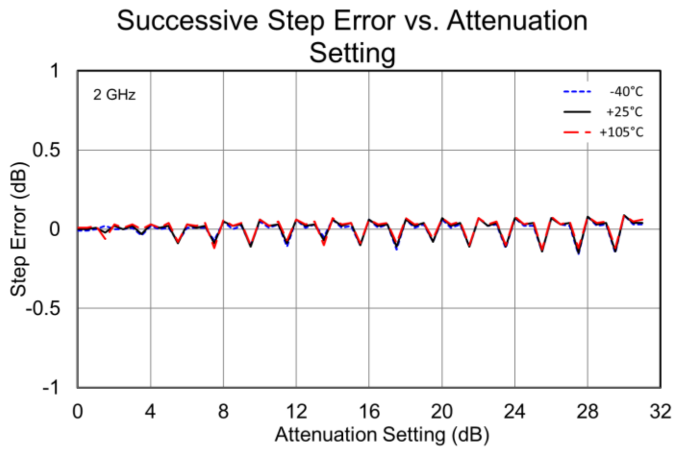


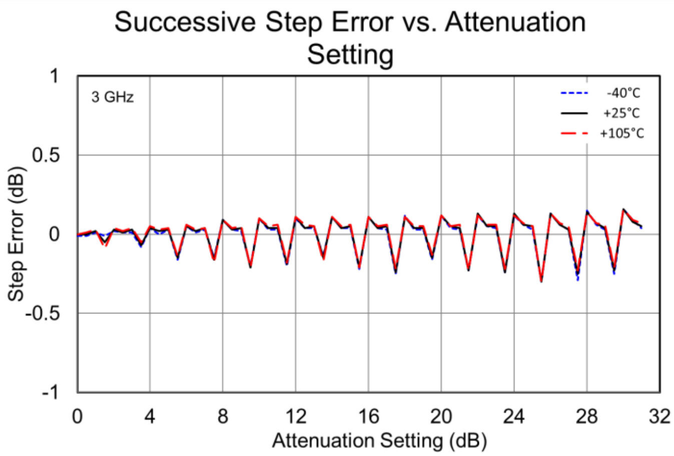


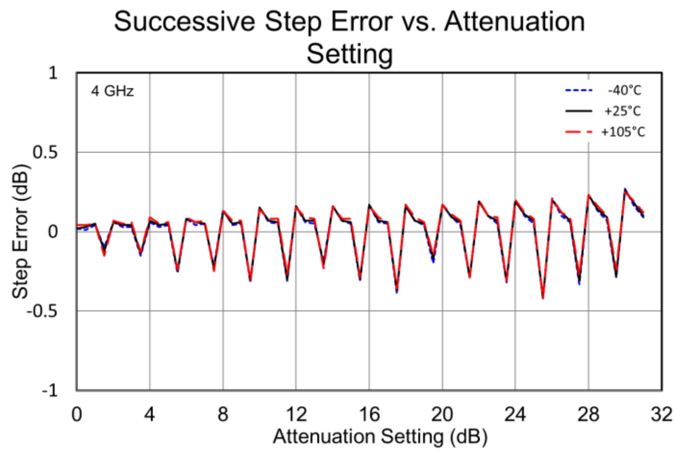
Performance Plots – QPC6614 (Continued)

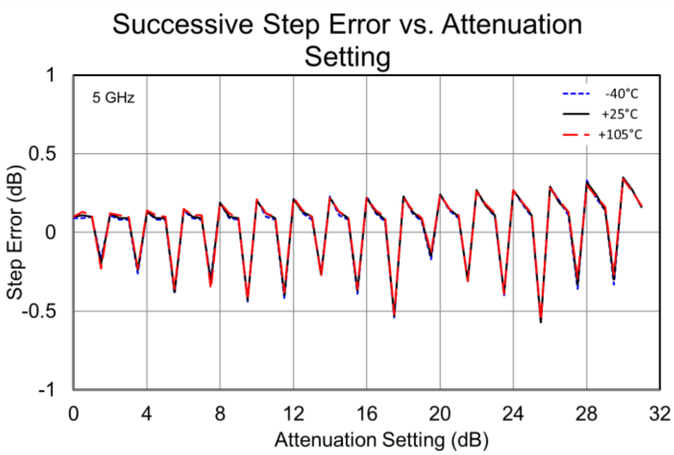
Test conditions unless otherwise noted: V_{DD} = +5.0 V, 50 Ω system, Temp = 25°C

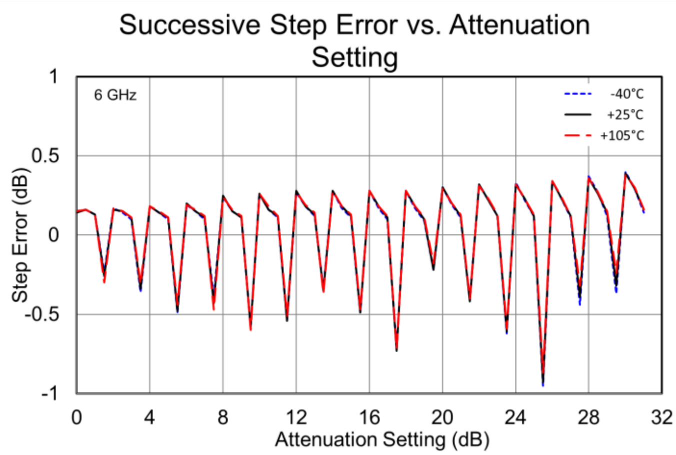






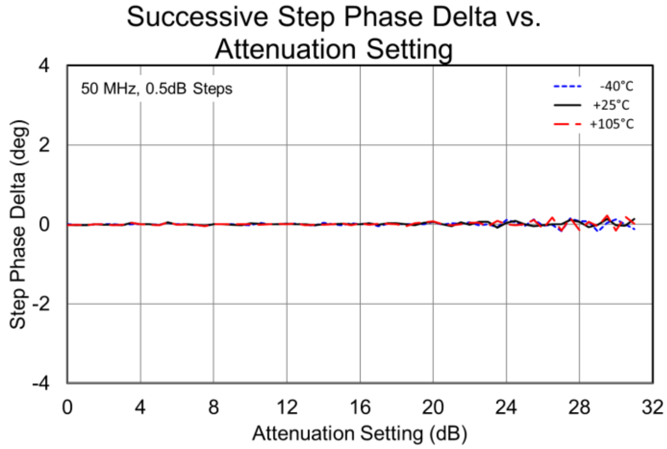


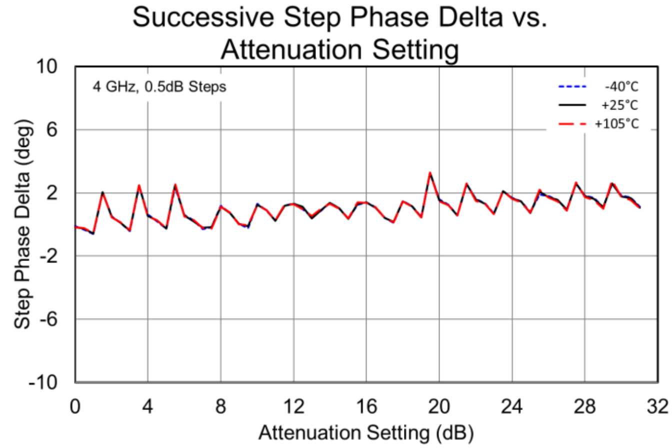


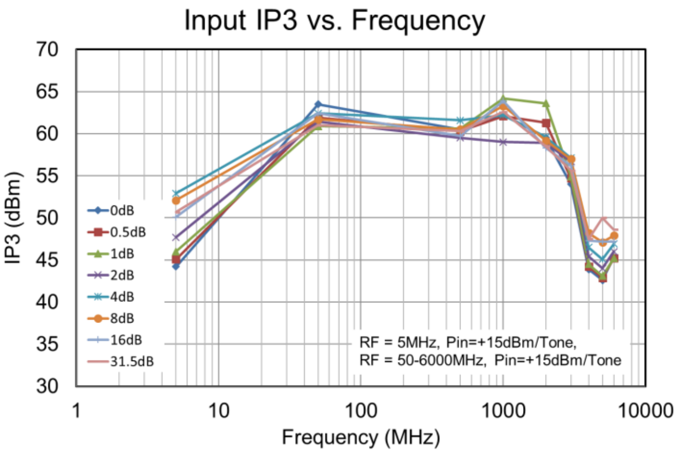


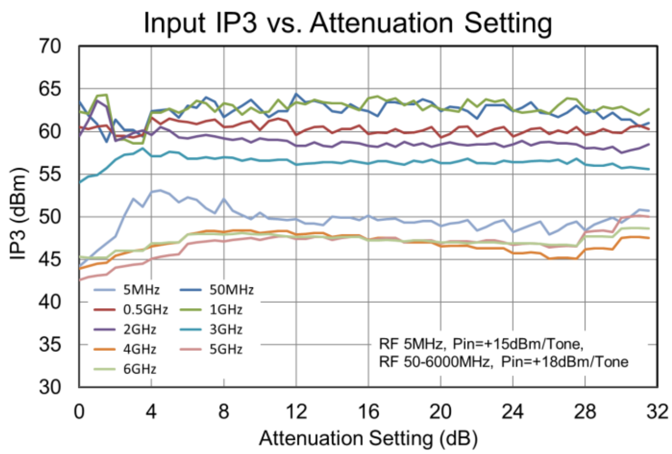
Performance Plots – QPC6614 (Continued)

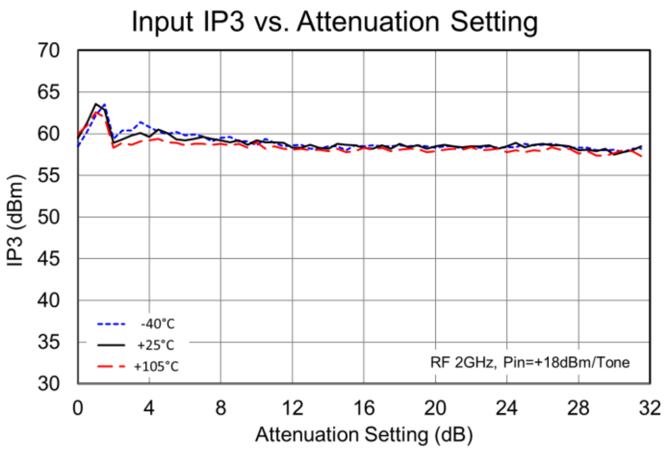
Test conditions unless otherwise noted: V_{DD} = +5.0 V, 50 Ω system, Temp = 25°C

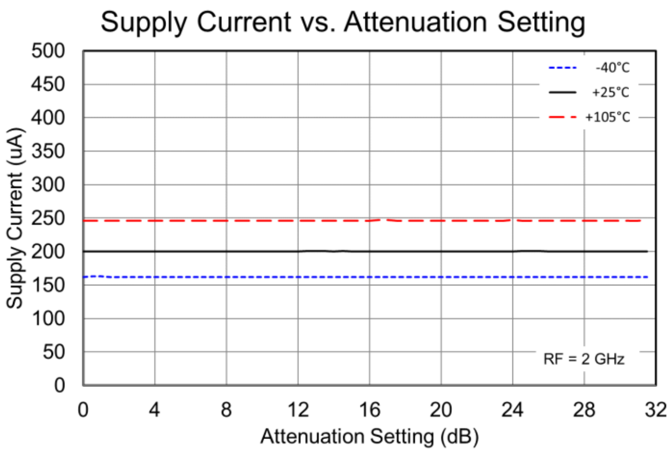




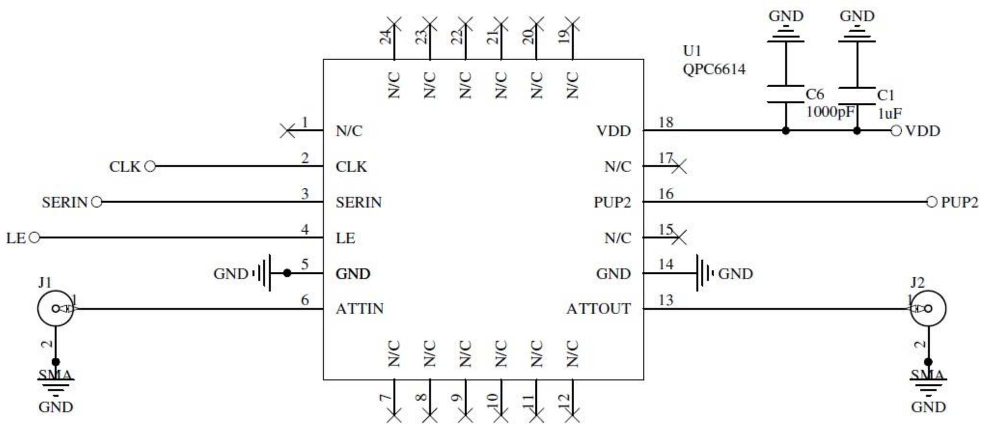








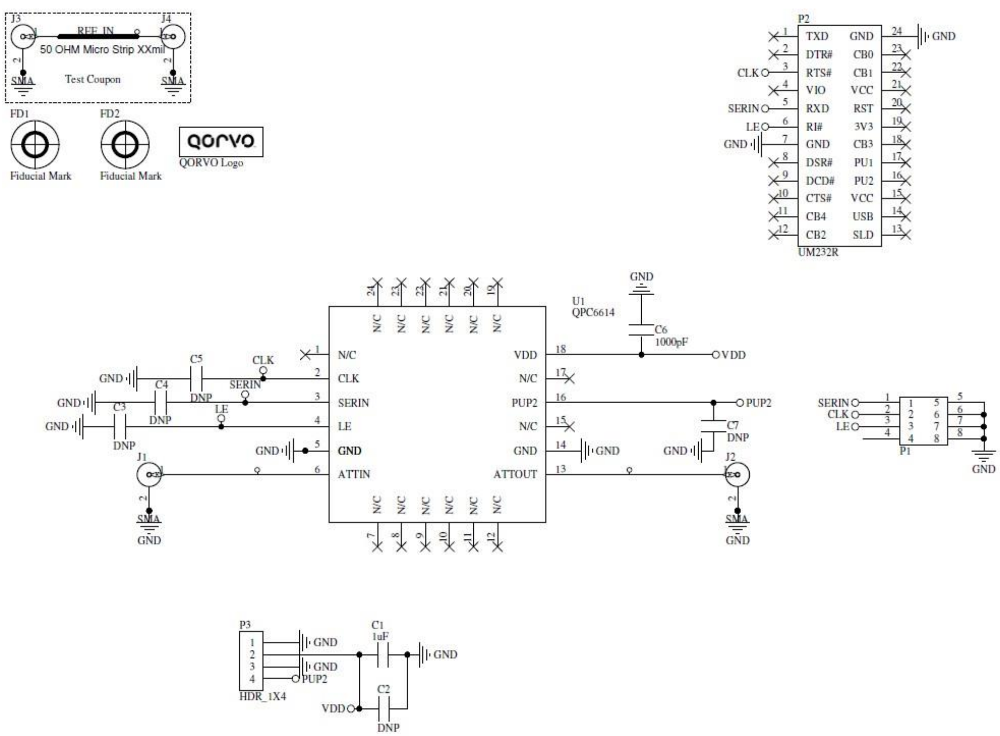
Typical Application Schematic – 5 MHz to 6000 MHz



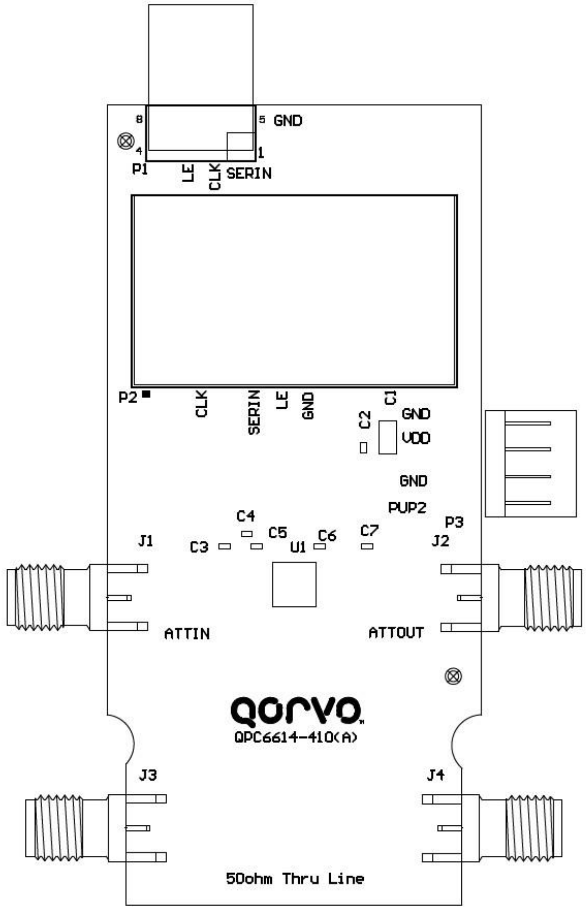
Notes:

1. If digital control signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of CLK, SERIN, LE and PUP2,

Evaluation Board Schematic – 50 MHz to 6000 MHz



Evaluation Board Assembly Drawing



Bill of Material – Evaluation Board

Reference Des.	Value	Description	Manufacturer	Part Number
	n/a	QPC6614-410	ViaSystems	QPC6614-410(A)
U1	n/a	Digital Step Attenuator 5 MHz to 6000 MHz	Qorvo	QPC6614SB
J1- J4		CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	Molex	SD-73251-4000
C1	1 uF	CAP, 1 µF, 10%, 25 V, X7R, 1206	Taiyo Yuden	CE TMK316B7105KL-T
C6	1000 pF	CAP, 1000 pF, 10%, 50 V, X7R, 0402	TDK Corporation	C1005X7R1H102KT000F
P2	n/a	CONN, SKT, 24-PIN DIP, .600", T/H	Aries Electronics Inc.	24-6518-10
M1[(1)]	n/a	MOD, USB TO SERIAL UART, SSOP-28	Future Technology	UM232R
P3	n/a	CONN, HDR, ST, 4-PIN, 0.100"	Samtec Inc..	TSW-104-08-S-S
P1	n/a	CONN, HDR, 2 X 4, RA, 0.100, T/H	Samtec Inc.	TSW-104-08-G-D-RA

Notes:
1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.

Evaluation Board Programming Using USB Interface

Serial Addressable Mode

Refer to the Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the software for use. Apply the supply voltage to P3. Select QPC6614 from the RFMD Parts List of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurements can be taken.

Evaluation Board Programming Using External Bus

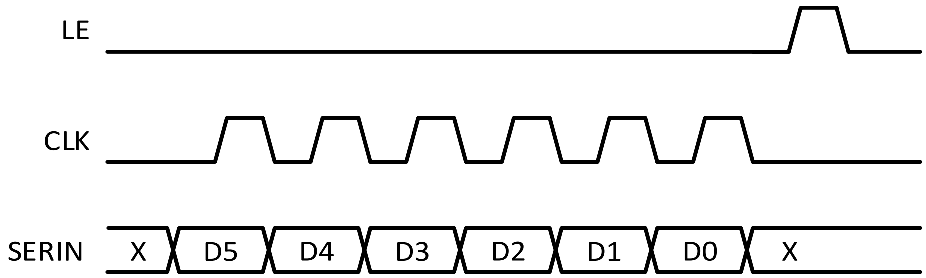
Serial Addressable Mode

This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. Note the top row of the P1 contains the serial bus signals and the bottom row is ground. Apply the supply voltage to P3. Send the appropriate signals onto the serial bus lines in accordance with the Serial Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken. If digital control signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of CLK, SERIN, LE and PUP2.

Default Power-up State

The attenuation state set during power-up can be controlled using the PUP2 pin. To power-up in the maximum attenuation state, apply a logic low to PUP2 pin prior to applying supply voltage V_{DD}. To power-up in the minimum attenuation state apply a logic high to the PUP2 pin prior to applying supply voltage V_{DD}.

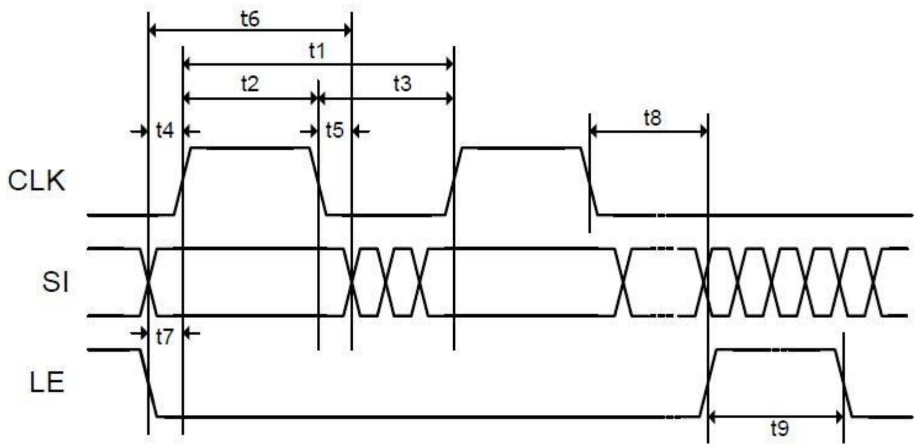
Serial Mode Timing Diagram



Serial Programmable Attenuation Word Truth Table

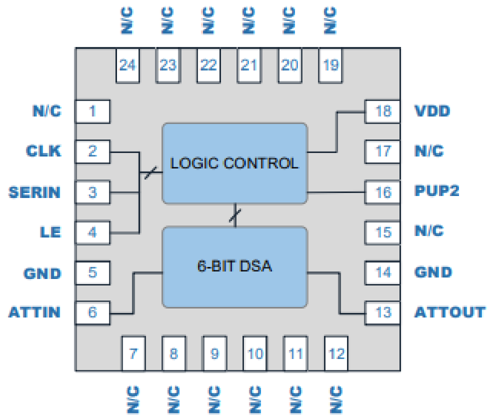
Attenuation Word						
D5 (MSB)	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**	**Attenuation State**
H	H	H	H	H	H	0dB / Reference Insertion Loss
H	H	H	H	H	L	0.5dB
H	H	H	H	L	H	1dB
H	H	H	L	H	H	2dB
H	H	L	H	H	H	4dB
H	L	H	H	H	H	8dB
L	H	H	H	H	H	16dB
L	L	L	L	L	L	31.5dB

Serial Bus Timing Specifications



Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	SI to CLK Setup Time
t5	5	ns min	SI to CLK Hold Time
t6	30	ns min	SI Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width

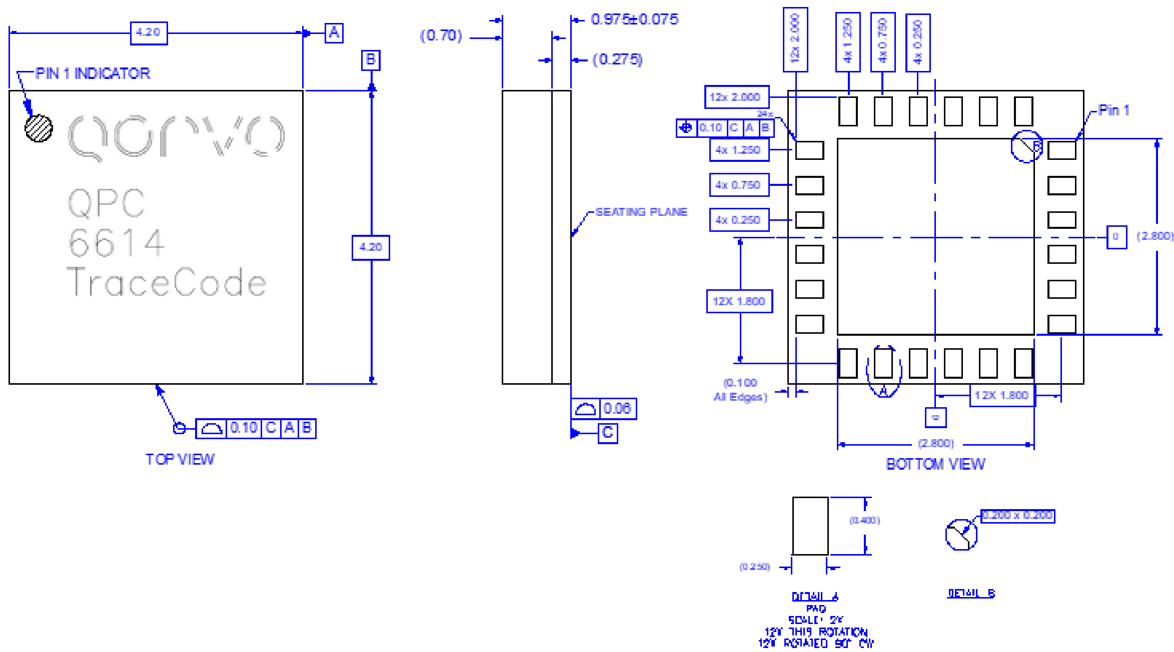
Pad Configuration and Description



Top View

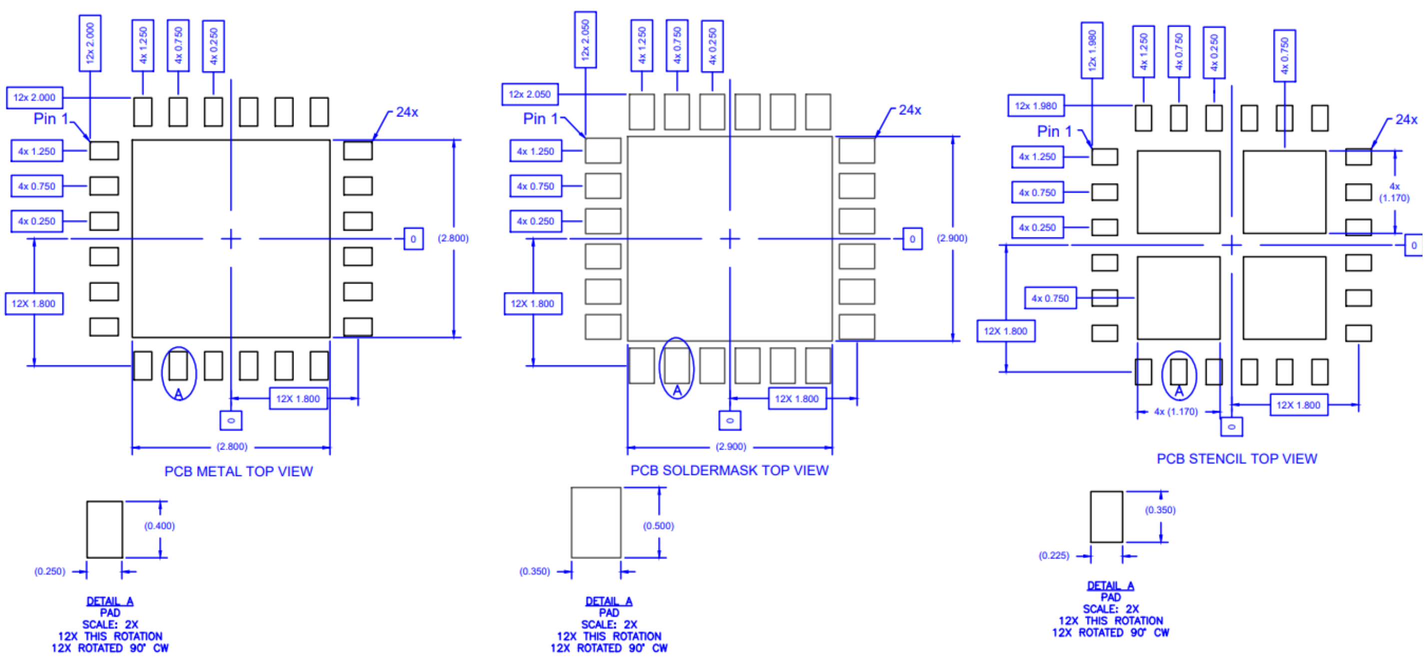
Pad No.	Label	Description
1	NC	No Internal Connection
2	CLK	Serial Clock Input. If signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of this pin.
3	SERIN	Serial Data Input. If signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of this pin.
4	LE	Latch Enable. If signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of this pin.
5	GND	Connect to PCB Ground
6	ATTIN	RF Input Pin. Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
7	NC	No Internal Connection
8	NC	No Internal Connection
9	NC	No Internal Connection
10	NC	No Internal Connection
11	NC	No Internal Connection
12	NC	No Internal Connection
13	ATTOUT	RF Output Pin. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
14	GND	Connect to PCB Ground
15	NC	No Internal Connection
16	PUP2	Power-up Programming Pin. See Default Power-up State Section for use. If signal of 4 - 5V is applied prior to V_{DD}, use series 1k Ohm resistor at the input of this pin.
17	NC	No Internal Connection
18	VDD	Supply Voltage
19	NC	No Internal Connection
20	NC	No Internal Connection
21	NC	No Internal Connection
22	NC	No Internal Connection
23	NC	No Internal Connection
24	NC	No Internal Connection

Package Marking and Dimensions



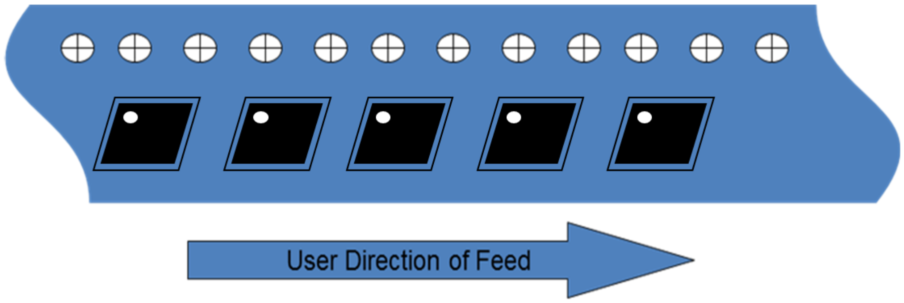
Notes:
1. All Dimensions in millimeters

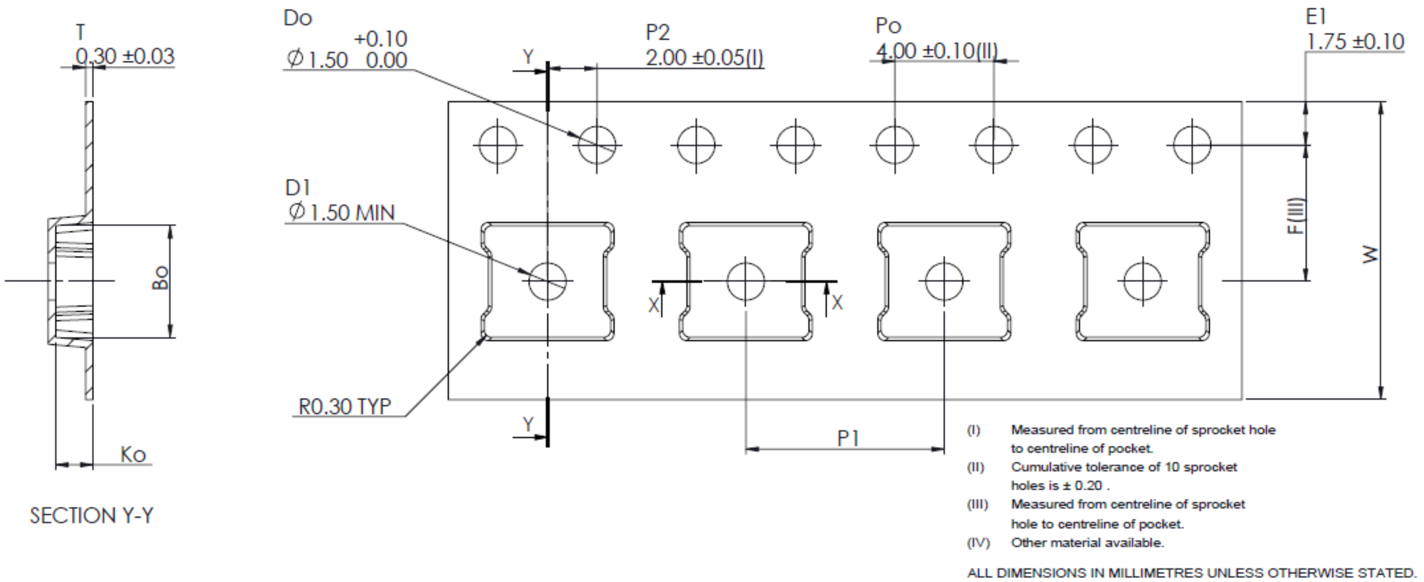
Recommended PCB Layout Pattern



Notes:
1. All Dimensions in millimeters. All angles are in degrees.

Tape and Reel Information – Carrier and Cover Tape Dimensions

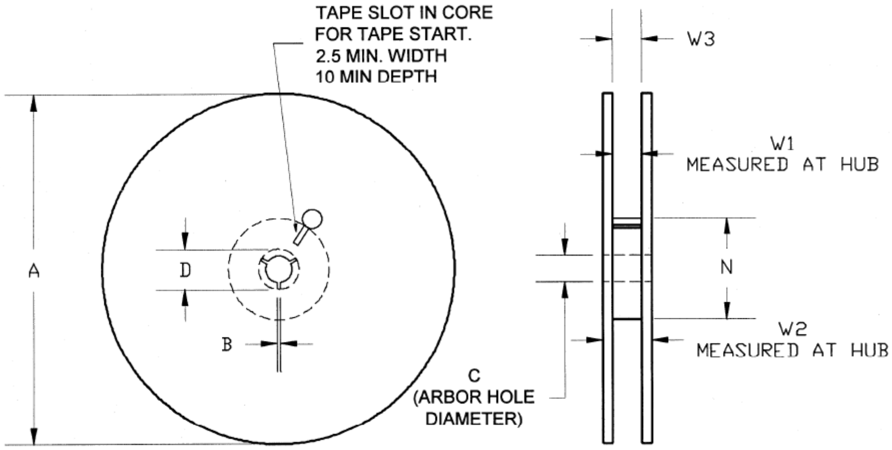




Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.177	4.5
	Width	B0	0.177	4.5
	Depth	K0	0.059	1.5
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

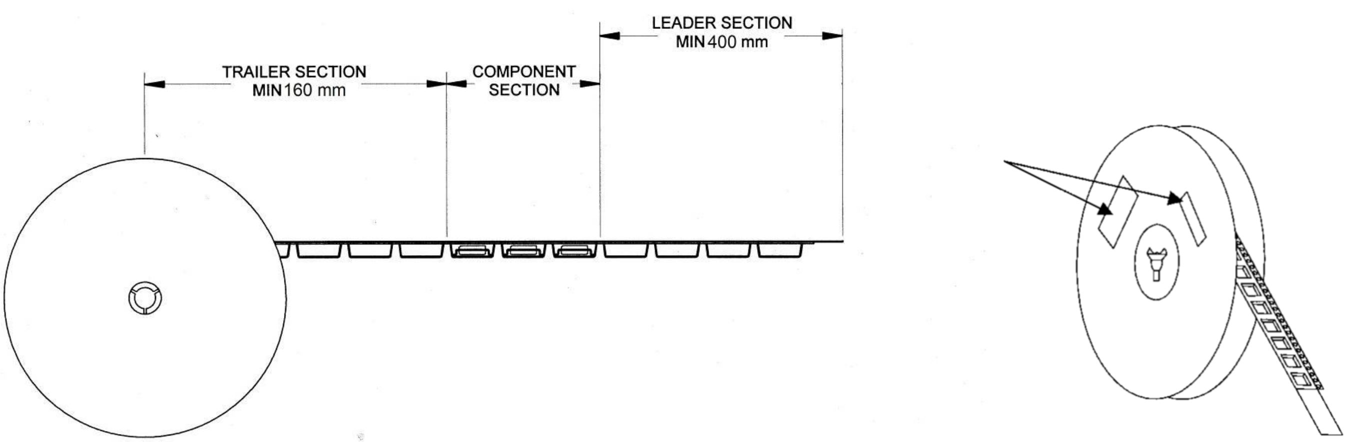
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JESD22-A114
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Ni/Pd/Au *(Electroless Ni 2-5 µm, Electroless Pd 0.11-0.18 µm, Electroless (hybrid) Au 0.07 – 0.12 µm)*

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Pb

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: **www.qorvo.com**

Tel: **1-844-890-8163**

Email: **customer.support@qorvo.com**

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