TGA2237-SM

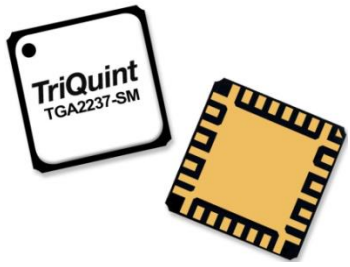
0.03–2.5 GHz 10 W GaN Power Amplifier

Product Overview

Qorvo's TGA2237-SM is a wideband distributed amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process. The TGA2237-SM operates from 0.03–2.5 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 50% power-added efficiency.

The TGA2237-SM is available in a low-cost, surface mount 32 lead 5 x 5 AIN QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2237-SM is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

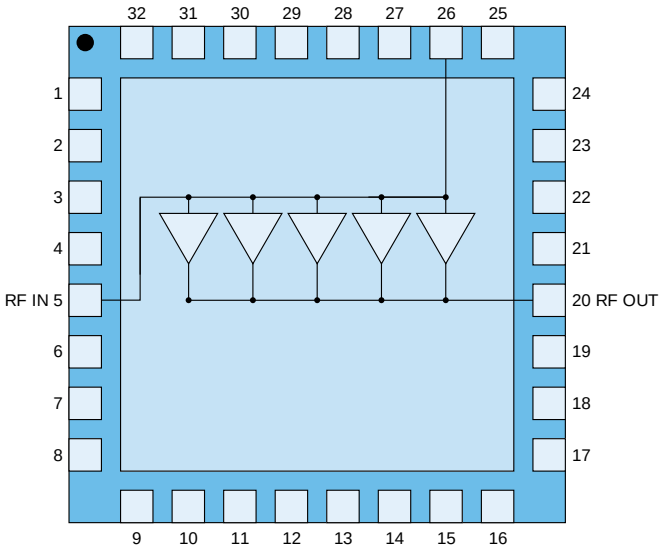
Lead-free and RoHS compliant.



Key Features

- Frequency Range: 0.03–2.5 GHz
- P_{SAT}: >40 dBm at P_{IN} = 27 dBm
- P1 dB: >33 dBm
- PAE: >50%
- Large Signal Gain: >13 dB
- Small Signal Gain: >19 dB
- Input Return Loss: >10 dB
- Output Return Loss: >12 dB
- Bias: V_D = 32 V, I_{DQ} = 360 mA
- Wideband Flat Power
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Functional Block Diagram



Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
TGA2237-SM	0.03–2.5 GHz 10 W GaN Power Amplifier
TGA2237-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	1.2 A
Gate Current (I_G)	-2.4 to 8.4 mA
Power Dissipation (P_{DISS}), 85 °C	19 W
Input Power (P_{IN}), CW, 50 Ω, 85 °C	33 dBm(*)
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 32V, 85 °C	33 dBm(*)
Max VSWR, CW, P_{IN} = 27 dBm, V_D = 32 V, 85 °C (Load)	10:1
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	32 V
Drain Current (I_{DQ})	360 mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

(*) Operational input power must be limited to 26 dBm when operating below 0.6 GHz to prevent excessive forward gate current.

Electrical Specifications

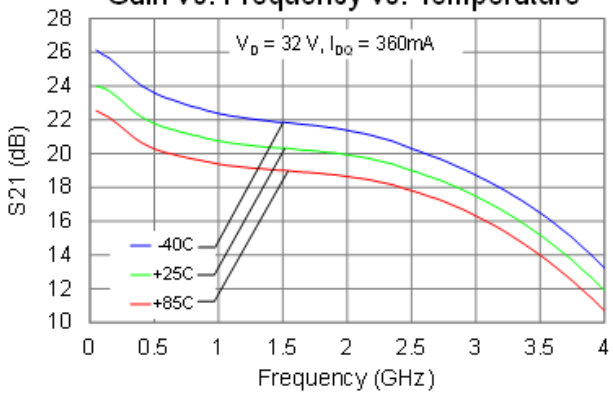
Test conditions unless otherwise noted: 25 °C, V_D = 32 V, I_{DQ} = 360 mA

Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		>19		dB
Input Return Loss		>10		dB
Output Return Loss		>12		dB
Output Power (P_{IN} = 27 dBm)		>40		dBm
Power Added Efficiency (P_{IN} = 27 dBm)		>50		%
Power @ 1 dB Compression (P1 dB)		>33		dBm
IM3 @ POUT/tone = 30 dBm		-25		dBc
IM5 @ POUT/tone = 30 dBm		-33		dBc
Small Signal Gain Temperature Coefficient		-0.03		dB/°C
Output Power Temperature Coefficient		-0.002		dBm/°C
Recommended Operating Voltage:	20	32		V

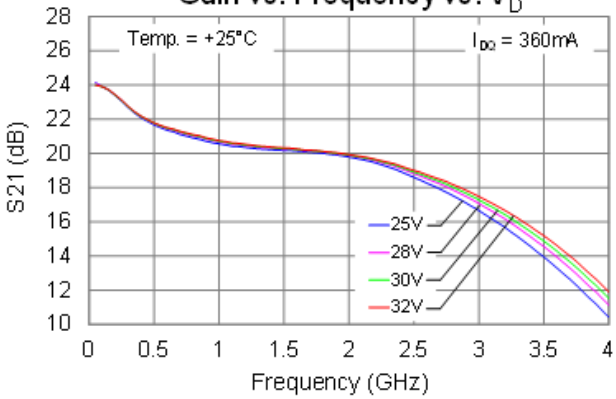
Typical Performance: Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

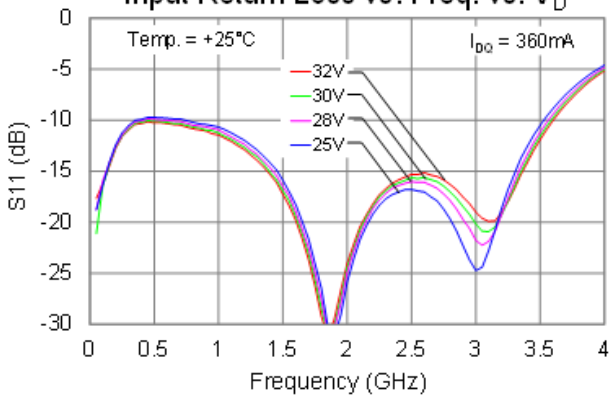
Gain vs. Frequency vs. Temperature



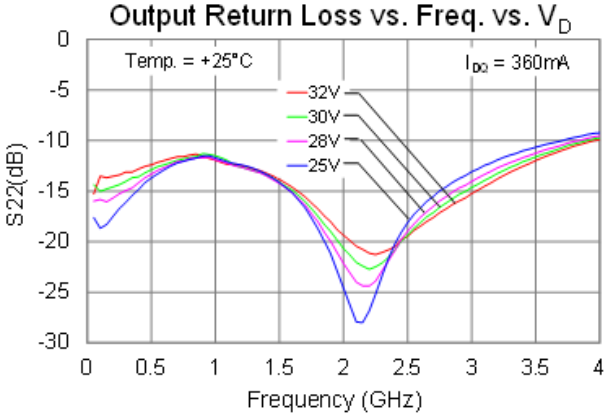
Gain vs. Frequency vs. V_D



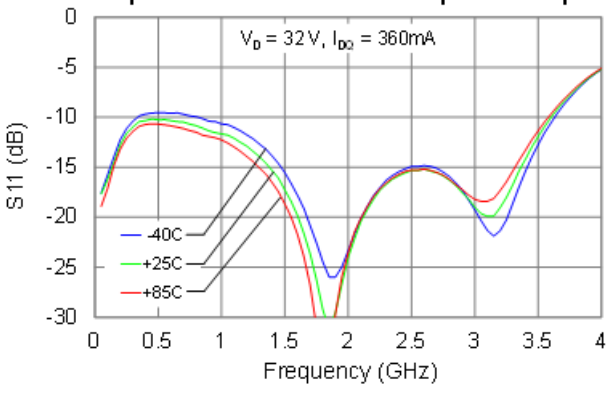
Input Return Loss vs. Freq. vs. V_D



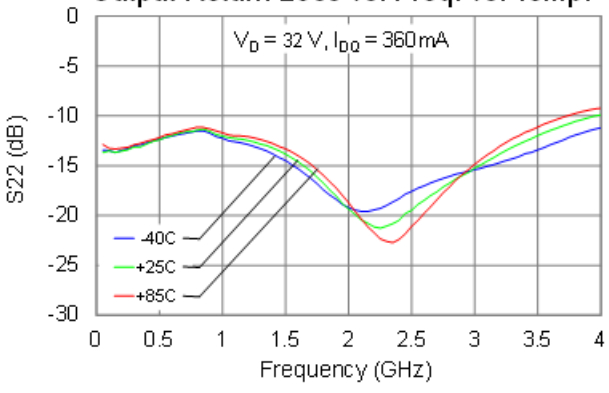
Output Return Loss vs. Freq. vs. V_D



Input Return Loss vs. Freq. vs. Temp.

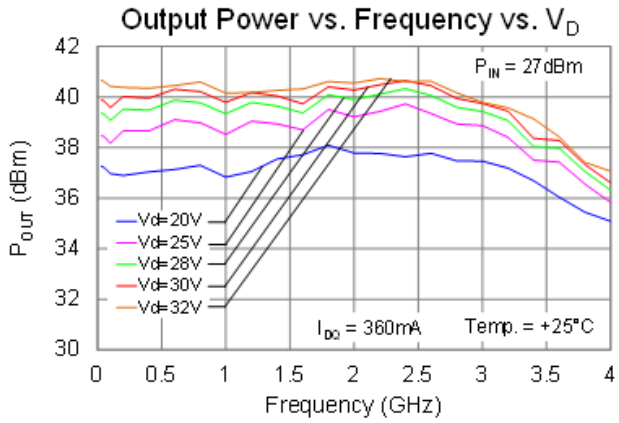


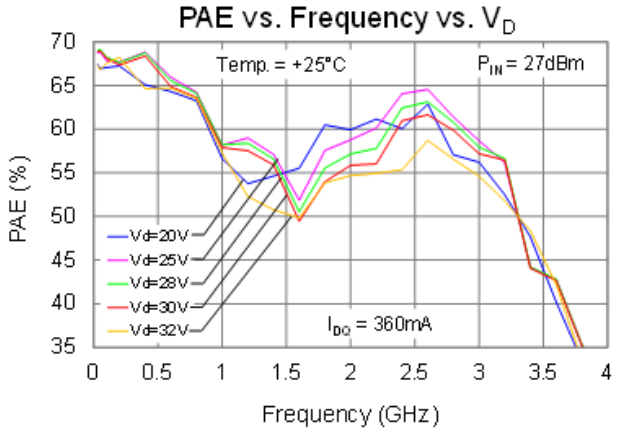
Output Return Loss vs. Freq. vs. Temp.

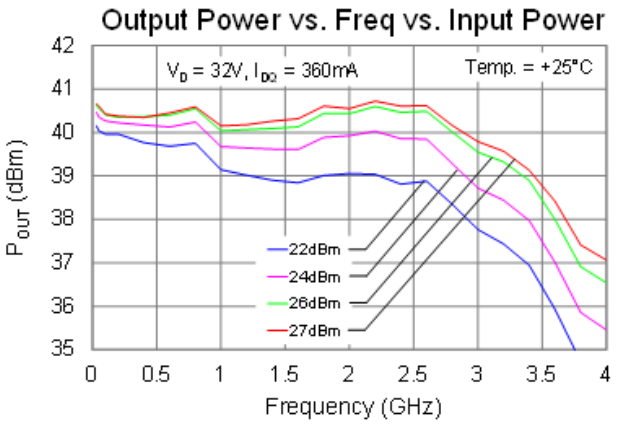


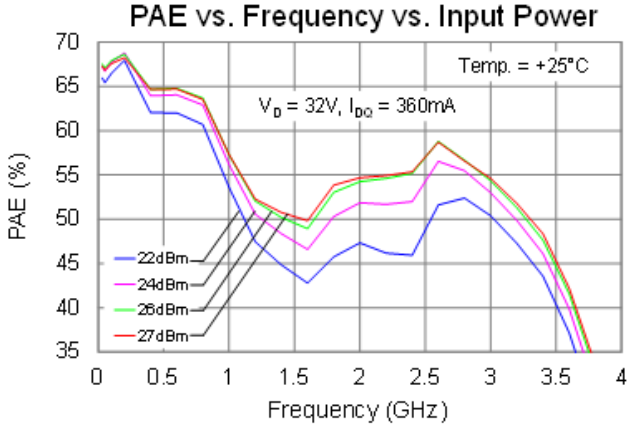
Typical Performance: Large Signal (CW)

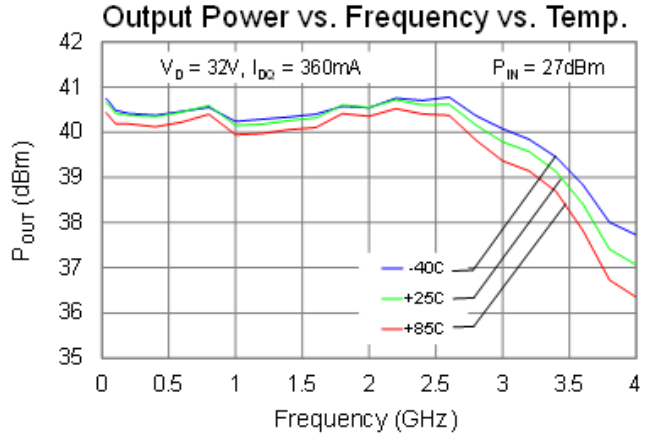
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

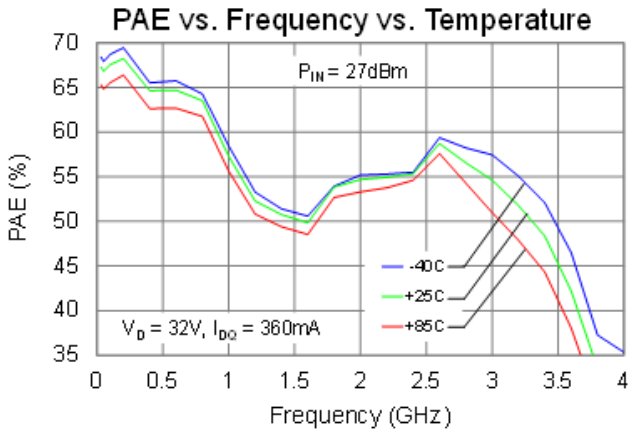












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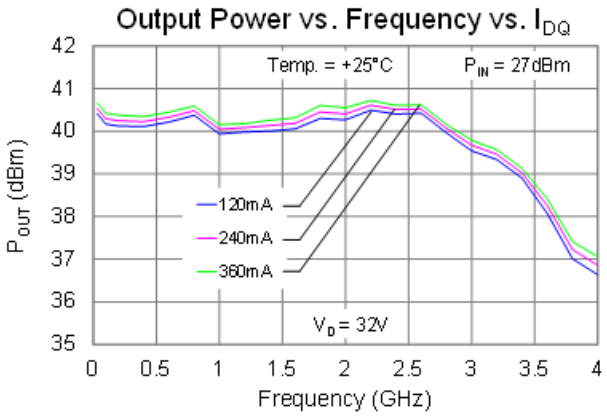
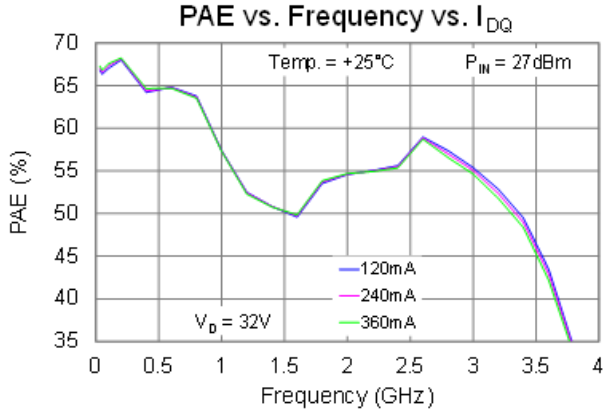
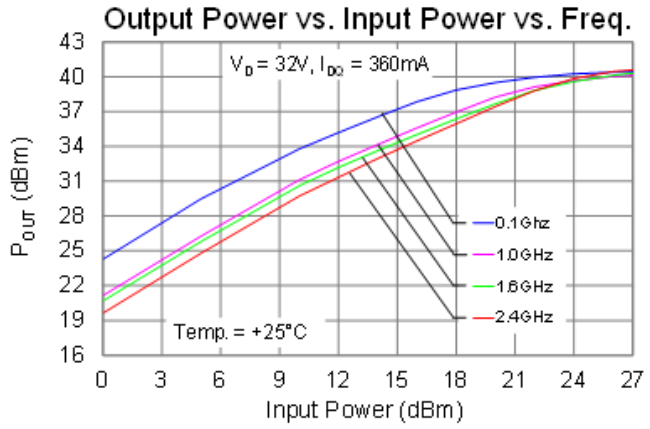
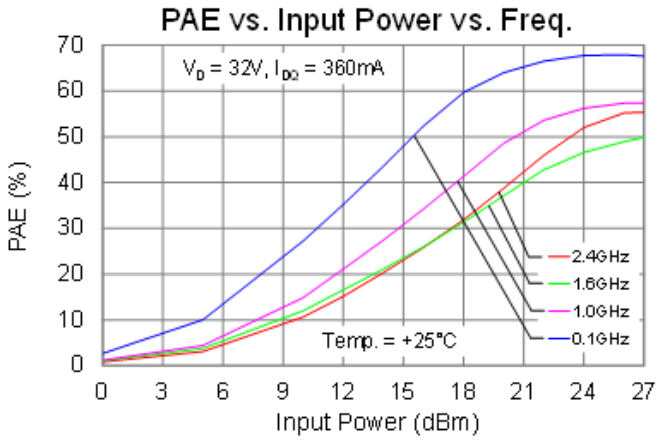
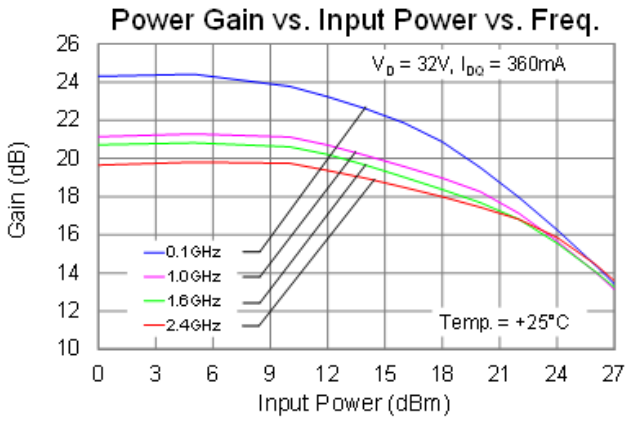
(See application circuit on page 11)

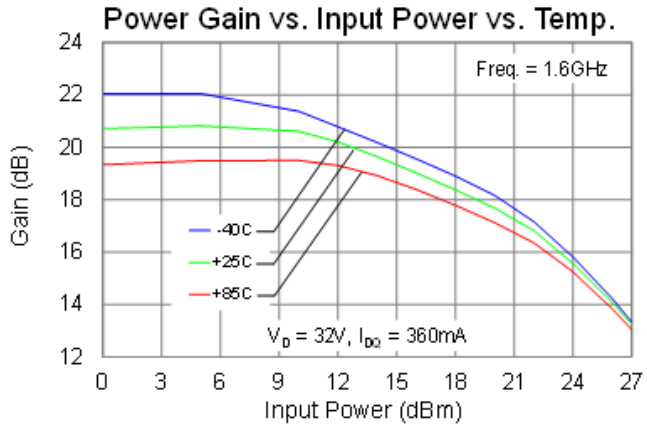






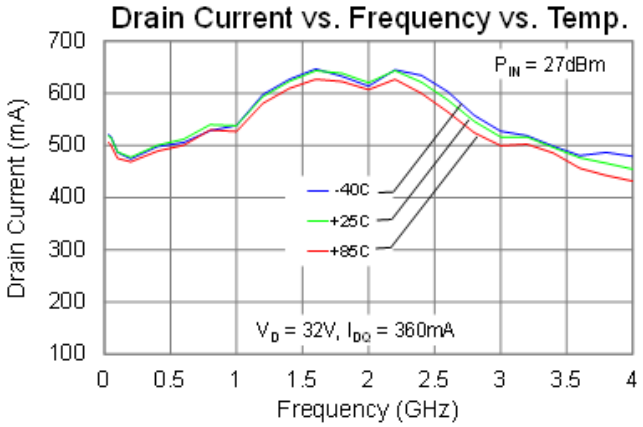


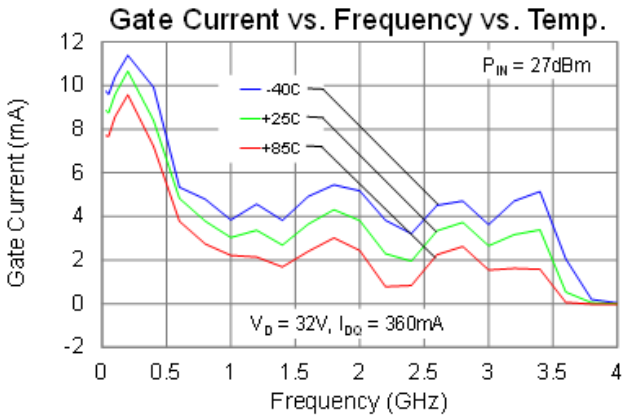


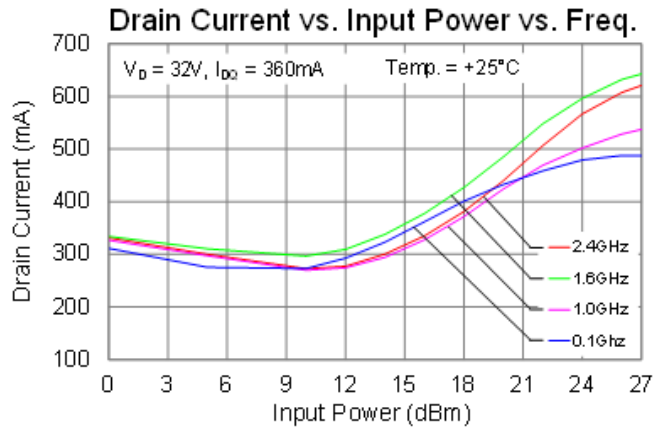


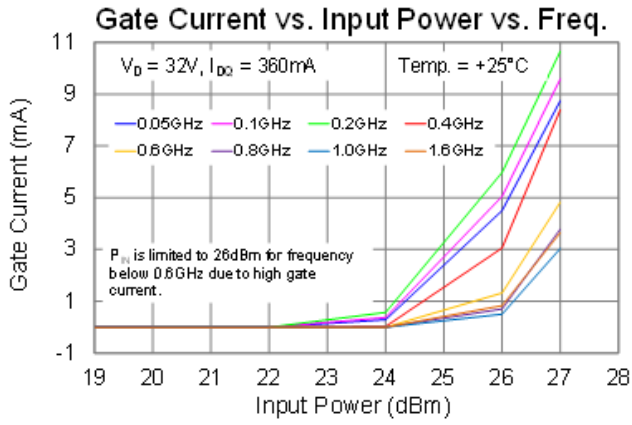
Typical Performance: Large signal (CW)

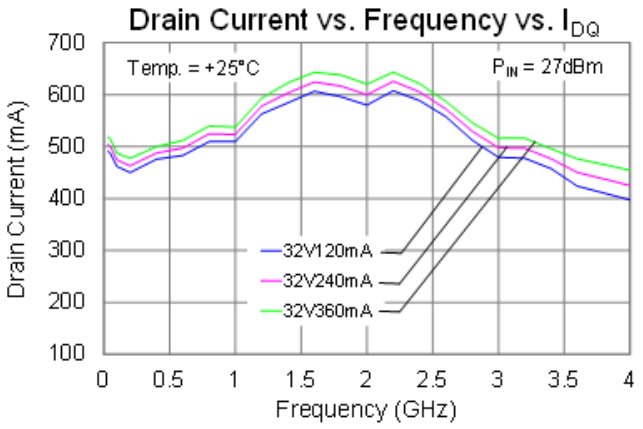
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

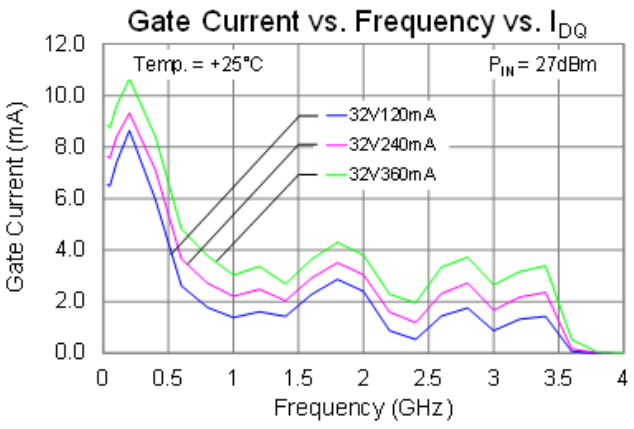






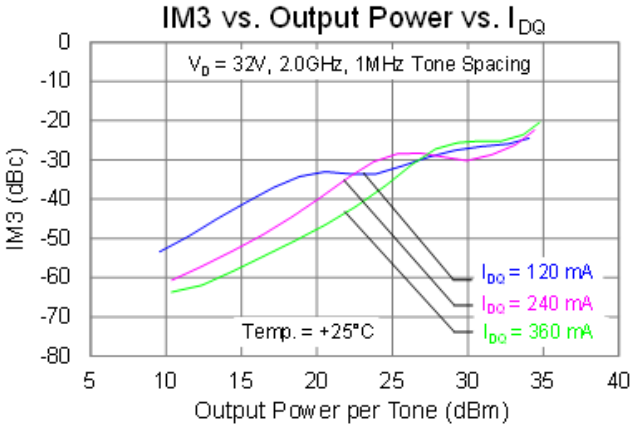


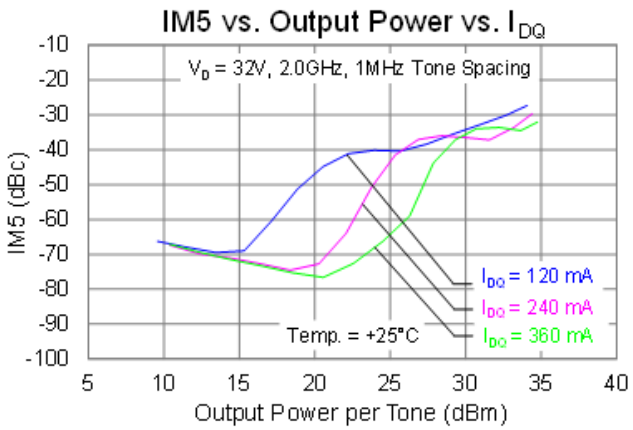


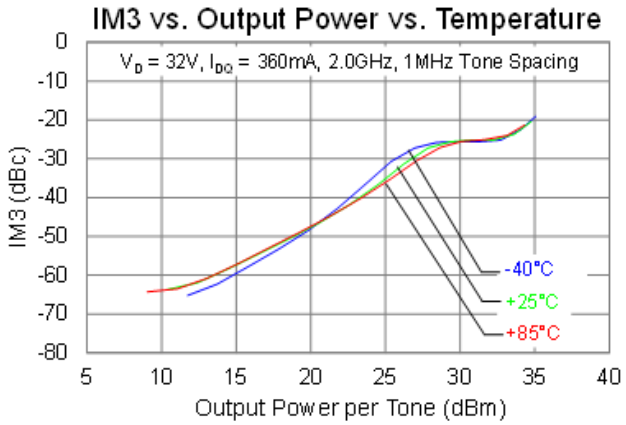


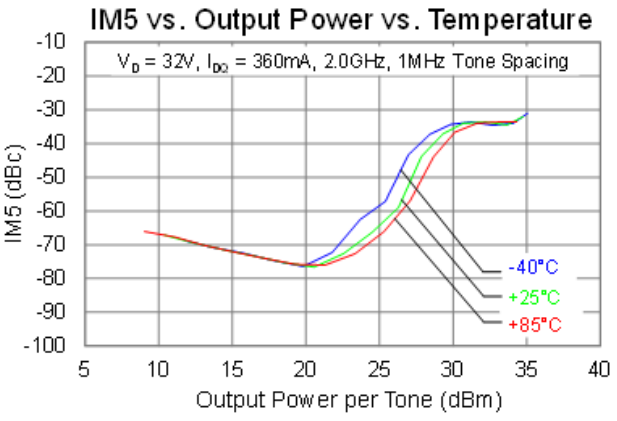
Typical Performance: Linearity

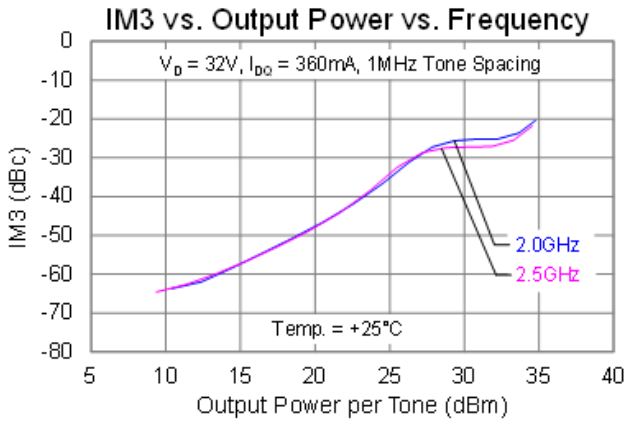
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

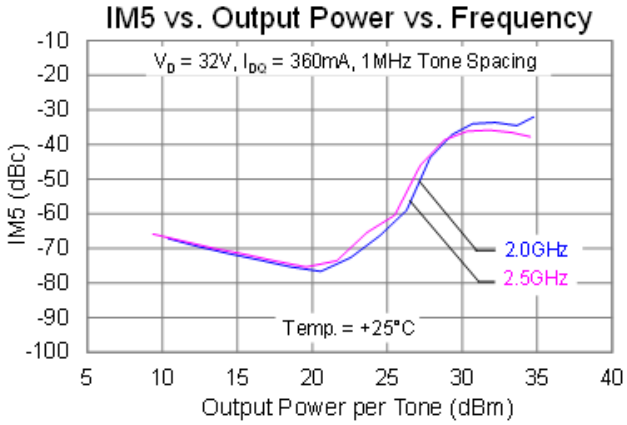






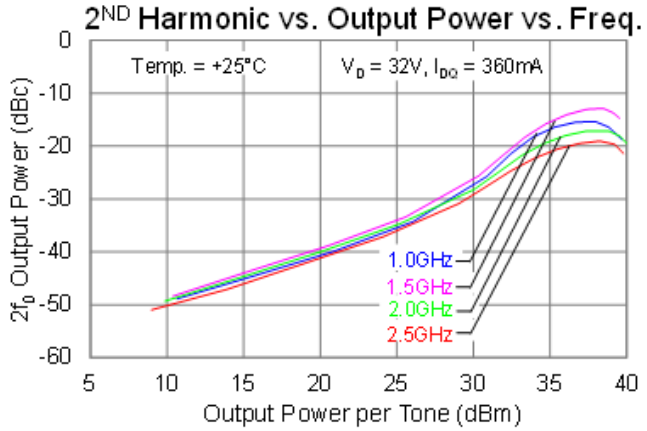


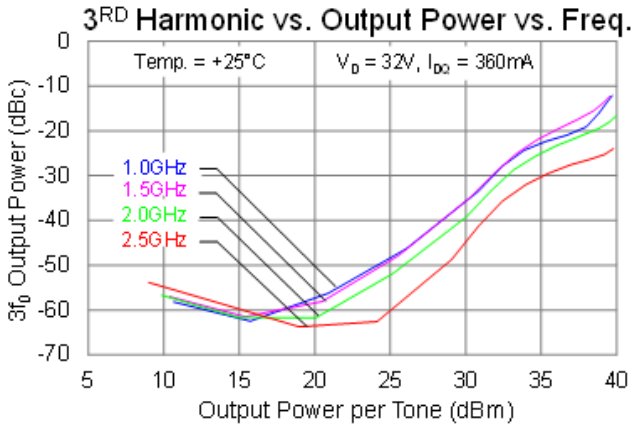


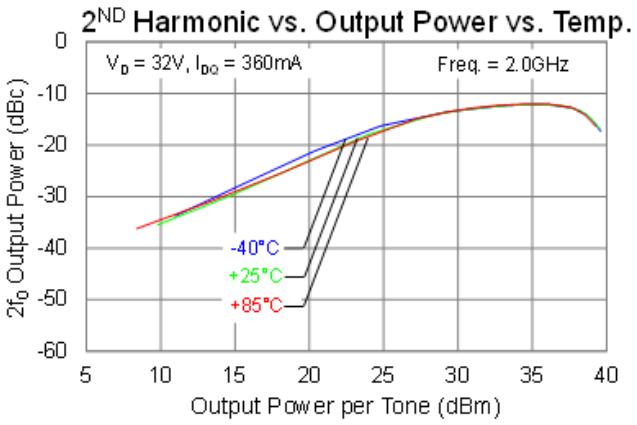


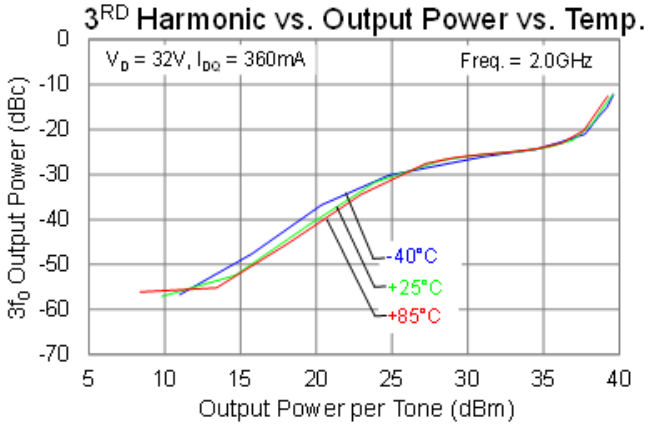
Typical Performance: Linearity

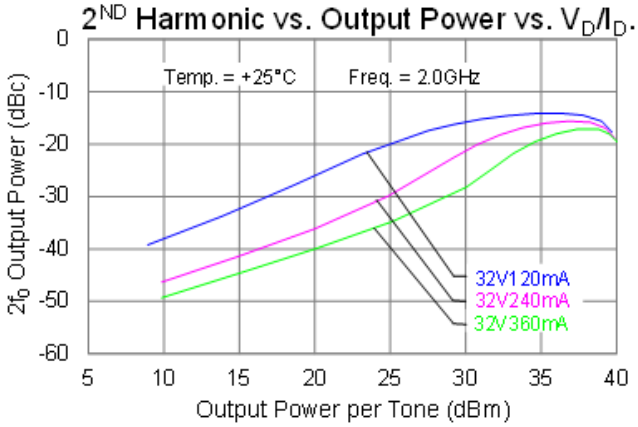
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

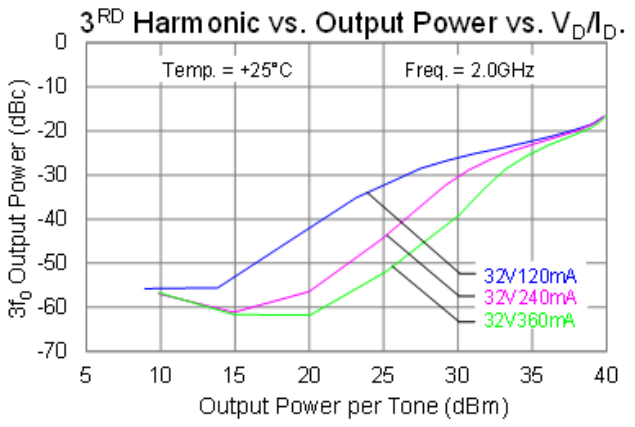






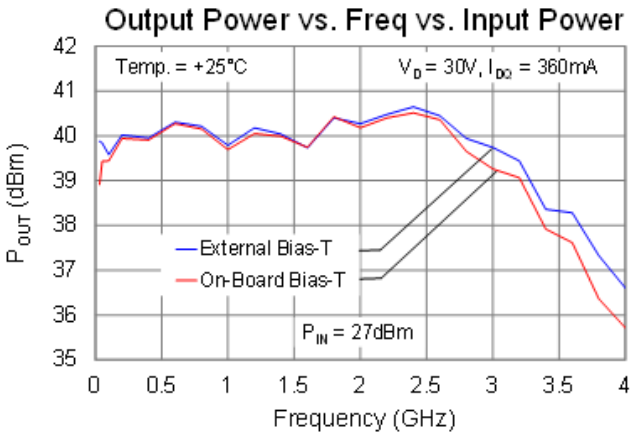


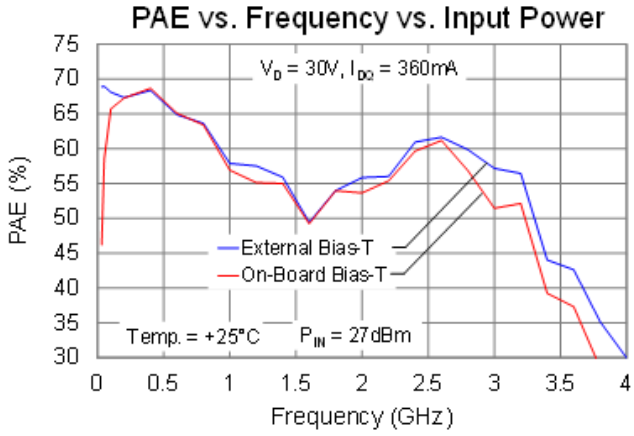




Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 11 and 13)



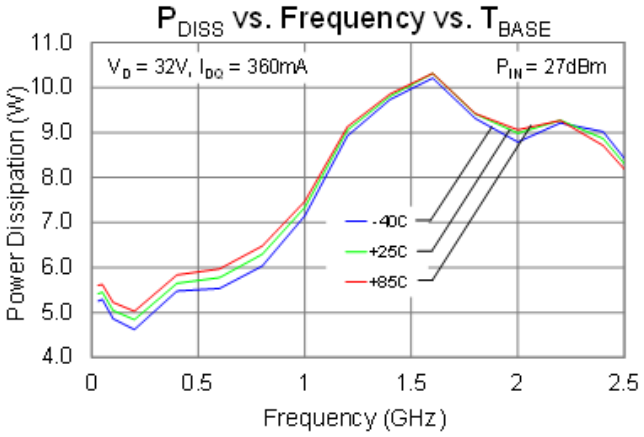


Thermal and Reliability Information

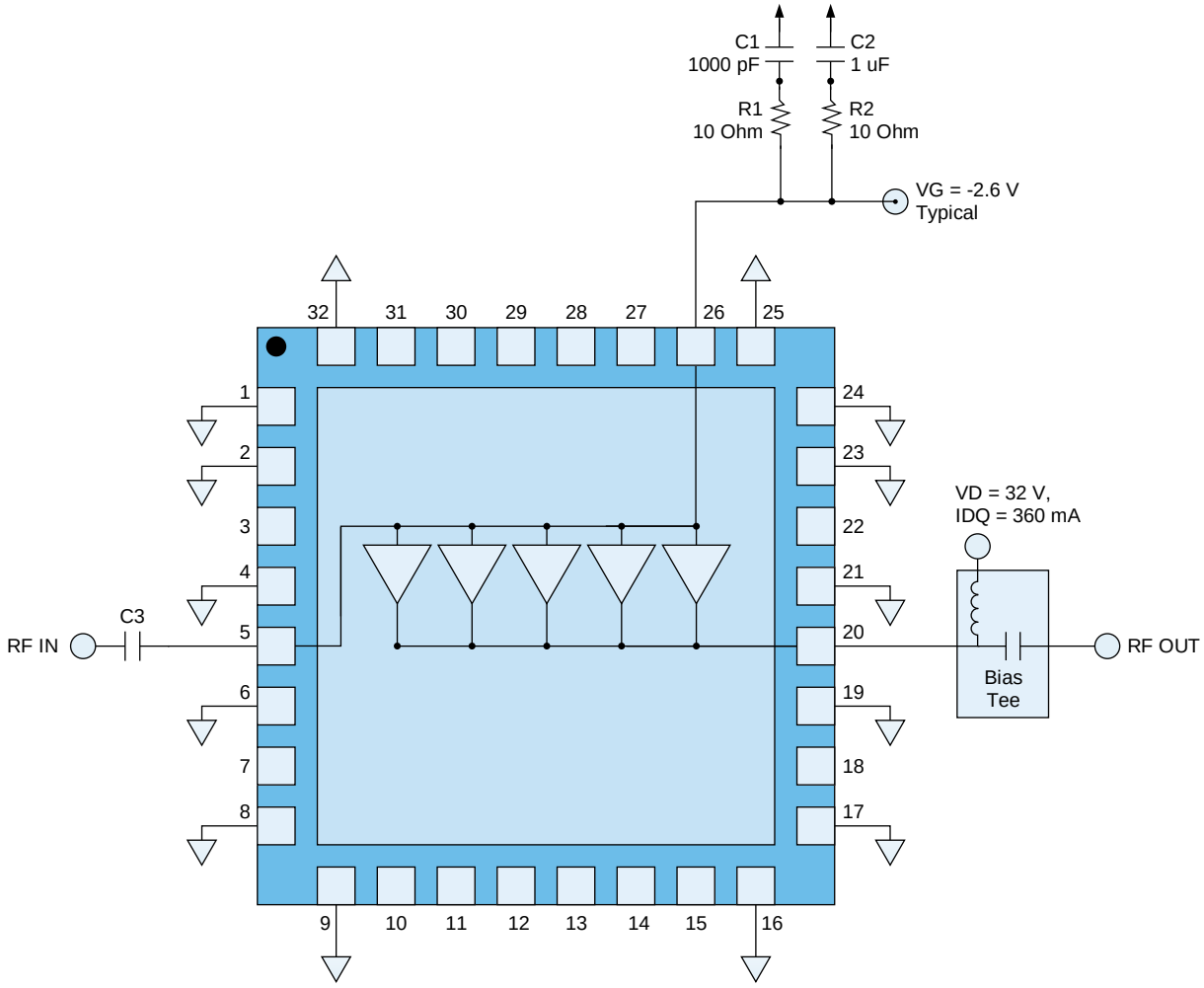
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 32 V, I_{DQ} = 360 mA, I_{D_Drive} = 630 mA, P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 10 W	6.79	ºC/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		152.9	°C

Notes:
1. Thermal resistance measured to back of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation



Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. Coaxial input DC block (C3) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

Bias-up Procedure

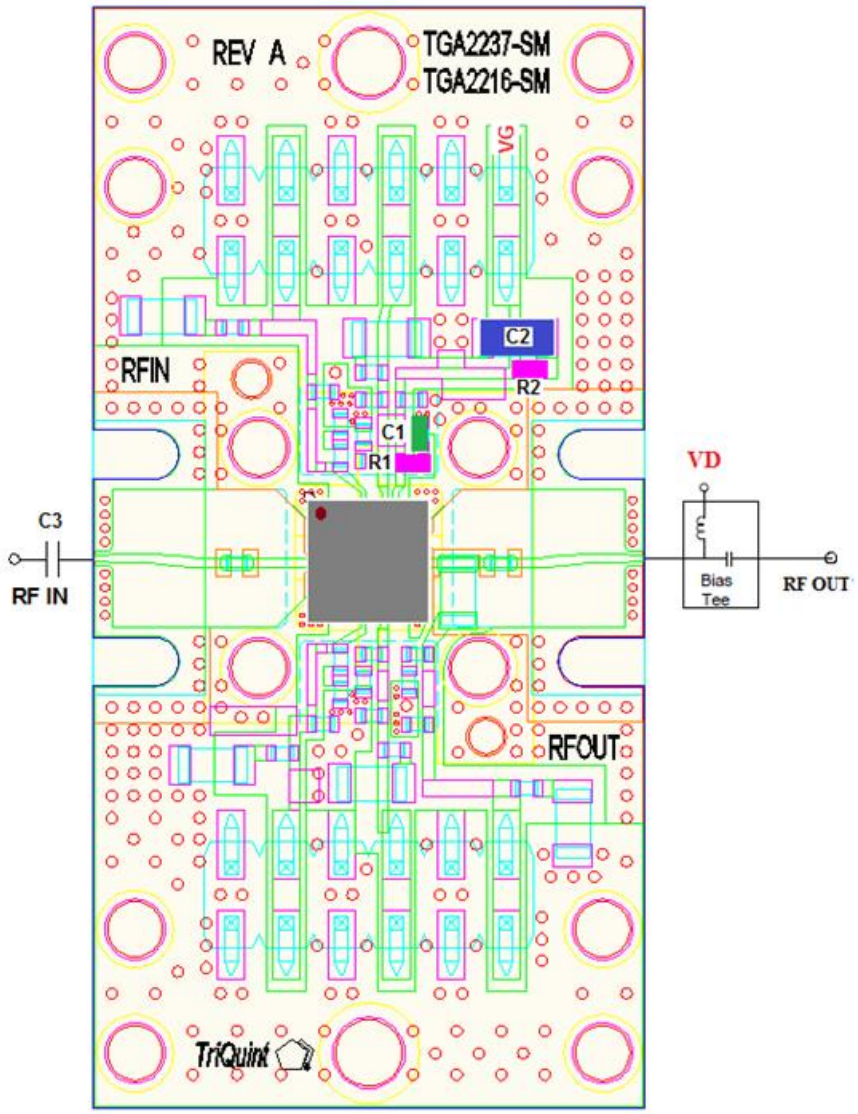
1. Set I_D limit to 700 mA, I_G limit to 7 mA
2. Set V_G to -5.0 V
3. Set V_D +32 V
4. Adjust V_G more positive until I_{DQ} = 360 mA (V_G ~ -2.6 V Typical)
5. Apply RF signal *

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

(*) P_{IN} is limited to 26 dBm for frequency < 0.6 GHz due to high gate current.

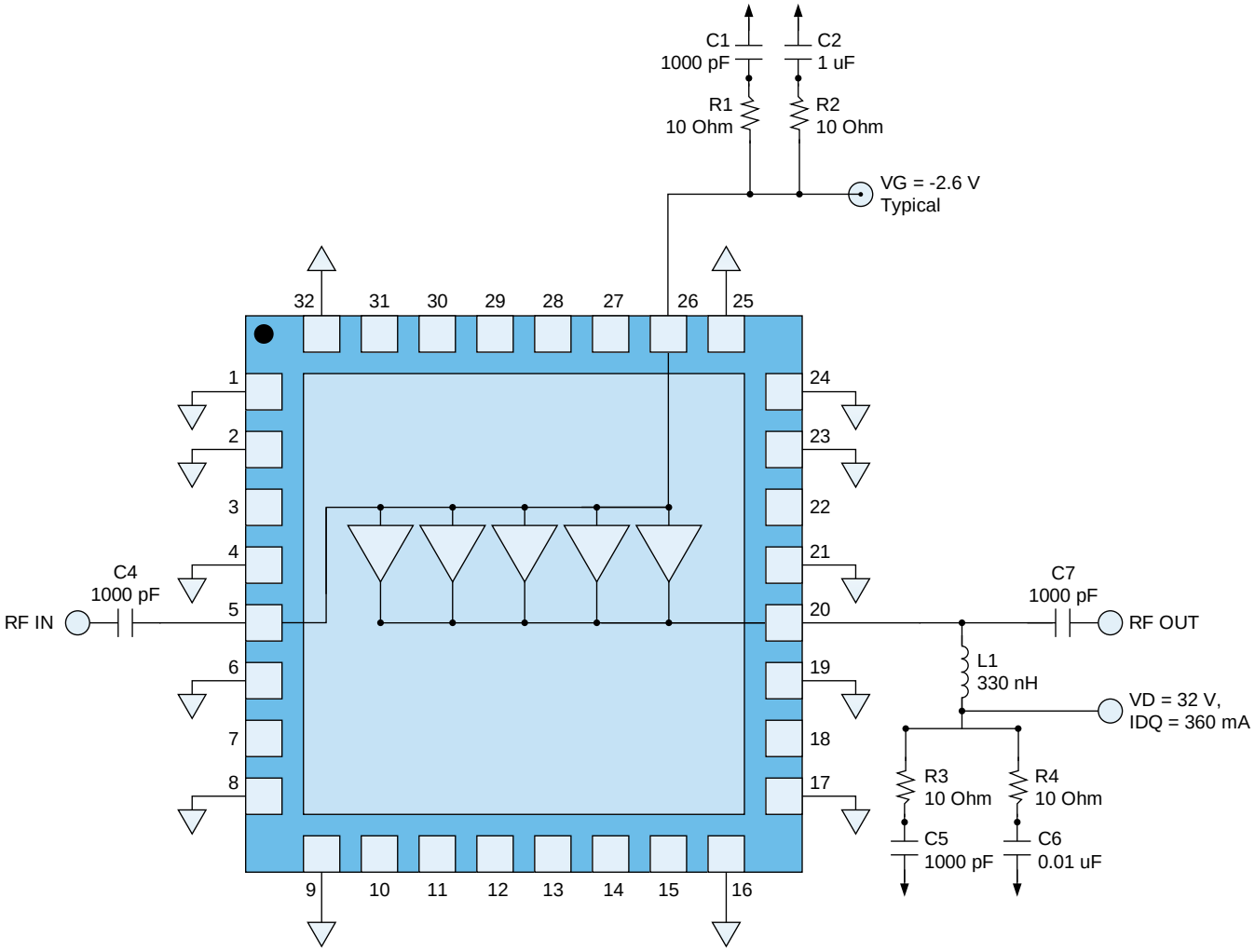
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

Reference Designator	Value	Description	Manufacturer	Part Number
C1	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C2	1 uF	Cap, 1206, 50 V, 10%, X7R	Various	
C3	1000 pF	DC Block	Various	
R1 – R2	10 Ω	Res, 0402	Various	

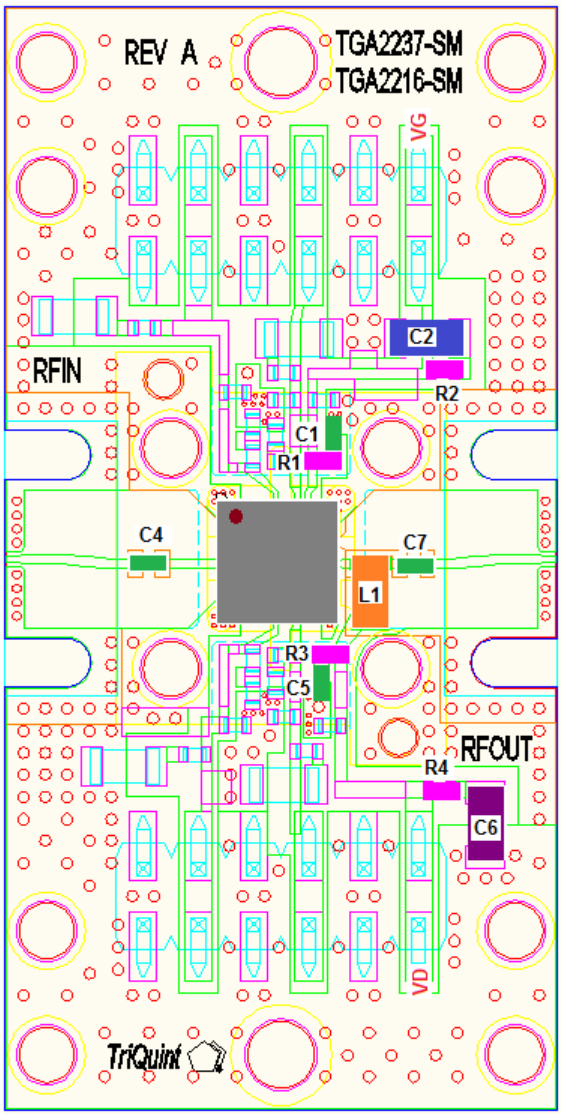
Application Circuit (Option with board-level DC blocks and output bias tee)



Notes:

1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

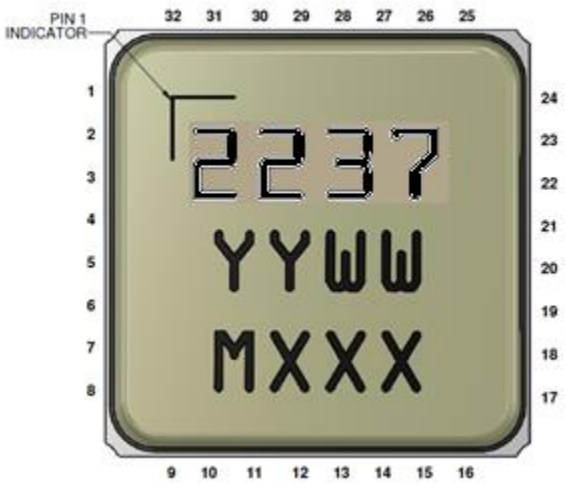
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option

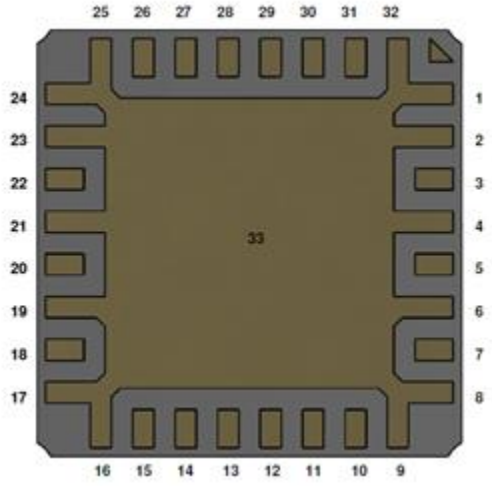


Bill of Materials For On-Board Bias-Tee

Reference Designator	Value	Description	Manufacturer	Part Number
C1, C4, C5, C7	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C2	1 uF	Cap, 1206, 50 V, 10%, X7R	Various	
C6	0.01 uF	Cap, 1206, 100 V, 10%, X7R	Various	
L1	330 nH	Ind, 1206, 100 V, 10%, X7R	Various	
R1 – R4	10 Ω	Res, 0402	Various	

Pin Layout

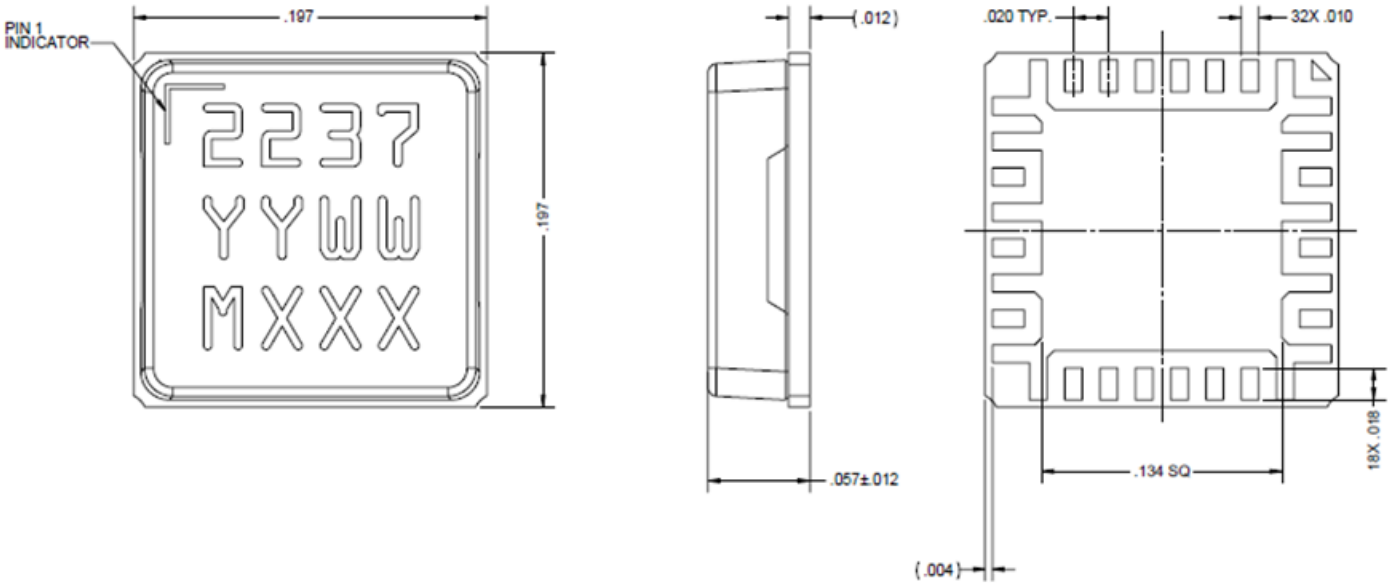




Pin Description

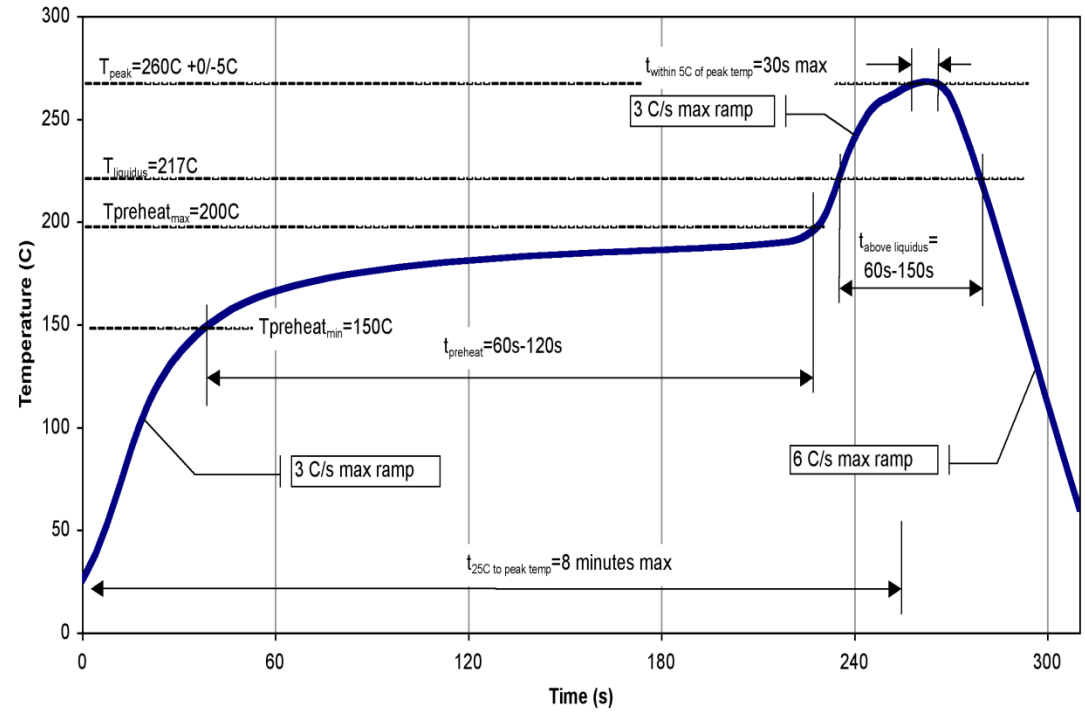
Pin No.	Symbol	Description
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB.
3, 7, 10-15, 18, 22, 27-31	NC	No connection.
5	RF IN	Input; matched to 50 Ω.
20	RF OUT/ DRAIN	Output; matched to 50 Ω.
26	GATE	GATE voltage; bias network is required; see recommended Application Information on page 11.
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Mechanical Information



Units: inches
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Base: Ceramic
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2237: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charge Device Model (CDM)	C2	JESD22-C101
Moistrue Sensitivity Level	MSL 1	J-STD-020, Level 1

Caution!

ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C. The use of no-clean solder to avoid washing after soldering is recommended.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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