ON Semiconductor®

PCS3P73U00A

USB 2.0 Peak EMI reduction IC

General Features

- 1x Peak EMI Reduction IC
- Input frequency:
  - 10MHz - 60MHz @ 2.5V
  - 10MHz - 70MHz @ 3.3V
- Output frequency:
  - 10MHz - 60MHz @ 2.5V
  - 10MHz - 70MHz @ 3.3V
- Supply Voltage: 2.5V±0.2V
  - 3.3V ±0.3V
- Analog Spread Selection up to ±0.5%
- ModRate selection option
- Commercial temperature range
- 8-pin TSSOP, SOIC and TDFN (2X2) COL Package
- Conforms to USB2.0 compliance standards
- The First True Drop-in Solution

Product Description

PCS3P73U00A is a versatile, 3.3V / 2.5V Peak EMI reduction IC. PCS3P73U00A accepts an input clock either from a Crystal or from an external reference (AC or DC coupled to XIN / CLKIN) and locks on to it delivering a 1x modulated clock output. PCS3P73U00A has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer to the *Frequency Selection Table* for details.

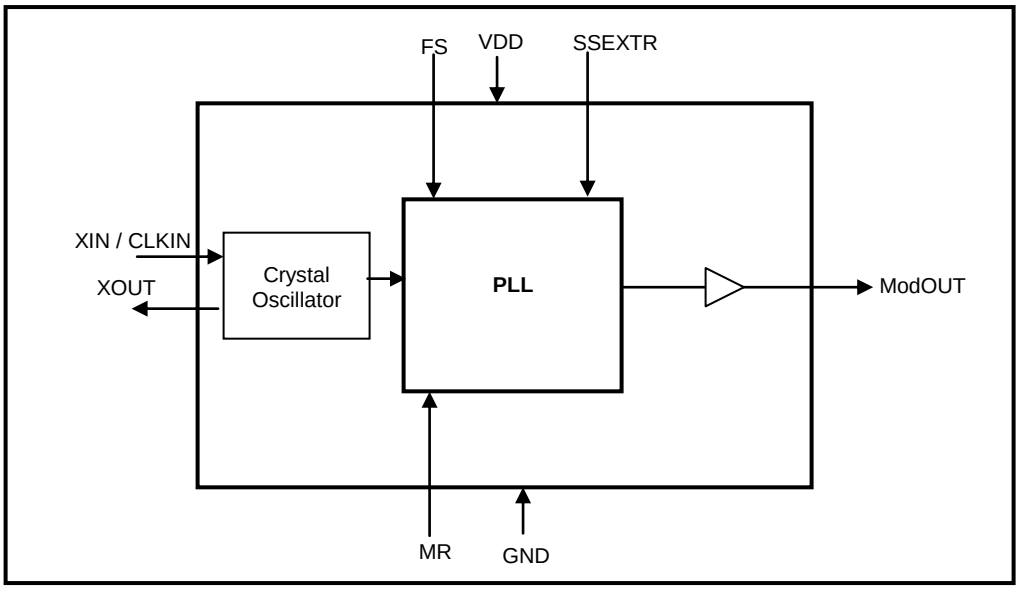
PCS3P73U00A has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected between SSEXTR and GND. Modulation Rate (MR) control selects two different Modulation Rates.

PCS3P73U00A operates from a 3.3V / 2.5V supply and is available in an 8-pin TSSOP, SOIC, and TDFN (2X2) COL packages, over Commercial temperature range.

Applications

PCS3P73U00A is targeted for USB applications. Refer to *SSEXTR Resistance Table for USB2.0 Compliance* for commonly used frequencies.

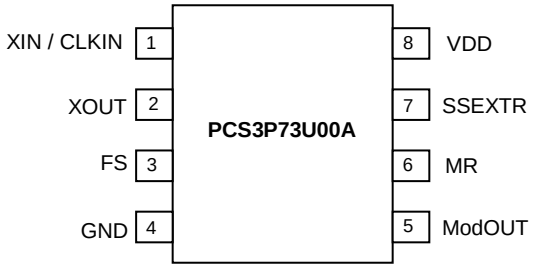
Block Diagram



JANUARY 2010 – Rev. 1

Publication Order Number:
PCS3P73U00/D

Pin Configuration



Pin Description

Pin #	Pin Name	Pin Type	Description
1	XIN / CLKIN	I	Crystal connection or external reference clock input.
2	XOUT	O	Crystal connection. If using an external reference, this pin should be left open.
3	FS	I	Frequency Select.Pull LOW to select Low Frequency range. Selects High Frequency range when pulled HIGH. Has an internal pull-up resistor (*see Frequency Selection Table* for details).
4	GND	P	Ground.
5	ModOUT	O	Buffered Modulated clock output.
6	MR	I	Modulation Rate Select. When LOW selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull-down resistor.
7	SSEXTR	I	Analog Spread Selection through external resistor to GND.
8	VDD	P	3.3V / 2.5V supply Voltage

Frequency Selection table

VDD(V)	FS	Frequency (MHz)
2.5V	0	10-20
	1	20-60
3.3V	0	10-27
	1	20-70

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{DD}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD(3.3V)}$	Supply Voltage	3.0	3.6	V
$V_{DD(2.5V)}$	Supply Voltage	2.3	2.7	V
T_A	Operating Temperature (Ambient Temperature)	0	+70	°C
C_L	Load Capacitance		10	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for 3.3V Supply voltage

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IL}	Input LOW Voltage					0.8	V
V_{IH}	Input HIGH Voltage			2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V				-50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA				0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		2.4			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled to GND				750	µA
I_{DD}	Dynamic Supply Current	Unloaded outputs	FS=0; @ 12MHz		8		mA
			FS=1; @ 48MHz		12		
Z_o	Output Impedance				30		Ω

Switching Characteristics for 3.3 Supply Voltage

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency	FS=0	10	12	27	MHz
	FS=1	20	48	70	
ModOUT	FS=0	10	12	27	
	FS=1	20	48	70	
Duty Cycle[1,2]	Measured at V_{DD} /2	45	50	55	%
Rise Time[1,2]	Measured between 20% to 80%		1.1		nS
Fall Time[1,2]	Measured between 80% to 20%		0.7		nS
Cycle-to-Cycle Jitter[1,2]	Loaded outputs		±150		pS
PLL Lock Time[2]	Stable power supply, valid clock presented on XIN / CLKIN pin			3	mS

Notes: 1. All parameters are specified with 10pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics for 2.5V Supply voltage

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			2.3	2.5	2.7	V
V_{IL}	Input LOW Voltage					0.7	V
V_{IH}	Input HIGH Voltage			1.7			V
I_{IL}	Input LOW Current	V_{IN} = 0V				-50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA				0.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		1.8			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled to GND				500	µA
I_{DD}	Dynamic Supply Current	Unloaded outputs	FS=0; @ 12MHz		5		mA
			FS=1; @ 48MHz		8		
Z_o	Output Impedance				40		Ω

Switching Characteristics for 2.5V Supply Voltage

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency	FS=0	10	12	20	MHz
	FS=1	20	48	60	
ModOUT	FS=0	10	12	20	
	FS=1	20	48	60	
Duty Cycle[1,2]	Measured at V_{DD} /2	45	50	55	%
Rise Time[1,2]	Measured between 20% to 80%		1.6		nS
Fall Time[1,2]	Measured between 80% to 20%		0.8		nS
Cycle-Cycle Jitter[1,2]	Loaded outputs		±200		pS
PLL Lock Time[2]	Stable power supply, valid clock presented on XIN / CLKIN pin			3	mS

Notes: 1. All parameters are specified with 10pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

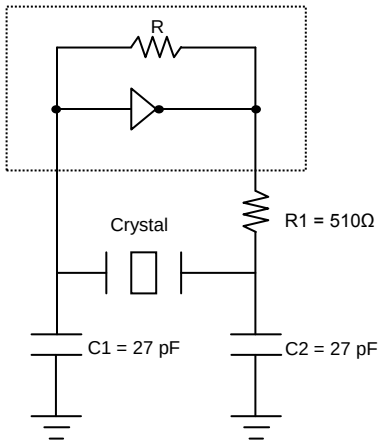


Fig. 1: Typical Crystal Interface Circuit

Note: For AC Coupled Interface refer to Application Brief: CT100801.

Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	48MHz
Frequency tolerance	±50ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

$R_{Compliance}$

The value of the compliance resistor, $R_{Compliance}$ sets the USB2.0 signaling rate (frequency) deviation to 1000ppm peak-to-peak (+/-500ppm). It causes a -4dB peak power EMI reduction at the 480MHz fundamental USB2.0 frequency. Higher harmonics are reduced more.

If the $R_{Compliance}$ is set to a lower value than its compliance limit, it will set the USB2.0 signaling rate (frequency) deviation to above 1000ppm peak-to-peak. For settings above 1000ppm the USB2.0 compliance pass/fail becomes gradually intermittent. USB2.0 functionality is maintained upto 3000ppm peak-to-peak signaling rate (frequency) deviation. The EMI tradeoff in the system is attenuation/compliance. While fully functional (and compliant intermittent) the 2000ppm frequency deviation can provide -7dB of EMI attenuation at the 480MHz fundamental.

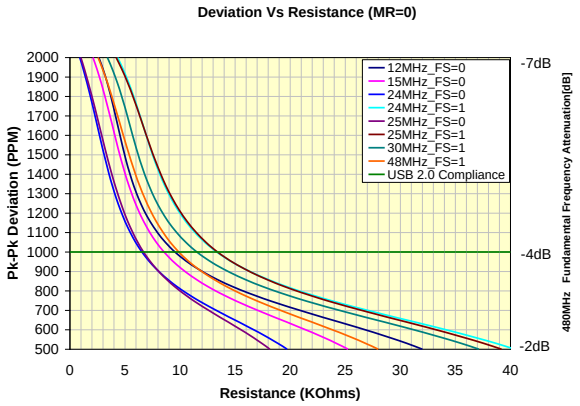


Fig. 2: Deviation Vs Resistance for USB 2.0 Compliance (MR=0)

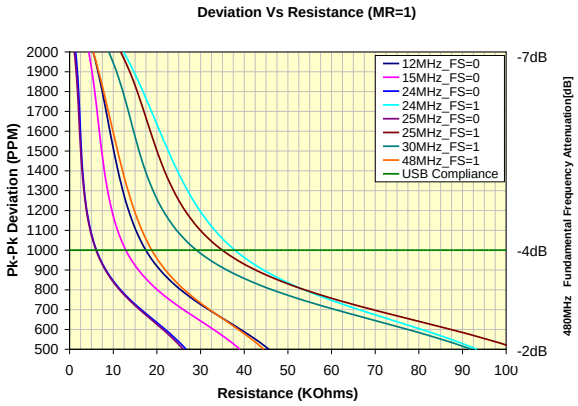


Fig. 3: Deviation Vs Resistance for USB 2.0 Compliance (MR=1)

SSEXTR Resistance Table for USB2.0 compliance ($R_{Compliance}$)

VDD = 3.3V; MR = 0

Frequency (MHz)	FS (MHz)	SSEXTR[1] Resistance (KΩ)
12	0	10
15	0	8.87
24	0	6.81
	1	13.7
25	0	6.98
	1	13.7
30	1	12.1
48	1	10

VDD = 3.3V; MR = 1

Frequency (MHz)	FS (MHz)	SSEXTR[1] Resistance (KΩ)
12	0	17.8
15	0	13
24	0	6.49
	1	39.2
25	0	6.49
	1	35.7
30	1	29.4
48	1	19.1

VDD = 2.5V; MR = 0

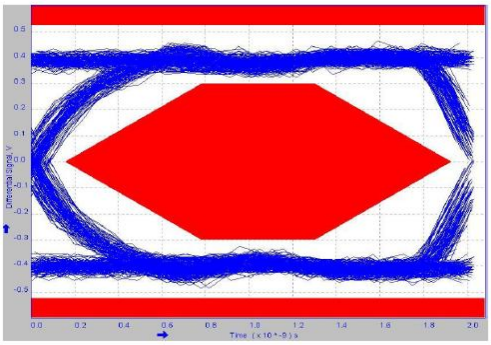
Frequency (MHz)	FS (MHz)	SSEXTR[1] Resistance (KΩ)
12	0	10
15	0	8.87
24	1	13.7
25	1	13.7
30	1	12.1
48	1	10

VDD = 2.5V; MR = 1

Frequency (MHz)	FS (MHz)	SSEXTR[1] Resistance (KΩ)
12	0	17.8
15	0	13
24	1	39.2
25	1	35.7
30	1	29.4
48	1	19.1

Note: 1. Standard 1% tolerance Resistors.
Device to Device variation of Deviation is ±10%.

Fig. 4:Eye Diagram example (480MHz) computed from the USB-IF test pattern during USB2.0 compliance verification of an existing HOST PHY ASIC clocked at 48MHz by PCS3P73U00A.



Eye Diagram

Results based on USB-IF / Waiver Limits:

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Monotonic Property	-	-	-	-	-	-	0	Pass
Eye Diagram Test	-	-	-	-	-	-	-	Pass
Signal Rate	471.8836Mbps	488.7984Mbps	479.8467Mbps	0.0000bps	2.881103Mbps	480.0828Mbps	512	Pass
EOP Width	-	-	15.74583ns	-	-	-	1	Pass
EOP Width (Bits)	-	-	7.555586	-	-	-	1	Pass
Rise Time	568.8889ps	854.1667ps	692.4406ps	285.2778ps	58.62538ps	694.8948ps	107	Pass
Fall Time	554.5263ps	825.0000ps	691.5909ps	270.4737ps	55.33780ps	693.7807ps	107	Pass

Monotonicity test is performed on the test limits of 25.0% and 75.0%.

Additional Information:

Consecutive Jitter range:	-79.57ps to 88.44ps	RMS Jitter	37.01ps
KJ Paired Jitter range:	-61.95ps to 75.99ps	RMS Jitter	17.61ps
JK Paired Jitter range:	-37.71ps to 49.32ps	RMS Jitter	15.43ps

*The Overall Result for this test is **Pass**, because one or more individual status of the measurements is **Pass**.
For this test, the recommended configuration for USB2 testing (as per USB-IF) is on Tier 1.

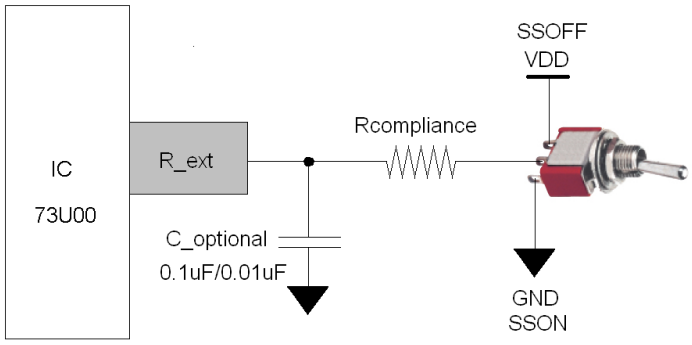


Fig. 5: EMI Radiated Emission Test Circuit (requires USB PHY ASIC, not shown here)

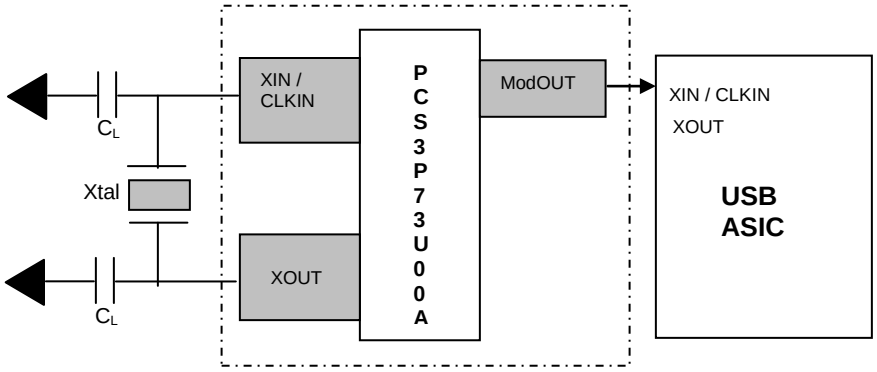
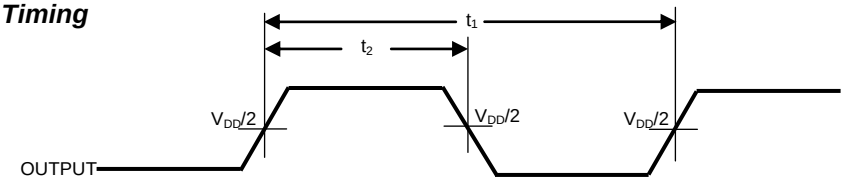


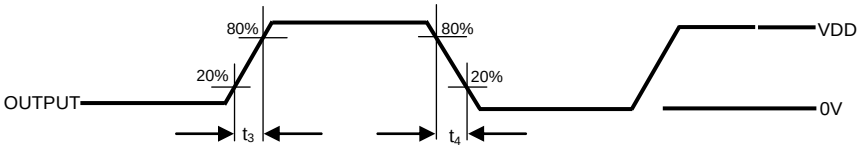
Fig. 6: Typical Application Circuit

Switching Waveforms

Duty Cycle Timing

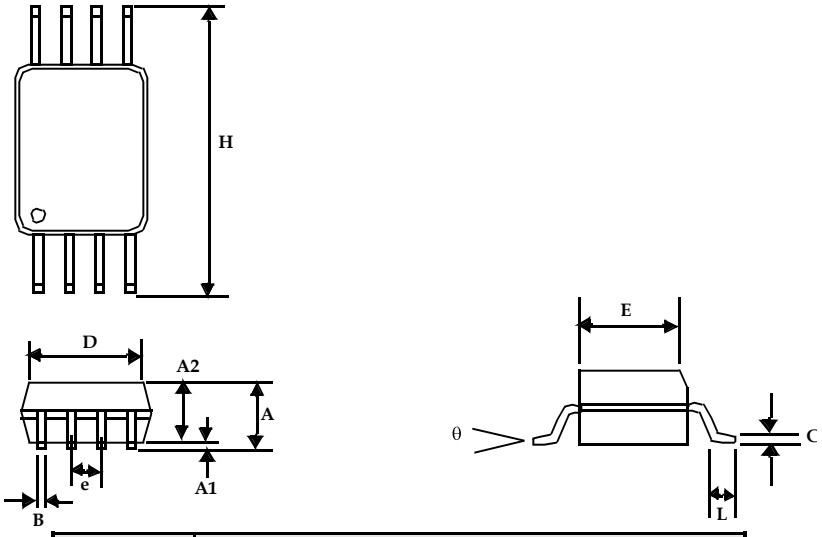


Output Rise/Fall Time



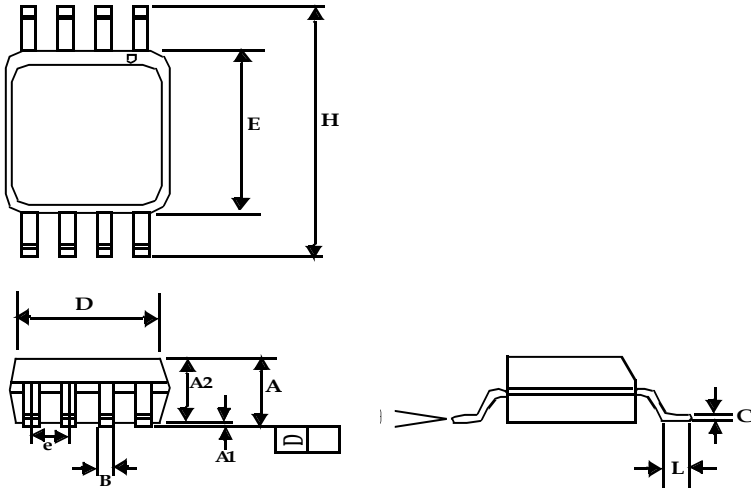
Package Information

8-lead TSSOP (4.40-MM Body)



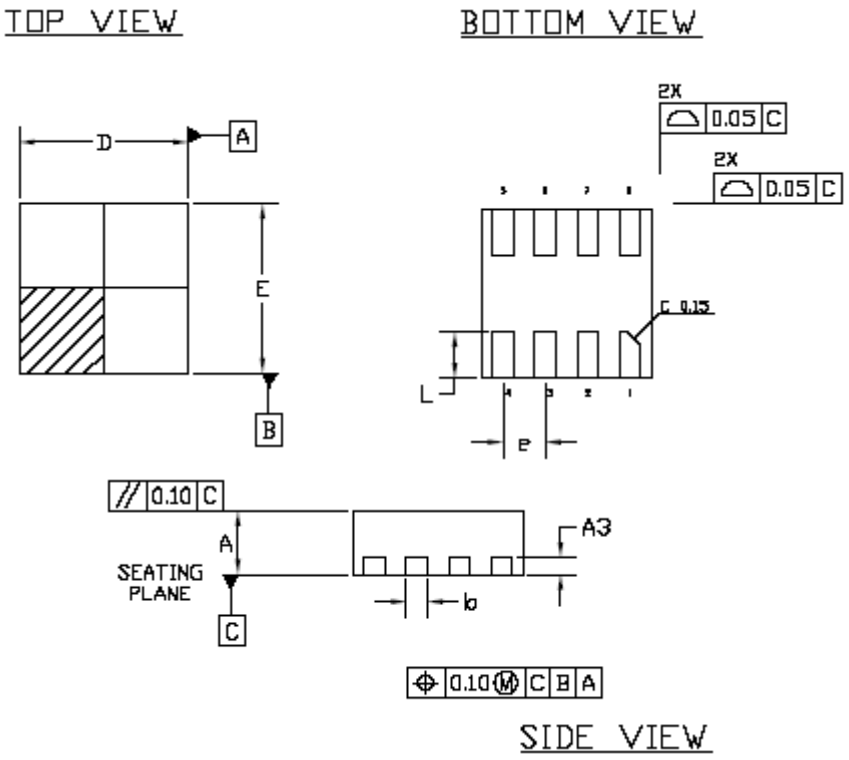
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

8-Pin SOIC



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

TDFN COL 2x2 8L package Outline drawing



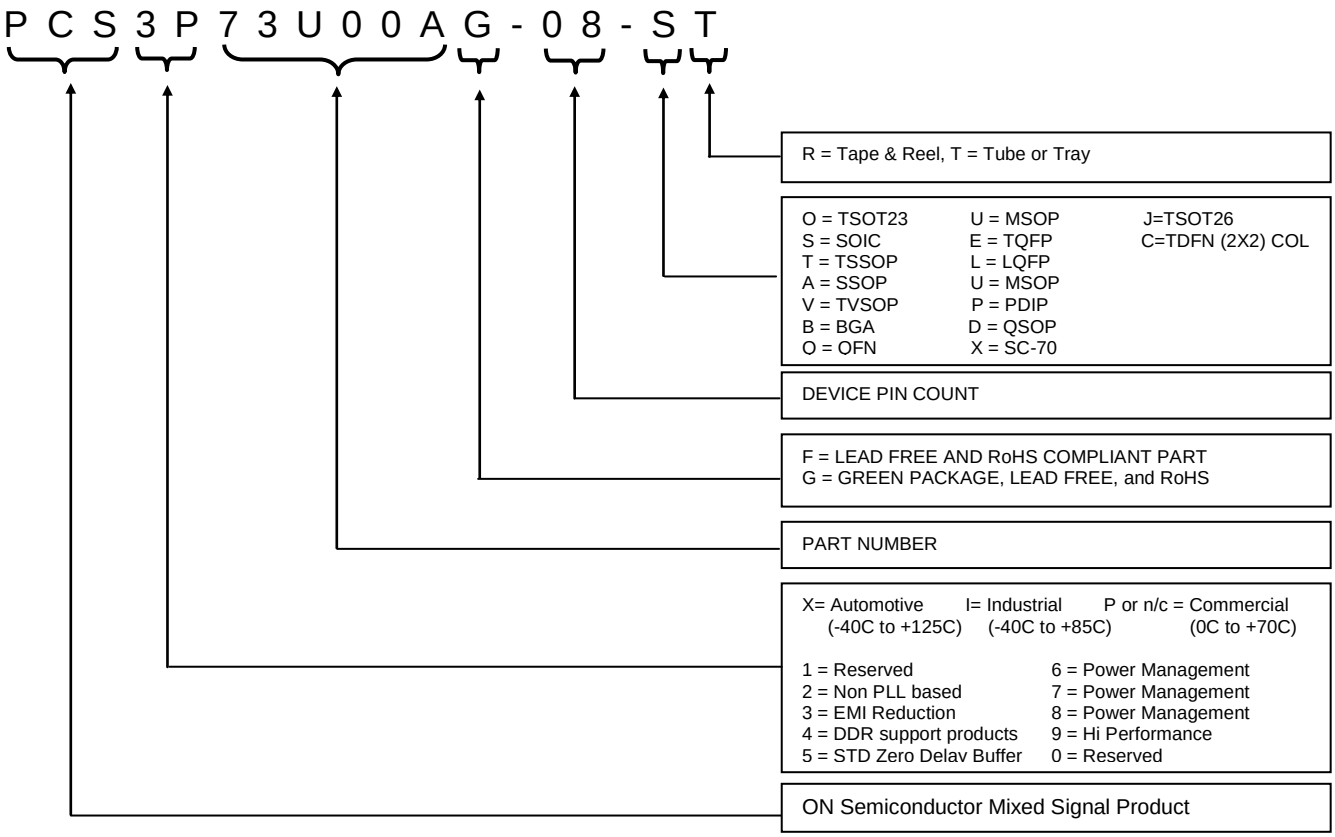
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.027	0.0315	0.70	0.80
A3	0.008 BSC		0.203 BSC	
b	0.008	0.012	0.20	0.30
D	0.079 BSC		2.00 BSC	
E	0.078 BSC		2.00 BSC	
e	0.020 BSC		0.50 BSC	
L	0.020	0.024	0.50	0.60
e	**0.020 BSC**		0.50 BSC	
L	**0.020**	**0.024**	**0.50**	0.60

Ordering Code

Part Number	Marking	Package	Temperature
P3P73U00AG-08SR	3P73U00AG	8-Pin SOIC, Tape & Reel, Green	Commercial
P3P73U00AG-08-ST	3P73U00AG	8-Pin SOIC, Tube, Green	Commercial
PCS3P73U00AG08TR	3P73U00AG	8-Pin TSSOP, Tape & Reel, Green	Commercial
P3P73U00AG-08-TT	3P73U00AG	8-Pin TSSOP, Tube, Green	Commercial
P3P73U00AG-08CR	AG1LL	8-Pin 2-mm TDFN, COL-Tape & Reel, Green	Commercial

LL = 2 Character LOT #

Device Ordering Information



Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

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