LNK623-626
LinkSwitch-CV Family

Energy-Efficient, Off-line Switcher with Accurate Primary-side Constant-Voltage (CV) Control

Product Highlights

Dramatically Simplifies CV Converters
- Eliminates optocoupler and all secondary CV control circuitry
- Eliminates bias winding supply – IC is self biasing

Advanced Performance Features
- Compensates for external component temperature variations
- Very tight IC parameter tolerances using proprietary trimming technology
- Continuous and/or discontinuous mode operation for design flexibility
- Frequency jittering greatly reduces EMI filter cost
- Even tighter output tolerances achievable with external resistor selection/trimming

Advanced Protection/Safety Features
- Auto-restart protection reduces delivered power by >95% for output short-circuit and all control loop faults (open and shorted components)
- Hysteretic thermal shutdown – automatic recovery reduces power supply returns from the field
- Meets HV creepage requirements between Drain and all other pins, both on the PCB and at the package

EcoSmart™– Energy Efficient
- No-load consumption <200 mW at 230 VAC and down to below 70 mW with optional external bias
- Easily meets all global energy efficiency regulations with no added components
- ON/OFF control provides constant efficiency down to very light loads – ideal for mandatory EISA and ENERGY STAR 2.0 regulations
- No primary or secondary current sense resistors – maximizes efficiency

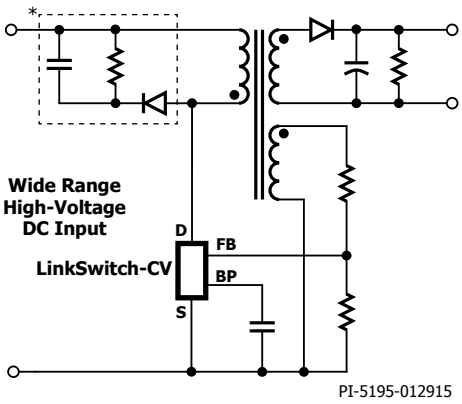
Green Package
- Halogen free and RoHS compliant package

Applications
- DVD/STB
- Adapters
- Standby and auxiliary supplies
- Home appliances, white goods and consumer electronics
- Industrial controls

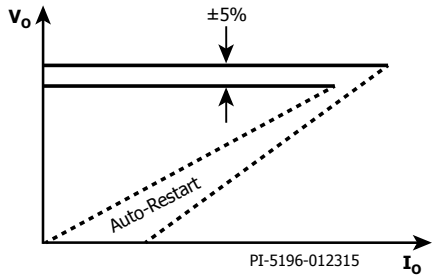
Description

The LinkSwitch™-CV dramatically simplifies low power, constant voltage (CV) converter design through a revolutionary control technique which eliminates the need for both an optocoupler and secondary CV control circuitry while providing very tight output voltage regulation. The combination of proprietary IC trimming and E-Shield™ transformer construction techniques enables Clampless™ designs with the LinkSwitch-CV LNK623/4.

LinkSwitch-CV provides excellent cross-regulation for multiple-output flyback applications such as DVDs and STBs. A 725 V power MOSFET and ON/OFF control state machine, self-biasing, frequency jittering, cycle-by-cycle current limit, and hysteretic thermal shutdown circuitry are all incorporated onto one IC.



(a) Typical Application Schematic



(b) Output Characteristic

Figure 1. Typical Application Schematic (a) and Output Characteristic Envelope (b). *Optional with LNK623-624PG/DG. (see Key Application Considerations section for clamp and other external circuit design considerations).

Output Power Table

Product[3]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Peak or Open Frame[2]	Adapter[1]	Peak or Open Frame[2]
LNK623PG/DG	6.5 W	9 W	5.0 W	6 W
LNK624PG/DG	7 W	11 W	5.5 W	6.5 W
LNK625PG/DG	8 W	13.5 W	6.5 W	8 W
LNK626PG/DG	10.5 W	17 W	8.5 W	10 W

Table 1. Output Power Table. Based on 5 V Output.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient (see Key Application Considerations section for more information).
3. Packages: P: PDIP-8C, D: SO-8C.

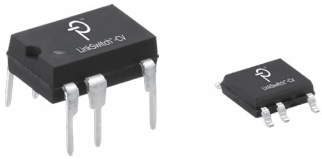


Figure 2. PDIP-8C and SO-8C Packages.

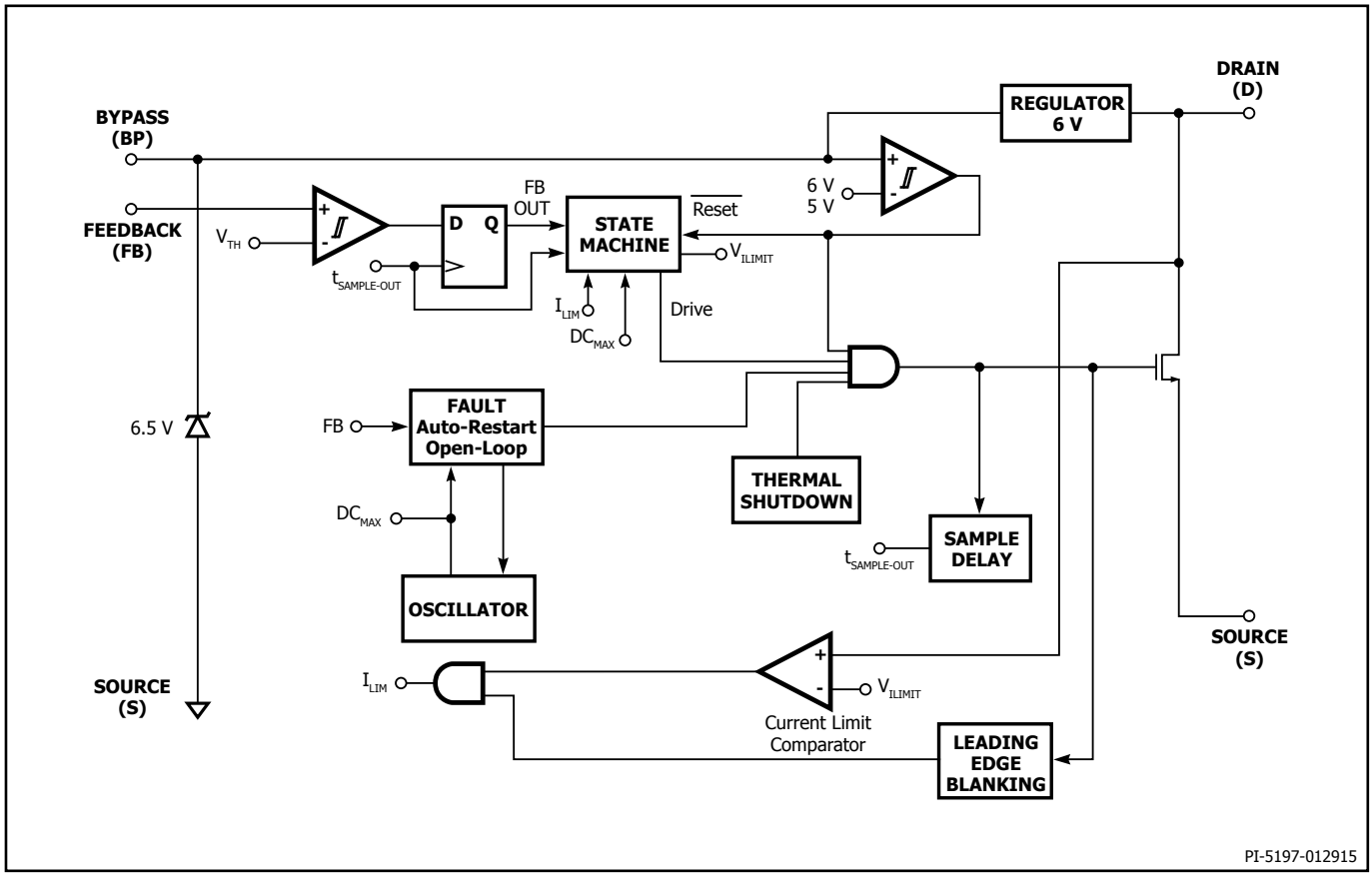


Figure 3 Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
This pin is the power MOSFET drain connection. It provides internal operating current for both start-up and steady-state operation.

BYPASS (BP) Pin:
This pin is the connection point for an external bypass capacitor for the internally generated 6 V supply.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. This pin senses the AC voltage on the bias winding. This control input regulates the output voltage based on the flyback voltage of the bias winding.

SOURCE (S) Pin:
This pin is internally connected to the output MOSFET source for high-voltage power and control circuit common returns.

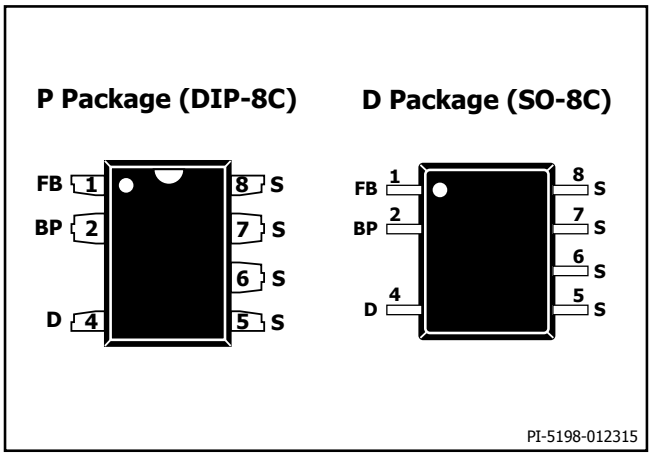


Figure 4. Pin Configuration.

LinkSwitch-CV Functional Description

The LinkSwitch-CV combines a high-voltage power MOSFET switch with a power supply controller in one device. Similar to the LinkSwitch-LP and TinySwitch-III it uses ON/OFF control to regulate the output voltage. The LinkSwitch-CV controller consists of an oscillator, feedback (sense and logic) circuit, 6 V regulator, over-temperature protection, frequency jittering, current limit circuit, leading-edge blanking, and ON/OFF state machine for CV control.

Constant Voltage (CV) Operation

The controller regulates the FEEDBACK pin voltage to remain at V_{FBth} using an ON/OFF state-machine. The FEEDBACK pin voltage is sampled 2.5 μs after the turn-off of the high-voltage switch. At light loads the current limit is also reduced to decrease the transformer flux density.

Auto-Restart and Open-Loop Protection

In the event of a fault condition such as an output short or an open loop condition the LinkSwitch-CV enters into an appropriate protection mode as described below.

In the event the FEEDBACK pin voltage during the Flyback period falls below V_{FBth}-0.3 V before the FEEDBACK pin sampling delay (~2.5 μs) for a duration in excess of 200 ms (auto-restart on-time (t_{AR-ON}) the converter enters into auto-restart. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

In addition to the conditions for auto-restart described above, if the sensed FEEDBACK pin current during the Forward period of the conduction cycle (switch "on" time) falls below 120 μA, the converter annunciates this as an open-loop condition (top resistor in potential divider is open or missing) and reduces the auto-restart time from 200 ms to approximately 6 clock cycles (90 μs), whilst keeping the disable period of 2.5 seconds. This effectively reduces the auto-restart duty cycle to less than 0.01%.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 60 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 60 °C, at which point the MOSFET is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

6.0 V Regulator

The 6 V regulator charges the bypass capacitor connected to the BYPASS pin to 6 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the device runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-CV to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 1 μF is sufficient for both high frequency decoupling and energy storage.

Applications Example

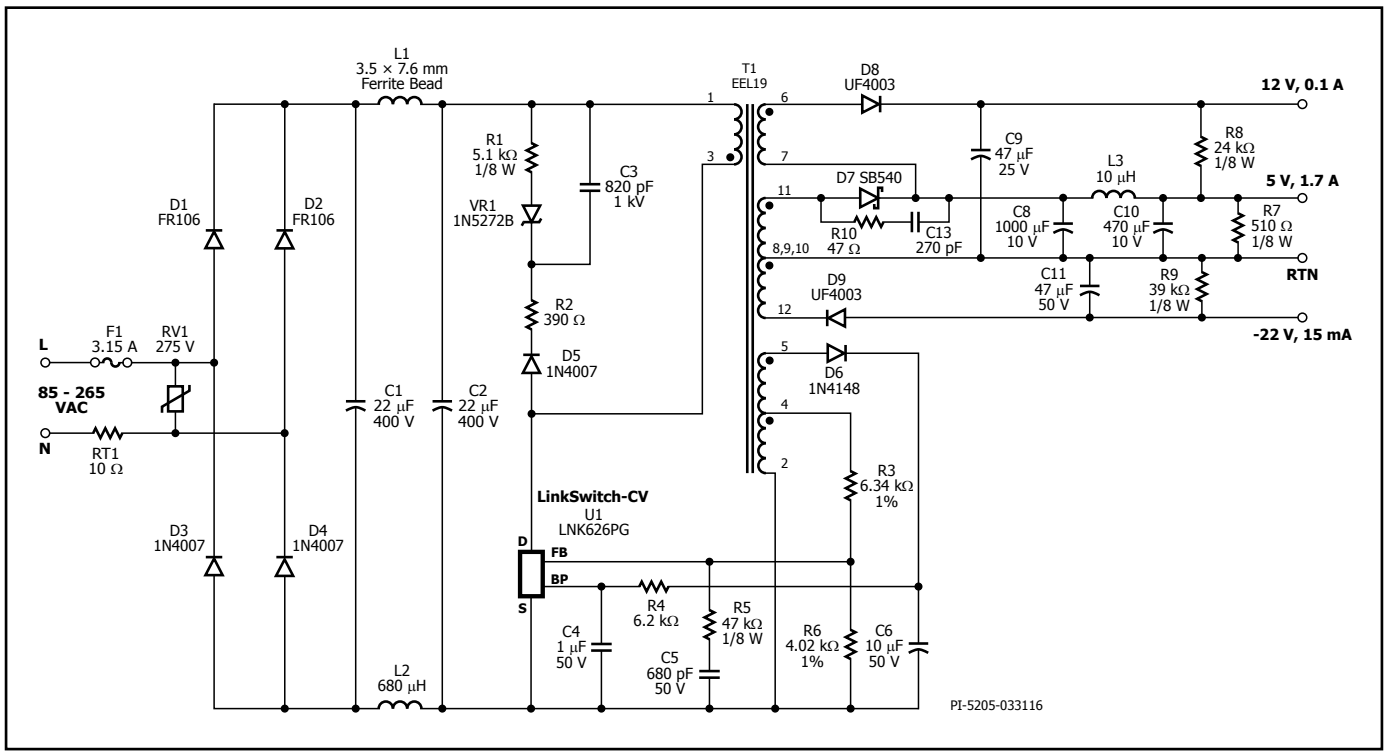


Figure 5. 7 W (10 W peak) Multiple Output Flyback Converter for DVD Applications with Primary Sensed Feedback.

Circuit Description

This circuit is configured as a three output, primary-side regulated flyback power supply utilizing the LNK626PG. It can deliver 7 W continuously and 10 W peak (thermally limited) from an universal input voltage range (85 – 265 VAC). Efficiency is >67% at 115 VAC /230 VAC and no-load input power is <140 mW at 230 VAC.

Input Filter

AC input power is rectified by diodes D1 through D4. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Inductor L1, L2, C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI noise. This configuration along with Power Integrations transformer E-shield technology allow this design to meet EMI standard EN55022 class B with good margin without requiring a Y capacitor. Fuse F1 provides protection against catastrophic failure. Negative temperature coefficient thermistor RT1 limits the inrush current when AC is first applied to below the maximum rating of diodes D1 through D4. Metal oxide varistor RV1 clamps the AC input during differential line transients, protecting the input components and maintaining the peak drain voltage of U1 below its 725 V BV_{DSS} rating. For differential surge levels at or below 2 kV this component may be omitted.

LNK626 Primary

The LNK626PG device (U1) incorporates the power switching device, oscillator, CV control engine, startup, and protection functions. The integrated 725 V MOSFET provides a large drain voltage margin in universal input AC applications, increasing reliability and also reducing the output diode voltage stress by allowing a greater transformer turns ratio. The device can be completely self-powered from the BYPASS pin and decoupling capacitor C4. In this design a bias circuit (D6, C6 and R4) was added to reduce no load input power below 140 mW.

The rectified and filtered input voltage is applied to one side of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated MOSFET in U1. The leakage inductance drain voltage spike is limited by the clamp circuit D5, R1, R2, C3 and VR1. The Zener bleed clamp arrangement was selected for lowest no-load input power but in applications where higher no-load input power is acceptable VR1 may be omitted and the value of R1 increased to form a standard RCD clamp.

Output Rectification

The secondaries of the transformer are rectified by D7, D8 and D9. A Schottky barrier type was used for the main 5 V output for higher efficiency. The +12 V and -22 V outputs use an ultrafast rectifier diode. The main output is post filtered by L3 and C10 to remove switching frequency ripple. Resistors R7, R8 and R9 provide a preload to maintain the output voltages within their respective limits when unloaded. To reduce high frequency ringing and associated radiated EMI an RC snubber formed by R10 and C13 was added across D7.

Output Regulation

The LNK626 regulates the output using ON/OFF control, enabling or disabling switching cycles based on the sampled voltage on the FEEDBACK pin. The output voltage is sensed using a primary referenced winding on transformer T1 eliminating the need for an optocoupler and a secondary sense circuit. The resistor divider formed by R3 and R6 feeds the winding voltage into U1. Standard 1% resistor values were used to center the nominal output voltages. Resistor R5 and C5 reduce pulse grouping by creating an offset voltage that is proportional to the number of consecutive enabled switching cycles.

Key Application Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained in a flyback converter under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher at 90 VAC input. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Secondary output of 5 V with a Schottky rectifier diode.
3. Assumed efficiency of 80%.
4. Continuous conduction mode operation (K_p = 0.4).
5. Reflected Output Voltage (V_{OR}) of 110 V.
6. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 110 °C for P package and 100 °C for D packaged devices.
7. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

Note: Higher output power are achievable if the efficiency is higher than 80%, typically for high output voltage designs.

BYPASS Pin Capacitor

A 1 μF BYPASS pin capacitor (C4) is recommended. The capacitor voltage rating should be equal to or greater than 6.8 V. The capacitor's dielectric material is not important. The capacitor must be physically located close to the LinkSwitch-CV BYPASS pin.

Circuit board layout

LinkSwitch-CV is a highly integrated power supply solution that integrates on a single die, both the controller and the high-voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply.

When designing a board for the LinkSwitch-CV based power supply, it is important to follow the following guidelines:

Single Point Grounding

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-CV SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.

Bypass Capacitor

The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.

Feedback Resistors

Place the feedback resistors directly at the FEEDBACK pin of the LinkSwitch-CV device. This minimizes noise coupling.

Thermal Considerations

The copper area connected to the SOURCE pins provide the LinkSwitch-CV heat sink. A rule of thumb estimate is that the LinkSwitch-CV will dissipate 10% of the output power. Provide enough copper area to keep the SOURCE pin temperature below 110° C to provide margin for part to part $R_{DS(ON)}$ variation.

Secondary Loop Area

To minimize leakage inductance and EMI, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Electrostatic Discharge Spark Gap

In chargers and adapters ESD discharges may be applied to the output of the supply. In these applications the addition of a spark gap is recommended. A trace is placed along the isolation barrier to form one electrode of a spark gap. The other electrode, on the secondary-side, is formed by the output return node. The arrangement directs ESD energy from the secondary to the primary side AC input. A 10 mil gap is placed near the AC input. The gap decouples any noise picked up on the spark gap trace to the AC input. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent unwanted arcing occurring and possible circuit damage.

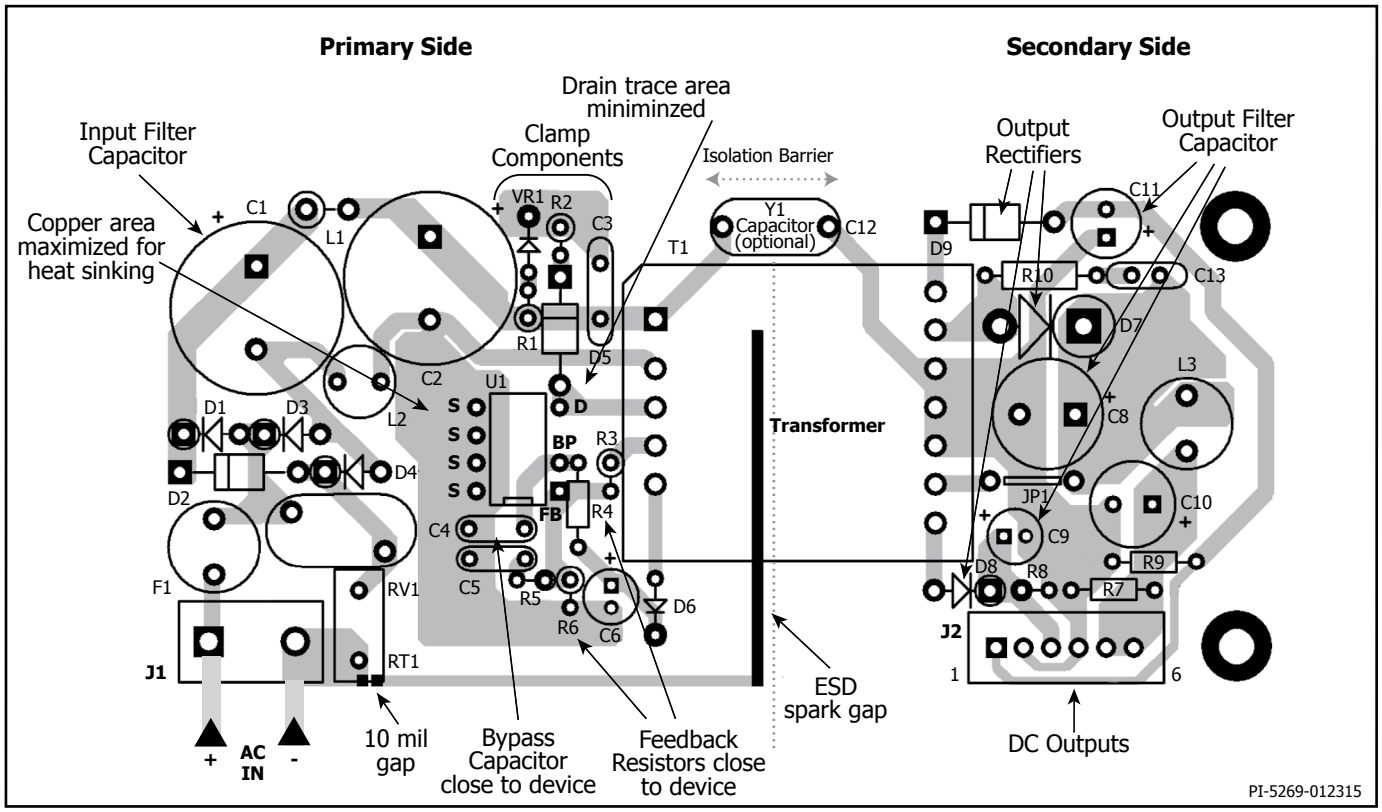


Figure 6. PCB Layout Example.

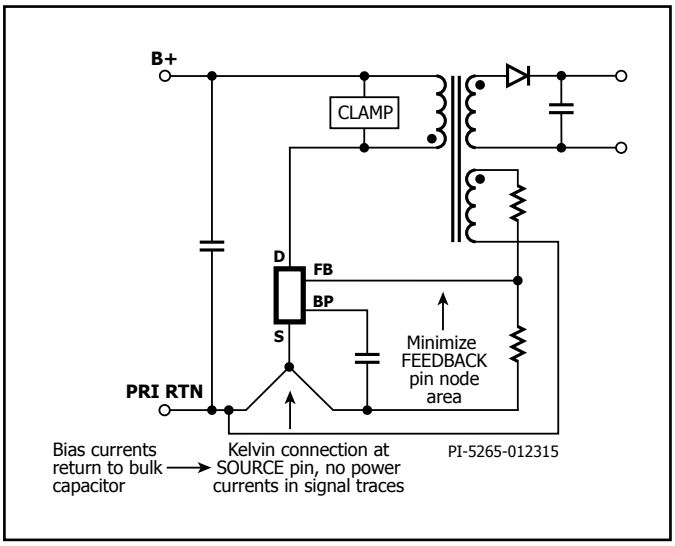


Figure 7. Schematic Representation of Recommended Layout without External Bias.

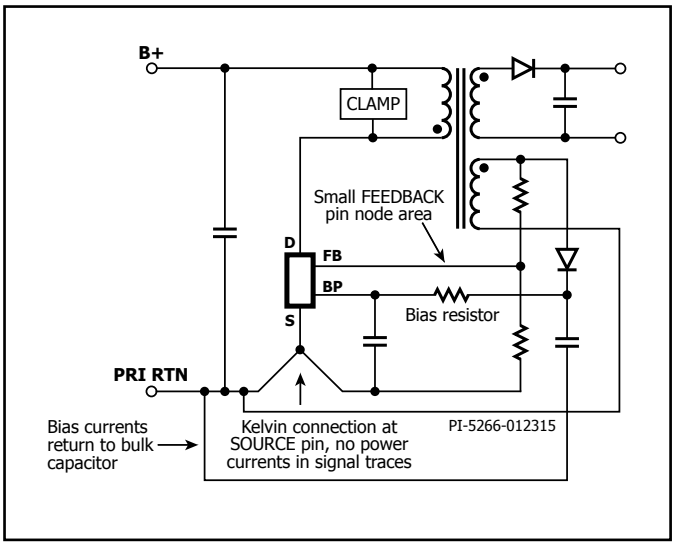


Figure 8. Schematic Representation of Recommended Layout with External Bias.

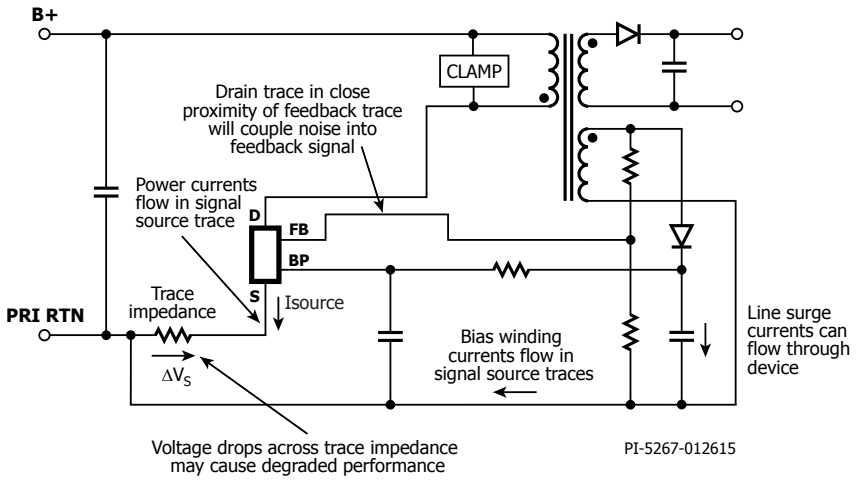
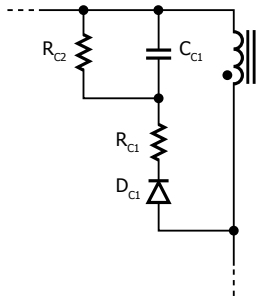


Figure 9. Schematic Representation of Electrical Impact of Improper Layout.

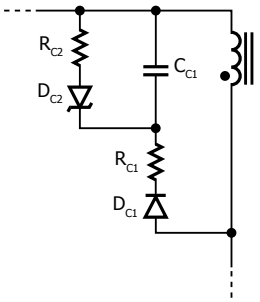
Drain Clamp

Recommended Clamp Circuits



PI-5107-012615

Figure 10. RCD Clamp, Low Power or Low Leakage Inductance Designs.



PI-5108-110308

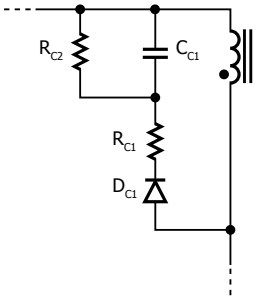
RCD Clamp With Zener Bleed. High Power or High Leakage Inductance Designs.

Components R1, R2, C3, VR1 and D5 in Figure 5 comprise the clamp. This circuit is preferred when the primary leakage inductance is greater than 125 µH to reduce drain voltage overshoot or ringing present on the feedback winding. For best output regulation, the feedback voltage must settle to within 1% at 2.1 µs from the turn off of the primary MOSFET. This requires careful selection of the clamp circuit components. The voltage of VR1 is selected to be ~20% above the reflected output voltage (V_{OR}). This is to clip any turn off spike on the drain but avoid conduction during the flyback voltage interval when the output diode is conducting. The value of R1 should be the largest value that results in acceptable settling of the FEEDBACK pin voltage and peak drain voltage. Making R1 too large will increase the discharge time of C3 and degrade regulation. Resistor R2 dampens the leakage inductance ring. The value must be large enough to dampen the ring in the required time but must not be too large to cause the drain voltage to exceed 680 V.

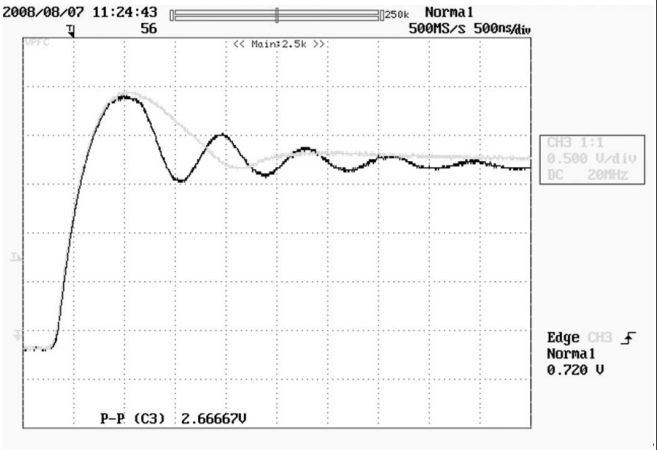
If the primary leakage inductance is less than 125 µH, VR1 can be eliminated and the value of R1 increased. A value of 470 kΩ with an 820 pF capacitor is a recommended starting point. Verify that the peak drain voltage is less than 680 V under all line and load conditions. Verify the feedback winding settles to an acceptable limit for good line and load regulation.

Effect of Fast (500 ns) versus Slow (2 µs) Recovery Diodes in Clamp Circuit on Pulse Grouping and Output Ripple.

A slow reverse recovery diode reduces the feedback voltage ringing. The amplitude of ringing with a fast diode represents 8% error in Figure 11.



PI-5107-012615



Black Trace: D_{C1} is a FR107 (fast type, t_{RR} = 500 ns)
Gray Trace: D_{C1} is a 1N4007G (standard recovery, t_{RR} = 2 µs)

Figure 11. Effect of Clamp Diode on FEEDBACK Pin Settling. Clamp Circuit (top). FEEDBACK Pin Voltage (bottom).

Clampless Designs

Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore the maximum AC input line voltage, the value of V_{OR}, the leakage inductance energy, (a function of leakage inductance and peak primary current), and the primary winding capacitance determine the peak drain voltage. With no significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only Clampless design:

1. Clampless designs should only be used for P_O ≤5 W using a V_{OR} of ≤90 V
2. For designs with P_O ≤5 W, a two-layer primary must be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF. A bias winding must be added to the transformer using a standard recovery rectifier diode (1N4003–1N4007) to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
3. For designs with P_O >5 W, Clampless designs are not practical and an external RCD or Zener clamp should be used.
4. Ensure that worst-case, high line, peak drain voltage is below the BV_{DSS} specification of the internal MOSFET and ideally ≤650 V to allow margin for design variation.

V_{OR} (Reflected Output Voltage), is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The V_{OR} adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.

Pulse Grouping

Pulse grouping is defined as 6 or more consecutive pulses followed by two or more timing state changes. The effect of pulse grouping is increased output voltage ripple. This is shown on the right of Figure 12 where pulse grouping has caused an increase in the output ripple.

To eliminate group pulsing verify that the feedback signal settles within 2.1 µs from the turn off of the internal MOSFET. A Zener diode in the clamp circuit may be needed to achieve the desired settling time. If the settling time is satisfactory, then a RC network across R_{LOWER} (R6) of the feedback resistors is necessary.

The value of R (R5 in the Figure 13) should be an order of magnitude greater than R_{LOWER} and selected such that R×C = 32 µs where C is C5 in Figure 13.

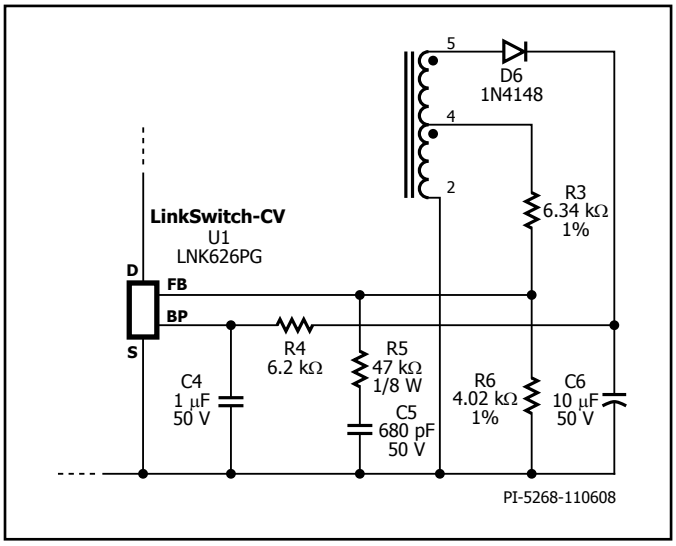
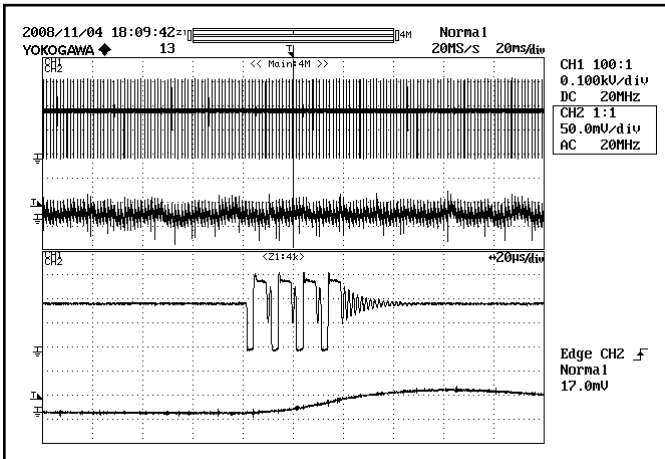
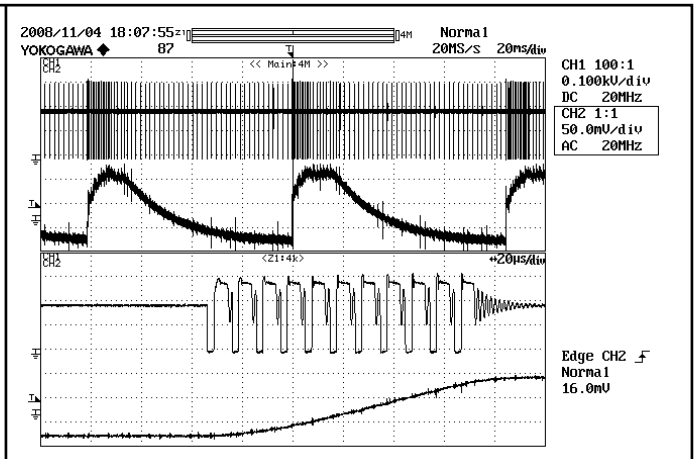


Figure 13. RC Network Across R_{BOTTOM} (R6) to Reduce Pulse Grouping.



Top Trace: Drain Waveform (200 V/div)
Bottom Trace: Output Ripple Voltage (50 mV/div)

Figure 12. Not Pulse Grouping (<5 Consecutive Switching Cycles).



Split Screen with Bottom Screen Zoom
Top Trace: Drain Waveform (200 V/div)
Bottom Trace: Output Ripple Voltage (50 mV/div)

Pulse Grouping (>5 Consecutive Switching Cycles).

Quick Design Checklist

As with any power supply design, all LinkSwitch-CV designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 680 V at highest input voltage and maximum output power.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch-CV has a leading edge blanking time of 215 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope for the drain current waveform at the end of the 215 ns blanking period.
3. Thermal check – At maximum output power, both minimum and maximum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for LinkSwitch-CV, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-CV, as specified in the data sheet. It is recommended that the maximum SOURCE pin temperature does not exceed 110 °C.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

Absolute Maximum Ratings[1,5]

DRAIN Voltage .....-0.3 V to 725 V
DRAIN Peak Current: LNK623 .....400 (600) mA[4]
LNK624 .....400 (600) mA[4]
LNK625 .....528 (790) mA[4]
LNK626 ..... 720 (1080) mA[4]
Peak Negative Pulsed DRAIN Current .....-100 mA[2]
Feedback Pin Voltage ..... -0.3 V to 9 V
Feedback Pin Current .....100 mA
BYPASS Pin Voltage ..... -0.3 V to 9 V
BYPASS Pin Current .....10 mA
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature.....-40 °C to 150 °C
Lead Temperature(3) ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Duration not to exceed 2 msec.
3. 1/16 in. from case for 5 seconds.
4. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
5. Maximum ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum ratings for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: P Package:
(θ_{JA}) ..... 70 °C/W[2]; 60 °C/W[3]
(θ_{JC})[1] ..... 11 °C/W
D Package:
(θ_{JA}) .....100 °C/W[2]; 80 °C/W[3]
(θ_{JC})[1] ..... 30 °C/W

Notes:
1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency	f_{OSC}	T_J = 25 °C, V_{FB} = V_{FBth}	LNK623/6	93	100	106	kHz
Frequency Jitter		Peak-Peak Jitter Compared to Average Frequency, T_J = 25 °C			±7		%
Ratio of Output Frequency at Auto-Restart	$f_{OSC(AR)}$	T_J = 25 °C Relative to f_{OSC}, See Note C			80		%
Maximum Duty Cycle	DC_{MAX}	T_J = 25 °C See Notes B, C		54			%
FEEDBACK Pin Voltage	V_{FBth}	T_J = 25 °C See Figure 15 C_{BP} = 1 µF See Note D	LNK623-624P	1.815	1.840	1.865	V
			LNK623-624D	1.855	1.880	1.905	
			LNK625P, LNK625D	1.835	1.860	1.885	
			LNK626P, LNK626D	1.775	1.800	1.825	
FEEDBACK Pin Voltage Temperature Coefficient	TC_{VFB}				-0.01		%/°C
FEEDBACK Pin Voltage at Turn-Off Threshold	$V_{FB(AR)}$				1.45		V
Power Coefficient	I^2f	$I^2f = I^2_{LIMIT(TYP)} \times f_{OSC(TYP)}$	LNK623/6P T_J = 25 °C	0.9 × I^2f	I^2f	1.17 × I^2f	A^2Hz
		$I^2f = I^2_{LIMIT(TYP)} \times f_{OSC(TYP)}$	LNK623/6D T_J = 25 °C	0.9 × I^2f	I^2f	1.21 × I^2f	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
Minimum Switch "On"-Time	$t_{ON(min)}$	See Note C			700		ns
FEEDBACK Pin Sampling Delay	t_{FB}			2.35	2.55	2.75	µs
DRAIN Supply Current	I_{S1}	FB Voltage > V_{FBth}			280	340	µA
	I_{S2}	FB Voltage = V_{FBth} -0.1, Switch ON-Time = t_{ON} (MOSFET Switching at f_{OSC})	LNK623/4		440	520	
			LNK625		480	560	
			LNK626		520	600	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V	LNK623/4	-5.8	-3.4	-1.8	mA
			LNK625/6	-8.2	-4.5	-2.0	
	I_{CH2}	V_{BP} = 4 V	LNK623/4	-4.0	-2.3	-1.0	
			LNK625/6	-5.6	-3.2	-1.4	
BYPASS Pin Voltage	V_{BP}			5.65	6.00	6.25	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.70	1.00	1.20	V
BYPASS Pin Shunt Voltage	V_{SHUNT}			6.2	6.5	6.8	V
Circuit Protection							
Current Limit	I_{LIMIT}	LNK623 di/dt = 50 mA/µs , T_J = 25 °C		196	210	225	mA
		LNK624 di/dt = 60 mA/µs , T_J = 25 °C		233	250	268	
		LNK625 di/dt = 80 mA/µs , T_J = 25 °C		307	330	353	
		LNK626 di/dt = 110 mA/µs , T_J = 25 °C		419	450	482	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note C		170	215		ns
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}				60		°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK623 I_D = 50 mA	T_J = 25 °C		24	28	Ω
			T_J = 100 °C		36	42	
		LNK624 I_D = 50 mA	T_J = 25 °C		24	28	
			T_J = 100 °C		36	42	
		LNK625 I_D = 62 mA	T_J = 25 °C		16	19	
			T_J = 100 °C		24	28	
		LNK626 I_D = 82 mA	T_J = 25 °C		9.6	11	
			T_J = 100 °C		14	17	
OFF-State Leakage	I_{DSS1}	V_{DS} = 560 V, See Figure 20 T_J = 125 °C, See Note A				50	µA
	I_{DSS2}	V_{DS} = 375 V, See Figure 20 T_J = 50 °C			15		
Breakdown Voltage	BV_{DSS}	T_J = 25 °C See Figure 20		725			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time	t_{AR-ON}	V_{FB} = 0 See Note C			200		ms
Auto-Restart OFF-Time	t_{AR-OFF}				1		s
Open-Loop FEEDBACK Pin Current Threshold	I_{OL}	See Note C			-120		µA
Open-Loop ON-Time		See Note C			90		µs

NOTES:

A. I_{DSS1} is the worst-case OFF-state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 265 VAC) for no-load consumption calculations.

B. When the duty cycle exceeds DC_{MAX} the LinkSwitch-CV operates in on-time extension mode.

C. This parameter is derived from characterization.

D. Mechanical stress induced during the assembly may cause shift in this parameter. This shift has not impact on the ability of LinkSwitch-CV to meet CV = ±5% in mass production given the design follows recommendation in AN-45 and good manufacturing practice.

Typical Performance Characteristics

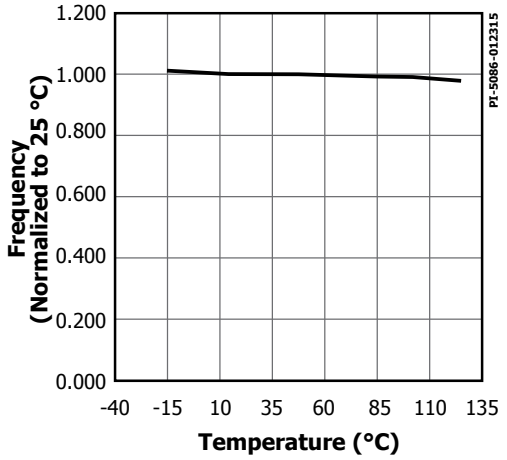


Figure 14. Output Frequency vs. Temperature.

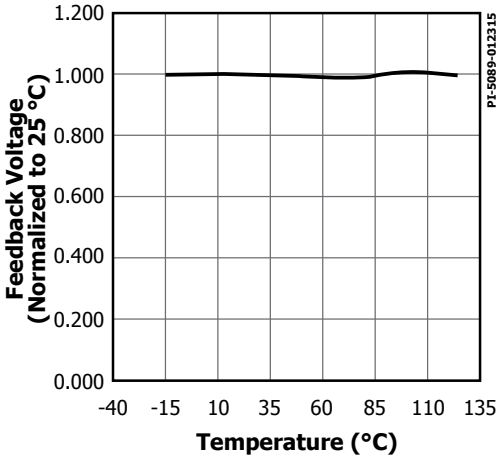


Figure 15. Feedback Voltage vs. Temperature.

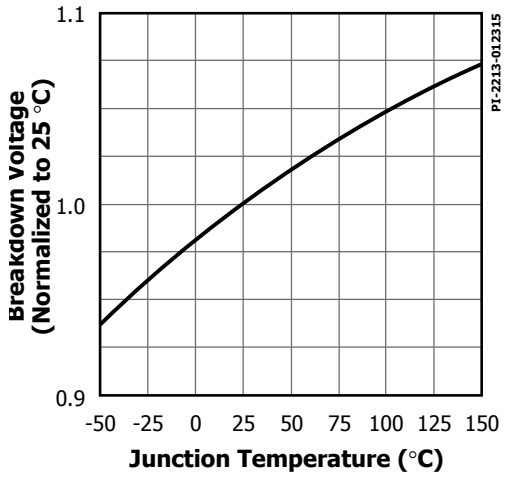


Figure 16. Breakdown vs. Temperature.

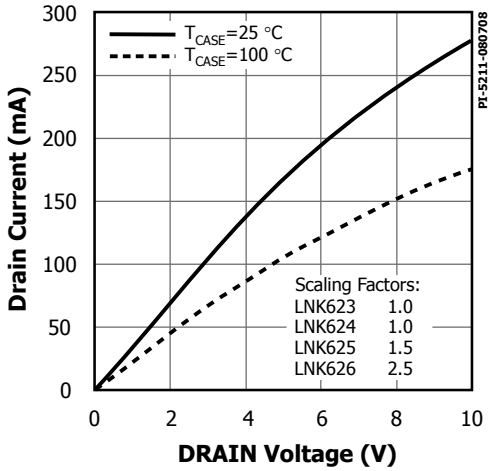


Figure 17. Output Characteristic.

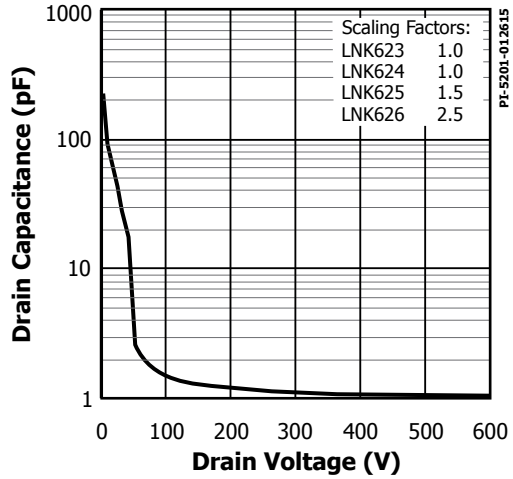


Figure 18. C_{OSS} vs. Drain Voltage.

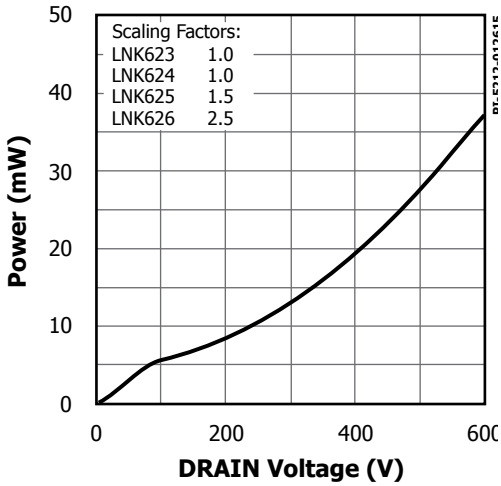
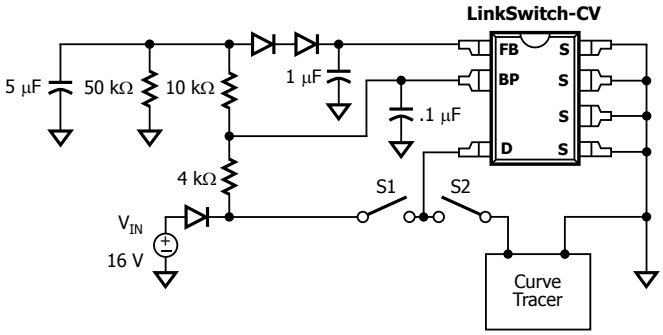


Figure 19. Drain Capacitance Power.

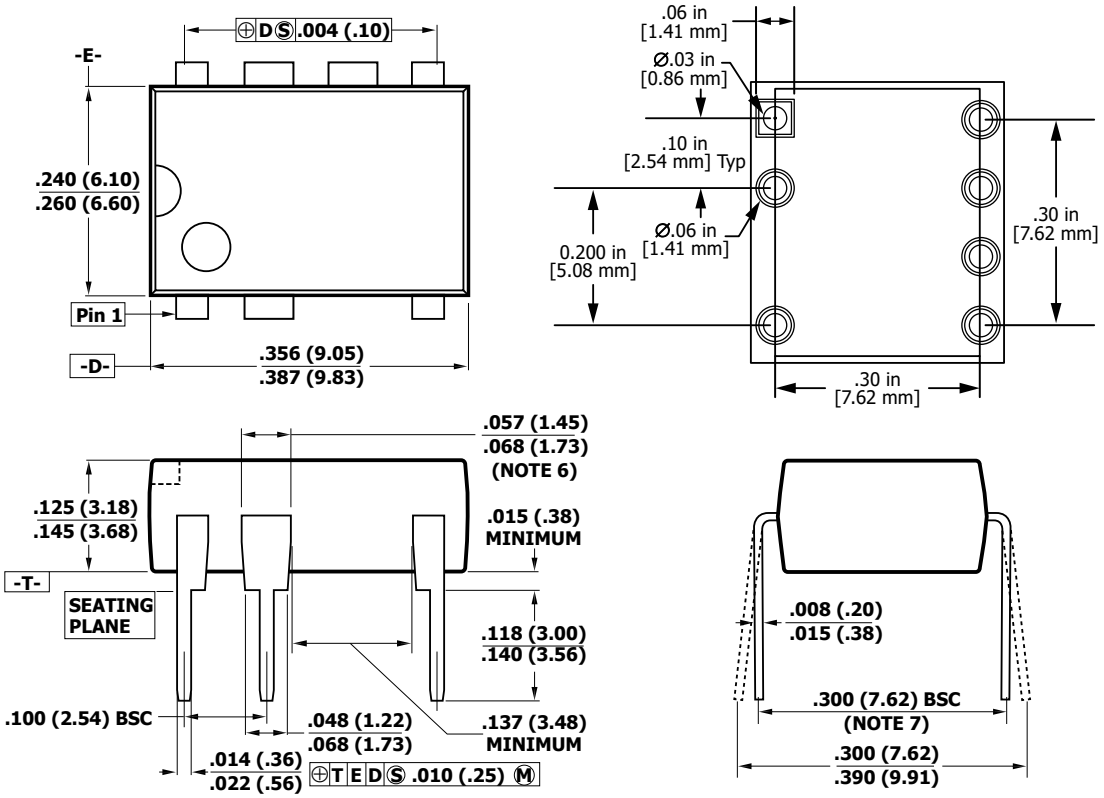


To measure BV_{DSS}, I_{DSS1}, and I_{DSS2} follow these steps:
1) Close S1, open S2
2) Power-up V_{IN} source (16 V)
3) Open S1, close S2
4) Measure I/V characteristics of DRAIN pin using the curve tracer

PI-5203-012615

Figure 20. Test Set-up for Leakage and Breakdown Tests.

PDIP-8C (P Package)

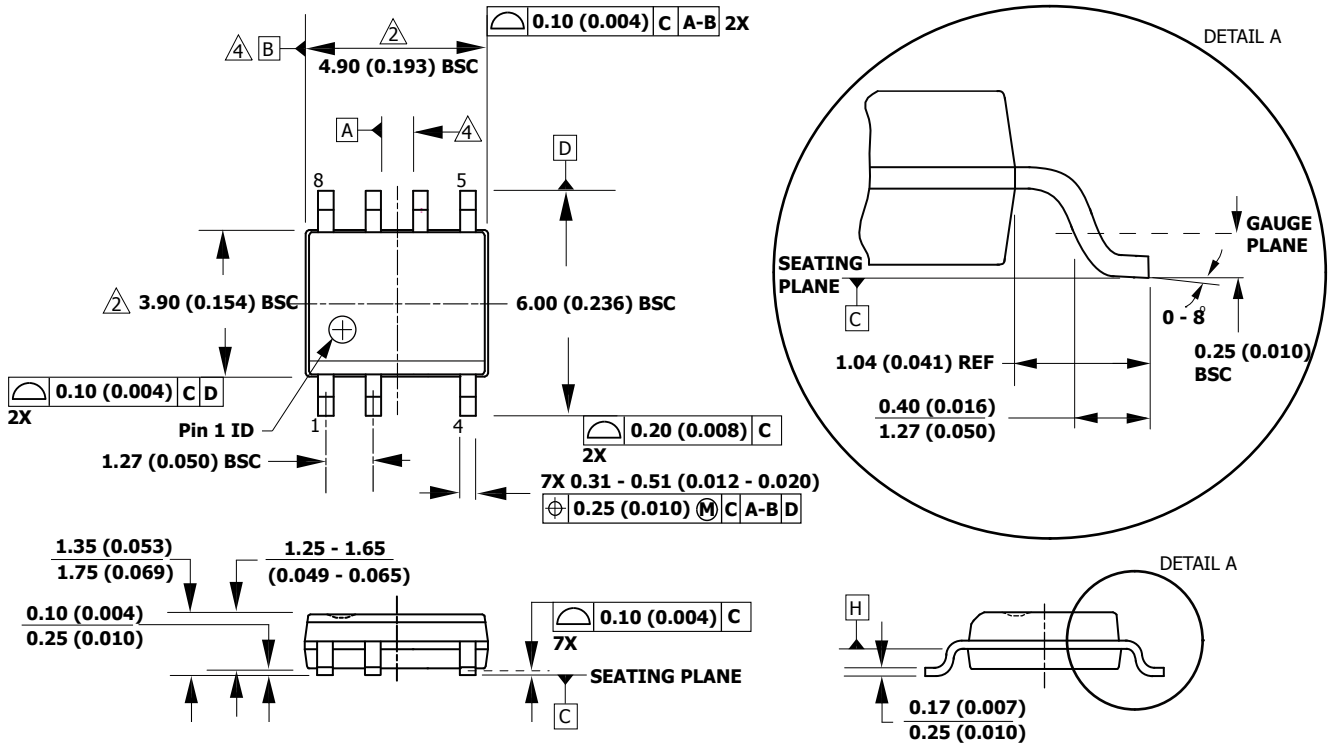


Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

P08C

PI-3933b-092920

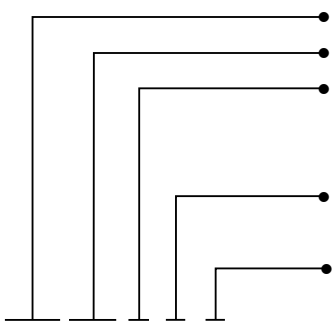
SO-8C (D Package)



Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

Part Ordering Information



- **LinkSwitch Product Family**
- **CV Series Number**
- **Package Identifier**
  - P — Plastic PDIP-8C
  - D — Plastic SO-8C
- **Package Material**
  - G — GREEN: Halogen Free and RoHS Compliant
- **Tape & Reel and Other Options**
  - Blank — Standard Configurations
  - TL — Tape & Reel, 2.5 k pcs for D Package. Not available for P Package.

Revision	Notes	Date
B	Release data sheet.	11/08
C	Correction made to Figure 5.	12/08
D	Introduced Max Current Limit when V DRAIN is below 400 V.	07/09
E	Introduced LNK626DG.	09/09
F	Added Note 4 to Parameter Table	02/10
F	Specified Max BYPASS Pin Current.	03/14
G	Figure removed "Test Set-up for FEEDBACK Pin Measurements" from previous version. Updated t_{AR-OFF} parameter. Updated to latest Brand Style.	02/15
H	Update BV_{DSS} from 700 V to 725 V	08/15
H	Corrected schematic error in Figure 5.	03/16
I	Updated PDIP-8C (P Package) per PCN-16232.	08/16
J	Updated I_{S1}, I_{CH1} and $t_{AR(OFF)}$ values.	06/20
K	Updated PDIP-8C (P Package) drawing.	05/21

Notes

For the latest updates, visit our website: www.power.com
Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at www.power.com/ip.htm.

Life Support Policy
POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com
