

# DATA SHEET

## **PDTA143T series**

PNP resistor-equipped transistors;

R1 = 4.7 k $\Omega$ , R2 = open

Product specification  
Supersedes data of 2003 Sep 08

2004 Aug 04

## PNP resistor-equipped transistors; R1 = 4.7 k $\Omega$ , R2 = open

## PDTA143T series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	–50	V
I <sub>O</sub>	output current (DC)	–	–100	mA
R1	bias resistor	4.7	–	k $\Omega$
R2	open	–	–	–

### DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA143TE	SOT416	SC-75	39	PDTC143TE
PDTA143TEF	SOT490	SC-89	10	PDTC143TEF
PDTA143TK	SOT346	SC-59	45	PDTC143TK
PDTA143TM	SOT883	SC-101	E6	PDTC143TM
PDTA143TS	SOT54 (TO-92)	SC-43	TA143T	PDTC143TS
PDTA143TT	SOT23	–	*42 <sup>(1)</sup>	PDTC143TT
PDTA143TU	SOT323	SC-70	*45 <sup>(1)</sup>	PDTC143TU

### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

PNP resistor-equipped transistors;  
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**SIMPLIFIED OUTLINE, SYMBOL AND PINNING**

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA143TS		1 2 3	base collector emitter
PDTA143TE PDTA143TEF PDTA143TK PDTA143TT PDTA143TU		1 2 3	base emitter collector
PDTA143TM		1 2 3	base emitter collector

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CB0</sub>	collector-base voltage	open emitter	–	–50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	–50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	–5	V
I <sub>O</sub>	output current (DC)		–	–100	mA
I <sub>CM</sub>	peak collector current		–	–100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT23	note 1	–	250	mW
	SOT54	note 1	–	500	mW
	SOT323	note 1	–	200	mW
	SOT346	note 1	–	250	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**Notes**

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	in free air		
	SOT23	note 1	500	K/W
	SOT54	note 1	250	K/W
	SOT323	note 1	625	K/W
	SOT346	note 1	500	K/W
	SOT416	note 1	833	K/W
	SOT490	note 1	500	K/W
	SOT883	notes 2 and 3	500	K/W

**Notes**

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### CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0	-	-	-1	$\mu$ A
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	-	-	-50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0	-	-	-100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -1 mA	200	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -5 mA; I <sub>B</sub> = -0.25 mA	-	-	-150	mV
R1	input resistor		3.3	4.7	6.1	k $\Omega$
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0; V <sub>CB</sub> = -10 V; f = 1 MHz	-	-	3	pF

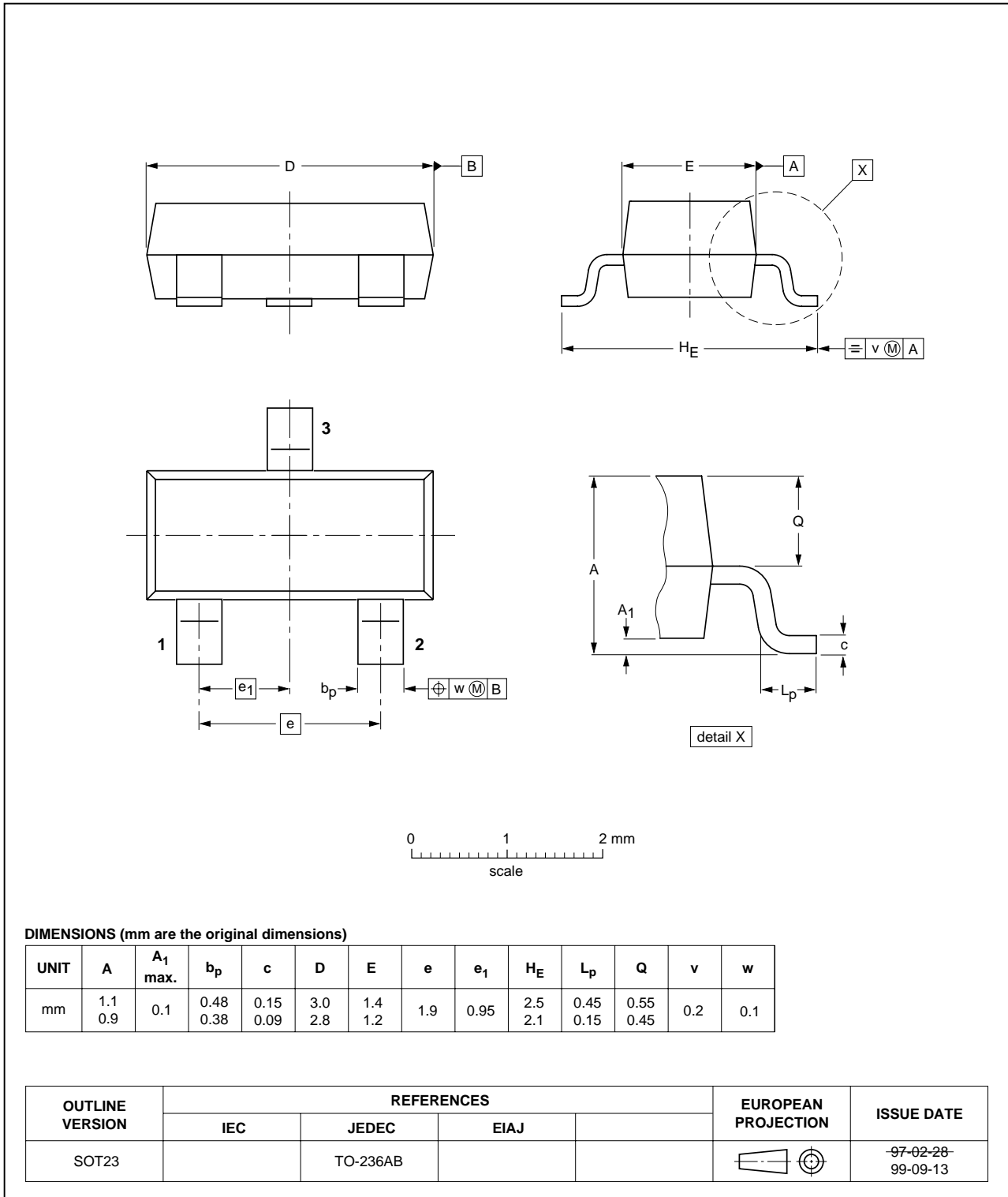
PNP resistor-equipped transistors;  
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PDTA143T series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23

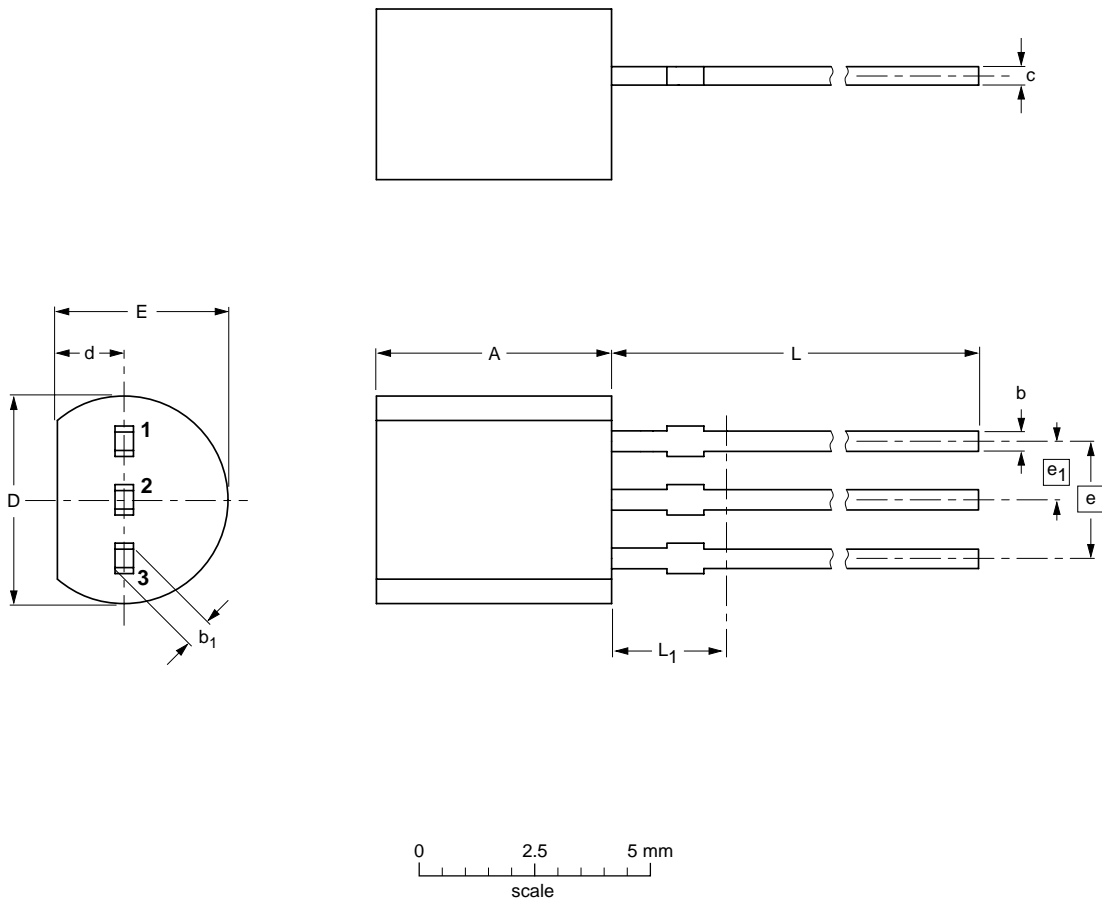


PNP resistor-equipped transistors;  
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PDTA143T series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

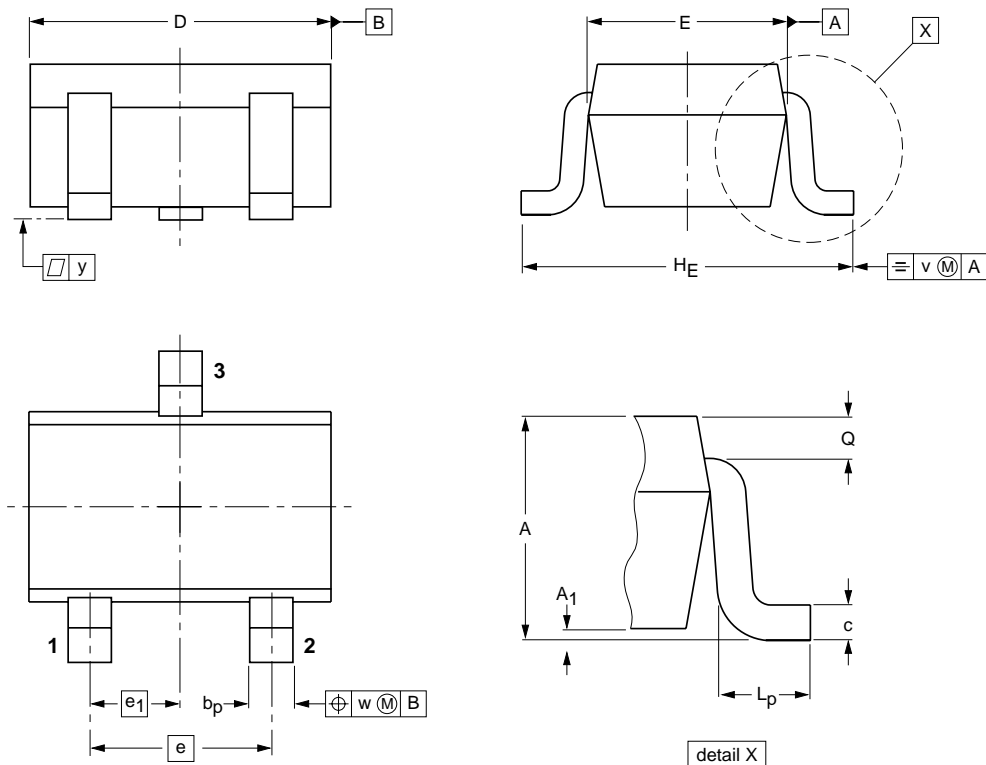
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		<del>97-02-28</del> 04-06-28

PNP resistor-equipped transistors;  
R1 = 4.7 kΩ, R2 = open

PDTA143T series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

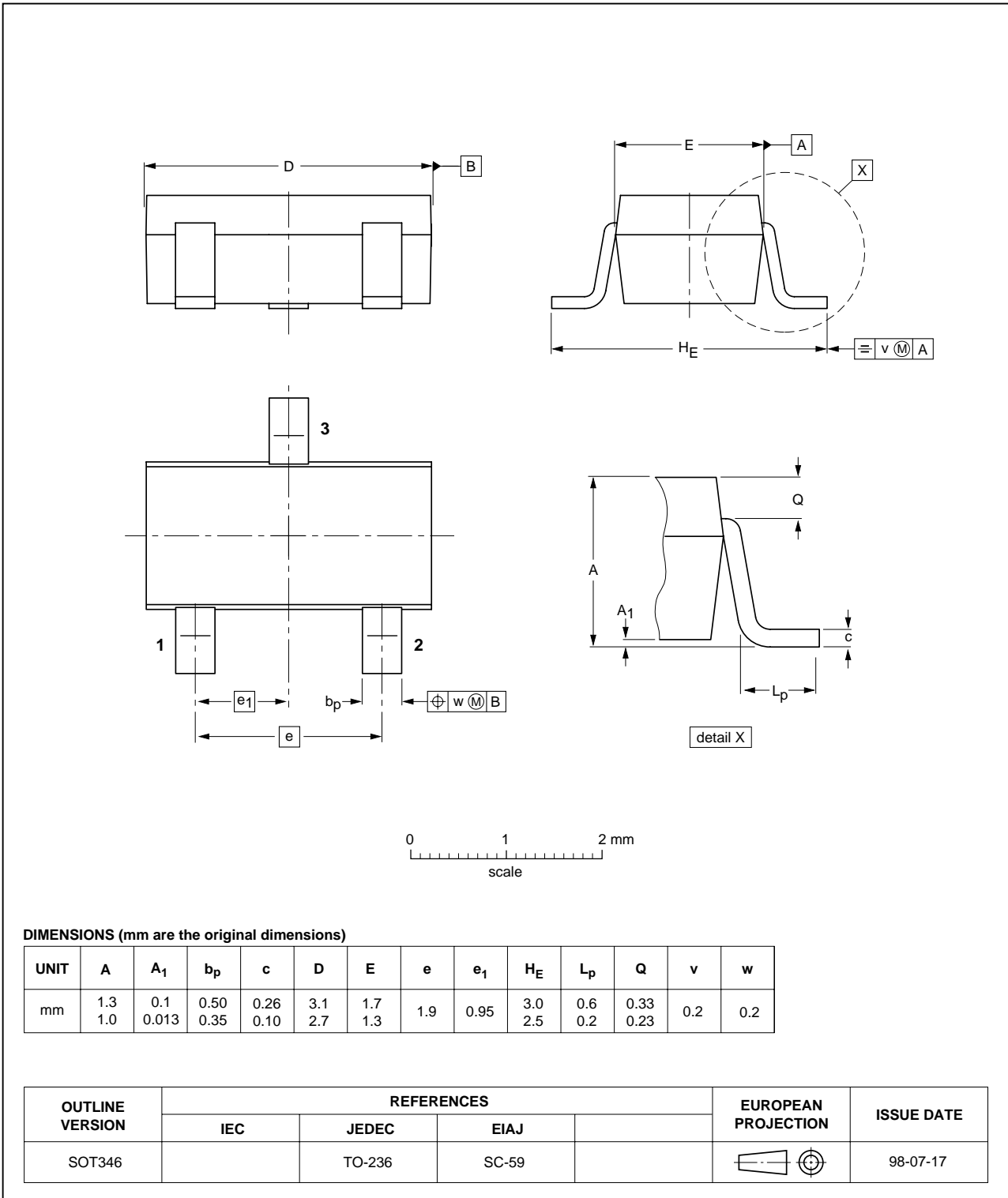


PNP resistor-equipped transistors;  
R1 = 4.7 kΩ, R2 = open

PDTA143T series

Plastic surface mounted package; 3 leads

SOT346

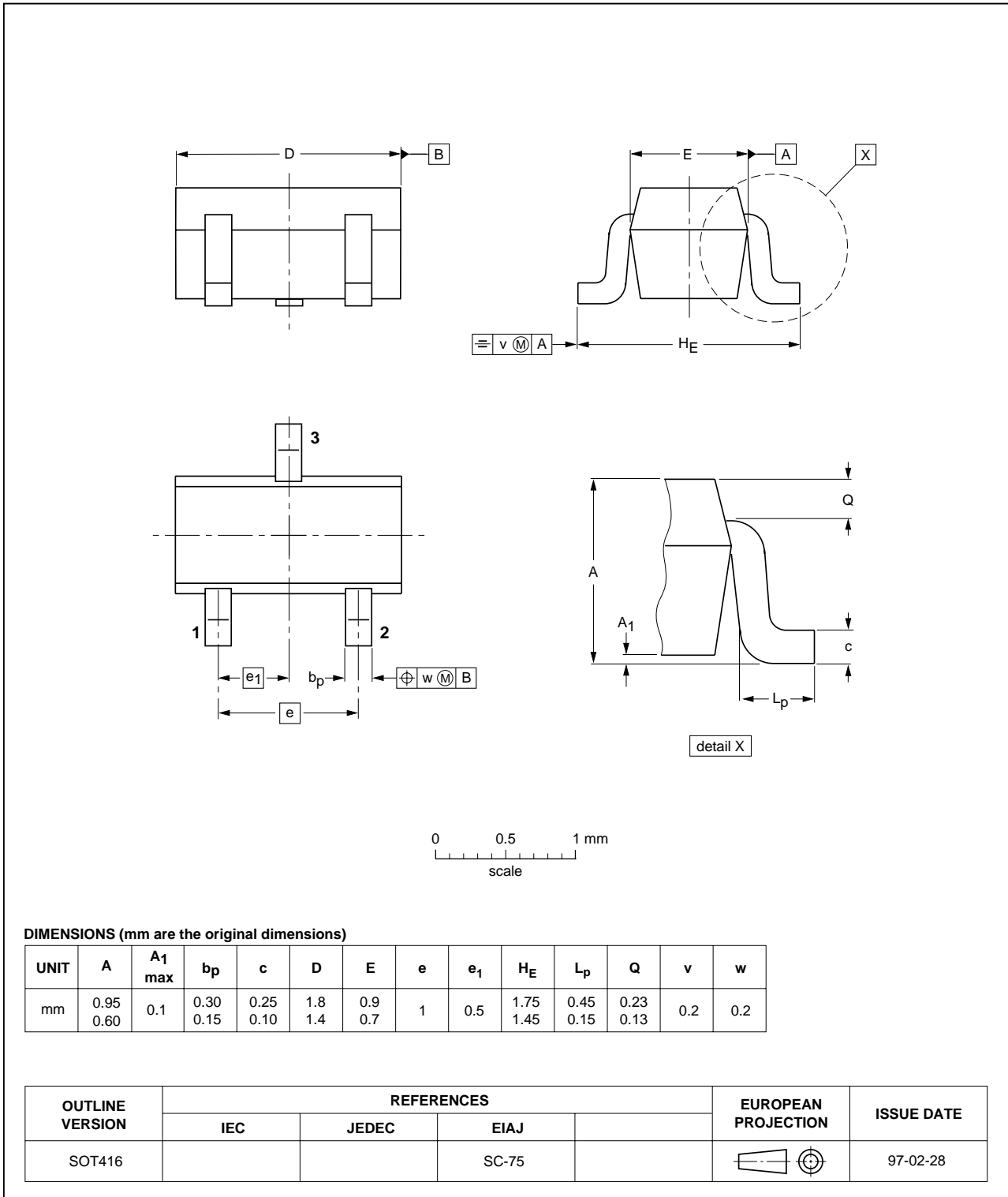


PNP resistor-equipped transistors;  
R1 = 4.7 kΩ, R2 = open

PDTA143T series

Plastic surface mounted package; 3 leads

SOT416

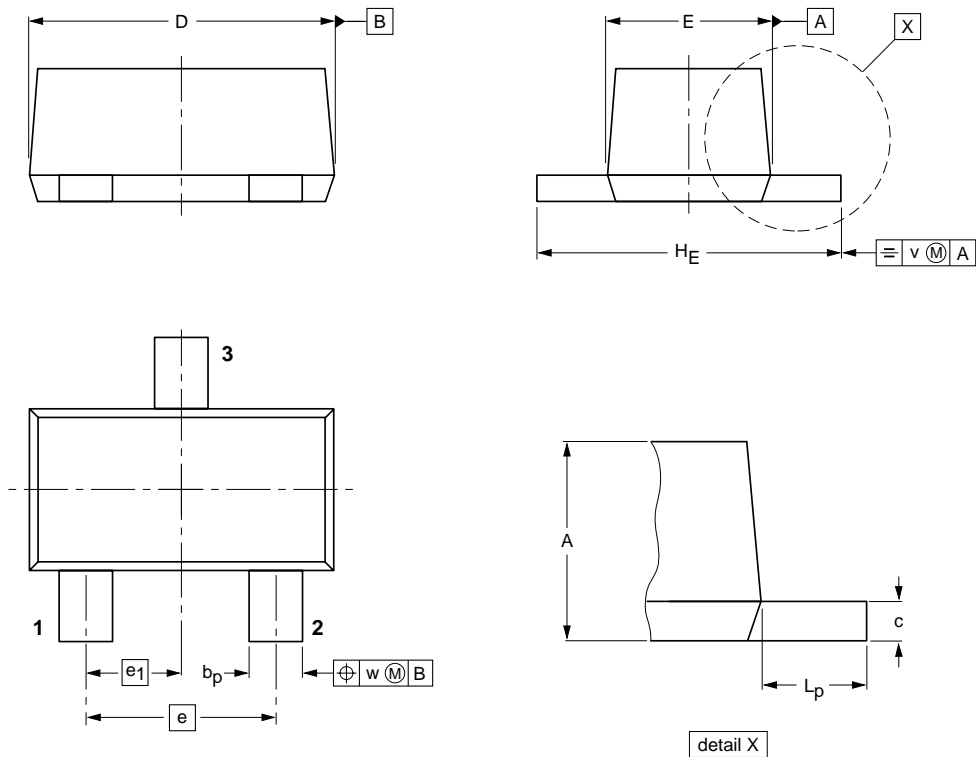


PNP resistor-equipped transistors;  
R1 = 4.7 kΩ, R2 = open

PDTA143T series

Plastic surface mounted package; 3 leads

SOT490



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

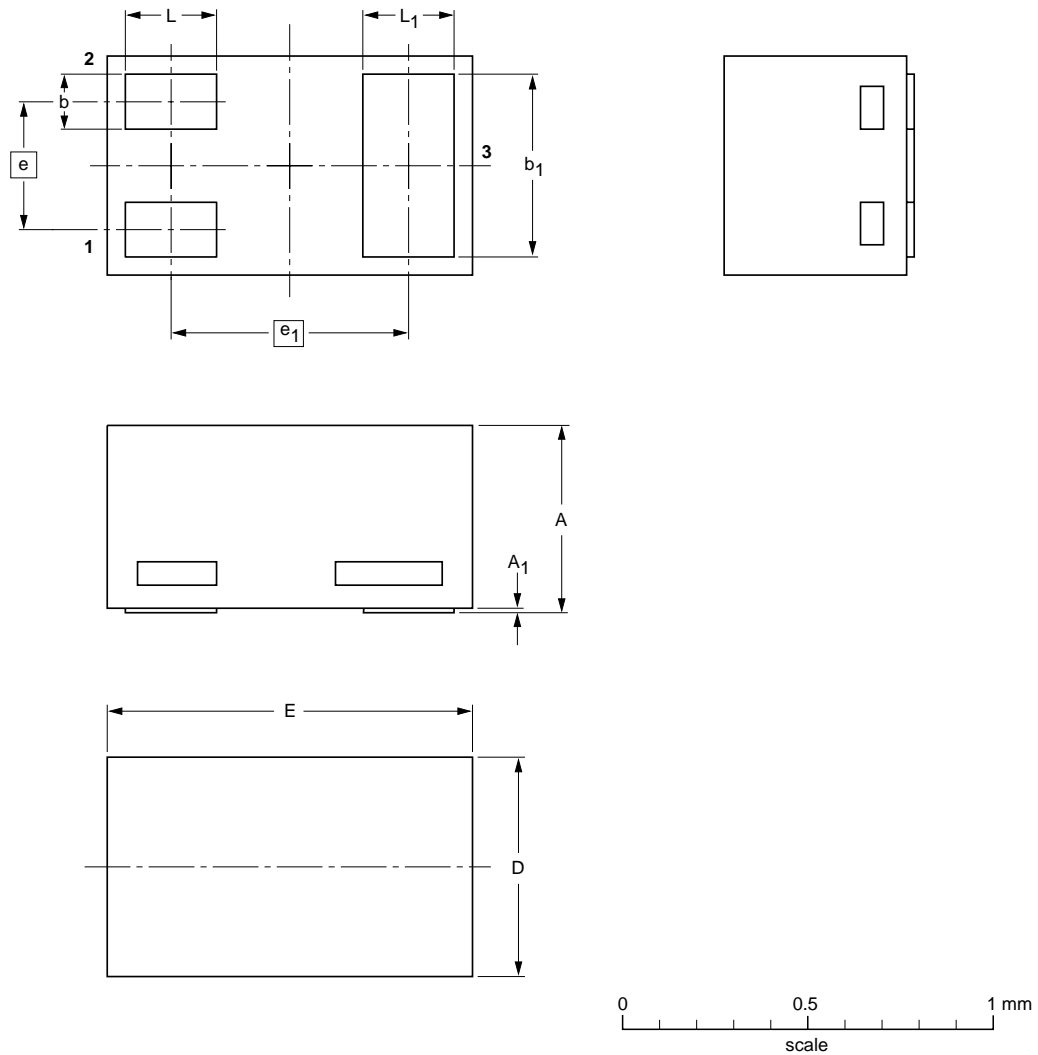
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT490			SC-89		98-10-23

PNP resistor-equipped transistors;  
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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup>	A <sub>1</sub> max.	b	b <sub>1</sub>	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

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PDTA143T series

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