NX5P2090

Logic controlled high-side power switch

Rev. 1 — 12 August 2013 **Preliminary data sheet**

1. General description

The NX5P2090 is an advanced power switch for USB OTG applications. The device includes under voltage and over voltage lockout, over-current, over-temperature, reverse bias and in-rush current protection circuits designed to automatically isolate a VBUS OTG voltage source from a VBUS interface pin when a fault condition occurs. The device features two power switch terminals, one input (VINT) and one output (VBUS); a current limit input (ILIM) for defining the over-current and in-rush current limit; a voltage detect output (VDET) to monitor the voltage level on VBUS; an open-drain fault output ($\overline{\text{FAULT}}$) to indicate when a fault condition has occurred and an enable input (EN) to control the state of the switch. When EN is set LOW the device enters a low power mode, disabling all protection circuits accept the under-voltage lockout. The low power mode can be entered at anytime unless the over temperature protection circuit has been triggered.

Designed for operation from 3 V to 5.5 V, it is used in power domain isolation applications to protect from out of range operation. The enable input includes integrated logic level translation making the device compatible with lower voltage processors and controllers.

2. Features and benefits

- Wide supply voltage range from 3 V to 5.5 V
- 30 V tolerant on VBUS
- I_{SW} maximum 2 A continuous current
- Very low ON resistance: 100 mΩ (maximum) at a supply voltage of 4.0 V
- Low-power mode (ground current 20 μA typical)
- 1.8 V control logic
- Soft start turn-on slew rate
- Protection circuitry
  - Over-temperature protection
  - Over-current protection with low current output mode
  - Reverse bias current/Back drive protection
  - Over-voltage lockout
  - Under-voltage lockout
  - Analog voltage limited VBUS monitor path
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
- Specified from –40 °C to +85 °C

3. Applications

- USB OTG applications

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5P2090UK	–40 °C to +85 °C	WLCSP9	wafer level chip-scale package; 9 bumps; body 1.36 × 1.36 x 0.51 mm. (Backside Coating included)	NX5P2090UK

5. Marking

Table 2. Marking codes

Type number	Marking code
NX5P2090UK	Nx5P2

6. Functional diagram

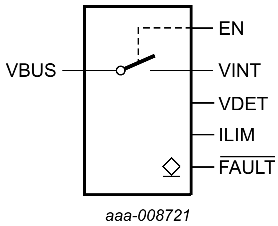


Fig 1. Logic symbol

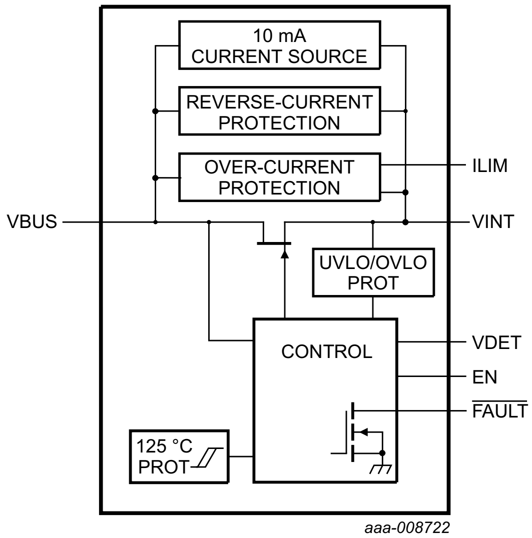


Fig 2. Logic diagram (simplified schematic)

7. Pinning information

7.1 Pinning

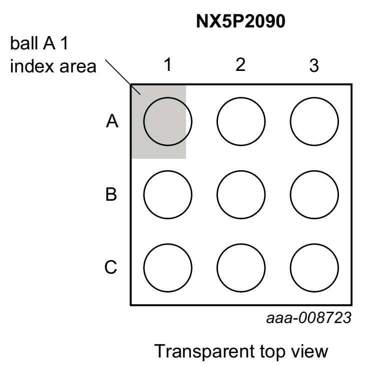


Fig 3. Pin configuration WLCSP9 package

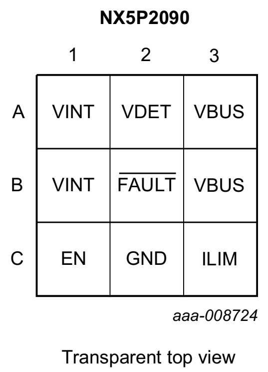


Fig 4. Ball mapping for WLCSP9

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VINT	A1, B1	internal circuitry voltage I
VBUS	A3, B3	external connector voltage O
EN	C1	enable input (active HIGH) I
ILIM	C3	current limiter I/O
VDET	A2	VBUS voltage level indicator O
$\overline{\text{FAULT}}$	B2	fault condition indicator (open-drain; active LOW)
GND	C2	ground (0 V)

8. Functional description

Table 4. Function table[1]

EN	VINT	VBUS	FAULT	Operation mode
X	0 V	Z	L	No supply
X	0 V	< 30 V	Z	Disabled; switch open
X	< 3.2 V	Z	L	Under-voltage lockout; switch open
H	> 5.5 V	Z	L	Over-voltage lockout; switch open
H	3.2 V to 5.5 V	Z	L	Over-temperature; switch open
L	3.2 V to 5.5 V	Z	Z	Disabled; switch open
H	3.2 V to 5.5 V	VBUS = VINT	Z	Enabled; switch closed; active
H	3.2 V to 5.5 V	0 V to VINT	L	Over-current; Switch open; constant current on VBUS
H	3.2 V to 5.5 V	0 V to VINT	L	When ILIM is connected to GND, VBUS is default supplied with 10 mA current source
H	3.2 V to 5.5 V	VINT + 30 mV < VBUS < VINT + 0.45 V (> 4 ms)	L	Reverse bias current/back drive; switch open
H	3.2 V to 5.5 V	VBUS > VINT + 0.7 V	L	Reverse bias current/back drive; switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state, X = Don’t care.

Table 5. Function table VDET versus VBUS[1]

VBUS	VDET	Operation mode
3 V < VBUS < 30 V	1.5 < VDET < 5.5 V	VDET detects VBUS voltage

[1] See Figure 22.

8.1 EN input

When the EN is set LOW the N-channel MOSFET will be disabled, the device will enter low-power mode disabling all protection circuits except the under-voltage lockout circuit and setting the FAULT output high impedance. When EN is set HIGH, all protection circuits will be enabled and then, if no fault conditions exist and an R_{ILIM} current limit resistor is detected, the N-channel MOSFET will be enabled.

8.2 Under-voltage lockout

Independently of the logic level on the EN pin, the under-voltage lockout (UVLO) circuit disables the N-channel MOSFET, sets the FAULT output LOW and enters low power mode until VINT > 3.2 V. Once VINT > 3.2 V the state of the N-channel MOSFET is controlled by the EN pin. The UVLO circuit remains active in low-power mode.

8.3 Over-voltage lockout

When EN is set HIGH, the over-voltage lockout (OVLO) circuit will disable the N-channel MOSFET and set the FAULT output LOW if VINT > 5.75 V. The OVLO circuit is disabled in low-power mode, and it will not influence the FAULT output state. If the OVLO circuit is active, setting the EN pin LOW will return the device to low-power mode.

8.4 ILIM

The over-current protection circuit's (OCP) trigger value I_{OS}, can be set using an external resistor R_{ILIM} connected to the ILIM pin (see Figure 6). When EN is set HIGH and the ILIM pin is grounded, the N-channel MOSFET will be disabled, VBUS will be supplied by the 10 mA current source and the $\overline{\text{FAULT}}$ output set LOW.

8.5 Over-current protection

If the current through the N-channel MOSFET exceeds I_{OS} for 20 μs or VBUS < VINT – 200 mV, the over-current protection (OCP) circuit will disable the N-channel MOSFET within 2 μs; supply VBUS from the 10 mA current source, and indicate a fault condition by setting the FAULT pin LOW. The OCP circuit is automatically reset when VINT > VBUS > VINT – 200 mV for 20 μs, the N-channel MOSFET assumes the state defined by the EN input, the 10 mA current source is disconnected and the $\overline{\text{FAULT}}$ pin is set high impedance. If the OCP circuit is active, setting the EN pin LOW will return the device to low-power mode.

8.6 Over-temperature protection

When EN is set HIGH, if the device temperature exceeds 125 °C the Over-temperature protection (OTP) circuit will disable the N-channel MOSFET and indicate a fault condition by setting the $\overline{\text{FAULT}}$ pin LOW. Any transition on the EN pin will have no effect. Once the device temperature decreases to below 115 °C the device will return to the defined state. The OTP circuit is disabled in low-power mode, however if the OTP circuit is active, setting the EN pin LOW will not return the device to low-power mode.

8.7 Reverse bias current/back drive protection

When EN is set HIGH, if (VINT + 30 mV) < VBUS < (VINT + 0.45 V) for longer than 4 ms; or if VBUS > (VINT + 0.45 V), the reverse-bias current protection (RCP) circuit will disable the N-channel MOSFET and indicate a fault condition by setting the $\overline{\text{FAULT}}$ pin LOW. Once VBUS < VINT for longer than 4 ms the device will return to the defined state. If the RCP circuit is active, setting the EN pin LOW will return the device to low-power mode.

8.8 $\overline{\text{FAULT}}$ output

The $\overline{\text{FAULT}}$ output is an open-drain output that requires an external pull-up resistor. If any of the UVLO, OVLO, RCP, OCP or OTP circuits is activated, the $\overline{\text{FAULT}}$ output will be set LOW to indicate a fault has occurred. The $\overline{\text{FAULT}}$ output will return to the high impedance state automatically once the fault condition is removed.

8.9 VDET output

VDET is an analog output that allows a controller to monitor the voltage level on VBUS.

8.10 In-rush current protection

When the N-channel MOSFET is enabled either by the EN pin or via a recovered fault condition, the in-rush current protection circuit causes the switch to effectively behave as a current source during the time VBUS ramps up to VINT - 200 mV. The current is determined by the resistor connected to ILIM. The in-rush current protection circuit is disabled in low-power mode.

9. Application diagram

The NX5P2090 typically connects a voltage source on VINT to the VBUS of a USB connector supporting USB3 OTG in a portable, battery operated device. The external resistor R_{ILIM} sets the maximum current limit threshold. The $\overline{FAULT}$ signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level it is connected to.

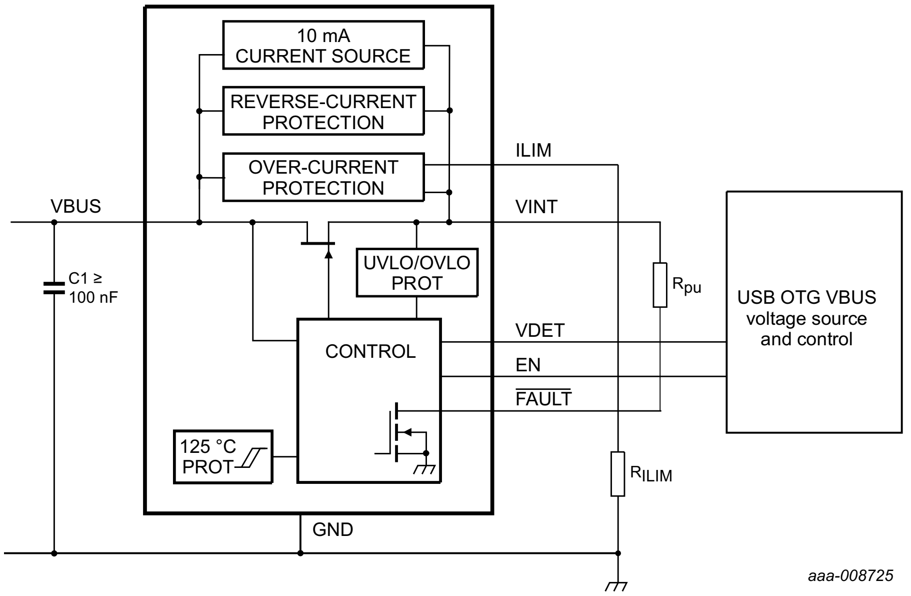


Fig 5. NX5P2090 application diagram

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS	[1]	–0.5	+32	V
		VINT	[1]	–0.5	+6.0	V
		EN, ILIM	[2]	–0.5	VINT + 0.5	V
V_O	output voltage	$\overline{FAULT}$		–0.5	+6.0	V
I_{IK}	input clamping current	EN: $V_I < -0.5$ V		–50	-	mA
I_{SK}	switch clamping current	VBUS; VINT; $V_I < -0.5$ V		–50	-	mA
I_{SW}	switch current	T_{amb} = 85 °C		-	±2000	mA
$T_{j(max)}$	maximum junction temperature			–40	+125	°C
T_{stg}	storage temperature			–65	+150	°C

Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation		[3]	-	73	mW

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VINT	3.0	5.5	V
		EN, ILIM	0	VINT	V
V_O	output voltage	VBUS; EN = LOW	0	30	V
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	400	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Please rely on the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts.

13. Static characteristics

Table 9. Static characteristics

$V_{I(VINT)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN input	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	EN input	-	-	0.4	-	0.4	V
V_O	output voltage	VDET; I_{VDET} = −2 mA; 3 V < VBUS < 30 V	1.5	-	5.5	1.5	5.5	V
V_{OL}	LOW-level output voltage	$\overline{FAULT}$, I_O = 8 mA	-	-	0.5	-	0.5	V
I_O	output current	Current source	-	10	-	8	15	mA
		EN = HIGH; $\overline{FAULT}$ = Hi-Z	-	-	I_{OS}	-	I_{OS}	mA
I_{OS}	output short-circuit current	EN = HIGH; see Figure 6	-	-	-	-	-	mA
R_{pu}	pull-up resistance	$\overline{FAULT}$	20	-	200	-	-	kΩ
V_{pu}	pull-up voltage	$\overline{FAULT}$	-	-	VINT	-	VINT	V
R_{ILIM}	current limit resistance	ILIM	40	-	300	40	300	kΩ
I_{GND}	ground current	VBUS open; EN = LOW; see Figure 7 and Figure 8	-	20	-	-	40	µA
		VBUS open; EN = HIGH; see Figure 7 and Figure 8	-	220	-	-	360	µA
I_{OFF}	power-off leakage current	VBUS = 0 V to 30 V; VINT = 0 V; see Figure 9 [2]	-	2	-	-	20	µA
$I_{S(OFF)}$	OFF-state leakage current	VBUS = 0 V to 30 V; see Figure 10 and Figure 11 [2]	-	2	-	-	20	µA
V_{UVLO}	undervoltage lockout voltage		3.0	3.2	3.4	3.0	3.4	V
V_{OVLO}	overvoltage lockout voltage		5.5	5.75	<tbd>	5.5	<tbd>	V
$V_{hys(OVLO)}$	overvoltage lockout hysteresis voltage		-	150	-	-	-	mV
C_I	input capacitance	EN	-	2	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	-	1	-	1	nF

[1] Typical values are measured at T_{amb} = 25 °C and $V_{I(VINT)}$ = 5.0 V.

[2] Typical value is measured at T_{amb} = 25 °C and $V_{I(VBUS)}$ = 5.0 V.

13.1 Graphs

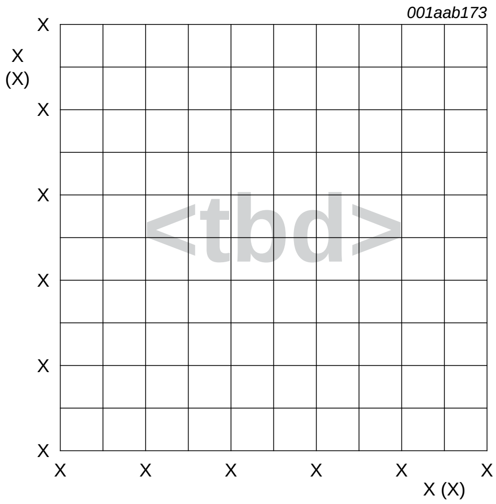
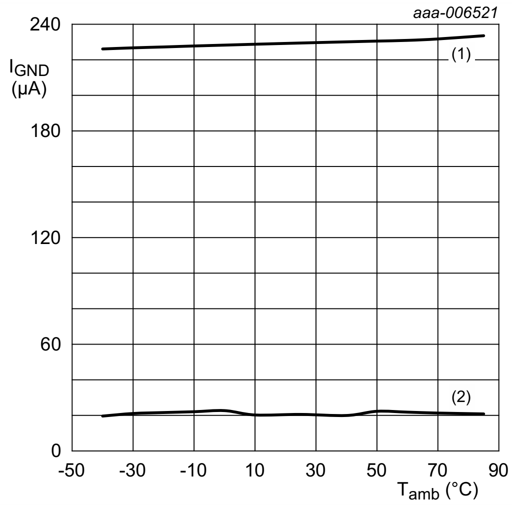


Fig 6. Typical over-current and in-rush current limit versus the external resistor value.



(1) Enabled

(2) Disabled

Fig 7. Typical ground current versus temperature

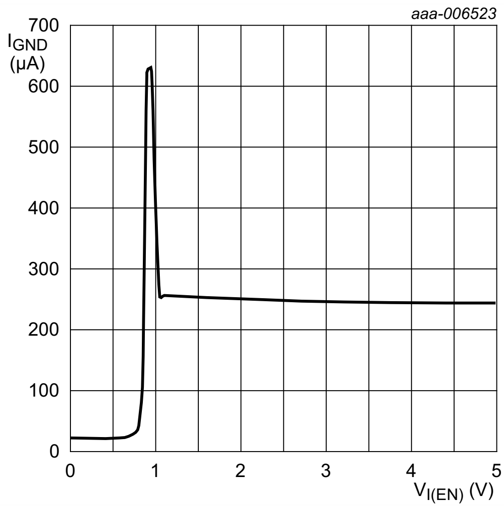
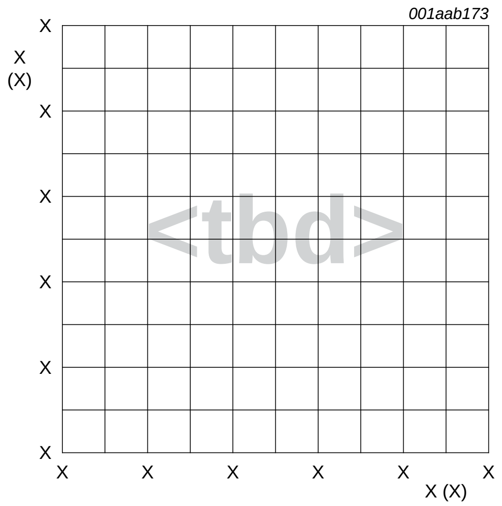


Fig 8. Typical ground current versus input voltage

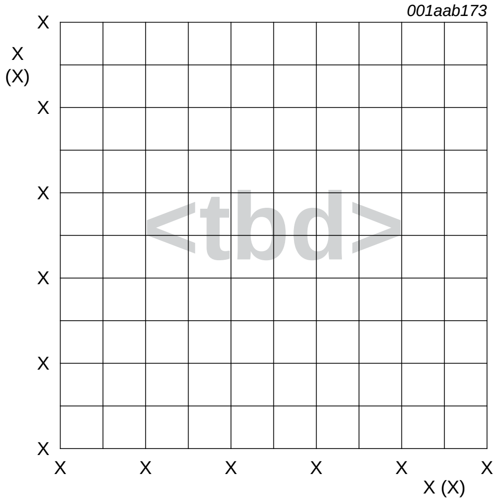


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 9. Typical power-off leakage current versus input voltage on pin VBUS

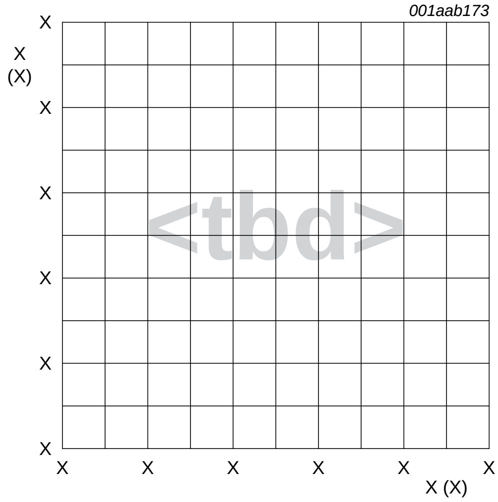


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. Typical OFF-state leakage current versus input voltage on pin VBUS



(1) $V_{I(VBUS)}$ = 15.0 V

(2) $V_{I(VBUS)}$ = 10.0 V

(3) $V_{I(VBUS)}$ = 5.0 V

Fig 11. Typical OFF-state leakage current versus temperature

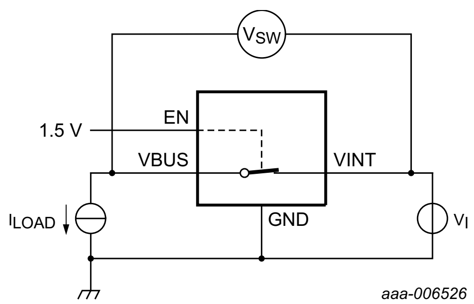
13.2 ON resistance

Table 10. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

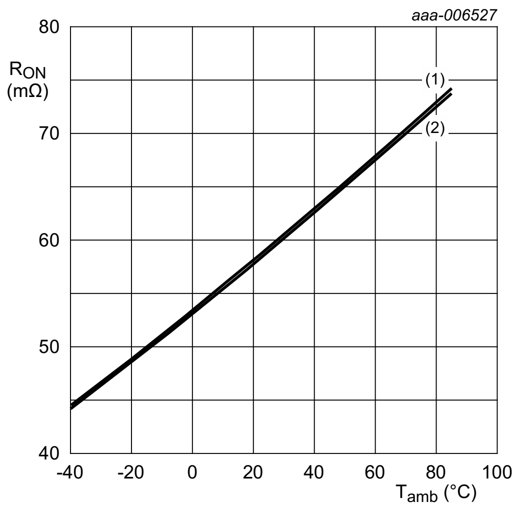
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	switch enabled; I_{LOAD} = 200 mA; see Figure 12, Figure 13 and Figure 14						
		$V_{I(VINT)}$ = 4.0 V to 5.5 V	-	60	-	-	100	mΩ

13.3 ON resistance test circuit and waveforms



$R_{ON} = V_{SW} / I_{LOAD}$.

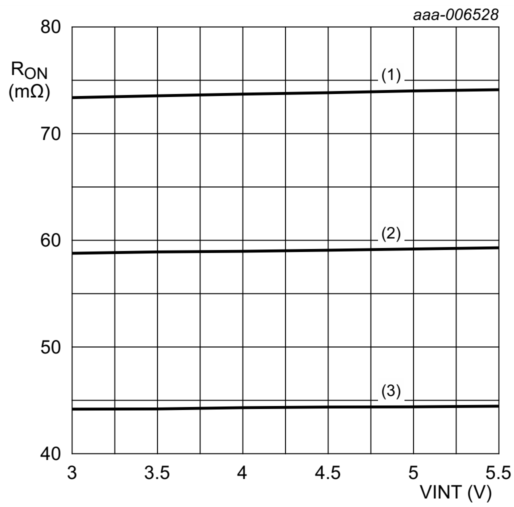
Fig 12. Test circuit for measuring ON resistance



(1) $V_{I(VINT)}$ = 5.5 V

(2) $V_{I(VINT)}$ = 4.0 V

Fig 13. Typical ON resistance versus temperature



(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 14. Typical ON resistance versus input voltage

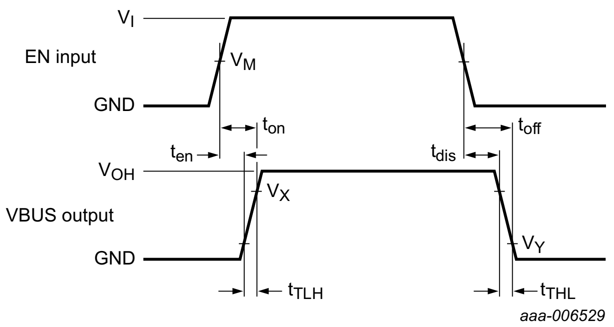
14. Dynamic characteristics

Table 11. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 16.
$V_{I(VINT)}$ = 4.0 V to 5.5 V.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	EN to VBUS; see Figure 15	-	0.24	-	0.16	-	ms
t_{dis}	disable time	EN to VBUS; see Figure 15	-	1.5	-	-	-	ms
t_{on}	turn-on time	EN to VBUS; see Figure 15	-	0.63	-	0.52	-	ms
t_{off}	turn-off time	EN to VBUS; see Figure 15	-	34.5	-	-	-	ms
t_{TLH}	LOW to HIGH output transition time	VBUS; see Figure 15	-	0.39	-	0.16	-	ms
t_{THL}	HIGH to LOW output transition time	VBUS; see Figure 15	-	33	-	-	-	ms

14.1 Waveform and test circuits



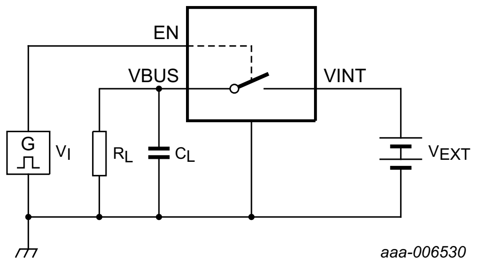
Measurement points are given in Table 12.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 15. Switching times

Table 12. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VINT)}$	V_M	V_X	V_Y
4.0 V to 5.5 V	$0.5 \times V_I$	$0.9 \times V_{OH}$	$0.1 \times V_{OH}$



Test data is given in Table 13.

Definitions test circuit:

R_L = Load resistance.

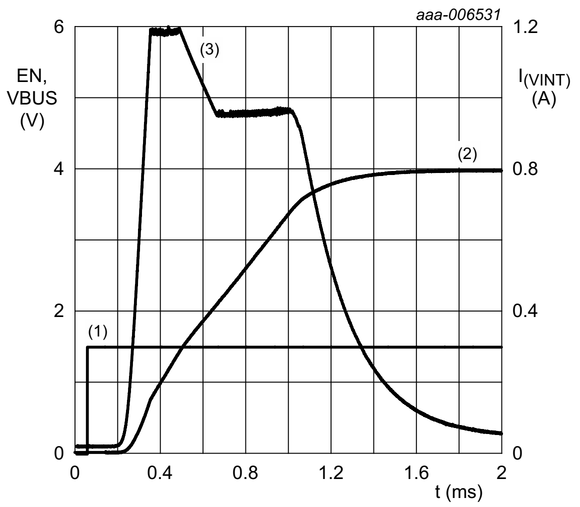
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 13. Test data

Supply voltage	Input	Load	
V_{EXT}	V_I	C_L	R_L
4.0 V to 5.5 V	1.5 V	100 μF	150 Ω



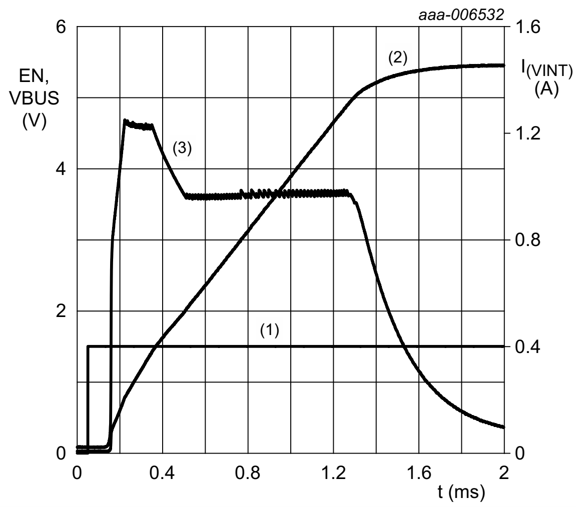
EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 220 μF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

(1) EN

(2) VBUS

(3) $I_{I(VINT)}$

Fig 17. Typical enable time and in-rush current



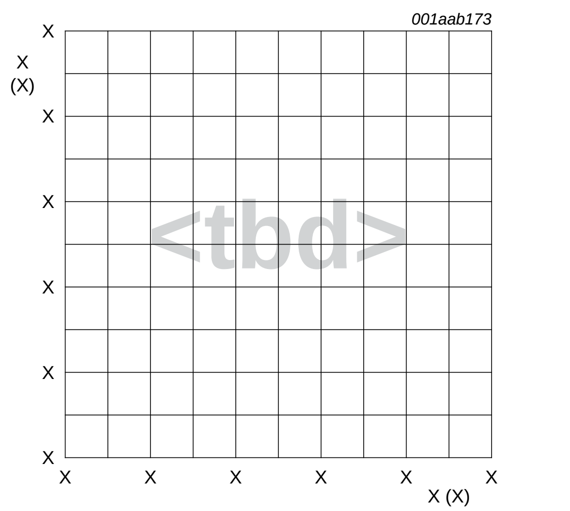
EN = 1.5 V; VINT = 5.5 V; R_L = 150 Ω; C_L = 220 μF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

(1) EN

(2) VBUS

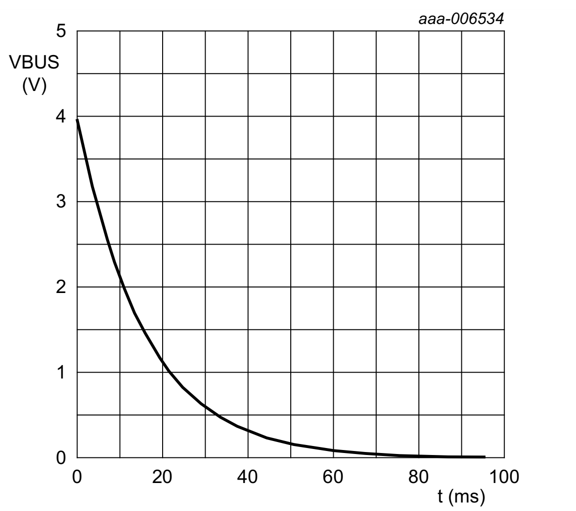
(3) $I_{I(VINT)}$

Fig 18. Typical enable time and in-rush current



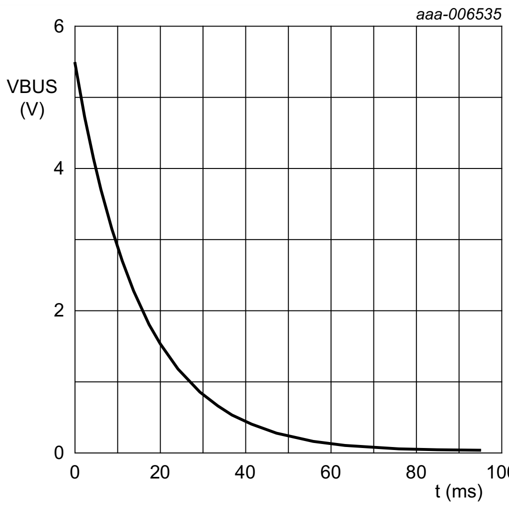
EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C.

Fig 19. Typical enable time versus current limit resistance (R_{ILIM})



EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 100 μF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

Fig 20. Typical disable time



EN = 1.5 V; VINT = 5.5 V; R_L = 150 Ω; C_L = 100 μF;
R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

Fig 21. Typical disable time

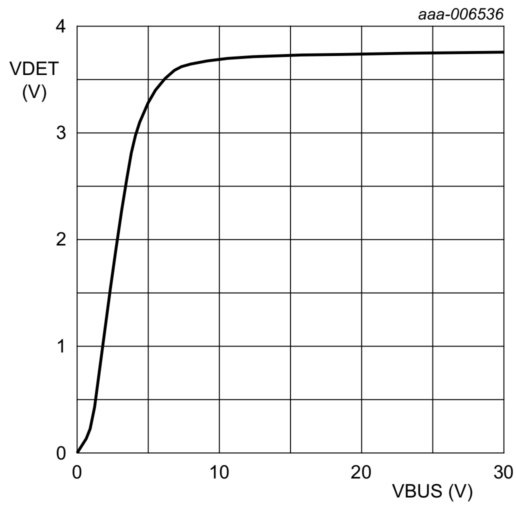
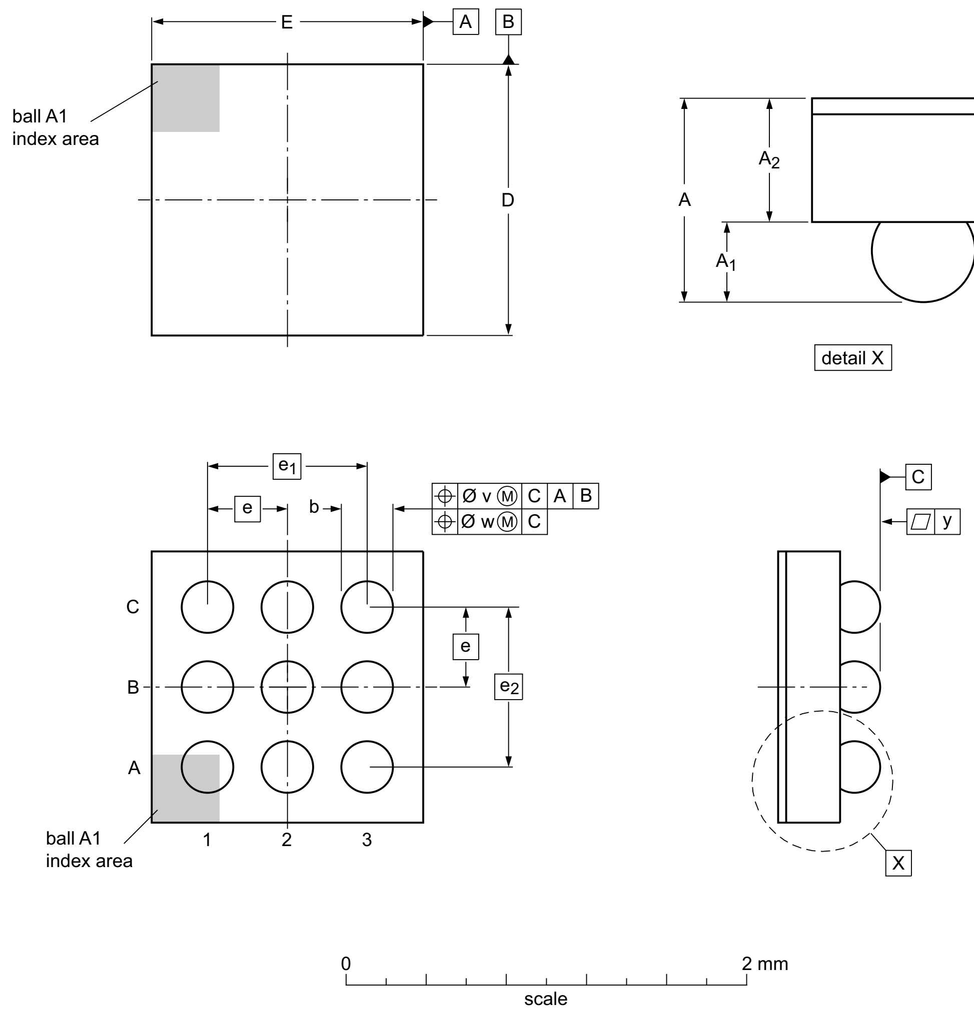


Fig 22. Typical VDET versus VBUS

15. Package outline

WLCSP9: wafer level chip-scale package;
9 bumps; body 1.36 x 1.36 x 0.51 mm (Backside Coating included) **NX5P2090UK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.55	0.23	0.34	0.29	1.39	1.39						
mm	nom	0.51	0.20	0.31	0.26	1.36	1.36	0.4	0.8	0.8	0.05	0.015	0.03
	min	0.47	0.17	0.29	0.23	1.33	1.33						

nx5p2090uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX5P2090UK						~~13-03-14~~ 13-03-26

Fig 23. Package outline WLCSP9 package

16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
OCP	Over-Current Protection
OTP	Over-Temperature Protection
RCP	Reverse Current Protection
USB OTG	Universal Serial Bus On-The-Go
UVLO	Under-voltage lockout
VBUS	USB Power Supply
OVLO	Over-voltage lockout

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P2090 v.1	20130812	Preliminary data sheet	-	-

18. Legal information

19. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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