# DATA SHEET

## NE56632-XX

Active-LOW system reset
with adjustable delay time

Product data

2002 Mar 25

Philips
Semiconductors

PHILIPS

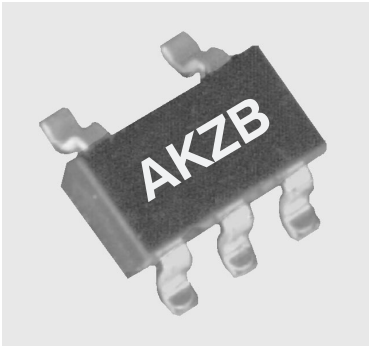
# Active-LOW system reset with adjustable delay time NE56632-XX

## DESCRIPTION

The NE56632-XX is a family of Active-LOW, power-on reset that offers precision threshold voltage detection within ±1.5% and super low operating supply current of typically 3.0 μA. It includes a reset delay that is user adjustable with an external capacitor.

Several detection threshold voltages are available at 1.9V , 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, and 4.6 V. Other thresholds are offered upon request at 100 mV steps from 1.9 V to 4.6 V.

With its ultra low supply current and high precision voltage threshold detection capability, the NE56632-XX is well suited for various battery powered applications such as reset circuits for logic and microprocessors, voltage check, and level detecting. It is available in the SOT23-5 package.




## FEATURES

- High precision threshold detection voltage: $V_S$ ±1.5%
- Super low operating supply current: 3 μA typ.
- Built-in hysteresis voltage: 50 mV typ.
- Detection threshold voltage: 1.9 V, 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, and 4.6 V.
- Reset Output: Active-LOW, open collector
- Other detection threshold voltages available upon request at 100 mV steps from 1.9 V to 4.6 V.
- Large low reset output current: 30 mA typ.
- Power-on reset delay time adjustable with external capacitor: 200 μs to 200 ms
- Reset assertion with $V_{CC}$ down to 0.65 V

## APPLICATIONS

- Reset for microprocessor and logic circuits
- Voltage level detection circuit
- Battery voltage check circuit
- Detection circuit for battery back-up

## SIMPLIFIED SYSTEM DIAGRAM

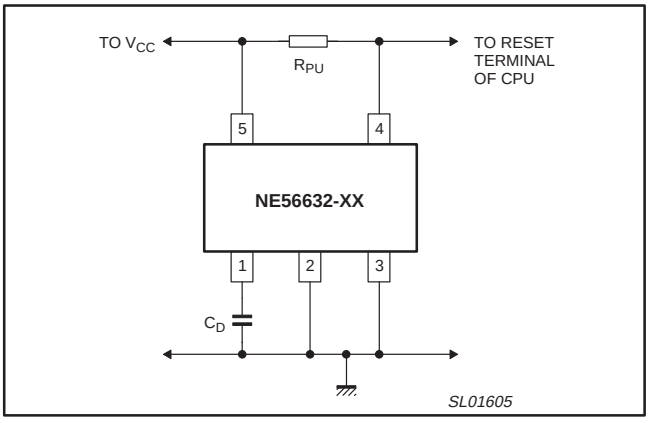



**Figure 1. Simplified system diagram.**

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | TEMPERATURE RANGE |
|---|---|---|---|
| | NAME | DESCRIPTION | |
| NE56632-**XX**D | SOT23-5 / SOT25 (SO5) | plastic small outline package; 5 leads (see dimensional drawing) | –20 to +75 °C |

**NOTE:**
The device has 12 voltage output options, indicated by the XX on the 'Type number'.

| XX | VOLTAGE (Typical) |
|---|---|
| 19 | 1.9 V |
| 20 | 2.0 V |
| 27 | 2.7 V |
| 28 | 2.8 V |
| 29 | 2.9 V |
| 30 | 3.0 V |
| 31 | 3.1 V |
| 42 | 4.2 V |
| 43 | 4.3 V |
| 44 | 4.4 V |
| 45 | 4.5 V |
| 46 | 4.6 V |

### Part number marking

The package is marked with a four letter code. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code.

| Part Number | Marking |
|---|---|
| NE56632-19D | AKZx |
| NE56632-20D | ALAx |
| NE56632-27D | ALBx |
| NE56632-28D | ALCx |
| NE56632-29D | ALDx |
| NE56632-30D | ALEx |
| NE56632-31D | ALFx |
| NE56632-42D | ALGx |
| NE56632-43D | ALHx |
| NE56632-44D | ALJx |
| NE56632-45D | ALKx |
| NE56632-46D | ALLx |

## PIN CONFIGURATION

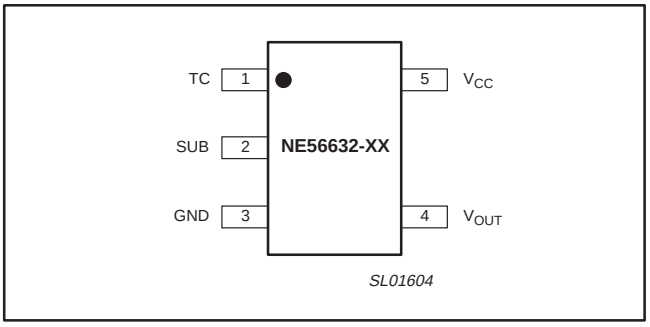



**Figure 2. Pin configuration.**

## PIN DESCRIPTION

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | TC | Delay time control; set with external capacitor. |
| 2 | SUB | Substrate. Connect to ground (GND). |
| 3 | GND | Ground. Negative supply. |
| 4 | $V_{OUT}$ | Reset output voltage. Active-LOW. |
| 5 | $V_{CC}$ | Positive supply voltage; detection threshold voltage input. |

## MAXIMUM RATINGS

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.3 | +10 | V |
| $T_{amb}$ | Ambient operating temperature | –20 | +75 | °C |
| $T_{stg}$ | Storage temperature | –40 | +125 | °C |
| P | Power dissipation | – | 150 | mW |

## ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 25 °C, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | -XX | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_S$ | Detection threshold | $V_{CC}$ = HIGH-to-LOW; $R_L$ = 4.7 kΩ; S1=ON; $V_{OL} \leq 0.4$ V; Test Circuit 1 (Figure 27) | 46 | 4.531 | 4.600 | 4.669 | V |
| | | | 45 | 4.432 | 4.500 | 4.568 | V |
| | | | 44 | 4.334 | 4.400 | 4.466 | V |
| | | | 43 | 4.235 | 4.300 | 4.365 | V |
| | | | 42 | 4.137 | 4.200 | 4.263 | V |
| | | | 31 | 3.053 | 3.100 | 3.147 | V |
| | | | 30 | 2.955 | 3.000 | 3.045 | V |
| | | | 29 | 2.856 | 2.900 | 2.944 | V |
| | | | 28 | 2.758 | 2.800 | 2.842 | V |
| | | | 27 | 2.659 | 2.700 | 2.741 | V |
| | | | 20 | 1.970 | 2.000 | 2.030 | V |
| | | | 19 | 1.871 | 1.900 | 1.929 | V |
| $V_{hys}$ | Hysteresis voltage | $R_L$ = 4.7 kΩ; $V_{CC}$ = LOW-to-HIGH-to-LOW; S1 = ON; Test Circuit 1 (Figure 27) | | 25 | 50 | 100 | mV |
| $V_S/\Delta T$ | Detection threshold voltage temperature coefficient | $R_L$ = 4.7 kΩ; $T_{amb}$ = –20 °C to +75 °C; S1 = ON; Test Circuit 1 (Figure 27) | | – | ±0.01 | – | %/°C |
| $V_{OL}$ | LOW-level output voltage | $V_{CC1} = V_{S(min)} – 0.05$ V; $R_L$ = 4.7 kΩ; S1 = ON; Test Circuit 1 (Figure 27) | | – | 0.2 | 0.4 | V |
| $I_{LO}$ | Output leakage current | $V_{CC1} = V_{CC2}$ = 10 V; S2 = ON; Test Circuit 1 (Figure 27) | | – | – | ±0.1 | µA |
| $I_{CCL}$ | Supply current (ON time) | $V_{CC1} = V_{S(min)} – 0.05$ V; $R_L = \infty$; Test Circuit 1 (Figure 27) | | – | 5.0 | 9.0 | µA |
| $I_{CCH}$ | Supply current (OFF time) | $V_{CC1} = V_{S(typ)}/0.85$; $R_L = \infty$; Test Circuit 1 (Figure 27) | | – | 3.0 | 5.0 | µA |
| $t_{PLH}$ | LOW-to-HIGH delay time | $C_L$ = 100 pF; $R_L$ = 4.7 kΩ; $C_D$ = 10 nF (Note 1) | | – | (Note 3) | – | ms |
| $t_{PHL}$ | HIGH-to-LOW delay time | $C_L$ = 100 pF; $R_L$ = 4.7 kΩ; $C_D$ = 10 nF (Note 2) | | – | (Note 3) | – | µs |
| $V_{OPL}$ | Minimum operating threshold voltage | $R_L$ = 4.7 kΩ; $V_{OL} \leq 0.4$ V; S1 = ON; Test Circuit 1 (Figure 27) | | – | 0.65 | 0.80 | V |
| $I_{OL1}$ | Output current (ON Time 1) | $V_O$ = 0.4 V; $R_L$ = 0; $V_{CC1} = V_{S(min)} – 0.05$ V; $V_{CC2}$ = 0.4 V; S2 = ON; Test Circuit 1 (Figure 27) | | 5 | – | – | mA |
| $I_{OL2}$ | Output current (ON Time 2) | $V_O$ = 0.4 V; $R_L$ = 0; $V_{CC1} = V_{S(min)} – 0.05$ V; $T_{amb}$ = –20 °C to +75 °C; S2 = ON; Test Circuit 1 (Figure 27) | | 3 | – | – | mA |

**NOTES:**

1. $t_{PLH}$: $V_{CC} = (V_{S(typ)} – 0.4$ V) to ($V_{S(typ)} + 0.4$ V); $t_{PLH}$ is release delay time (Test Circuit 2, Figure 28).
2. $t_{PHL}$: $V_{CC} = (V_{S(typ)} + 0.4$ V) to ($V_{S(typ)} – 0.4$ V); $t_{PHL}$ is assertion delay time (Test Circuit 2, Figure 28).
3. See Table 1.

### Table 1. NE56632-XX series typical delay time

| –XX | $t_{PLH}$ | $t_{PHL}$ |
|---|---|---|
| 46 | 195 ms | 140 µs |
| 45 | 190 ms | 140 µs |
| 44 | 185 ms | 140 µs |
| 43 | 180 ms | 140 µs |
| 42 | 175 ms | 140 µs |
| 31 | 120 ms | 120 µs |
| 30 | 115 ms | 120 µs |
| 29 | 110 ms | 120 µs |
| 28 | 105 ms | 100 µs |
| 27 | 100 ms | 100 µs |
| 20 | 65 ms | 100 µs |
| 19 | 60 ms | 100 µs |

## TYPICAL PERFORMANCE CURVES, NE56632-20

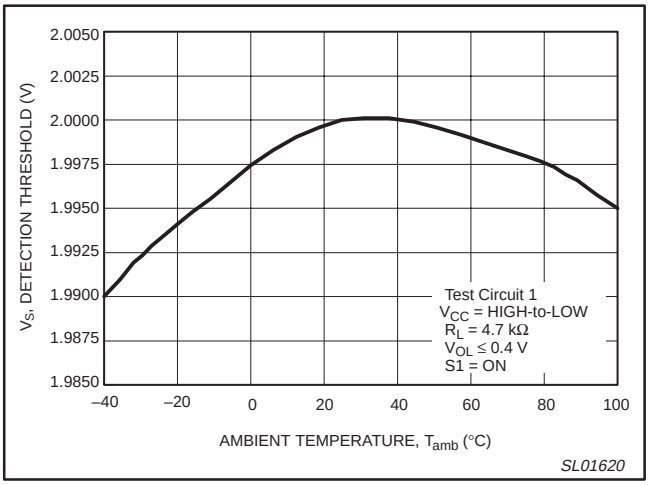



**Figure 3. Detection threshold versus temperature.**

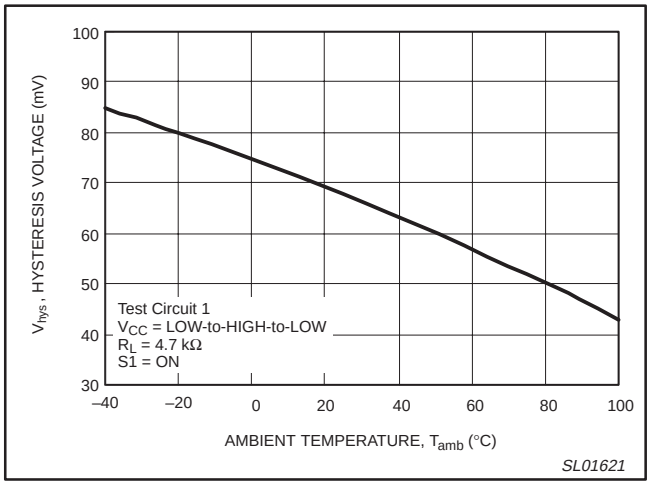



**Figure 4. Hysteresis voltage versus temperature.**

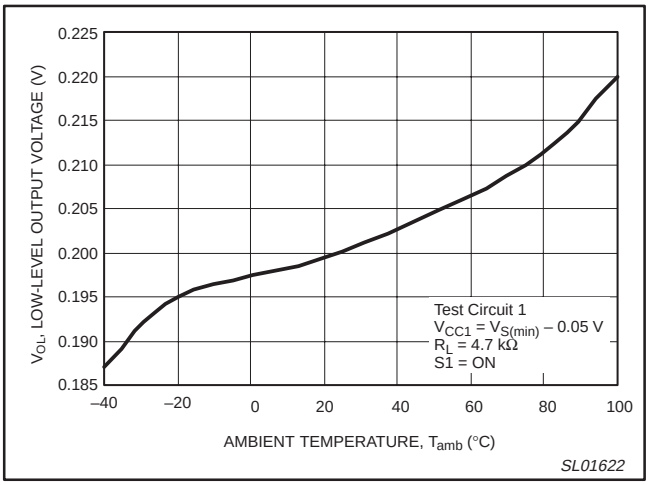



**Figure 5. LOW-level output voltage versus temperature.**

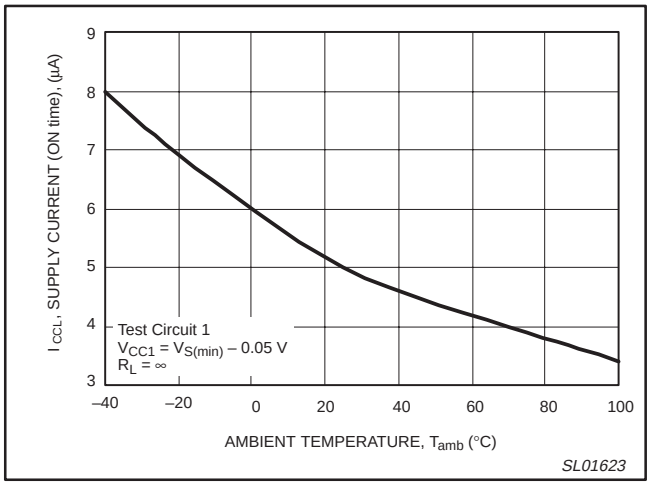



**Figure 6. Supply current (ON time) versus temperature.**

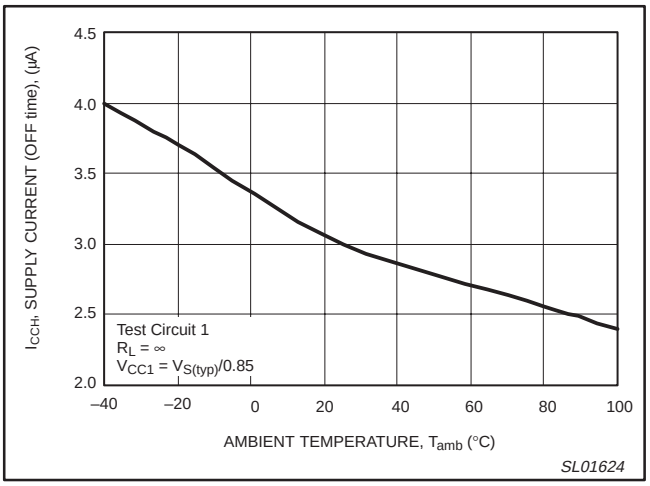



**Figure 7. Supply current (OFF time) versus temperature.**

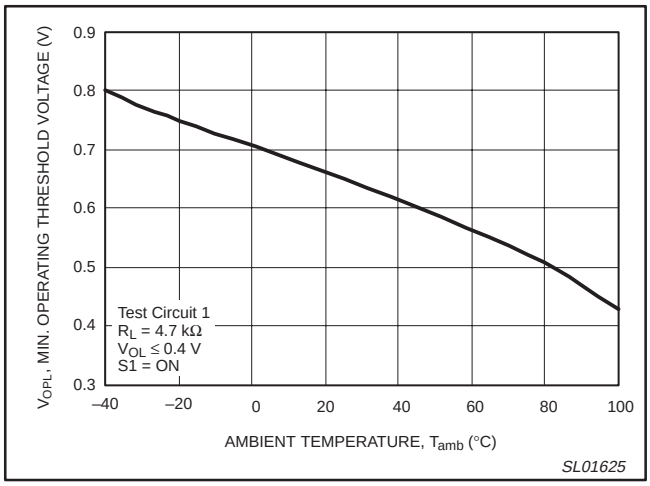



**Figure 8. Min. operating threshold voltage versus temperature.**

## TYPICAL PERFORMANCE CURVES, NE56632-20 *(continued)*

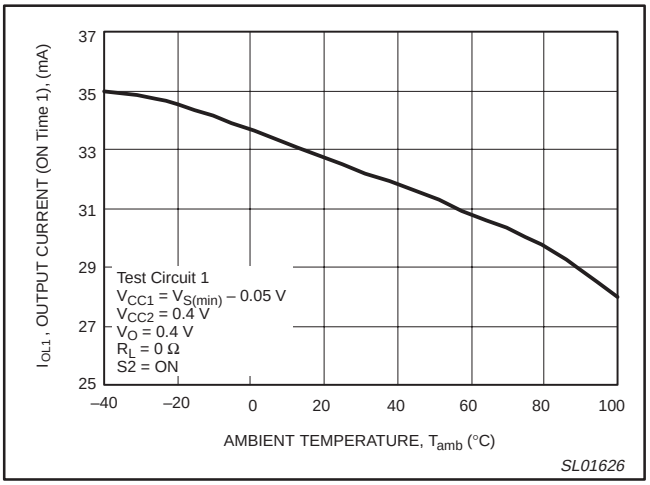



**Figure 9. Output current (ON time 1) versus temperature.**

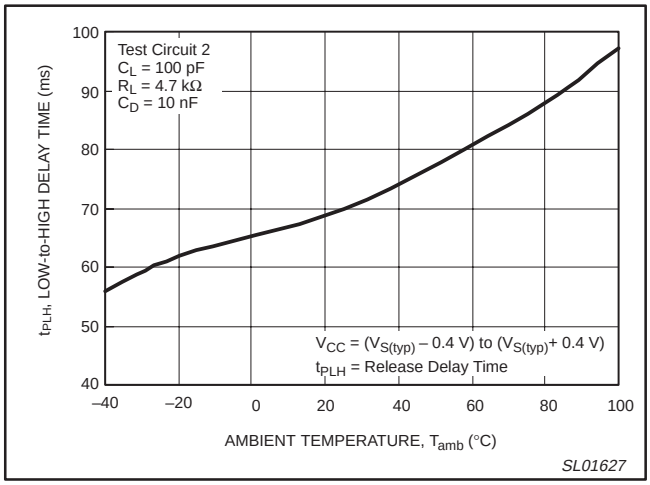



**Figure 10. LOW-to-HIGH delay time versus temperature.**

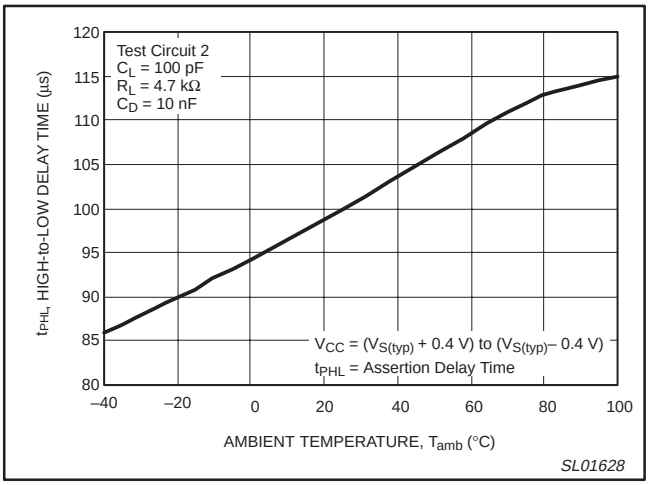



**Figure 11. HIGH-to-LOW delay time versus temperature.**

## TYPICAL PERFORMANCE CURVES, NE56632-31

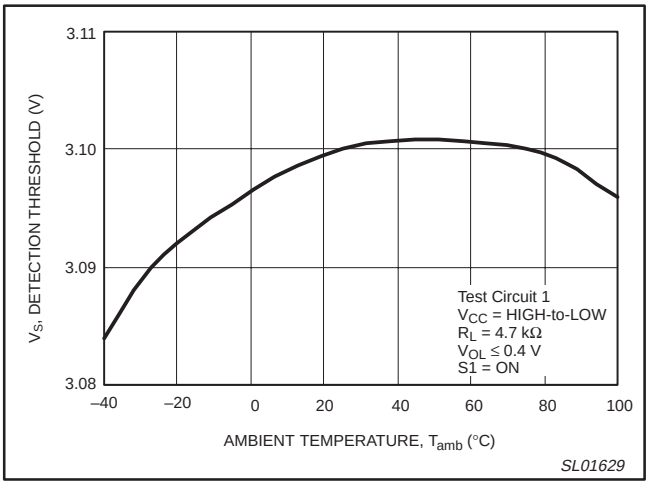



**Figure 12. Detection threshold versus temperature.**

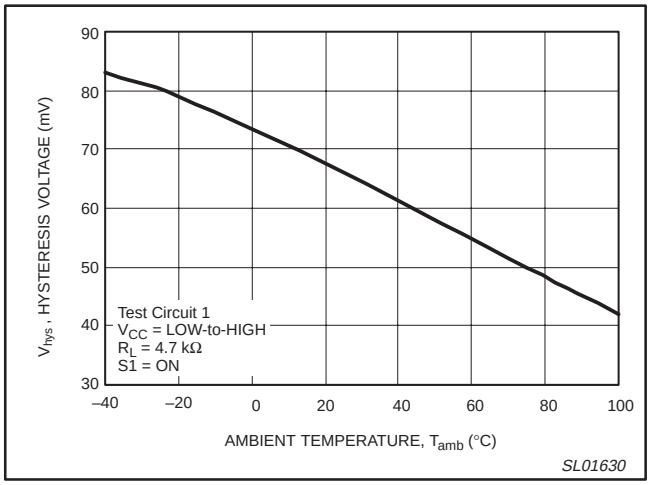



**Figure 13. Hysteresis voltage versus temperature.**

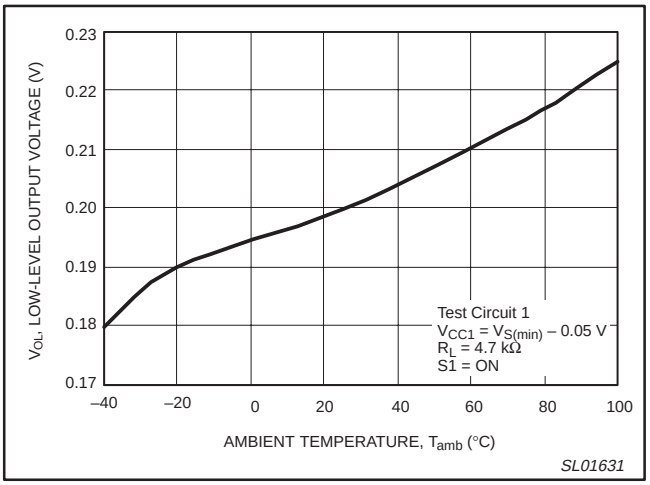



**Figure 14. LOW–level output voltage versus temperature.**

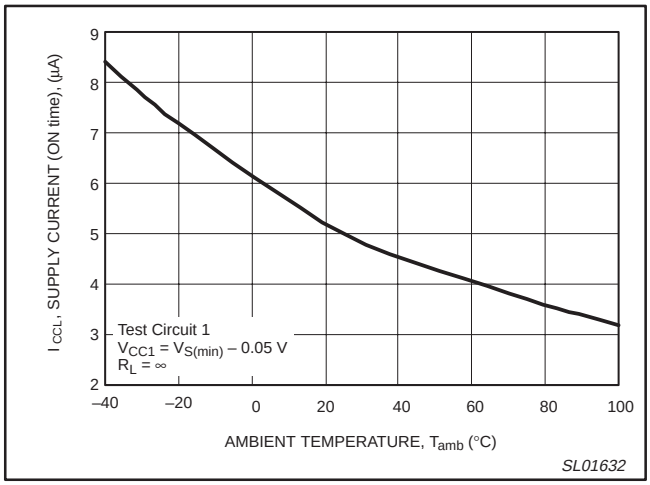



**Figure 15. Supply current (ON time) versus temperature.**

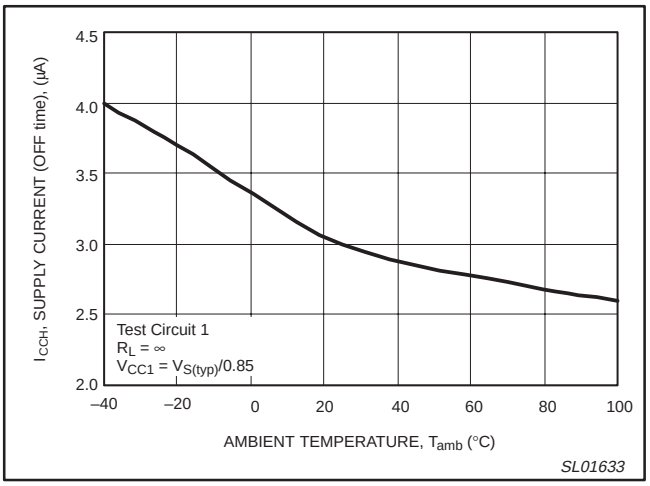



**Figure 16. Supply current (OFF time) versus temperature.**

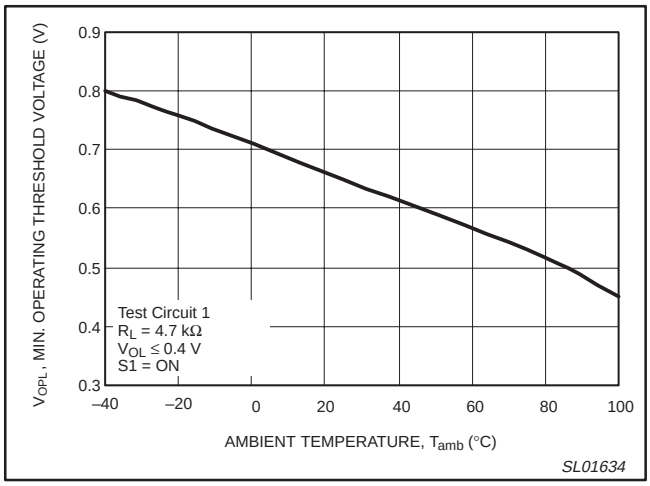



**Figure 17. Min. operating threshold voltage versus temperature.**

## TYPICAL PERFORMANCE CURVES, NE56632-31 *(continued)*

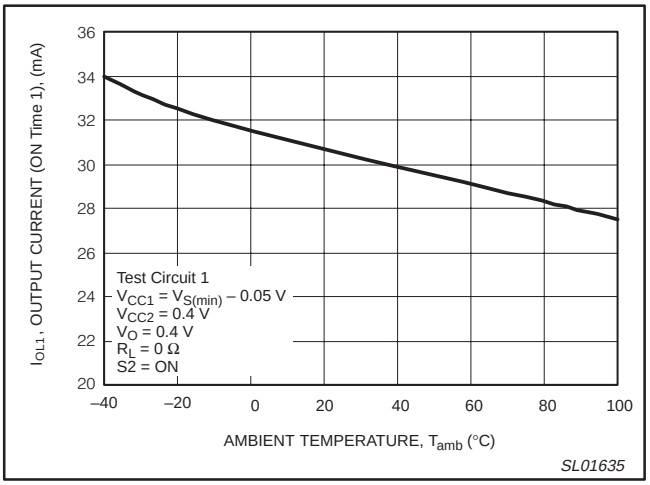



**Figure 18. Output current (ON time 1) versus temperature.**

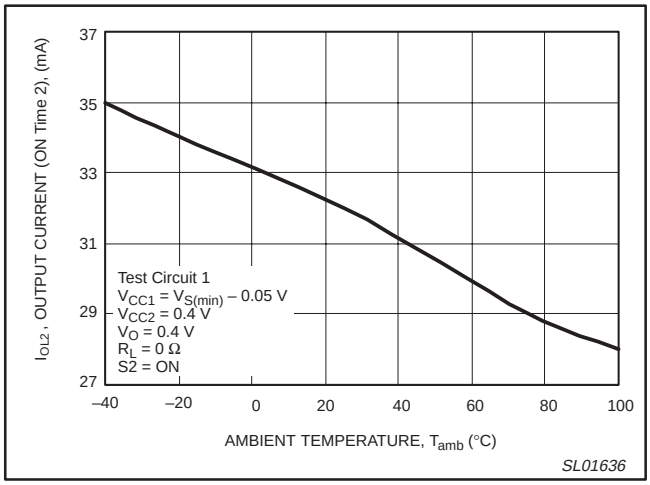



**Figure 19. Output current (ON time 2) versus temperature.**

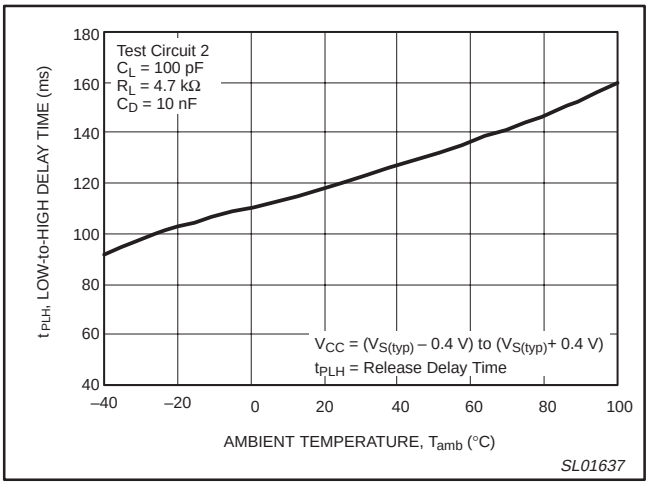



**Figure 20. LOW-to-HIGH delay time versus temperature.**

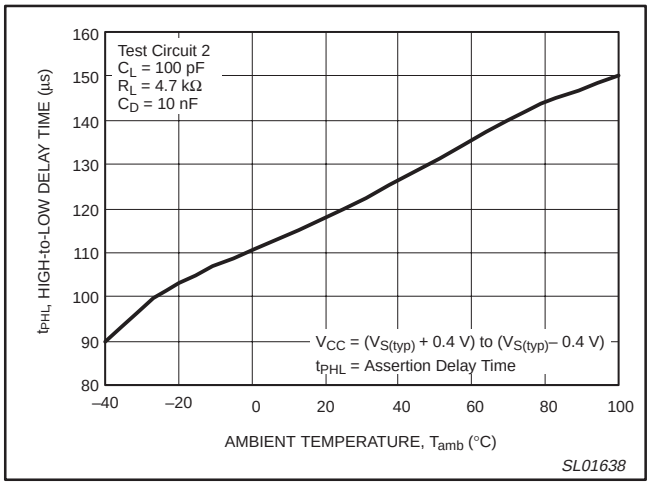



**Figure 21. HIGH-to-LOW delay time versus temperature.**

## TECHNICAL DISCUSSION

The NE56632-XX is a bipolar IC designed to provide power source monitoring and a system reset function in the event the power sags below an acceptable level for the system to operate reliably. The reset threshold incorporates a typical hysteresis of 50 mV to prevent erratic reasserts from being generated. An internal delay time circuit provides a adjustable power-on reset delay of typically 200 μs to 200 ms using an external capacitor.

The output of the NE56632-XX utilizes an open collector topology, which requires an external pull-up resistor to $V_{CC}$. Though this may be regarded as a disadvantage, it is advantageous in many sensitive applications. Because the open collector output cannot source reset current when both are operated from a common supply, the NE56632-XX offers a safe interconnect to a wide variety of microprocessors.

The NE56632-XX operates at low supply currents, typically 3 μA, while offering precision threshold detection (±1.5%).

Figure 22 is a functional block diagram of the NE56632-XX. The internal reference source voltage, $V_{REF}$, is typically 0.65 V over the temperature range. The reference voltage is connected to the non-inverting inputs of the threshold Comparator 1 and Comparator 2, while the inverting input of Comparator 1 monitors the supply voltage through a voltage divider (R1 and R2). The output of the comparator drives the series base resistor, R3 of a common emitter amplifier, Q1. The collector of Q1 is connected to the inverting terminal of Comparator 2. The output of Comparator 2 is connected to the series base resistor, R4 of the output common emitter transistor, Q2. The open collector output of Q2 provides the reset output.

The Delay Time Control is outputted at the junction of the collector of Q1 and the inverting input of Comparator 2. The reset release time delay, $t_{PLH}$ is set with an external capacitor. Figures 25 and 26 show $t_{PLH}$ as a function of the external delay capacitor, $C_D$.

When the supply voltage sags to the threshold detection voltage, the resistor divider network supplies a voltage to the inverting terminal of the threshold comparator which is less than $V_{REF}$, causing the output of the comparator to go to a HIGH state. This causes the common emitter amplifier, Q1 to turn ON pulling down the non-inverting terminal of Comparator 2 which causes its output to go to a HIGH state. This HIGH output level turns on the output common emitter transistor, Q2. The collector output of Q2 is pulled LOW through the external pull-up resistor, thereby asserting the Active-LOW reset.

Threshold hysteresis is established by turning on the bipolar common emitter transistor, Q1 when the input threshold Comparator 1 goes to a HIGH state. This occurs when $V_{CC}$ sags to or below the threshold level. With the output of Q1 connected to the non-inverting terminal of Comparator 2, the non-inverting terminal has a level near ground at about 0.4 V when the reset is asserted (Active-LOW). For the Comparator 2 to reverse its output, the Comparator 1 output and Q1 must overcome the additional pull-down voltage present on the inverting input of Comparator 2. The differential voltage required to do this establishes the hysteresis voltage of the sensed threshold voltage. Typically, it is 50 mV.

When $V_{CC}$ sags, and it is below the detection Threshold ($V_{SL}$), the device will assert a Reset LOW output at or near ground potential. As $V_{CC}$ rises from ($V_{CC} < V_{SL}$) to $V_{SH}$ or higher, the Reset is released and the output follows $V_{CC}$. Conversely, decreases in $V_{CC}$ from ($V_{CC} > V_{SL}$) to $V_{SL}$ will cause the output to be pulled to ground.

Hysteresis voltage = Release voltage – Detection Threshold voltage

$$V_{hys} = V_{SH} - V_{SL}$$

where:

$$V_{SH} = V_{SL} + V_{hys}$$
$$V_{SL} = V_{SH} - V_{hys}$$

When $V_{CC}$ drops below the minimum operating voltage, typically 0.65 V, the output is undefined and the output reset low assertion is no longer guaranteed. At this level of $V_{CC}$ the output will try to rise to $V_{CC}$. As $V_{CC}$ drops even further to zero, $V_{OUT}$ reset also goes to zero.

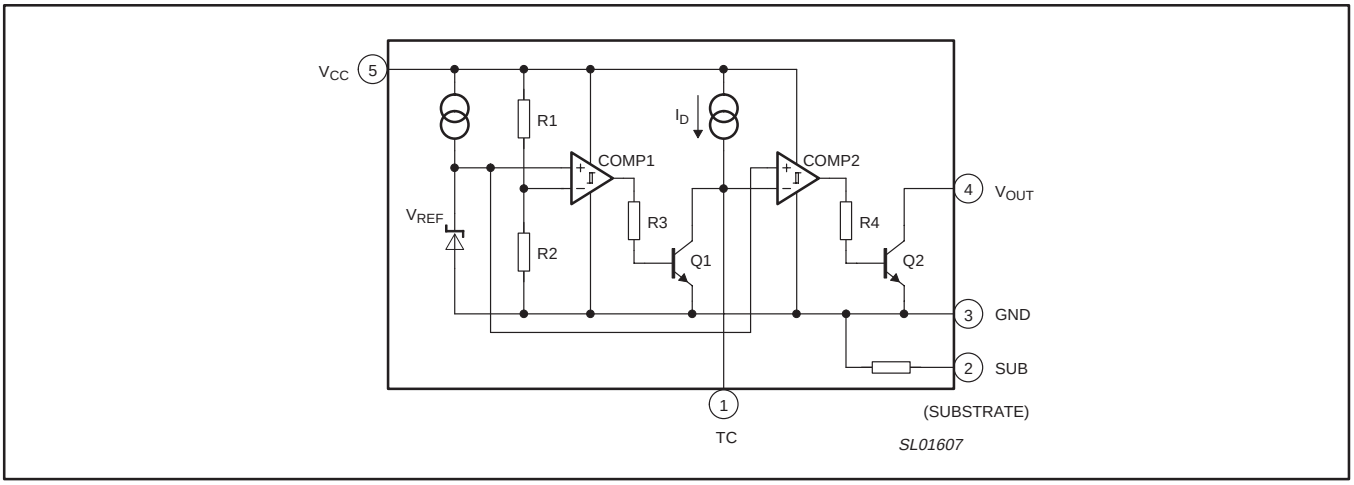



**Figure 22. Functional diagram.**

## TIMING DIAGRAM

The timing diagram in Figure 23 depicts the operation of the device. Letters A–N on the TIME axis indicates specific events.

**A:** At "A", $V_{CC}$ begins to increase. Also the $V_{OUT}$ voltage initially increases but abruptly decreases when $V_{CC}$ reaches the level (approximately 0.65 V) that activates the internal bias circuitry and $\overline{\text{RESET}}$ is asserted.

**B:** At "B", $V_{CC}$ reaches the threshold level of $V_{SH}$. At this point the delay time, $t_{PLH}$ is initiated while $V_{CC}$ rises above $V_{SH}$ to its normal operating level. The $V_{OUT}$ voltage remains in a low voltage state.

**C:** At "C", $V_{CC}$ is above $V_{SL}$ and the delay time elapses. At this instant, the IC releases the hold on the $V_{OUT}$ reset. The reset output then goes HIGH (assuming the reset pull-up resistor $R_{PU}$ is connected to $V_{CC}$). In a microprocessor based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

**D-E:** At "D", $V_{CC}$ begins to fall, causing $V_{OUT}$ to follow. $V_{CC}$ continues to fall until the $V_{SL}$ undervoltage detection threshold is reached at "E". This causes a reset signal to be generated ($V_{OUT}$ goes LOW).

**E-F:** Between "E" and "F", $V_{CC}$ continues to fall and then starts rising.

**F:** At "F", $V_{CC}$ rises to the $V_{SH}$ level. Once again, the device initiates the delay timer.

**F-G:** $V_{CC}$ rises above $V_{SH}$ and returns to normal. At "G", the delay ($t_{PLH}$) times out and once again, then it releases the hold on the $V_{OUT}$ reset.

**G-H:** At "G", $V_{CC}$ is above the upper threshold and begins to fall, causing $V_{OUT}$ to follow it. As long as $V_{CC}$ remains above the $V_{SH}$, no reset signal will be generated.

**H:** At event "H", $V_{CC}$ falls until the $V_{SL}$ undervoltage detection threshold is reached. At this level, a $\overline{\text{RESET}}$ signal is generated and $V_{OUT}$ goes LOW.

**H-I:** Between "H" and "I", $V_{CC}$ continues to fall and then starts to rise rising. $V_{CC}$ rises to the $V_{SH}$ level at "I", where the delay time is again initiated.

**I-J:** Between "I" and "J", $V_{CC}$ rises above $V_{SH}$ to $V_{CC}$ normal and then falls back to $V_{SL}$ level at "J". At "J", the reset signal is reasserted before the delay time has elapsed. The time between "I" and "J" is less than $t_{PLH}$ (reset delay time). Thus, the reset is not released and the reset output remains LOW.

**K–L:** Between "K" and "L", $V_{CC}$ rises again back to normal operating level causing the reset delay to be initiated at "K" and the reset to be released at "L".

**M:** At "M", $V_{CC}$ falls to $V_{SL}$ where the reset is asserted ($V_{OUT}$ Reset goes LOW).

**N:** At "N", the $V_{CC}$ voltage has decreased until normal internal circuit bias is unable to maintain a $V_{OUT}$ reset. As a result, $V_{CC}$ may rise to less than 0.65 V. As $V_{CC}$ decreases further, the $V_{OUT}$ reset also decreases to zero.

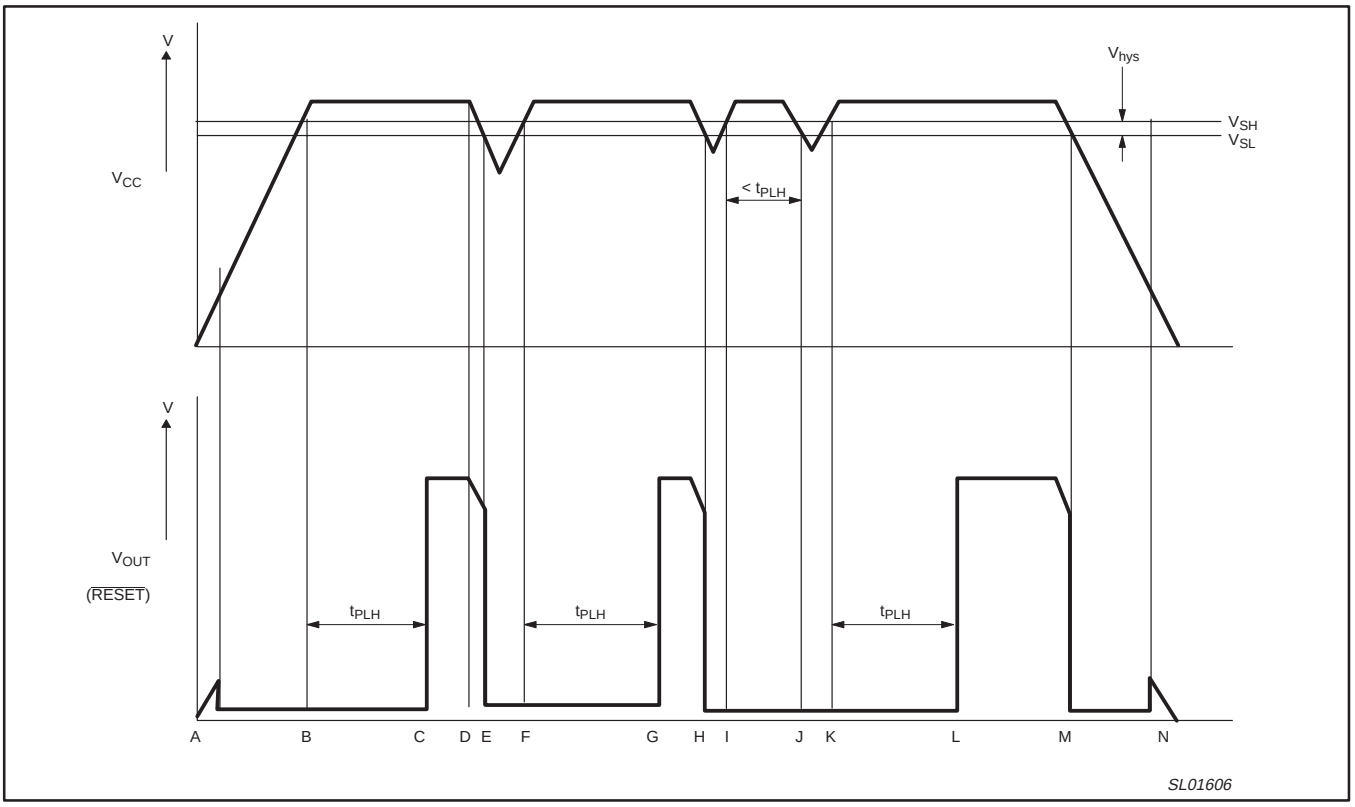



**Figure 23. Timing diagram.**

## APPLICATION INFORMATION

A typical application circuit for the NE56632-XX is shown in Figure 24. Note that a pull-up resistor, $R_{PU}$ is necessary since the output is an open collector. The value of RPU is calculated by the following expression.

$$R_{PU} \geq (V_{CC} - V_{\overline{RESET}}) / I_{OL}$$

where:

$V_{CC} = V_{S(min)} - 0.05$ V (for a 3 V reset this is 2.905 V)

$V_{\overline{RESET}} = 0.4$ V (this is $V_{OL(max)}$)

$I_{OL} = 5$ mA; minimum output current at $T_{amb} = 25$ °C

Substituting these values into the expression and calculating, finds $R_{PU}$ should be greater than or equal to 510 Ω. To ensure that the Active-LOW level is sufficient, a value of 4.7 kΩ is chosen in the test and application examples.

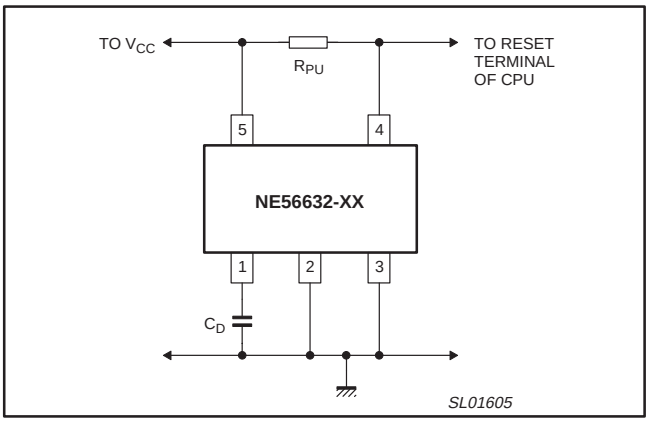



**Figure 24. Typical application.**

Figure 25 (NE56632-20 $C_D$ versus $t_{PLH}$) and Figure 26 (NE56632-44 $C_D$ versus $t_{PLH}$) show how $t_{PHL}$, the "H" transmission delay or reset release delay time varies as a function of the external delay capacitance, $C_D$. From Figure 26, typical range of the delay capacitance is 1 pF to 10 nF which yields typical delays from 200 µs to 200 ms.

The following formula can be used to find the approximate delay time based on external delay capacitance, $C_D$ and the delay time coefficient, d shown in Table 2.

$$t_{PLH}\ (ms) \approx C_D\ (\mu F) \times d$$

For example, a NE56632-44 using an external capacitor, $C_D$ = 1 nF = 1000 pF yields:

$$t_{PLH}\ (ms) \approx (1 \times 10^{-3})\ (1.85 \times 10^4) \approx 18.5\ ms$$

Compare this to the value of $t_{PLH} \approx 17$ ms for $C_D$ = 1000 pF that is extracted from Figure 26.

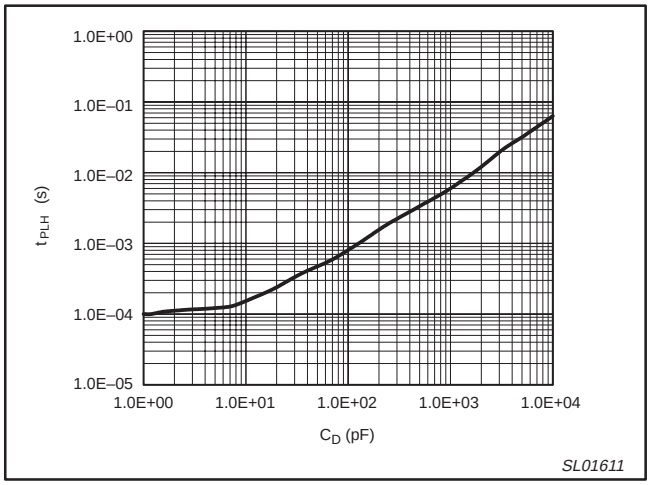



**Figure 25. NE56632-20 $C_D$ versus $t_{PLH}$ characteristics.**

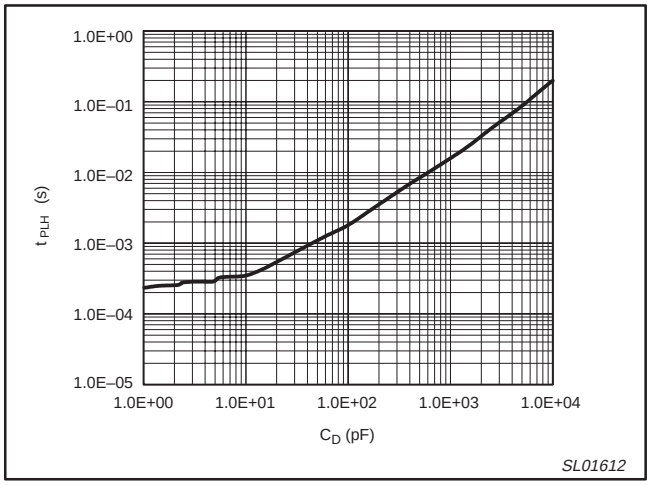



**Figure 26. NE56632-44 $C_D$ versus $t_{PLH}$ characteristics.**

**Table 2. Delay time coefficient**

| Device | d |
|---|---|
| NE56632–46 | $1.95 \times 10^4$ |
| NE56632–45 | $1.90 \times 10^4$ |
| NE56632–44 | $1.85 \times 10^4$ |
| NE56632–43 | $1.80 \times 10^4$ |
| NE56632–42 | $1.75 \times 10^4$ |
| NE56632–31 | $1.20 \times 10^4$ |
| NE56632–30 | $1.15 \times 10^4$ |
| NE56632–29 | $1.10 \times 10^4$ |
| NE56632–28 | $1.05 \times 10^4$ |
| NE56632–27 | $1.00 \times 10^4$ |
| NE56632–20 | $0.65 \times 10^4$ |
| NE56632–19 | $0.60 \times 10^4$ |

## TEST CIRCUITS

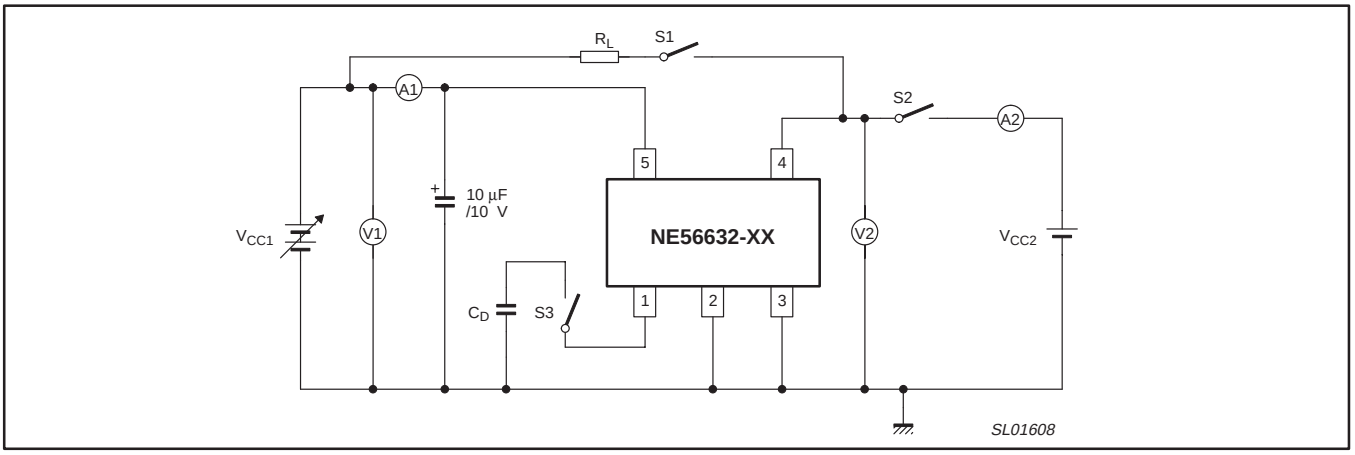



**Figure 27. Test circuit 1.**

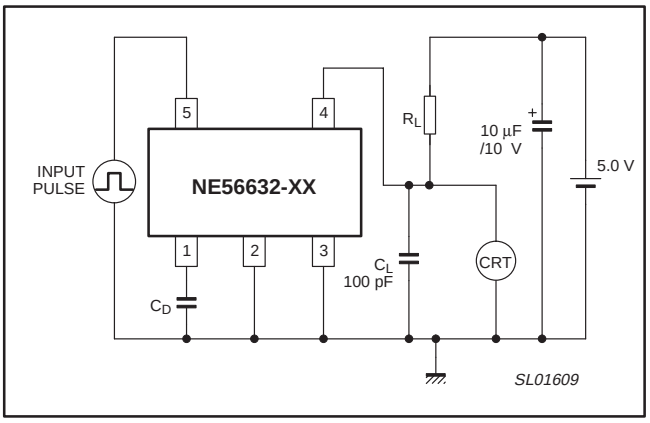



**Figure 28. Test circuit 2.**

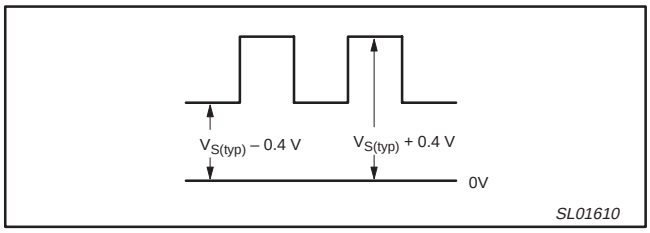



**Figure 29. Input pulse.**

**NOTES:**
A = DC amperemeter
V = DC voltmeter
CRT = oscilloscope

## PACKING METHOD

The NE56632-XX is packed in reels, as shown in Figure 30.

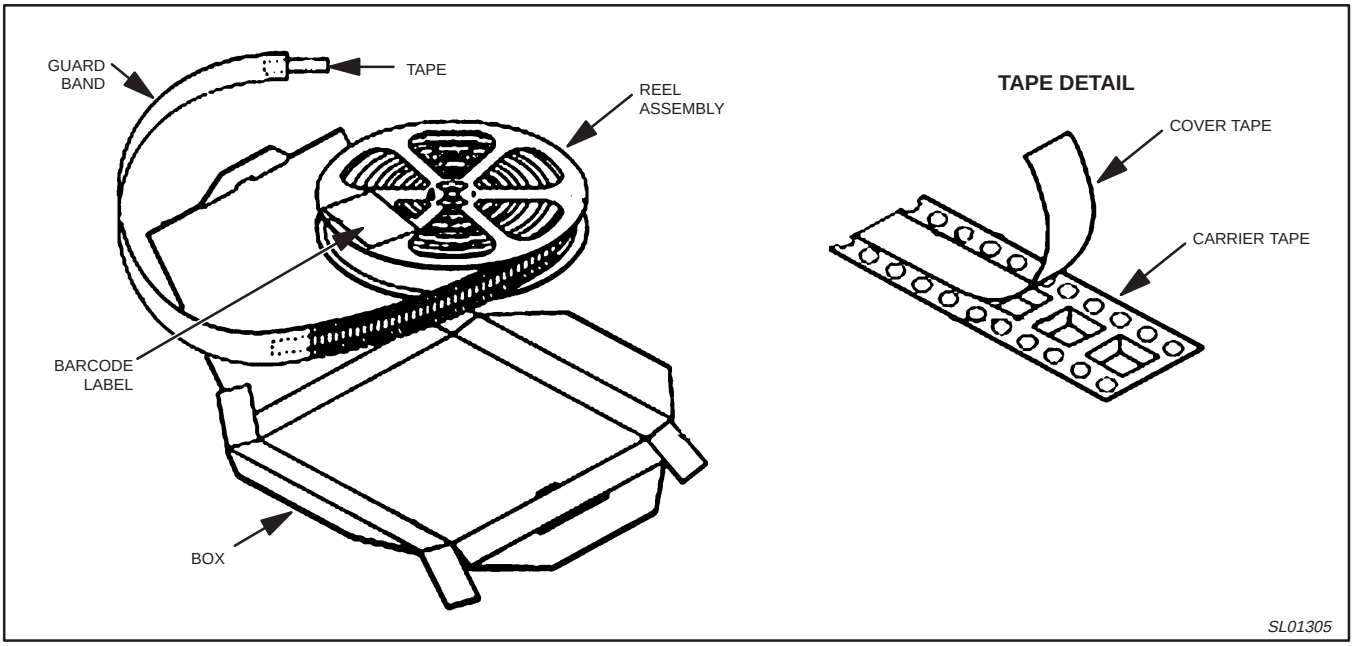
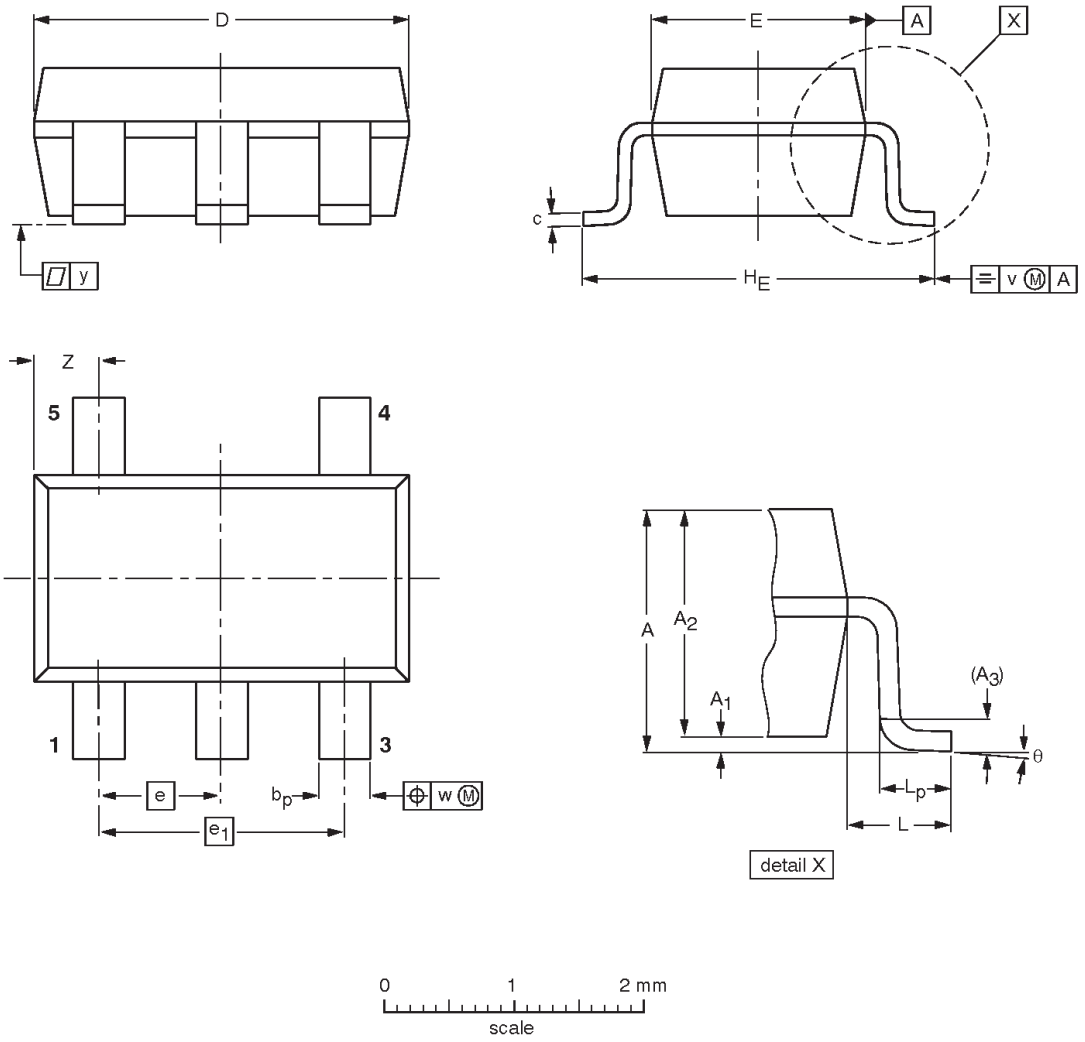



**Figure 30. Tape and reel packing method.**

**SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | $H_E$ | L | $L_p$ | | | y | | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.35 | 0.05<br>0.15 | 1.2<br>1.0 | 0.025 | 0.55<br>0.41 | 0.22<br>0.08 | 3.00<br>2.70 | 1.70<br>1.50 | 0.95 | 1.90 | 3.00<br>2.60 | 0.60 | 0.55<br>0.35 | | | 0.1 | | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | |
|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | |
| | | MO-178 | | |

**NOTES**

## Data sheet status

| Data sheet status [1] | Product status [2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information please visit
**http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
**sales.addresses@www.semiconductors.philips.com**.



Date of release: 08-02

Document order number: 9397 750 10239

Let's make things better.

**Philips Semiconductors**

PHILIPS