INTEGRATED CIRCUITS

DATA SHEET

74ALVCH16601
18-bit universal bus transceiver (3-State)

Product specification
Supersedes data of 1998 Aug 31
IC24 Data Handbook

1998 Sep 24

Philips
Semiconductors

PHILIPS

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Current drive ± 24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16601 is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$ and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock (CP_{AB} and CP_{BA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if CP_{AB} is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CP_{AB}. When $\overline{OE}_{AB}$ is Low, the outputs are active. When $\overline{OE}_{AB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CE}_{BA}$/$\overline{CE}_{AB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, LE_{BA} and CP_{BA}.

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ and $\overline{OE}_{AB}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

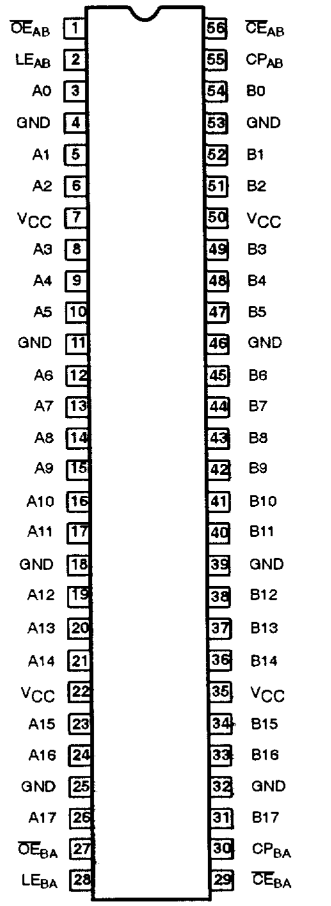
SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.1 2.8	ns
$C_{I/O}$	Input/Output capacitance			8.0	pF
C_I	Input capacitance			4.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	21	pF
			Outputs disabled	3	

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

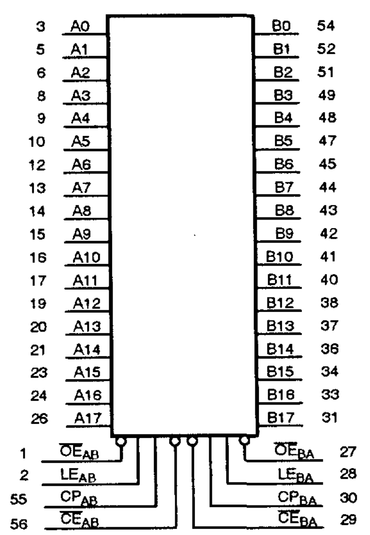
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16601 DGG	SOT364-1

PIN CONFIGURATION



SW00129

LOGIC SYMBOL

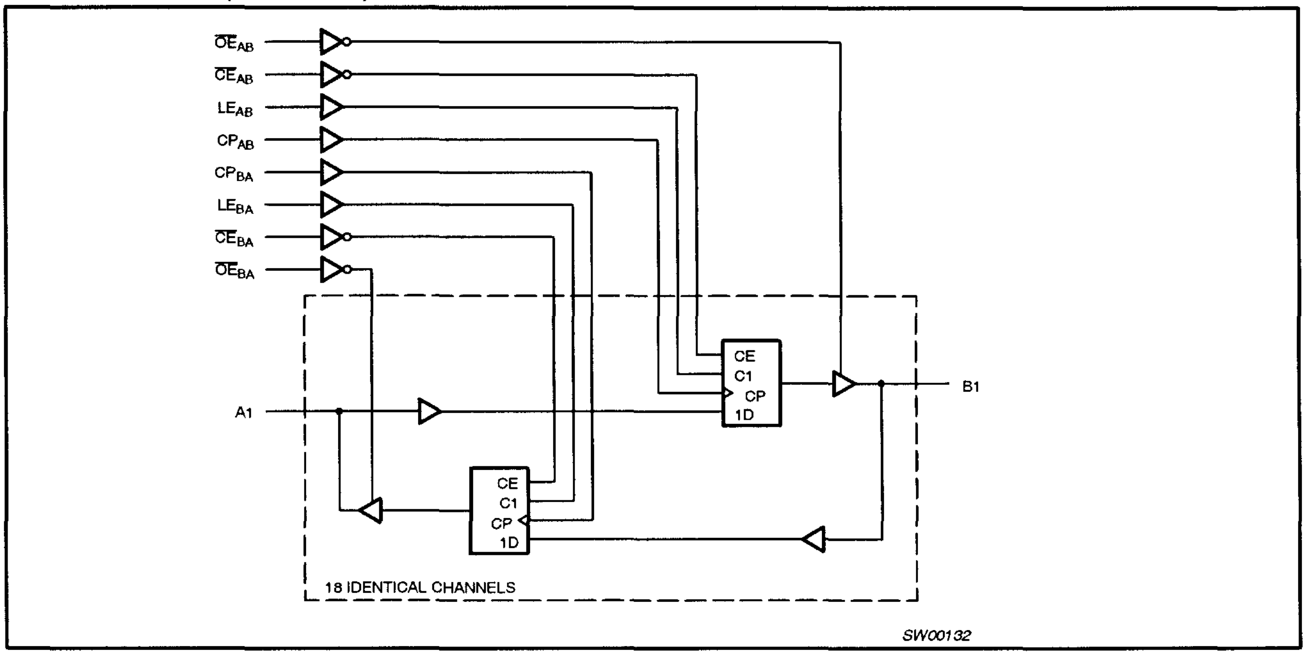


SW00130

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	CP_{BA}	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	CP_{AB}	Clock input A-to-B
56	$\overline{CE}_{AB}$	Clock enable A-to-B

LOGIC DIAGRAM (one section)

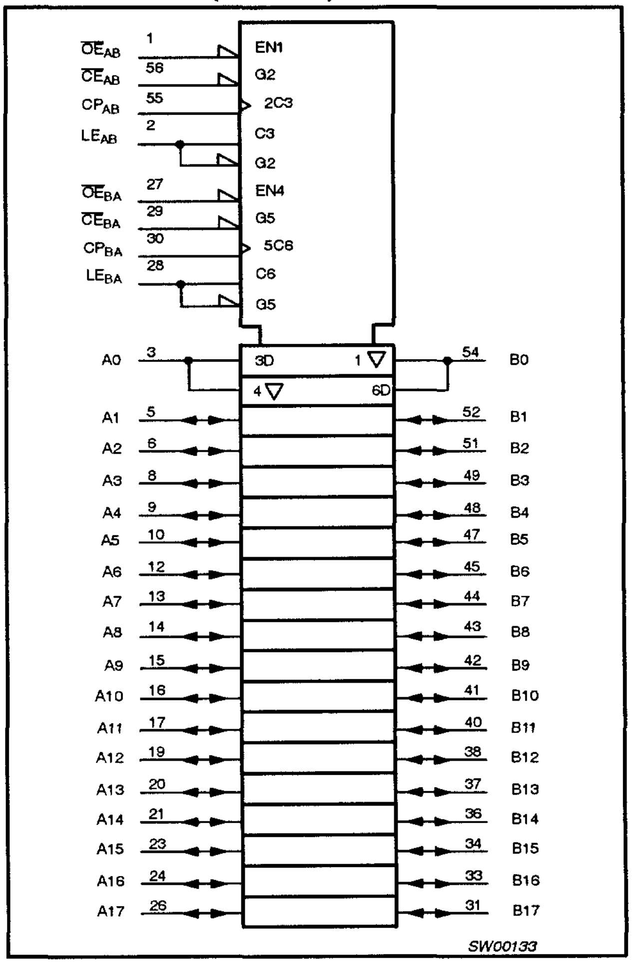


FUNCTION TABLE

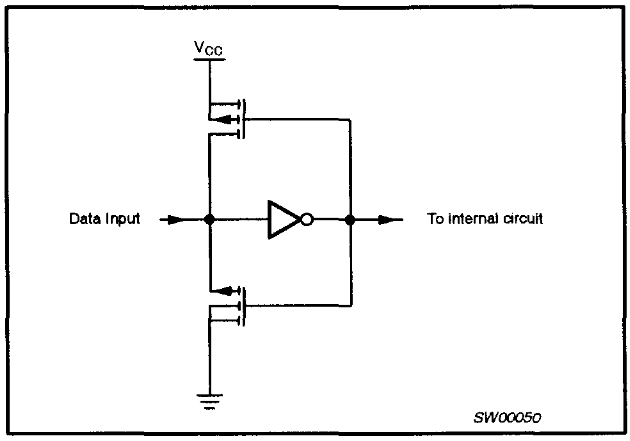
INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	CP_{XX}	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparent
H	L	L	X	X	NC	Hold
L L	L L	L L	↑ ↑	h l	H L	Clock + display
L L	L L	L L	L H	X X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
l = LOW state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I <0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	± 50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = −100μA	V_{CC} − 0.2	V_{CC}		V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = −6mA	V_{CC}−0.3	V_{CC}−0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC}−0.6	V_{CC}−0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC}−0.5	V_{CC}−0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC}−0.6	V_{CC}−0.09		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 1.0	V_{CC}−0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100μA		GND	0.20	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND		0.1	5	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	μA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	μA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; V_I = V_{CC} − 0.6V; I_O = 0		150	750	μA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		μA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	−45			μA
		V_{CC} = 3.0V; V_I = 2.0V[2]	−75	−175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			μA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	−500			μA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ± 0.2V MIN	TYP[1]	MAX	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	1, 2	1.0	3.1	5.2	ns
	Propagation delay LE_{AB}, LE_{BA} to Bn, An		1.0	3.6	6.2	
	Propagation delay CP_{AB}, CP_{BA} to Bn, An		1.0	3.4	5.9	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_{BA}$, OE_{AB} to An,Bn	3	1.1	3.1	5.3	ns
t_{PHZ}/t_{PLZ}	3-State output enable time $\overline{OE}_{BA}$, OE_{AB} to An,Bn	3	1.4	2.8	4.9	ns
t_W	Pulse width HIGH LE_{AB} or LE_{BA}	2	3.3	1.6	–	ns
	Pulse width HIGH or LOW CP_{AB}, CP_{BA}		3.3	2.0	–	
t_{SU}	Set-up time An, Bn to CP_{AB}, CP_{BA}	4	2.3	–0.2	–	ns
	Set-up time An, Bn to LE_{AB}, LE_{BA}		1.3	0.1	–	
	Set-up time CE_{AB}, CE_{BA} to CP_{AB}, CP_{BA}		2.0	–0.4	–	
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	4	1.2	0.3	–	ns
	Hold time An, Bn to LE_{AB}, LE_{BA}		1.3	0.2	–	
	Hold time CE_{AB}, CE_{BA} to CP_{AB}, CP_{BA}		1.1	0.4	–	
f_{MAX}	Maximum clock frequency		150	390	–	MHz

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	1, 2	1.0	2.8	4.2		3.1	4.7	ns
	Propagation delay LE_{AB}, LE_{BA} to Bn, An		1.0	3.1	4.9		3.4	5.4	
	Propagation delay CP_{AB}, CP_{BA} to Bn, An		1.3	3.1	5.0		3.5	5.8	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An	3	1.1	2.8	5.2		3.3	6.1	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}_{BA}$ to An	3	1.2	3.2	4.4		3.3	4.8	ns
t_W	LE pulse width LE_{AB}, LE_{BA} to CP_{AB}, CP_{BA}	2	3.3	0.9		3.3	0.7		ns
	LE pulse width HIGH or LOW CP_{AB}, CP_{BA}		3.3	0.9		3.3	1.2		
t_{SU}	Set-up time An, Bn to CP_{AB}, CP_{BA}	4	2.1	–0.2		2.4	0.0		ns
	Set-up time An, Bn to LE_{AB}, LE_{BA}		1.1	0.3		1.2	–0.2		
	Set-up time CE_{AB}, CE_{BA} to CP_{AB}, CP_{BA}		1.7	–0.2		2.0	–0.7		
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	4	1.0	–0.1		1.1	0.3		ns
	Hold time An, Bn to LE_{AB}, LE_{BA}		1.4	0.1		1.6	0.1		
	Hold time CE_{AB}, CE_{BA} to CP_{AB}, CP_{BA}		1.1	0.4		1.2	0.6		
f_{MAX}	Maximum clock frequency		150	340		150	333		MHz

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

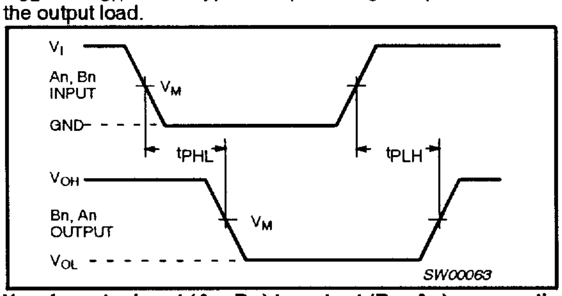
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

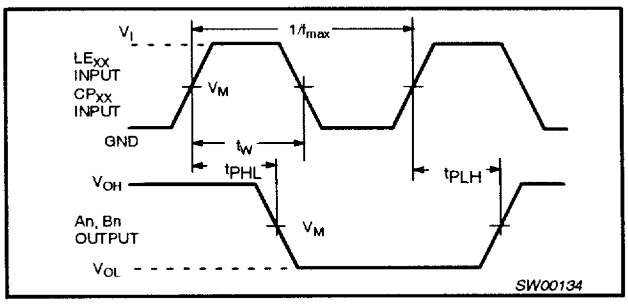
1. $V_M = 0.5$ V
2. $V_X = V_{OL} + 0.15V$
3. $V_Y = V_{OH} - 0.15V$
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

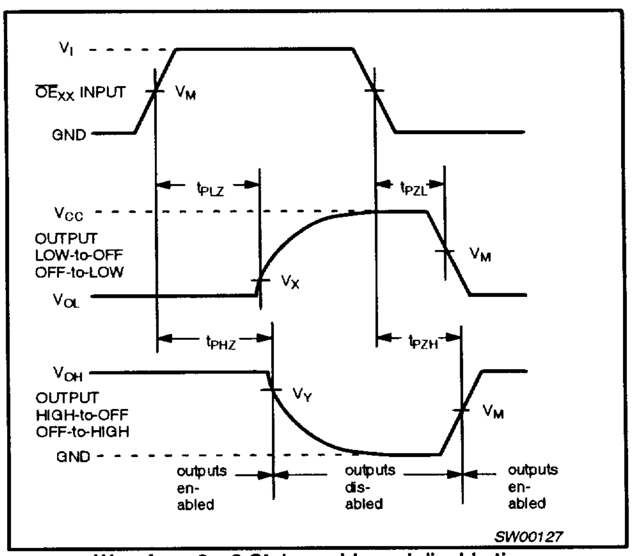
1. $V_M = 1.5$ V
2. $V_X = V_{OL} + 0.3V$
3. $V_Y = V_{OH} - 0.3V$
4. $V_I = 2.7$ V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



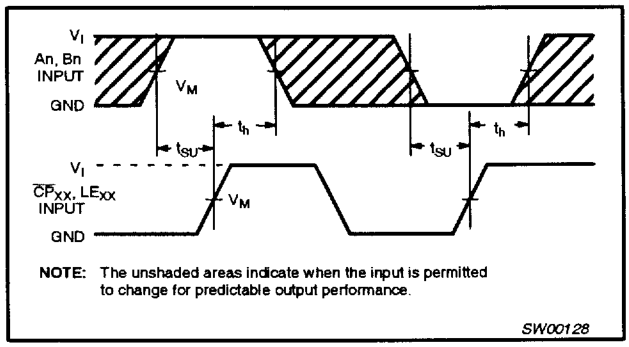
Waveform 1. Input (An, Bn) to output (Bn, An) propagation delays



Waveform 2. Latch enable input (LE_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width

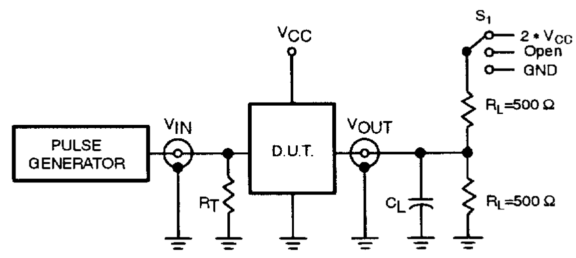


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{BA} inputs

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

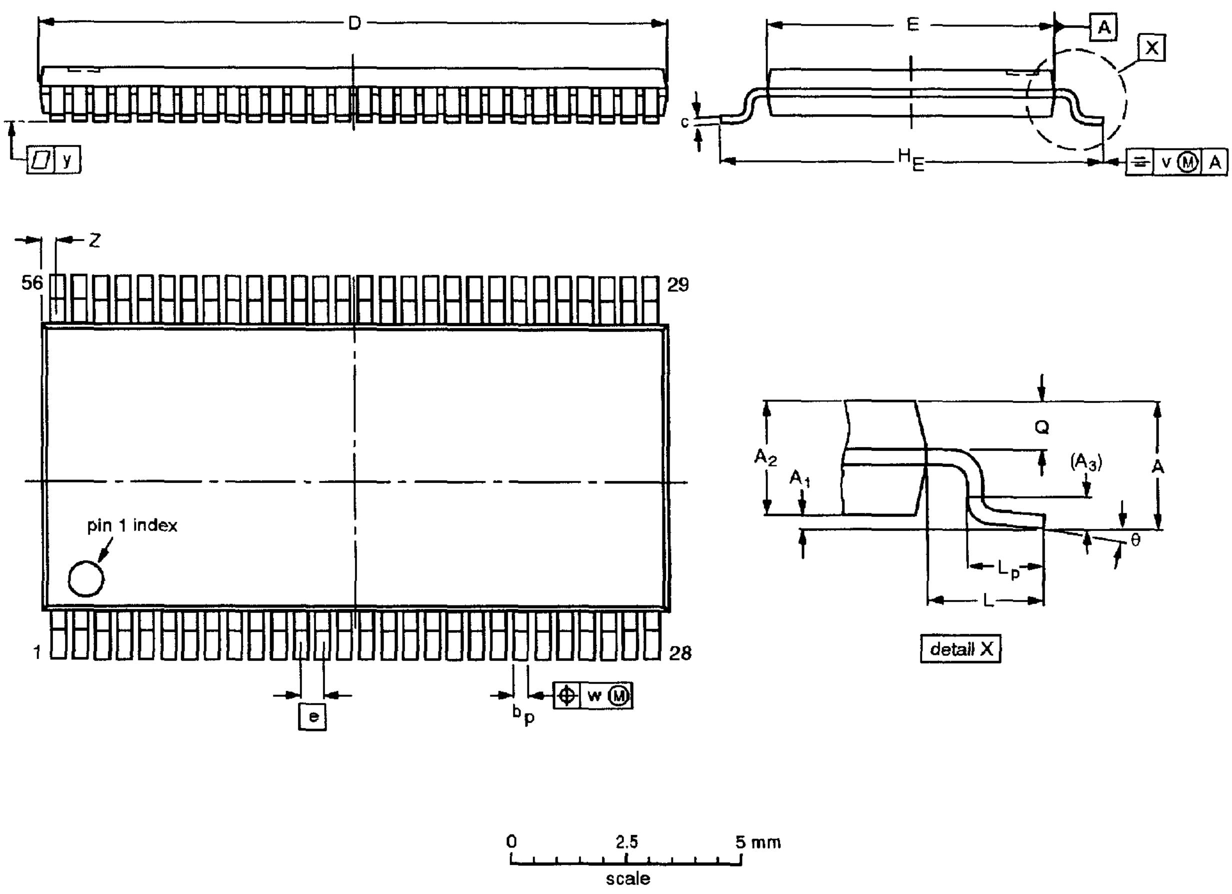
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Load circuitry for switching times

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				~~93-02-03~~ 95-02-10

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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Product Information

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General Description	Features	Applications	Datasheet
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Products & packages	Parametrics	Similar	

Description

The 74ALVCH16601 is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OE_{AB} and OE_{BA})latch enable (LE_{AB} and LE_{BA}) , and clock (CP_{AB} and CP_{BA}) inputs. For A-to-B data flowthe device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if CP_{AB} is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CP_{AB}. When OE_{AB} is Low, the outputs are active. When OE_{AB} is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs (CE_{BA} /CE_{AB}).

Data flow for B-to-A is similar to that of A-to-B but uses $OE_{BA}LE_{BA}$ and CP_{BA}.

To ensure the high impedance state during power up or power down, OE_{BA} and OE_{AB} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Features

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Current drive ± 24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C

Applications

Ground And VCC Bounce Of High-Speed Integrated Circuits (date 01-Jan-93)
Interfacing 3 Volt and 5 Volt Applications
Live Insertion Aspects of Philips Logic Families (date 22-Jul-99)
Hardware and software verification procedure (date 07-Oct-98)

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74ALVCH16601	18-bit universal bus transceiver (3-State)	24-Sep-98	Product Specification	12	96	Download

Products, packages, availability and ordering

Type number	North American Type number	Order code (12nc)	marking/packing IC packing info	package	device status	buy online
74ALVCH16601DGG	74ALVCH16601DG	9352 625 46112	Standard Marking * Tube	SOT364-1 (TSSOP56)	Full production	order this -
	74ALVCH16601DG-T	9352 625 46118	Standard Marking * Reel Pack, SMD, 13"	SOT364-1 (TSSOP56)	Full production	order this -

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Support & tools

CMOS 16-bit microcontroller family(date 01-May-98)

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