

DATA SHEET

74F14

Hex inverter Schmitt trigger

Product specification

1990 Nov 26

IC15 Data Handbook

Hex inverter Schmitt trigger

74F14

FEATURE

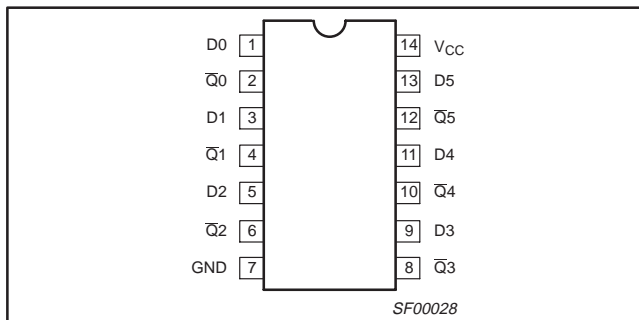
- Industrial temperature range available (−40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F14	5.0ns	18mA

DESCRIPTION

The 74F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going input threshold (typically 800mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V _{CC} = 5V ±10%, T _{amb} = 0°C to +70°C	INDUSTRIAL RANGE V _{CC} = 5V ±10%, T _{amb} = −40°C to +85°C	
14-pin plastic DIP	N74F14N	I74F14N	SOT27-1
14-pin plastic SO	N74F14D	I74F14D	SOT108-1

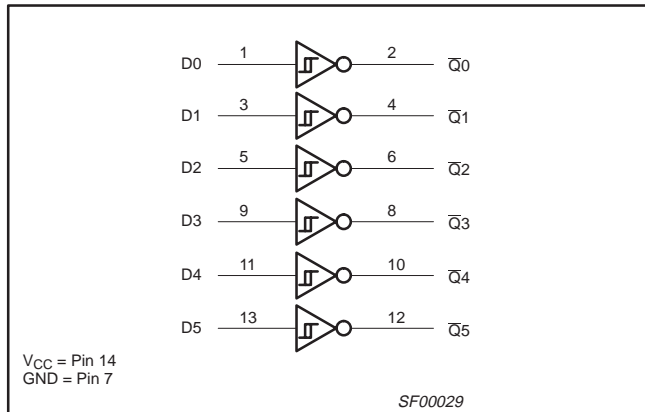
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D _n	Data inputs	1.0/1.0	20µA/0.6mA
Q _n	Data output	50/33	1.0mA/20mA

NOTE:

1 One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUT
D _n	Q _n
L	H
H	L

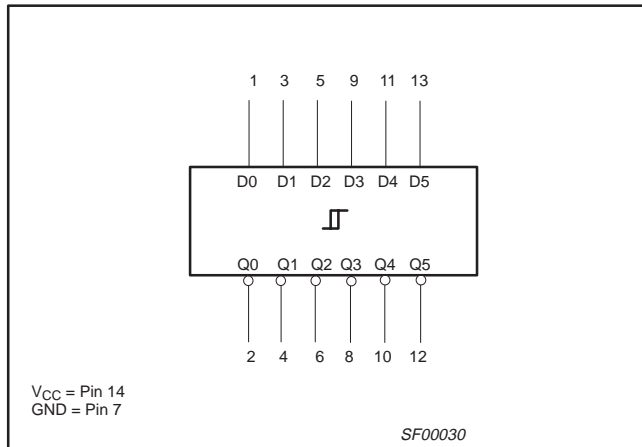
NOTES:

- H = High voltage level
- L = Low voltage level

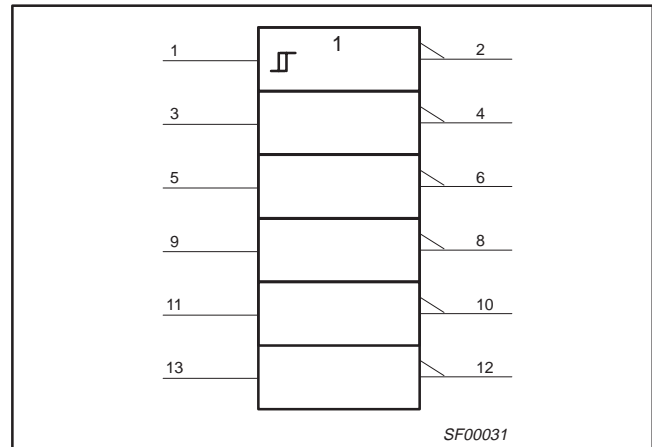
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LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT	
V _{CC}	Supply voltage		-0.5 to +7.0	V	
V _{IN}	Input voltage		-0.5 to +7.0	V	
I _{IN}	Input current		-30 to +5	mA	
V _{OUT}	Voltage applied to output in high output state		-0.5 to V _{CC}	V	
I _{OUT}	Current applied to output in low output state		40	mA	
T _{amb}	Operating free-air temperature range		Commercial range	0 to +70	°C
			Industrial range	-40 to +85	°C
T _{stg}	Storage temperature range		-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT	
		MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{IH}	High-level input voltage	2.0			V	
V _{IL}	Low-level input voltage			0.8	V	
I _{IK}	Input clamp current			-18	mA	
I _{OH}	High-level output current			-1	mA	
I _{OL}	Low-level output current			20	mA	
T _{amb}	Operating free air temperature range		Commercial range	0	+70	°C
			Industrial range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			MIN	TYP ²	MAX		
V_{T+}	Positive-going threshold	$V_{CC} = 5.0V$	1.4	1.7	2.0	V	
V_{T-}	Negative-going threshold	$V_{CC} = 5.0V$	0.7	0.9	1.1	V	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5.0V$	0.4	0.8		V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_I = V_{T-\text{MIN}}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V	
			$\pm 5\%V_{CC}$	2.7	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_I = V_{T+\text{MAX}}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	0.50	V
			$\pm 5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_{T+}	Input current at positive-going threshold	$V_{CC} = 5.0V, V_I = V_{T+}$		0		μA	
I_{T-}	Input current at negative-going threshold	$V_{CC} = 5.0V, V_I = V_{T-}$		-175		μA	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-60		-150	mA	
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$	$V_{IN} = \text{GND}$	13	22	mA
		I_{CCL}	$V_{CC} = \text{MAX}$	$V_{IN} = 4.5V$	23	32	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ C$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

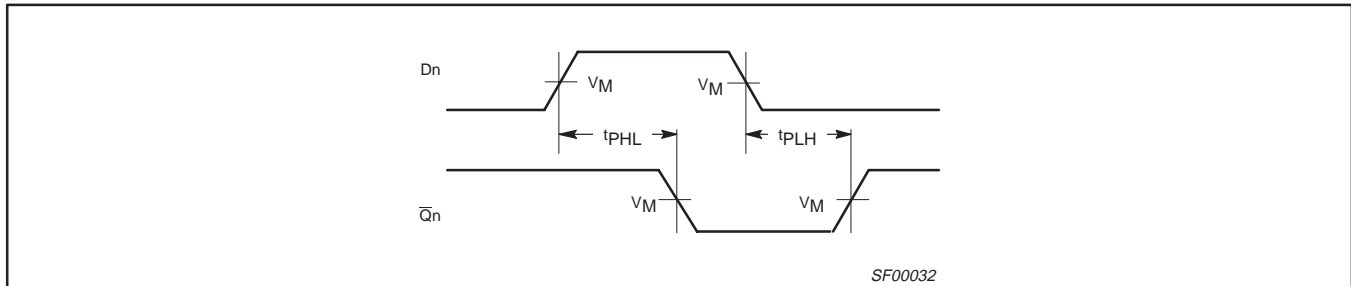
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$V_{CC} = +5.0V$ $T_{amb} = +25^\circ C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^\circ C \text{ to } +70^\circ C$ $C_L = 50pF, R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = -40^\circ C \text{ to } +85^\circ C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t_{PLH} t_{PHL}	Propagation delay Dn to $\bar{Q}n$	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	3.0 3.5	10.5 9.0	ns

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AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs

NOTE:

For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Totem-Pole Outputs

The circuit consists of a PULSE GENERATOR connected to the input V_{IN} of a D.U.T. (Device Under Test). The input V_{IN} is terminated with a resistor R_T to ground. The output V_{OUT} is connected to a load consisting of a capacitor C_L and a resistor R_L in parallel, which is also terminated to ground. The supply voltage V_{CC} is connected to the D.U.T.

Input Pulse Definition

The waveforms show the input pulse characteristics. For a NEGATIVE PULSE, the signal transitions from 90% V_M to 10% V_M and back. The pulse width t_w is defined between the 50% V_M points. The rise time t_{TLH} (t_r) is the time from 10% V_M to 90% V_M. The fall time t_{THL} (t_f) is the time from 90% V_M to 10% V_M. For a POSITIVE PULSE, the signal transitions from 10% V_M to 90% V_M and back. The definitions for t_w, t_{TLH} (t_r), and t_{THL} (t_f) are similar.

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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