PN5190B1

NFC Frontend

Rev. 4.3 — 11 May 2026 Product data sheet

1 General description

This document describes the functionality and electrical specification of the high-power NFC-IC PN5190B1, silicon version B1, using firmware or V2.0 or higher.

Additional documents supporting a design-in of the PN5190B1 are available from NXP, this additional design-in information is not part of this document.

The PN5190B1 supports highly innovative and unique features, which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

The independence of real-time host controller interactions makes this product a good fit for systems, which operate a preemptive multitasking OS like Linux or Android.

In this document, the term „MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Plus, MIFARE Ultralight, or MIFARE DESFire product family.

2 Features and benefits

2.1 RF functionality

- As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this NFC frontend IC utilizes a modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.
  PN5190B1 supports communication with all products of the MIFARE product-based card family including MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2, and MIFARE Plus cards CRYPTO implemented in hardware for R/W of all NXP MIFARE product-based cards (includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE products).
  The PN5190B1 frontend IC supports the following RF operating modes:

2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kBit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kBit/s and 424 kBit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
- Proprietary data rates based on ISO/IEC15693 with 106 kbit and 212 kbit/s (for NXP NTAG 5 communication)

2.1.7 ISO/IEC 18000-3 Mode 3

- Reader/writer mode supporting ISO/IEC 18000-3 Mode 3

2.1.8 ISO/IEC 18092

- ISO/IEC 18092 (NFC-IP1)

2.1.9 ISO/IEC 21481

- ISO/IEC 21481 (NFC-IP-2)

2.1.10 Peer to peer

- P2P Passive 106 kbit/s TO 424 kbit/s, initiator and target

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- P2P Active 106 kbit/s TO 424 kbit/s, initiator and target
- Proprietary passive communication for type A up to 848 kbit/s
- Functionality according to ISO/IEC 21481 (NFC-IP-2)

2.1.11 Card emulation

- ISO/IEC4443-A card mode from 106 kbit/s up to 848 kbit/s (PICC) with active load modulation for increased communication range.

2.2 Host interface

- One host interface based on SPI is implemented:
  - SPI interface with data rates up to 15 Mbit/s with MOSI, MISO, NSS, and SCK signals
  - Interrupt request line to inform host controller on events
  - Independent TX and RX buffer for RF data with size of 1024 bytes each

2.3 Integrated DC-DC

- The PN5190B1 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.
  A single supply concept for the RF system, e.g. with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.
  The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.
  The usage of the DC-DC is optional.
  For applications making use of the low-power card detection, the DC-DC is available. For applications using the ultra low-power card detection (ULPCD), the DC-DC cannot be used.

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3 Applications

- Payment
- Physical access
- eGov

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4 Firmware versions

Firmware versions covered by this data sheet:

Version 2.00:

- This version cannot be replaced by FW versions using smaller version numbers (e.g. replacing FW2.0 by FW1.9 is not possible)
- This FW version is not available on volume production devices, but can be installed by the user
  Before using this firmware in Peer to Peer target mode, for better communication stability the EEPROM address 0x292 (default A6E813C**0**) shall be initialized with the value (A6E813C**1** - 0x292:0xC1 0x203: 0x13 0x294:0xE8 0x295:0xA6). This setting has no influence on reader or card emulation modes.

Version 2.01:

- This version is functionally equivalent to Version FW2.0 but offers updated EEPROM Settings compared to FW2.0
- This version cannot be replaced by FW versions using smaller version numbers (e.g. replacing FW2.1 by FW1.9 is not possible)
- This FW version is installed by default on volume production devices of PN5190 B1
- This FW and all upcoming FW versions use the EEPROM Setting at address 0x292 = A6E813C**1** to configure the Peer to Peer target mode for better communication stability.

Version 2.02:

- Skipped, not available

Version 2.03:

- This FW version is not available on volume production devices, but can be installed by the user
- The GPIO1 (general-purpose input/output) pin can be enabled to wake up an external DC-DC from power down for the VDDPA supply during LPCD.
- Updated Type-A 106 antenna-specific Protocol register settings for EMVCo to solve few EMVCo Card activation failures during fast card movement within the Field.
- PN5190 FW updated to handle SWITCH_MODE_NORMAL (Abort) scenarios even when Functional CMD and SWITCH_MODE_NORMAL CMD are sent to back within 10 microseconds
- Introduced a new DPC_CONFIG register to handle Dynamic Enable/Disable of DPC without depending on the DPC setting from EEPROM User Area.
- Card Mode (SWITCH_MODE_AUTOCOLL Command) support with Ultra Low-Power standby feature (in Autonomous mode with Standby mode) along with the existing Low-Power standby configuration using EEPROM settings.
- various updates to increase the configuration flexibility for FeliCa communication:
  - Updated PN5190 FW to indicate Length Error when received FeliCa response is greater than 28 Bytes when RX_MULTIPLE is Enabled
  - Updated PN5190 FW to indicate correct numbers of received bytes when RETRIEVE_RF_DATA is used to retrieve FeliCa response packets received when RX_MULTIPLE is Enabled.
  - Updated to fix the issue of EXCHANGE_RF_DATA returning with success even before Receiving RF Response on few ICs upon POR.
  - Updated PN5190 FW to clear all pending Interrupt Status bits before performing RF Exchange to fix TX Failure observed when FeliCa response is received around FDT timeout.

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– Added a new feature to extend RX Guard Timer in Integer multiple of ‘dwRXIRQ_GuardTime’ EEPROM timeout configuration to extend RX Guard Timeout beyond 1.048 sec.

Version 2.04:

Skipped, not available

Version 2.05:

- Xtal error during boot generates error event in boot status now
- New features:
  1. Extended CONFIGURE_TESTBUS_ANALOG
  2. New CONFIGURE_MULTIPLE_TESTBUS_DIGITAL
  3. New FastFieldOn bit in System Config register 0000h
- New registers added:
  1. TIMER0_OUTPUT
  2. TIMER1_OUTPUT
  3. TIMER2_CONFIG
  4. TIMER2_RELOAD
  5. TIMER2_OUTPUT
- Improved setting for DPC_GUARD_TIME (087h): The default setting changed from 0x64 to 0xFF

Version 2.06:

- Added a new command:GET_CRC_USER_AREA[0x29]: This command is used to calculate the CRC for the complete User area including the Protocol area. This command helps the user to ensure the integrity of the RF and analog settings by detecting manipulation of this area and eases the version control of dedicated configurations during development.
- Modified SOF timing: In this FW version, the protocol settings of Type B106 had been improved for the SOF / EOF timing, and by this provides better results during EMVCo L1 analog test.

Version 2.07:

- This version is available on the product programmed during production on product version PN5190B1.
- Fixed an issue where in commands UPDATE_RF_CONFIGRUATION and GET_RF_CONFIGURATION commands when used for TX index 0x0F (ISO180003m3_TARI_18.88us) and 0x10 (ISO180003m3_TARI_9.44us).
- Fixed an issue of not-restoring the analog TX settings when switching from reader mode to card mode. Removing of type-b detection during Autocoll. Supporting only Type-A and Type-F detection as part of an Autocoll procedure.
- Added a new EEPROM configuration: ENABLE_ULFO_TRIM_CALIBRATION (0xCEC).
- Deprecated the P2P active communication target mode functionality.

Version 2.08:

- Resolved a corner case issue of DPC not recovering to expected VDDPA regulation value during load change conditions.

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Version 2.09:

- Feature implemented DPR (Dynamic Power Regulation). Added new register DYNAMIC_POWERLEVEL_REG (Reg Addr: 0x64)
- Feature implemented LFO timing calibration using frequency meter for higher LPCD pulse interval accuracy. Added new EEprom setting LFO_TRIM_CALIBRATION (EEprom Addr.0xCED)
- Updated the DPC algorithm for higher control accuracy
- Updated command GET_CRC_USER_AREA (Command code: 0x29)

Version 2.0A:

- Added new LPCD command option which makes the IC enter LPCD mode and returns with an Autocoll Event if an external RF is detected.
  In SWITCH_MODE_LPCD (0x23) command, bControl field option LPCD_WITH_AUTOCOLL_EVENT (0x13) is added to support LPCD with Autocoll event when wake-up occurs due to load change/Ext RF from LPCD standby scenarios.
  Added a new EEPROM field to configure the time-out for Autocoll expiry:
  Name: LpcdWithAutocollExpiryInterval. Address Offset: 0xCEE Size: 1 Byte.
  Description: This field is the time before Autocoll expires when LPCD is used with Autocoll option. 1unit - 100 ms.
  The default is 10 ms.
- Added a new command CTS_FAST_CONFIGURE (0x2B) which both configures and enables CTS.
  For Enabling CTS, the Length should be 0x27 (including both Configs and Enabling bytes).
  This command cannot be used for disabling CTS.
  First fast Init+Configure takes about 50 ms, second time onwards about 50 µs.
- Added configuration to initialize the pullup/down state of SPI Pads (ATX Pins) in the secure flash init.
  This feature is disabled by default. Added the following EEPROM fields for reconfiguration of SPI pad configurations:
  Name: EnableHIFPadsReConfig. Address Offset: 0xCEF Size: 1 Byte.
  Description: Enable/Disable reconfiguration of the SPI Pads configuration.
  Name: SPIPadReConfig. Address Offset: 0xCF0 Size: 4 Bytes.
  Description: SPI Pads PullUp/Down Configuration.
- Fixed an issue which prevented exit from Autocoll in some scenarios, when external RF is removed.
- Fixed an issue that caused changes in amplitude of response during Host Card emulation, when higher VDDPA values are used in APC TX entries.

Version 2.0B:

- Fix for issue in the second MIFARE Classic authentication, seen only with a particular card and only when the coupling between card and reader is strong enough.
- Update in firmware to improve robustness during LPCD and Standby power modes.

Version 2.0D:

- Added Delay Feature to support scenarios where Standby entry is prevented when the Host is slow to deassert NSS.
  Delay Feature: Added a new EEPROM field to configure NSS time delay, how long to wait for NSS to go low while entering standby.
  Name: bDelayNTSAssert. Address Offset: 0xD0D Size: 1 Byte.
  Description: Time to wait in microseconds for NSS to go low while entering standby The default is 0x64 = 100 µs.

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5 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD_{(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$VDD_{(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
I_{ULPCD}	average ultra-low-power card detection current	T_{amb} = 25 °C, VDD(VDDPA) = VDD(VDDIO) =VDD(VDD) 3.0 V, 330 ms Polling interval, 50 R antenna matching	-	22	-	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	Transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB,	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

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6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5190B1HN/C121Y	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 4000 pcs, the ending Y in the product name is indicating the packing "reel" Initialized with FW 2.1, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C121E	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one tray, bakeable, MSL=3. Minimum order quantity = 490 pcs, the ending E in the product name is indicating the packing "single tray" Initialized with FW 2.1, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C127Y	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 4000 pcs, the ending Y in the product name is indicating the packing "reel" Initialized with FW 2.7, supports encrypted firmware download	SOT2062-1
PN5190B1HN/C127K	VFLGA40	very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in multiple trays, MSL=3. Minimum order quantity = 2450 pcs, the ending K in the product name is indicating the packing "multiple trays" Initialized with FW 2.7, supports encrypted firmware download	SOT2062-1
PN5190B1EV/C121Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel" Initialized with FW 2.1, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C121E	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 490 pcs The ending E in the product name is indicating the packing "single tray" Initialized with FW 2.1, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C127Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel" Initialized with FW 2.7, supports encrypted firmware download	SOT1307-2
PN5190B1EV/C127K	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 2450 pcs, the ending K in the product name is indicating the packing "multiple trays" Initialized with FW 2.7, supports encrypted firmware download	SOT1307-2

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7 Block diagram with VFBGA64 connections

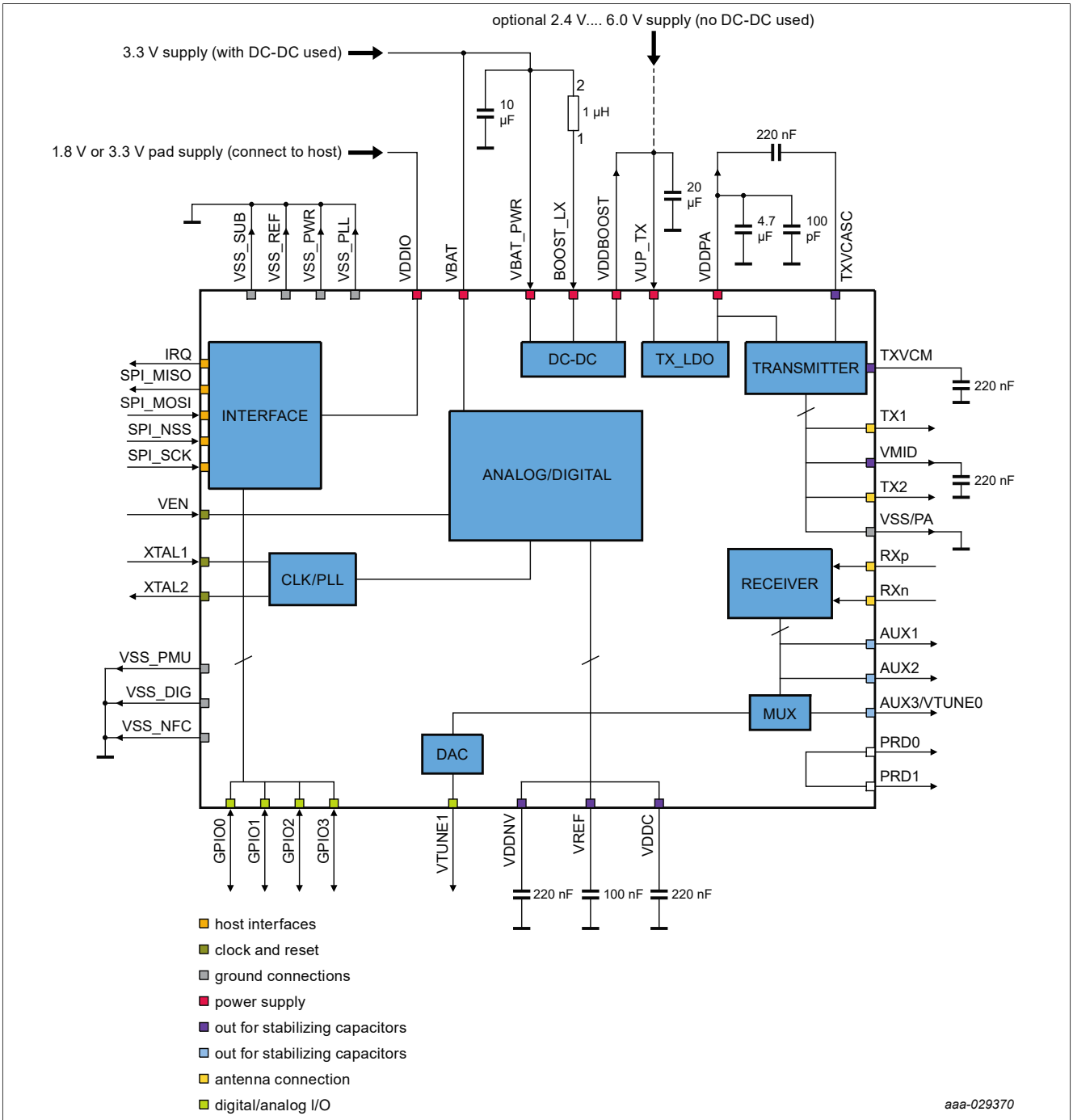


Figure 1. Block diagram (external connections: DC-DC mode)

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8 Pinning information

8.1 Pin description VFBGA64

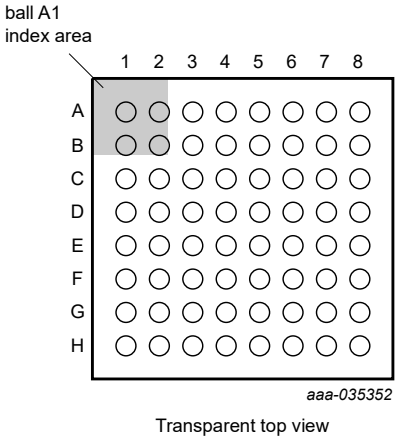


Figure 2. Pin configuration for VFBGA64

Table 3. Pin description VFBGA64

Pin Number	Symbol	Type	Description
Host Interface			
E6	ATX_A	Output	SPI target[1] data output
E5	ATX_B	Input	SPI clock input
D6	ATX_C	Input	SPI target select input
D5	ATX_D	Input	SPI target data input
B7	IRQ	Output	Host communication/ event interrupt signal
F8	XTAL1	Input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal
B3	VEN	Input	Hardware reset, low active (independent from V_{VDDIO}) Avoid a floating or unexpected toggling of the pin.
Supply pins			
H2	VSS_PA	Supply GND	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)
A2	VSS_PWR	Supply GND	DC-DC boost ground
D3	VSS_REF	Supply GND	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground
C3	VSS_PMU	Supply GND	PMU ground
F4	VSS_DIG	Supply GND	Digital ground
F3	VSS_NFC	Supply GND	NFC ground
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references

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Table 3. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description
A8	VDDIO	Supply	I/O pads power supply
G1	VDDPA	Supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO
B1	VDDBOOST	Supply	DC-DC boost supply
A1	BOOST_LX	Output	Boost inductance loopback, to be connected to boost inductor
A3	VBATPWR	Supply	To be connected to boost inductor and transmitter power supply
Outputs for stabilizing cap			
A4	VDDNV	Output	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF Debug signals			
G7	AUX_1	Output	Test bus 1
F7	AUX_2	Output	Test bus 2
H8	AUX_3 / VTUNE0	Output	Test bus 3 / VTUNE0 (digital-to-analog output 0)
Antenna connections			
H5	RXP	Input	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2
Analog/Digital inputs and outputs			
H7	VTUNE1	Output	Digital-to-analog output 1
E8	GPIO0	Input/ Output	General Purpose Output 0
D8	GPIO1	Input/ Output	General Purpose Output 1
E7	GPIO2	Input/ Output	General Purpose Output 2
D7	GPIO3	Input/ Output	General Purpose Input/Output 3 If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.

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Table 3. Pin description VFBGA64*...continued*

Pin Number	Symbol	Type	Description
Security feature			
B4	PRD1	Input/ Output	Package removal detection, internally connected to PRD2
G4	PRD2	Input/ Output	Package removal detection, internally connected to PRD1
Pins connected on PN76 family only			
A5	PVDD_OUT	Output	Do not connect
A6	I2CM_SDA	Input/Output	Do not connect
A7	DWL_REQ	Input	Recommended: Do not connect - entering secure firmware download by command. If connected, this pin allows to enter the Secure firmware download mode if set high during hardware reset.
B5	GPIO5	Input/Output	Do not connect
B6	I2CM_SCL	Input	Do not connect
B8	SWDIO	Input/Output	Do not connect
C2	TEST	Input/Output	Internal test pin. To be connected to GND
C4	ISO_INT_AUX	Input/Output	Do not connect
C5	GPIO4	Input/Output	Do not connect
C6	HOST_IF_SEL1	Input	Do not connect
C7	HOST_IF_ SEL0	Input	Do not connect
C8	SWD_CLK	Input	Do not connect
D1	USB_VBUS	Input	Do not connect
D4	ISO_IO_AUX	Input/Output	Do not connect
E2	AD1	Input	Do not connect
E4	ISO_CLK_AUX	Input	Do not connect
F5	SPIM_MOSI	Input	Do not connect
F6	SPIM_MISO	Output	Do not connect
G5	SPIM_SCLK	Input	Do not connect
G6	SPIM_NSS	Input	Do not connect

[1] Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I^2C and JEDEC SPI standards organization

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

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8.2 Pin description VFLGA40

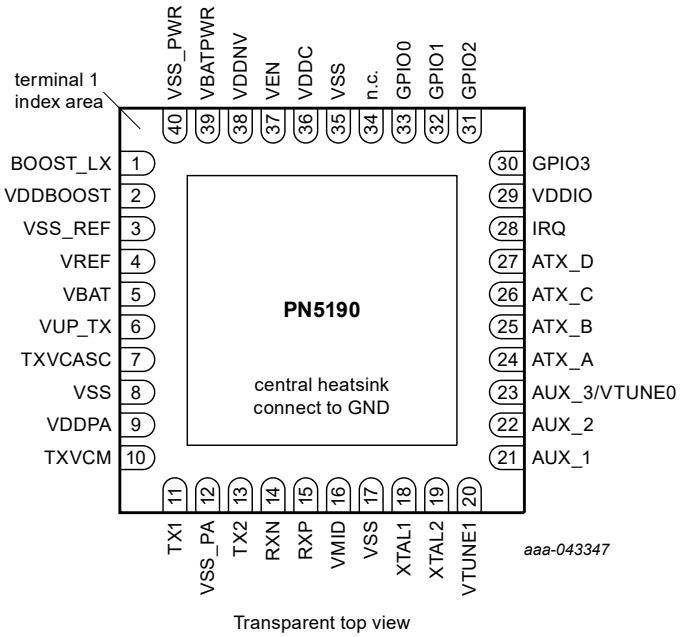


Figure 3. Pin configuration for VFLGA40 (SOT2062-1)

Table 4. Pin description VFLGA40

Pin Number	Symbol	Type	Description
1	BOOST_LX	Output	Boost inductance loopback, to be connected to boost inductor pin 1
2	VDDBOOST	Supply	Boosted supply voltage output
3	VSS_REF	Supply GND	PMU ground
4	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
5	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references
6	VUP_TX	Supply	Input supply voltage for transmitter LDO
7	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA
8	VSS	Supply GND	Ground
9	VDDPA	Supply	Transmitter supply
10	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
11	TX1	Output	Antenna driver output 1
12	VSS_PA	Supply GND	Transmitter ground
13	TX2	Output	Antenna driver output 2
14	RXN	Input	Receiver Input "Negative"
15	RXP	Input	Receiver input "Positive"

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Table 4. Pin description VFLGA40*...continued*

Pin Number	Symbol	Type	Description
16	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground)
17	VSS	Supply GND	Ground
18	XTAL1	Input	Crystal / System clock input
19	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal
20	VTUNE1	Output	Digital-to-analog output 0
21	AUX_1	Output	Test bus 1
22	AUX_2	Output	Test bus 2
23	AUX_3 / VTUNE0	Output	Test bus 3 / VTUNE0 digital-to-analog output 1
24	ATX_A	Output	SPI target data output
25	ATX_B	Input	SPI clock input
26	ATX_C	Input	SPI target select input
27	ATX_D	Input	SPI target data input
28	IRQ	Output	Host communication/ event Interrupt signal
29	VDDIO	Supply	I/O pads power supply
30	GPIO3	Input/Output	General Purpose Input/Output 3 - If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.
31	GPIO2	Input/Output	General Purpose General Purpose Output 2
32	GPIO1	Input/Output	General Purpose General Purpose Output 1
33	GPIO0	Input/Output	General Purpose General Purpose Output 0
34	n.c.	-	-
35	VSS	Supply GND	Ground
36	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
37	VEN	Input	Hardware reset, low active (independent from V_{PVDD}) Avoid a floating or unexpected toggling of the pin.
38	VDDNV	Output	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap
39	VBAT_PWR	Supply	To be connected to boost inductor pin 2 and transmitter power supply
40	VSS_PWR	Supply GND	DC-DC boost ground

For best performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

Compared to the BGA package, all ground connections named VSS are connected on the leadframe of the package. Therefore general VSS pins do exist, pins are not distinguished by function like on the BGA package type e.g. VSS_PMU. The exceptions are the pins VSS_PWR, VSS_PA and VSS_REF.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

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9 Functional description

9.1 Functional overview

The PN5190B1 is an NFC frontend with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuitry and all the low-level functionality to realize an NFC Forum and EMVCo compliant reader.

Connection to host controller

The PN5190B1 connects to a host microcontroller with a fast SPI interface (15 Mbit/s) for configuration, NFC data exchange and high-level NFC protocol implementation. An optimized TLV-based framing is supported to reduce the command handling overhead on the host controller and to reduce command-response latencies.

Clock supply

The PN5190B1 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies.

Integrated DC-DC

The integrated DC-DC allows a single supply voltage while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The usage of the integrated DC-DC is the preferred choice for a stable RF performance, even in case of a de-charged battery. Optimized usage of a battery charge can be achieved by directly connecting the transmitters to the supply. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software.

The DC-DC clock is synchronized with the clock of the receiver - this avoids the typical performance reduction by DC-DC noise which can be seen in systems using external DC-DCs.

Transmitter LDO (TX_LDO)

The Transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the TX_LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

Low-power card detection

The low-power card detection (LPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the low-power card detection provides a functionality, which allows to power down the reader for a certain amount of time to safe energy. After some time, the reader becomes active again to poll for cards. If no card is detected, the reader can go back to the power down state. During the polling time, a host controller can be set to a power-saving mode. An interrupt request from the PN5190B1 allows waking up the host controller in case an antenna detuning by a card or cell phone had been detected.

Two modes for the low-power card detection are available:

- LPCD (software based) which allows maximum detection range. For detecting a card presence, I/Q channel information is used.
- ULPCD (hardware based) which offers maximum current savings. For detecting a card presence, only the amplitude information is used.

Dynamic power control 2.0

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The next generation Dynamic Power Control (DPC2.0) with true transmitter current measurement works autonomous without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matchings.

Adaptive wave shape control

The Adaptive Wave Shape Control (AWC) helps to keep the waveshapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true Baseband Amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An Integrated Chip scope allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual comfort interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system.

Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the Host Controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptions in case of future possible specification changes.

Automatic antenna tuning

Two analog outputs are available to connect variable capacitors for automatic antenna tuning (AAT). The automatic antenna tuning allows compensating for production tolerances or changing environments like surrounding metal. This is especially beneficial for applications which make use of OEM NFC Modules which are finally used in an unknown environment. The automatic antenna tuning is performed command triggered.

Firmware update

The PN5190B1 supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set, but a framing which is not different from the standard host interface commands used for NFC operation of the device. In Secure Firmware update mode, the PN5190B1 requires no dedicated physical handling of the SPI interface lines. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN5190B1 will be in download mode.

Register configuration

Internal registers of the PN5190B1 store volatile configuration data and accessible by the host interface. The internal registers are reset to configurable initial values in case of powerON, hardware-reset and standby.

The configuration for dedicated RF protocols and antenna-dependent configuration is defined in non-volatile memory. This configuration is typically done only once during production, and is performed by a command issued from the host microcontroller.

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EEPROM configuration

Non-Volatile EEPROM memory of the PN5190B1 is used to store configuration data that needs to be preserved in case the PN5190B1 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory and copied to volatile registers by a host interface command. In addition, other configuration data which needs to be preserved during power supply disconnect is stored in this EEPROM memory as well. Examples for this are configurations for DPC, LPCD and ULPCD configurations.

RF configuration

The PN5190B1 allows a fast RF protocol selection based on the command Load_RF_configuraton and pre-defined user configuration data in non-volatile memory (EEPROM).

On the one hand, the configuration of modulation-related parameters can be done (e.f. selection of ISO/IEC14443-A), on the other hand antenna-specific parameters can be configured.

For more information, see ref.[1].

9.2 Endianness

The endianness describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234

address x: 12

address x+1: 34

The location of word-sized data (16 bit) is as follows:

Value hex: 0x1234

address x: 34

address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is large endian, the placement of nibbles of the variable is small endian.

Value hex: 0xAABBCCDD

address x: BB

address x+1: AA

address x+2: DD

address x+3: CC

The location of double word-sized data (32 bit) is as follows:

Value hex: 0xAABBCCDD

address x: DD

address x+1: CC

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address x+2: BB

address x+3: AA

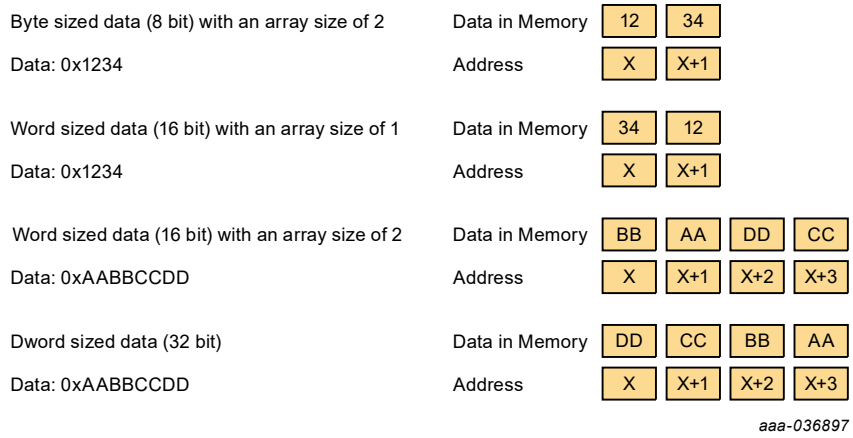


Figure 4. Endianness examples

Data from the EEPROM is read in little-endian format - LSB first. This means that the byte at the lower address is read first.

9.3 Initial calibration

The PN5190B1 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following (as those registers contain RFU Bits, a read->mask->write must be done to avoid modification of the RFU Bits):

Write EEPROM CfgNovCal (0xC83) – 0x40 mask [1:0] and set those bits to "00b", write back.

NewValue = "readValue & 0xFC";

Write REGISTER TX_NOV_CALIBRATE_AND_STORE (addr: 0x5d) - 0x01 mask[1:0] and set "01b", write back.

NewValue = "readValue | 0x01";

Write EEPROM CfgNovCal (0xC83) – 0x42 mask [1:0] and set those bits to "10b",

write back. NewValue = "readValue < 0x02";

Note: *The calibration phase must be executed with a reliable power supply beeing connected, where no fluctuations are present on the pins of the device.*

9.4 System power states

The PN5190B1 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

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Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT. Power state change will also be triggered by certain events - VDDIO Loss, overcurrent detection, overtemperature.

In addition, state changes are triggered possible by host commands.

Disconnecting and connecting the power supply on VBAT restarts the PN5190B1 always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN5190B1 always in Active State.

The following power states are supported:

Table 5. System power states

Power state	Description	typical current consumption
Power OFF	The NFC system (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO). In all other power states, the Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in power off mode. Device is not functional	-
PMU OFF	The NFC system is disabled by the host via a low signal on pin VEN. No internal clocks of the PN5190B1 are active. Entry to PMU OFF can also be triggered by power loss on VDDIO. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, RX ULPCD detect, ULP abort signal on PIN3, VDDIO restore.	5 µA
ULP standby	The host can set the PN5190B1 into Ultra-low power card detection state (ULP Standby state) via programming of the ULPCD bit (Switch mode command). In the ULP standby state, the PN5190B1 is able to activate the transmitter and receiver after defined time (expiry of wake-up timer) to detect the card. If a card is not detected, the transmitter and receiver is deactivated and the wake-up timer restarted. Power consumption of ULP Standby mode is much lower than Hard power down State and standby State. Only the wake-up timer is active during ULP standby state Wake-up events: Power reset on pin VBAT, VEN rising edge, GPIO3 level, Card detected. Variant 1: Configurable wake-up timer allows system to boot into active Variant 2: Configurable wake-up timer allows checking regularly for a card in the field.	Variant 1: 5 µA Variant2: 22 µA
Standby	The NFC system can be switched into a low-power mode to minimize power dissipation. The RF functionality is not available in this case. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, ULPDET, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on.	45 µA
Suspend	All power sources are available. LFO and HFO clocks are available. CPU subsystem clock sources are gated, except for the LFO. I/Os are available.	2.5 mA
Active	The PN5190B1 is able to process internal or external events or data. All external power supply sources and the external clock need to be available, and all internal clocks are active.	20 mA (system without RF current)

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9.5 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations needs to be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance.
  In this configuration the DPC, current measurement and overcurrent protection is not available.

9.5.1 System power supply overview

The PN5190B1 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIOs (VDDIO)

2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)

3. Supply of the RF drivers (VDDPA), DC-DC (VBAT_PWR), and TX_LDO (VUP)

The functionality of the GPIOs, Host Interface and internal analog and digital blocks is independent from the supply of the RF driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in Power Off mode.

9.5.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors need to be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

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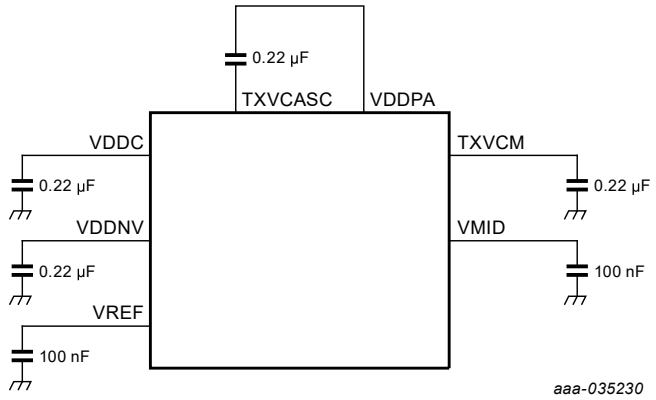


Figure 5. Blocking capacitors

9.5.3 Transmitter power supply

The PN5190B1 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG (0000h) - Enables/disables and configures the DC-DC according to the external supply connections.

TX_LDO_CONFIG (address 0002h) - Enables/disables and configures the TX_LDO.

TX_LDO_VDDPA_HIGH (address 0006h) - initial out voltage when DPC is used.

TX_LDO_VDDPA_LOW (address 0007h) - lowest VDDPA when DPC is used.

TX_LDO_VDDPA_MAX_RDR (address 0008h) - maximum voltage to be set in reader mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

9.5.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

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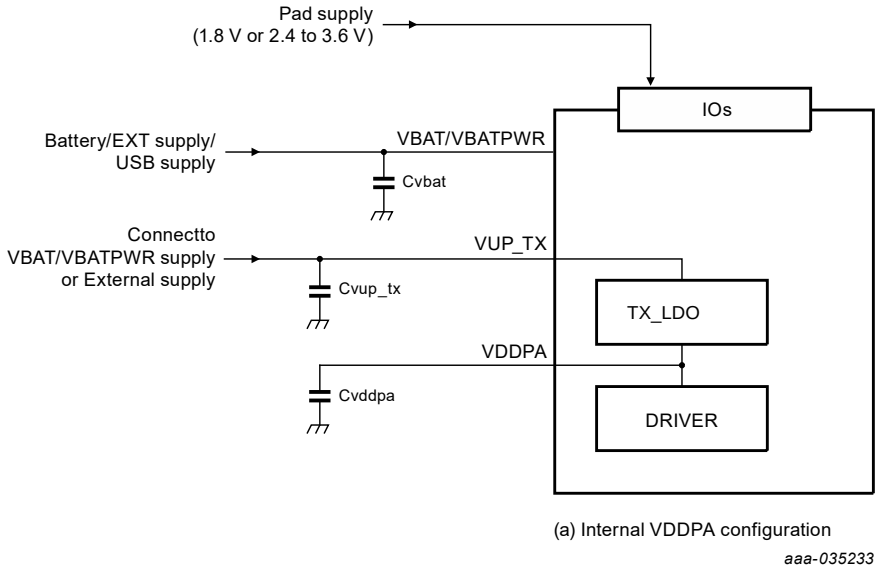


Figure 6. Transmitter supply

9.5.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBATPWR.

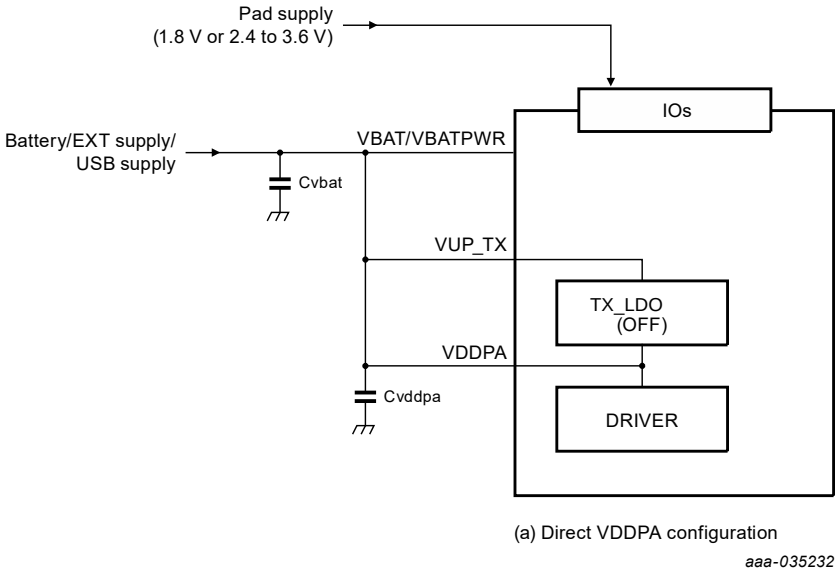


Figure 7. Direct transmitter supply

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9.5.3.3 DC-DC (boost) supply

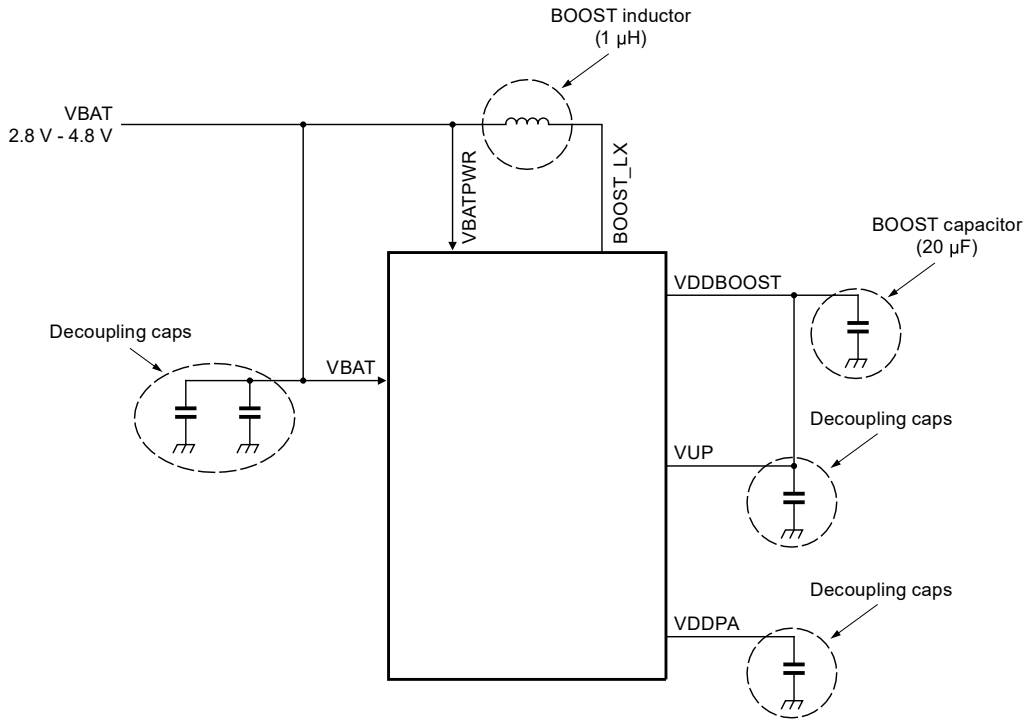


Figure 8. Transmitter supply by DC-DC (DC-DC is enabled)

9.5.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR and must be same voltage level.

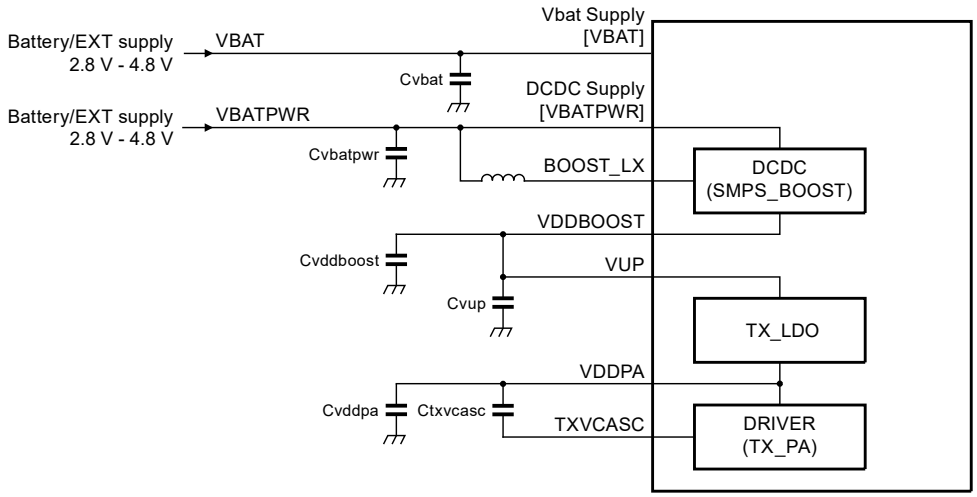


Figure 9. DC-DC active

Note: *VBAT and VBAT_PWR shall be routed as separate supply lines with separated block capacitors but connected to the same source.*

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9.5.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR and must be same voltage level.

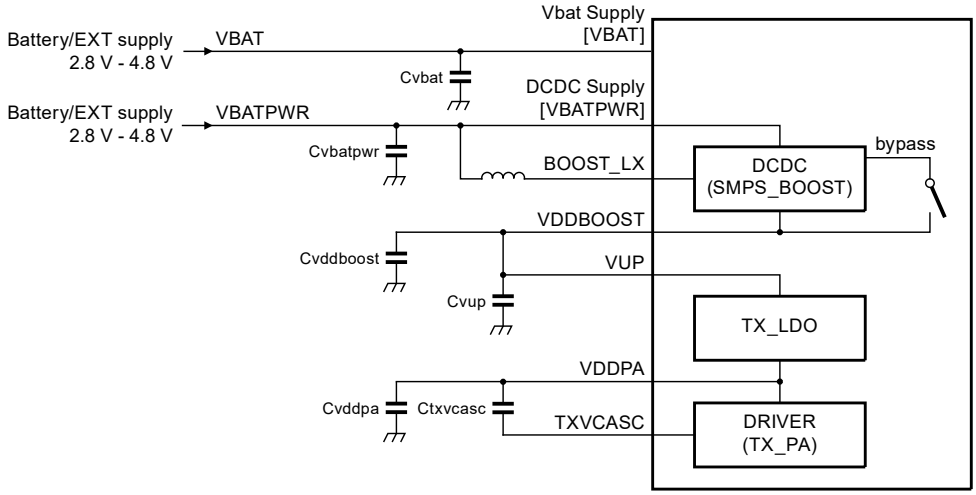


Figure 10. DC-DC bypassed (in DCDC_PWR_CONFIG)

Note: *VBAT and VBAT_PWR shall be routed as separate supply lines with separated block capacitors but connected to the same source.*

9.5.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

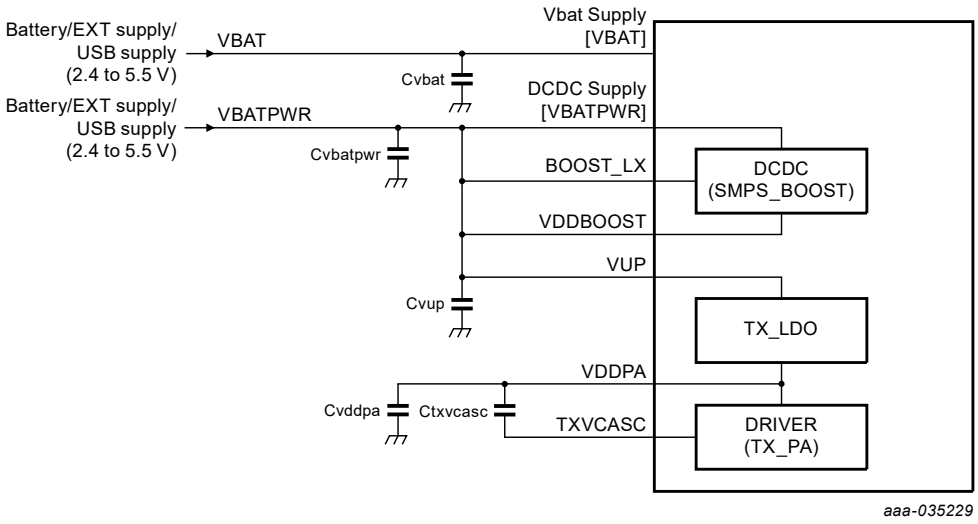


Figure 11. No DC-DC used

Note: *VBAT and VBAT_PWR should be routed as separate supply lines with separated block capacitors but connected to the same source.*

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9.5.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

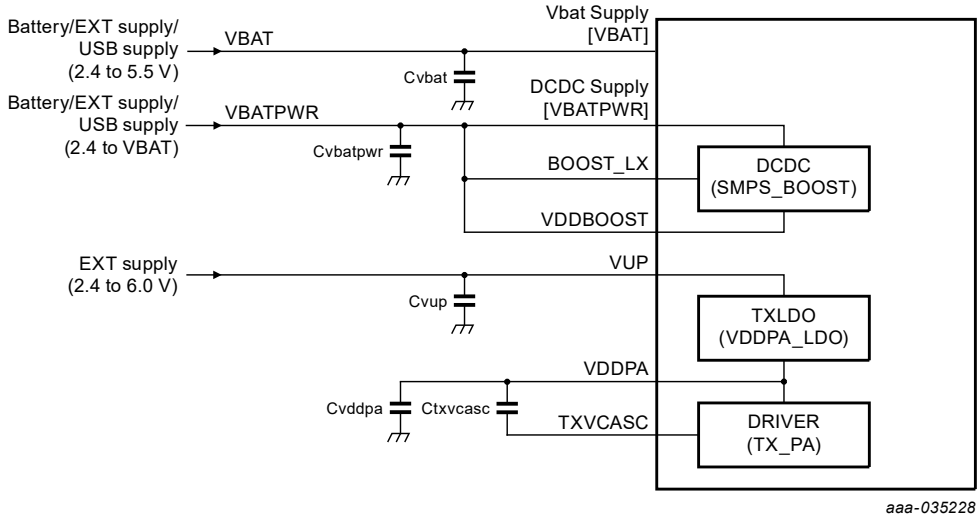


Figure 12. No DC-DC used

9.5.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

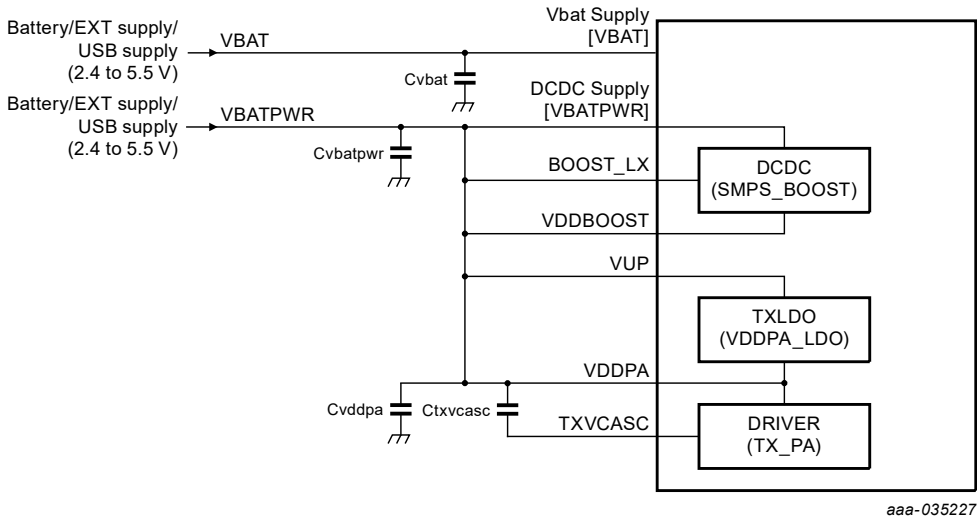


Figure 13. No DC-DC used - no TX_LDO

Note: *VBAT and VBAT_PWR should be routed as separate supply lines but connected to the same source*

9.5.3.9 Supply voltage range for transmitter supply configuration examples

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Table 6. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independently from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x30	NA
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	NA
TXLDO_VDDPA_MAX_RDR (0008h)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x21	0x00
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)
TXLDO_VDDPA_MAX_RDR (0008h)	NA	NA	NA	NA	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA

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Table 7. Supply voltage range

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independently from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
VBAT	2.8 V … 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V … 5.5 V	2.4 V … 5.5 V
VBATPWR	2.8 V ... 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V ... 5.5 V	2.4 V … 5.5 V
VUP	3.1 V … 6.0 V	2.8 V … < VBATPWR	2.4 V ... 5.5 V	2.4 V … 6.0 V	2.4 V … 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO. max 5.7 V	VBATPWR - 0.5 V voltage drop	VUP-0.3V drop of TX_LDO	VUP-0.3V drop of TX_LDO	2.4 V … 5.5 V

9.6 Clock generation

The device supports the operation with two clock options, which is configured in EEPROM address CLK_INPUT_FREQ (0012h).

One option is clocking by a crystal (default), the other a clocking by an external clock input frequency.

It is important to consider additional phase noise introduced e.g. by clock drivers in the design. Phase noise of the external clock has an impact on the RF performance which can be achieved.

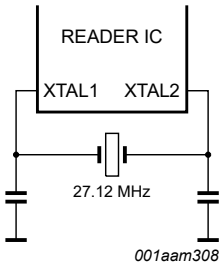


Figure 14. Clocking by crystal

9.7 External interfaces

The PN5190B1 requires the connection of a power supply, and a clock source like crystal or external clock and a host microcontroller connected by the SPI interface for operation.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIO's (on PN5190B1 only outputs are implemented) and 2x DAC functionality (analog outputs).

The GPIO's implement internal Pull-up/Pull-down resistors. The output of the GPIO's can be configured in the pad configuration PAD_CONFIG (0052h).

For more information, see ref.[2].

9.8 Transmitter overcurrent and temperature protection

Note: *Refer to the errata sheet.*

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The PN5190B1 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the Transmitter Driver in case of a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG (0002h), bit 11: overcurrent enable (0: disable, 1: enable)

On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM TEMP_WARNING (0014h). Three temperatures can be configured: 114 °C, 2:125 °C, 3:130 °C. GPIO0 is used to indicate this temperature warning to a connected host.

The actual measured temperature is available in the register TEMP_SENSOR (005Bh).

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

9.9 Loading a dedicated RF configuration

The PN5190B1 allows an efficient selection of a dedicated RF protocol.

The selection of one RF protocol is done by sending a command to the PN5190B1. This instruction is used to load the RF configuration from EEPROM into registers.

It is possible to configure RF technology, mode (target/initiator) and baud rate.

Configurations can be loaded separately for the receiver (RX configuration) and transmitter (TX configuration).

The Command used for loading a dedicated RF protocol is LOAD_RF_CONFIGURATION (0Dh).

9.10 FeliCa RF functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification.

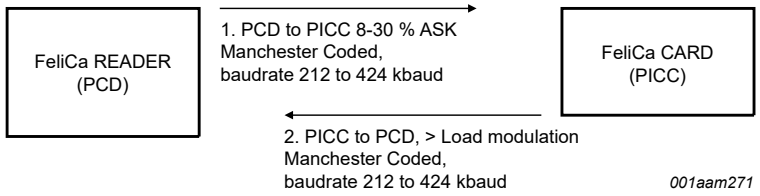


Figure 15. FeliCa read/write communication diagram

The physical parameters are described in the table below:

Table 8. Communication for FeliCa reader/writer

Communication direction	Signal type	Transfer speed FeliCa	FeliCa higher transfer speeds
		212 kbit/s	424 kbit/s
Reader to card (send data from the PN5190B1 to a card) f_c = 13.56 MHz	reader side modulation	8 % to 30 % ASK	8 % to 30 % ASK
	bit encoding	Manchester encoding	Manchester encoding
	bit rate	$f_c/64$	$f_c/32$
Card to reader (PN5190B1 receives data from a card)	card side modulation	Load modulation,	Load modulation,
	bit encoding	Manchester encoding	Manchester encoding

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The PN5190B1 needs to be connected to a host which implements the FeliCa protocol.

Multiple reception cycles (RxMultiple)

For FeliCa timeslot handling in PCD mode, PN5190B1 implements multiple reception cycles. The feature is enabled by setting the control bit RX_MULTIPLE_ENABLE in the register TRANSCEIVE_CONTROL in combination with the transceive state machine.

Unlike for normal operation, the receiver is enabled again after a reception is finished. As there is only one receive buffer available, but several responses are expected, the buffer is split into sub buffers of 32 byte length. Hence, the maximum number of responses which can be handled is limited to 8. As the maximum length defined for a FeliCa response is 20 bytes, the buffer size defined does fulfill the requirements for that use case. The first data frame received is copied onto buffer address 0. The subsequent frames are copied to the buffer address 32 * NumberOfReceivedFrames. The maximum number of data bytes allowed per frame is limited to 28.

All bytes in the buffer between the payload and the status byte are uninitialized and therefore invalid. The firmware on the host shall not use these bytes. The last word of the sub buffer (position 28 to 31) contains a status word. The status word contains the number of received bytes (may vary from the FeliCa length in case of an error), the CLError flag indicating any error in the reception (which is a combination of 3 individual error flags DATA_INTEGRITY_ERROR || PROTOCOL_ERROR || COLLISION_DETECTED) the individual error flags and the LenError flag indicating an incorrect length byte (either length byte is greater than 28 or the number of received bytes is shorter than indicated by the length byte). All unused bits (RFU) are masked to 0.

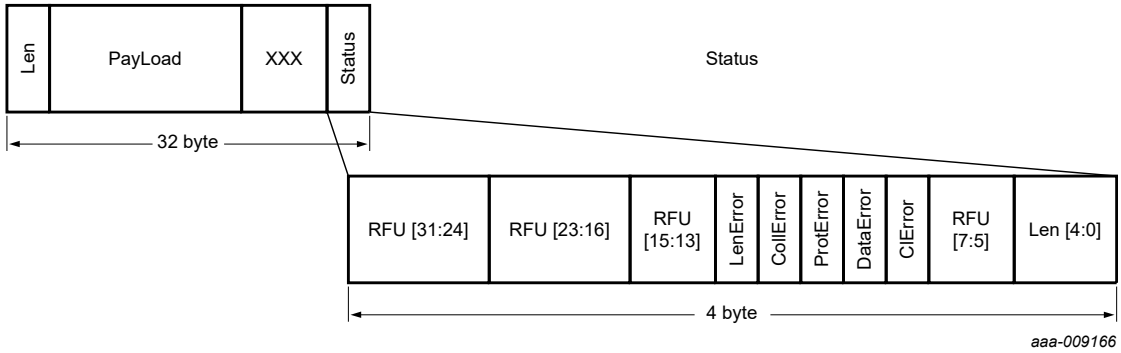


Figure 16. RxMultiple data format

There are 4 different cases possible for a reception:

1. *Correct reception* - Data integrity is correct (no CRC error), and additionally the number of bytes received is equal to the length byte. Data is written to the buffer. No error set in status byte.
2. *Erroneous reception* - Data is incorrect (data integrity error - CRC wrong) but frame length is correct. Data is written to buffer and the bits CLError and DataError in the status byte are set.
3. *Erroneous reception* - the length byte received indicates a frame length greater than 28. Data is written to buffer and the bit LenError in status byte is set.
4. *Erroneous reception* - the length byte is larger than the number of data bytes, which have been received. Data received is written to buffer and the ProtocolError bit in the status byte is set.

At the end of the reception, additionally the bit field RX_NUM_FRAMES_RECEIVED in the register RX_STATUS_REG is updated to indicate the number of received frames. Upon start of a new EXCHANGE_RF_DATA command, the flag RX_NUM_FRAMES_RECEIVED is cleared.

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9.11 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong in close proximity of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host needs to configure the chip after each reset or power-off.

The following EEPROM settings are most relevant for the DPC configuration:

0x76: DPC_Config: Enables/Disables the DPC (enable: 0x77, disable: 0x70)

0x77 and 0x78: DPC_TargetCurrent: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.

0x79 and 0x7C: DPC_Hysteresis (loading and unloading): Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

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0x8B: DPC_Lookup_Table: configures the current reduction

The DPC_LOOKUP_TABLE allows in addition to the limitation of the current, to configure

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10% and ASK100% modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM_RSSI

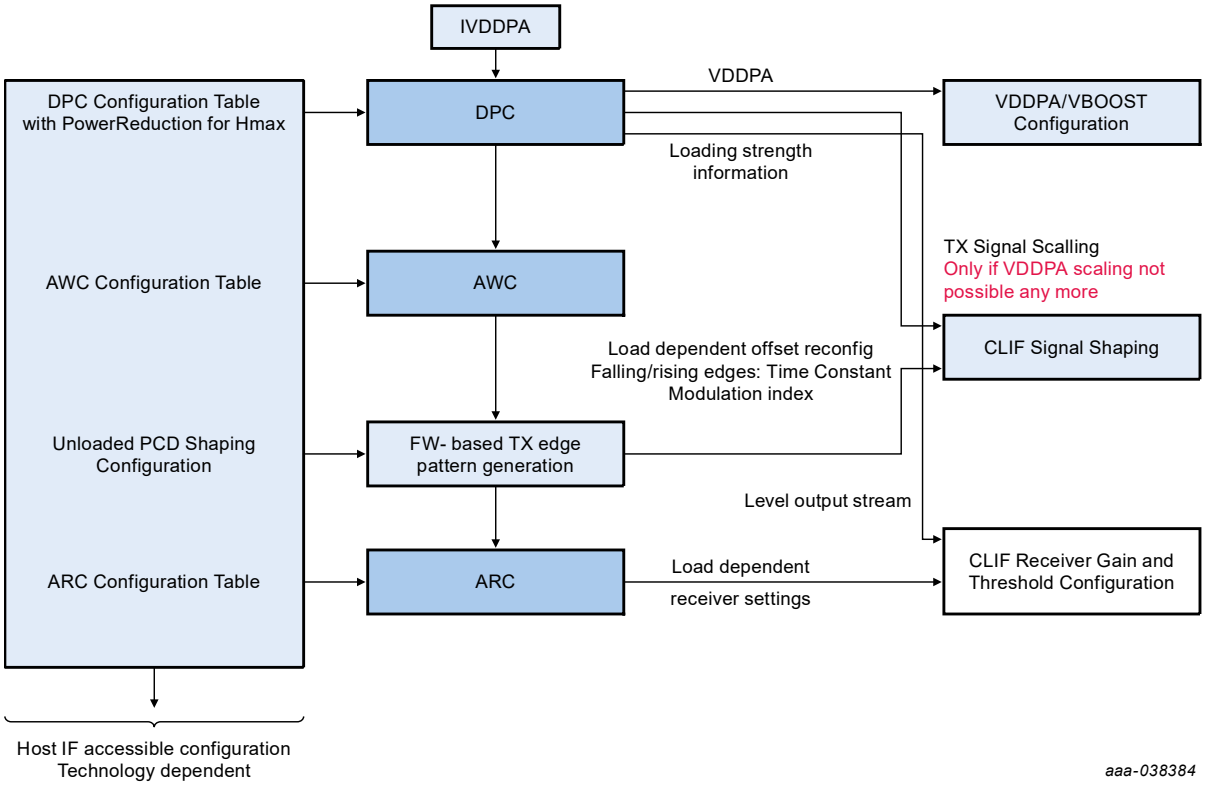


Figure 17. System overview: DPC, AWC and ARC

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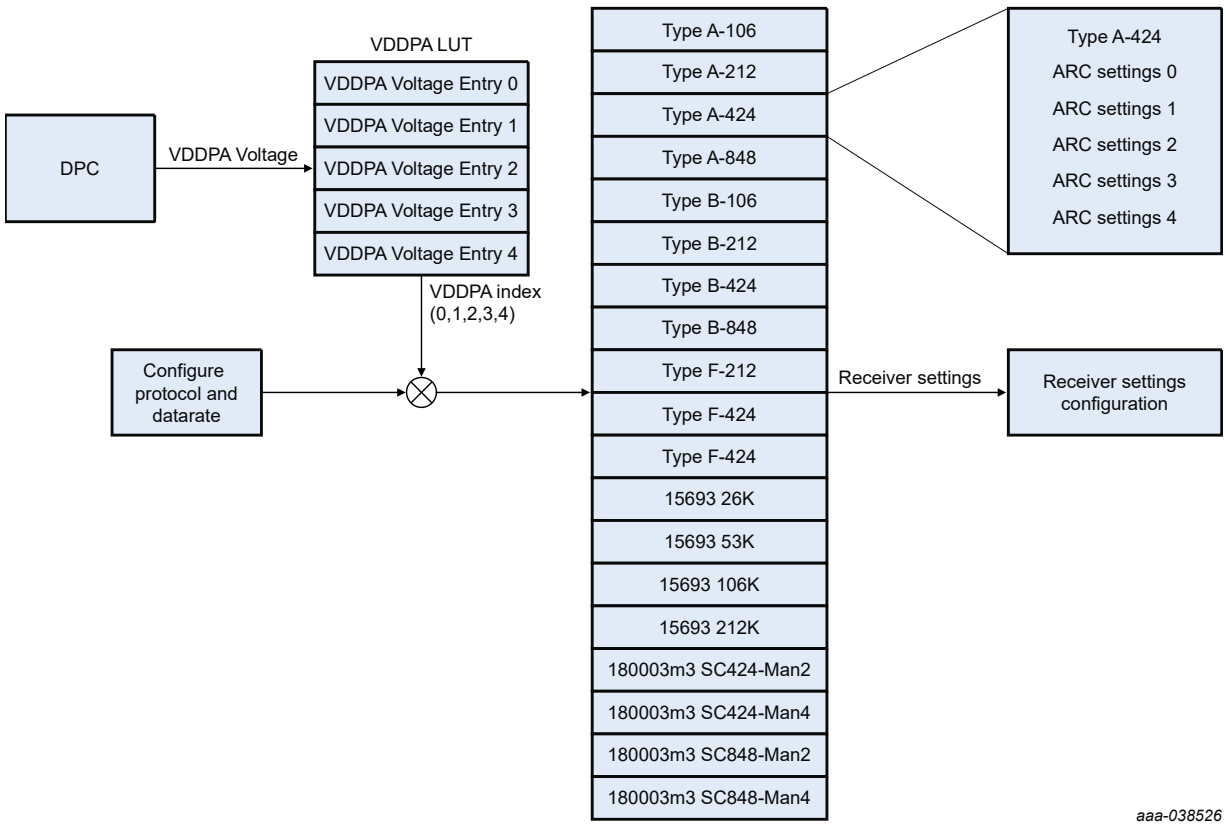


Figure 18. System overview: DPC, AWC and ARC

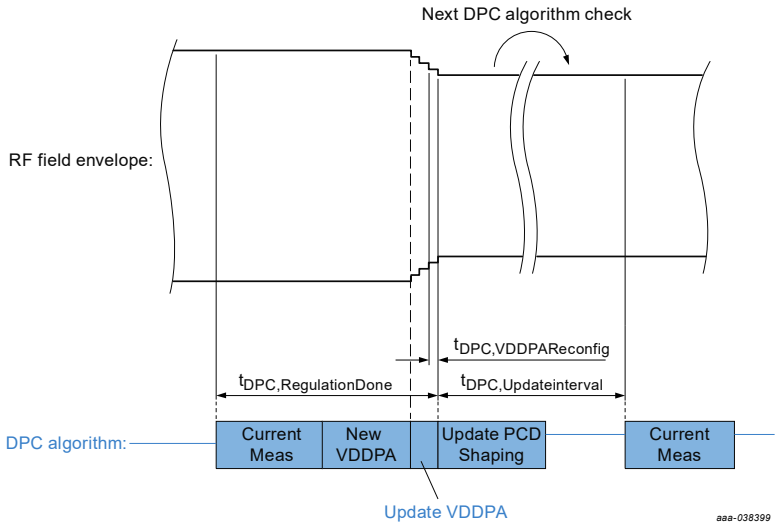


Figure 19. System overview: DPC, AWC and ARC

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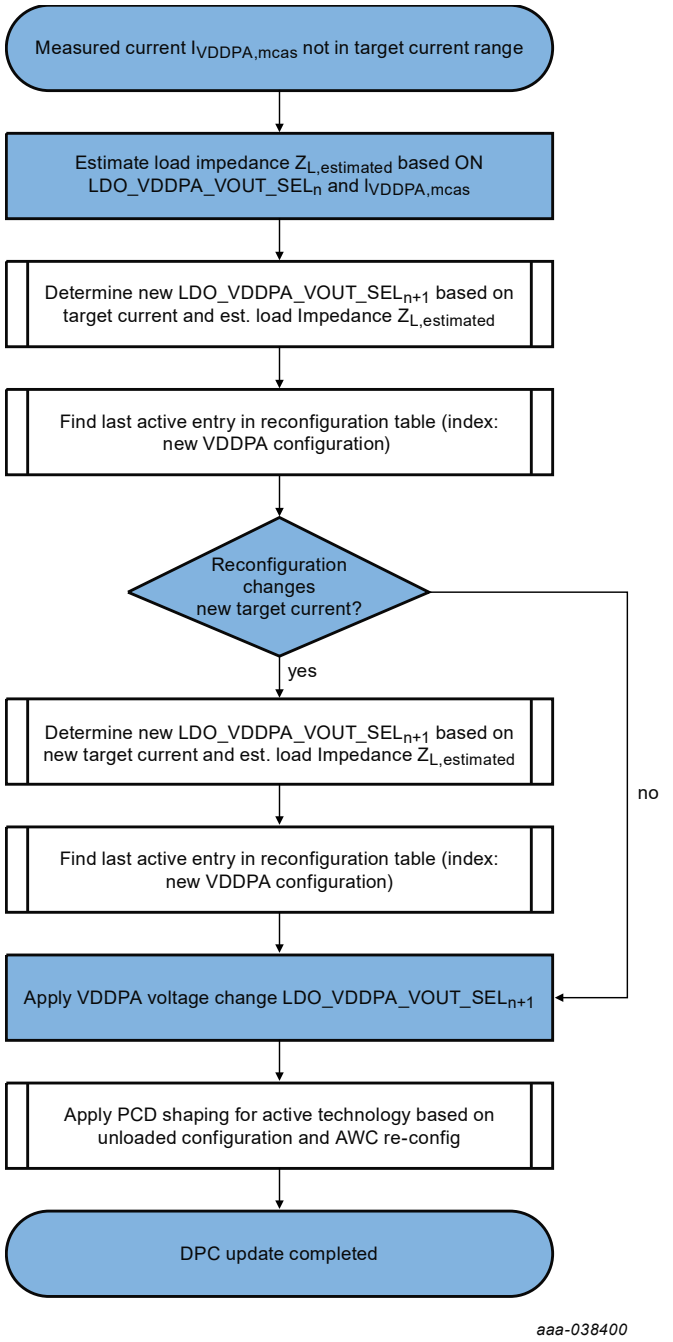


Figure 20. System overview: DPC, AWC and ARC

9.11.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current
   VDDPA New (for target current of Itarget) = VDDPA Voltage / VDDPA current * Itarget
3. Update VDDPA: Perform output power update

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4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

Example:

Unloaded configuration After Field ON:

- VDDPA max set to 42 (5.7 V)
- Target current set to 280 mA
- Technology B106: amp_mod=200
- Falling edge time constant = rising edge time constant = 3

Table 9. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:24	ENTRY 0 - LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 - MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

- DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.
- Target current stays at 280 mA.
- Technology B106: amp_mod = 205
- Falling edge time constant = 2
- Rising edge time constant = 0

9.12 Adaptive waveshape control (AWC)

Depending on the level of detected detuning of the antenna, wave shaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)

2. Lookup table based shaping (4,5,6)

The Firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

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The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.

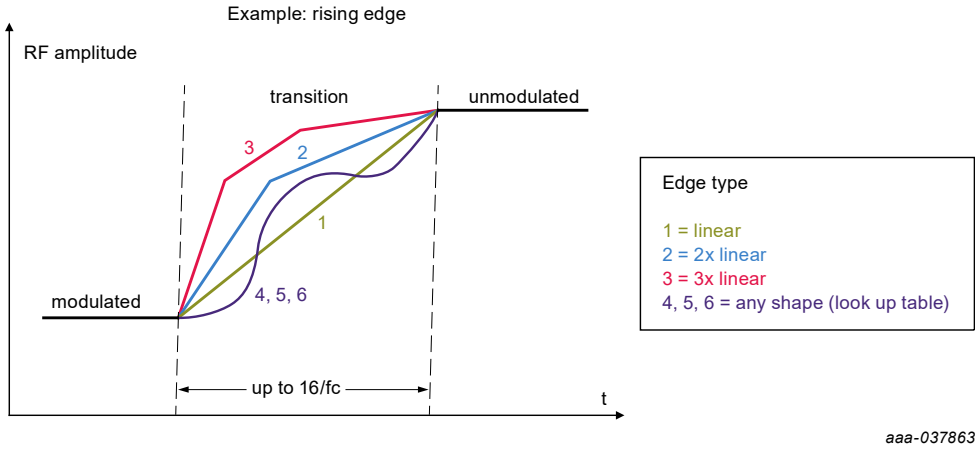


Figure 21. Waveshaping transitions

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated wave shaping configuration for the corresponding detuning condition. But allows in addition to configure the wave shaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels

2. Two linear transition´s between amplitude levels and

3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE_TYPE_(protocol), and can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers EDGE_STYLE_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE_LENGTH_(protocol) define the total length of the edge pattern.

The figures below illustrate the edge type for the falling edge.

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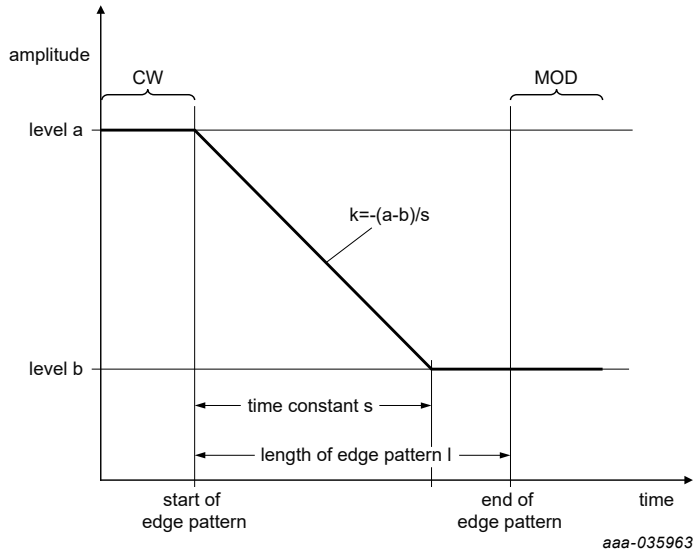


Figure 22. One linear transition (example falling edge)

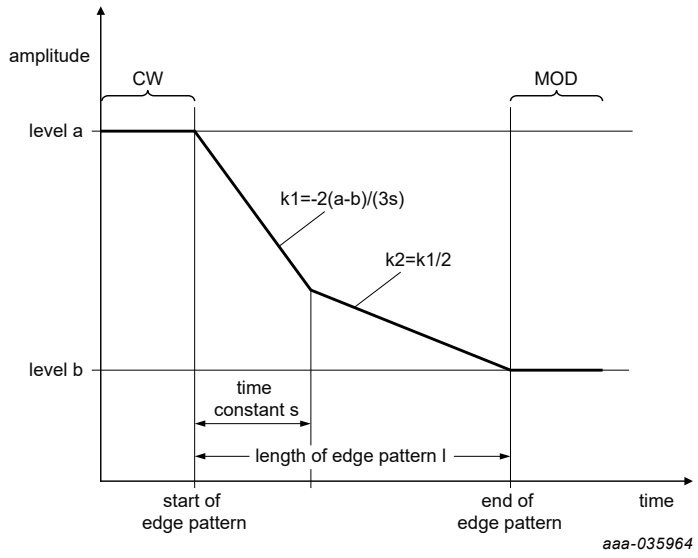


Figure 23. Two linear transitions (example falling edge)

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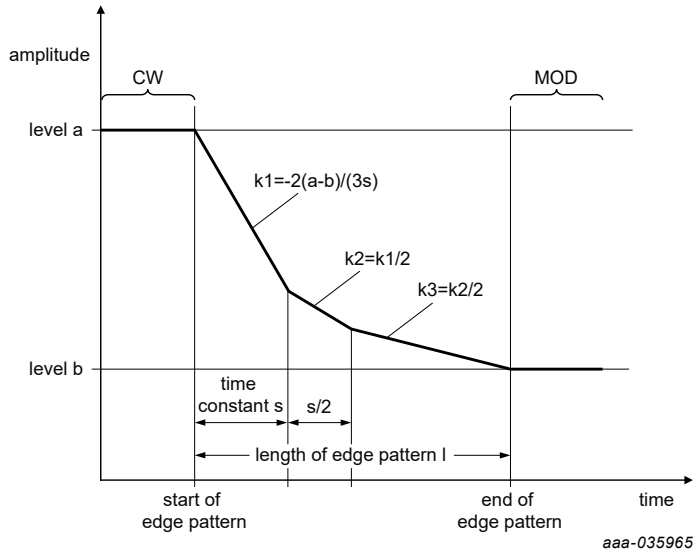


Figure 24. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (e.g. resonant circuitry parameters) to the emitted RF envelope.

9.13 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG (30h) ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG (22h) ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION (0Dh).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table define maximum five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

Table 10. ARC_VDDPA (0139Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
13D	ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4

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Table 10. ARC_VDDPA (0139Eh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
13C		7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3
13B		7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2
13A		7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1
139		7:0	Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Following table show ARC settings for Type A-106.

Table 11. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
146	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
144	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
142	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
140	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT,

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Table 11. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
13E	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

9.14 Timer

The PN5190B1 implements three different types of timers: 2 general-purpose timers (only general-purpose Timer0 is accessible by the user, Timer1 is used by the PN5190B1 as FDT Timer), 1 wake-up timer and 1 low frequency timer.

General-purpose timer

The PN5190B1 implements two 20-bit wide general-purpose timers - Timer0 and Timer1.

Timer0 can be configured by 2 registers each (TIMER0_CONFIG, TIMER0_RELOAD).

Timer 1 is typically used for as FDT and EMD timer configuration. Configuration can be done from the host but the associated IRQ is handled by the firmware of the PN5190B1. The Timer1 events are consumed by the PN5190B1 FW and respective Time-out status is included as part of the command response.

The general-purpose Timer0 and the FTD Timer1 have a max count of 1.048.575.

The register TIMER0_CONFIG, TIMER0_RELOAD configure if either the 13.56 MHz clock of the RF interface is used as Timer input, or if a divided clock frequency is used as input. These registers configure as well the start conditions for the timer.

The following clock frequencies can be selected for the prescaler:

000b - 6.78 MHz counter

001b - 3.39 MHz counter

010b - 1.70 MHz counter

011b - 848 kHz counter

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100b - 424 kHz counter

101b - 212 kHz counter

110b - 106 kHz counter

111b - 53 kHz counter

Wake-up timer

The PN5190B1 implements one 10-bit wide wake-up timer.

Max count of the wake-up timer is 1023, input clock is the LFO CLK = 380 kHz. The max timeout is 269 ms.

The wake-up time is configured via the SWITCH_MODE_STANDBY / SWITCH_MODE_LPCD commands. There is no dedicated register available for this timer. The PN5190B1 enters the standby state by the switch mode command SWITCH_MODE_STANDBY/ SWITCH_MODE_LPCD. The counter value is part of the command and has to be sent as one configuration parameter. The 2-byte parameter value for the standby counter is indicating the counting time in milliseconds. The value needs to be provided in little-endian format.

Low frequency timer

The wakeup-counter for the ULPCD mode has a width of 12bits.

The input clock for this timer is 1 kHz. ULPCD uses the ULP_STANDBY command, and for this the wake-up timer is feed by the 1 kHz clock. Count down value (12 bits counter; ULFO CLK / 4096 = 0.244 Hz i.e. 1 ms per bit).

The max timeout is 4.096 s.

Timer for contactless interface

In addition to the timers above, to guarantee correct protocol timing, a guard period timer is implemented for the RF_EXCHANGE command in reception and transmission mode (TX_WAIT, RX_WAIT counting).

No configuration of this timer is available for the user, setup, and counting is managed completely by the hardware. Therefore this timer is not indicated in the timer overview.

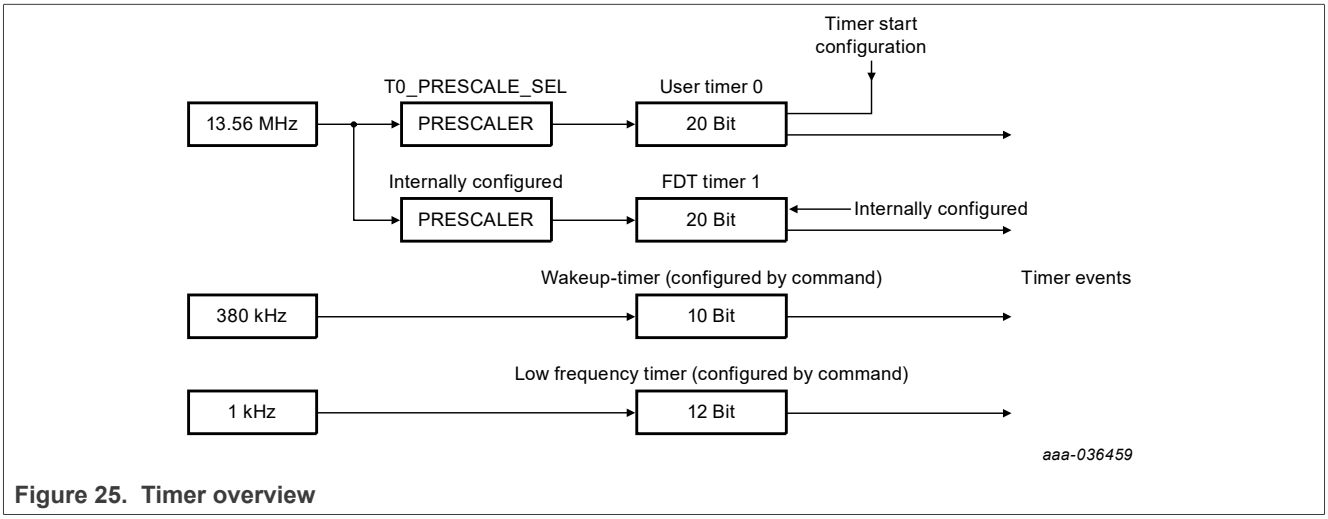


Figure 25. Timer overview

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9.15 Energy-saving card detection

The low-power card detection (LPCD) and ultra-low power card detection (ULPCD) are an energy-saving card polling configuration for the PN5190B1. During LPCD and ULPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

There is no trimming for the Low Frequency Timer required.

The SWITCH_MODE instruction allows entering the LPCD or ULPCD mode with a given standby duration value.

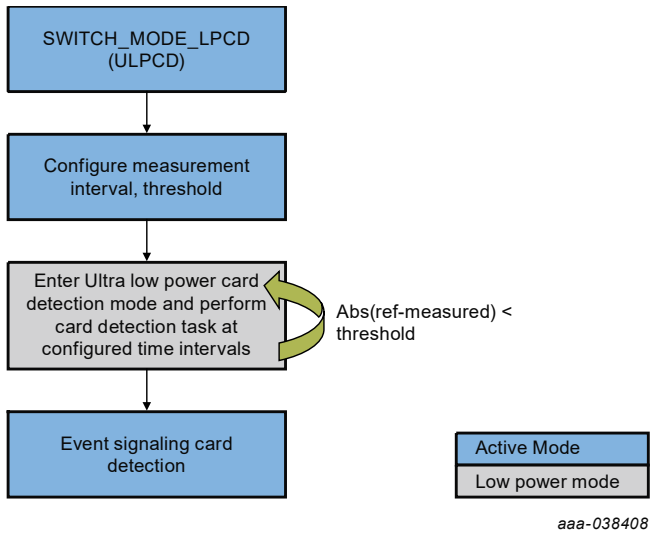


Figure 26. LPCD configuration and card detection loop

9.15.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN5190B1. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN5190B1.

The LPCD mode offers highest sensitivity at the cost of slightly higher current consumption compared to the ULPCD mode.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN5190B1 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

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The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

The SWITCH_MODE instruction allows entering the LPCD mode with a given standby duration value.

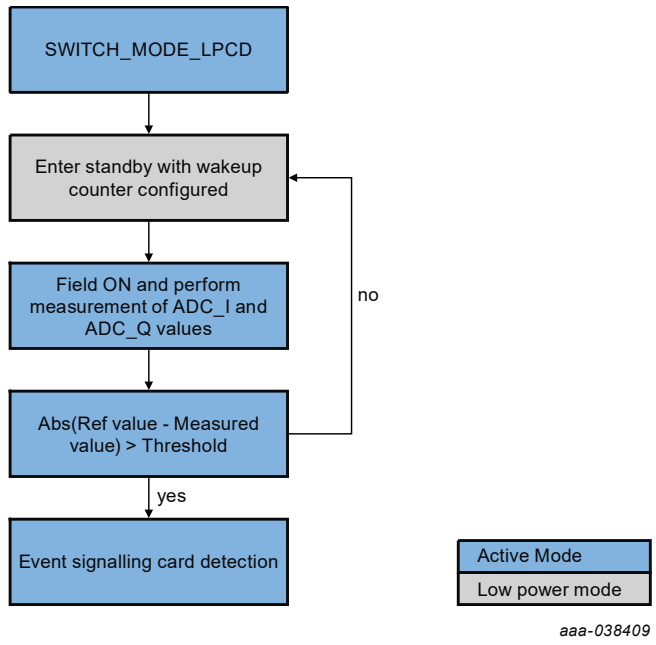


Figure 27. LPCD configuration

The LPCD mode is entered by the host interface command SWITCH_MODE_LPCD (23h), and terminated by the command SWITCH_MODE_NORMAL (20h). In addition, terminating the LPCD mode is possible by toggling a GPIO, by a reset (VEN) of the PN5190B1 or a signal of the RF Level detector.

Before entering the LPCD mode, ADC_I and ADC_Q reference value needs to be determined. This is done during the so-called calibration.

LPCD calibration phase

a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.

b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

The LPCD loop itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN5190B1.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, a LPCD_IRQ is raised to the host. The register configurations done by the host to support a dedicated RF protocol are not restored after wake-up command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, no LPC_IRQ is raised and the IC is set to the first phase (Standby mode) again.

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These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).

- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.

- NTS on host interface

- RF Level Detected

- GPIO toggle

As functionality from FW2.03 onwards, the GPIO1 (general-purpose input/output) pin can be enabled to wake up an external DC-DC from power down for the VDDPA supply. The GPO1 allows setting to high before the transmitter is switched on. This allows the wake-up of an external DC-DC from power down. The GPO1 can be set to low after the RF field is switched off to set an external DC-DC into Power-down mode. The time of toggling the GPO1 in relation to the RF-on and RF-off timings can be configured:

EEPROM field LpcdExtDcdcEnable (0xCE0) is used to enable the use of EXT DC-DC during LPCD.

EEPROM field: LpcdExtDcdcDelayToOn (0xCE1) is used to configure the delay to turn on the DC-DC in 8usecs steps.

EEPROM field: LpcdExtDcdcDelayToOff (0xCE2) is used to configure the delay to turn off the DC-DC in 8usecs steps.

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 12. Low-Power Card Detection: relevant EEPROM configuration

EEPROM address	Name	Description
0492	LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
0494	LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
0496	LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
049A	LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
04B5	LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
0013	XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). For fastest start-up this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

9.15.2 Semi-autonomous mode (LPCD)

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LPCD semi-autonomous mode

The LPCD can be invoked by the host in the semi-autonomous mode wherein the ADC_I and ADC_Q values that are measured is returned back to the host.

In this mode, standby is not entered and the difference between the measured and reference values are not checked against the threshold. Nevertheless, the host may check the measured values against a reference and threshold to detect a card and also put the PN5190B1 in Standby mode between measurements, using the SWITCH_MODE_STANDBY command.

This mode is especially useful to find optimized settings for the LPCD, since it does not offer no significant current saving.

Table 13. Low-Power Card Detection - semi-autonomous mode: relevant REGISTERS

REGISTER address	Name	Description
0050	LPCD_CALIBRATE_CTRL	Writing to this register triggers the LPCD calibration with the LPCD RSSI_HYSTERESIS and LPCD RSSI_TARGET values. After calibration is completed, calibration status is available in LPCD_ CALIBRATE_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ_CHANNEL_VALS
0051	IQ_CHANNEL_VALS	Actual I/Q channel value
0053	LPCD_CALIBRATE_STATUS	1: if successful - a new calibration clears this value

9.15.3 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET_N) of the PN5190B1.

The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX_LDO transmitter supply" or "Direct transmitter supply" is recommended.

Only the wake-up timer is active during ULP standby state.

The ULPCD comprises 2 phases:

1. **Calibration phase**
   In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.
2. **Measurement phase**
   In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the SWITCH_MODE_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN5190B1 into ultra-low power card detection state (ULP standby state) via the instruction SWITCH_MODE_LPCD.

XTAL_CHECK_DELAY (0013h) allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD_VOLTAGE_CTRL (address 4C6h)
- ULPCD_RSSI_GUARD_TIME (04C9h)

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- ULPCD_RSSI_SAMPLE_CFG (04CAh)
- ULPCD_THRESH_LVL(04CBh)
- ULPCD_GPIO3 (04CCh) - Allows to abort the ULPCD based on GPIO input.

Note: *The RF level detector acts as wakeup source for the ULPCD if activated. Since the RF level detector is very sensitive, it can contribute to an increased level of false wakeups. If no wakeup by the RF level detector is required by the application, it is recommended to deactivate the RF level detector before entering the ULPCD mode.*

9.16 Automatic EMD error handling

The PN5190B1 supports a configurable EMD handling according to the ISO14443 or EMVCo standard. To support further extensions or changes of these standards, the EMD block is configurable.

After being configured, the PN5190B1 restarts both the receiver and a timeout timer automatically without host interaction in case of a detected EMD event.

Features of the Automatic EMD Error Handling:

- No real-time constraints
- Less processing load on the host processor
- Configurable, anticipating future specification changes

In addition to the EMD error handling according to ISO14443 and EMVCo, the PN5190B1 implements special features for FeliCa™ preamble processing.

Registers CLIF_RX_EMD_1_CONFIG(0x47) and CLIF_RX_EMD_0_CONFIG(0x48) hold the configurations for the EMD configurations for ISO/IEC14443, and NFC Forum.

EMVCo EMD configuration is supported in the register EMD_CONTROL (0x03).

9.17 Autocoll (card emulation)

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC Forum Active and Passive Target activation (card emulation mode).

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip enters Standby mode automatically
- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip does not enter Standby mode.

At startup, the Autocoll state machine automatically performs a LOAD_RF_CONFIG with the General Target Mode Settings. When a technology is detected during activation, the Autocoll state machine performs an additional LOAD_RF_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled (EEPROM configuration), a random UID is generated after each RF-off.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own field.

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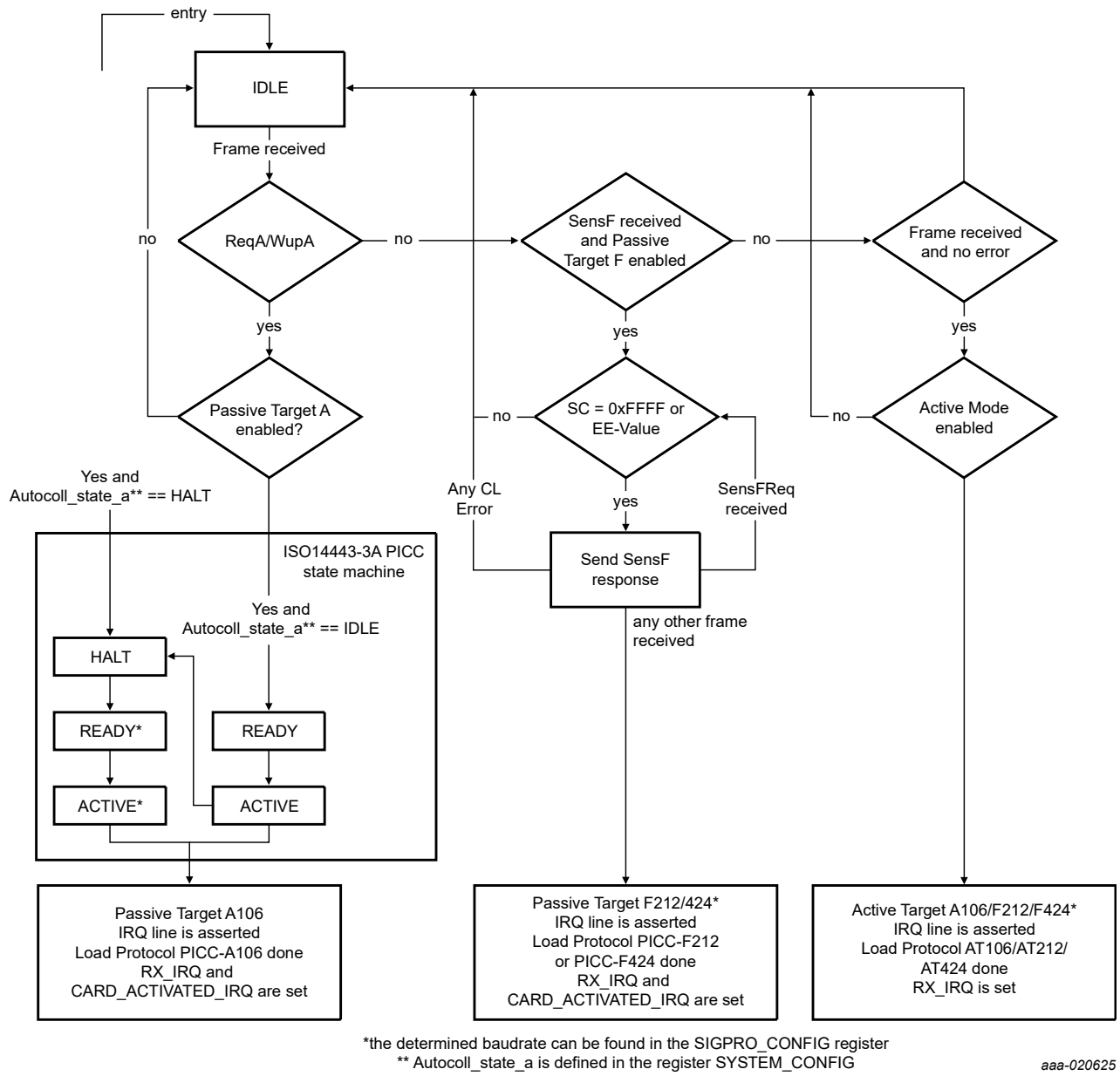


Figure 28. Autocoll state machine

9.18 RF-level detection

The PN5190B1 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

During ultra low-power card detection (ULPCD), a specific ultra low-power RF level detector is used as RF level detector(RFLD). This can be enabled as wake-up source.

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The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN5190B1 from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

9.19 Antenna connection

The PN5190B1 allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.

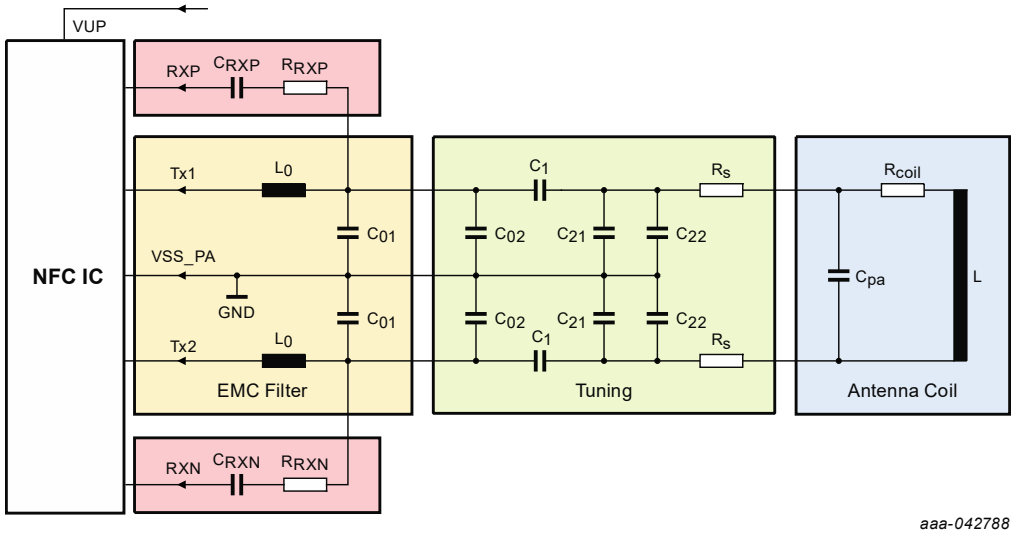


Figure 29. Push-Pull driver configuration

The PN5190B1 allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

Note:

*The RSSI Target for SE needs to be calculated as follows and differs from the differential antenna: RSSI Target = Target RX Peak Voltage*1024/ (1.8*2)*

*Example: For a 1.2 V target: DGRM_RSSI_TARGET = 1.2 * 1024 / (1.8*2) = 341d = 0x155*

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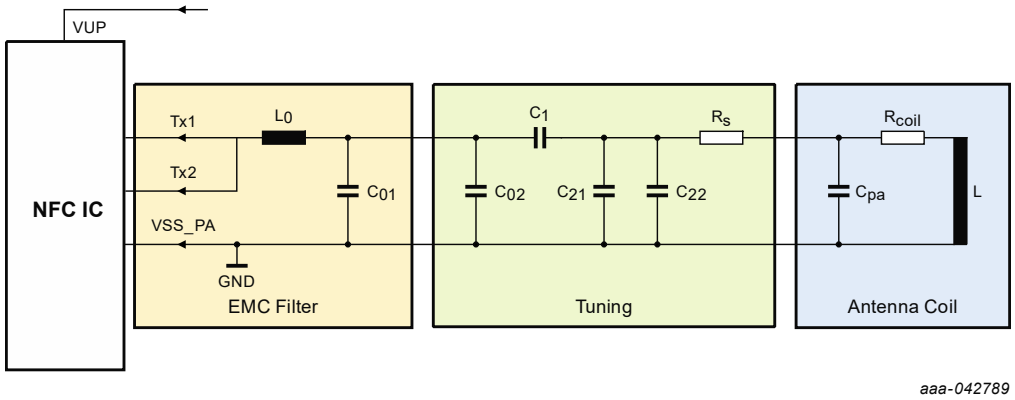


Figure 30. Push-Push driver configuration

The PN5190B1 allows to connect to antennas, one to each of the available driver outputs. The Figure below shows as well the receiver schematics for the RXN which is applicable for the Push-Push deriver configuration as well.

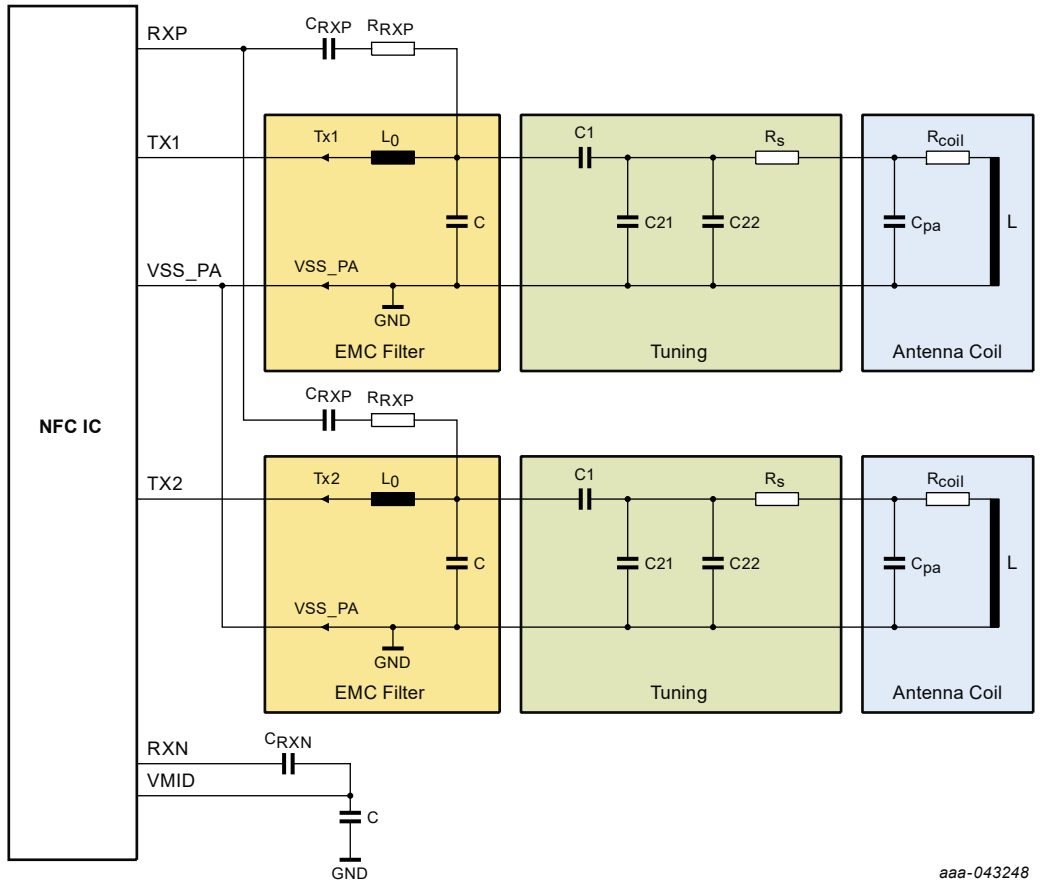


Figure 31. Two antennas connected to TX1, TX2 each

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Table 14. Antenna register configuration

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2	Single-Ended TX1 driving	Single-Ended TX2 driving
SS_TX_CFG (0x15) Stored as part of the RF protocol configuration	TX2_USE_ TX1_CONF	1b	1b	0b	0b
SS_TX1_ RMCFG (0x16)	TX1_CLK_ MODE_ TRANS_RM	111b	111b	111b	001b
SS_TX1_ RMCFG (0x16)	TX1_CLK_ MODE_MOD_ RM	111b	111b	111b	001b
SS_TX1_ RMCFG (0x16)	TX1_CLK_ MODE_CW_RM	111b	111b	111b	001b
SS_TX2_ RMCFG (0x17)	TX2_CLK_ MODE_ TRANS_RM	do not care	do not care	001b	111b
SS_TX2_ RMCFG (0x17)	TX2_CLK_ MODE_MOD_ RM	do not care	do not care	001b	111b
SS_TX2_ RMCFG (0x17)	TX2_CLK_ MODE_CW_RM	do not care	do not care	001b	111b
DGRM_RSSI (0x30) Stored as part of the RF protocol configuration	DGRM_RSSI_ TARGET	direct entry	as per calculation for SE (RSSI Target = Target RX Peak Voltage*1024/ (1. 8*2))	as per calculation for SE (RSSI Target = Target RX Peak Voltage*1024/ (1. 8*2))	as per calculation for SE (RSSI Target = Target RX Peak Voltage*1024/ (1. 8*2))
ANA_RX_ CTRL (0x43) Stored as part of the RF protocol configuration	RX_MIXER_ SE_MODE_EN	0	1	1	1
ANACTRL_ TX_CONFIG. TX_INVP_RM (0x44) Stored in EEPROM TX_INV_ RM (0018h) loaded during load protocol	TX_INVP_RM	10b	00b	no impact	no impact

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Table 14. Antenna register configuration*...continued*

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2	Single-Ended TX1 driving	Single-Ended TX2 driving
ANACTRL_ TX_CONFIG. TX_PWM_ MODE_RM (0x44) Stored in EEPROM TX_ SHAPING_ CONFIG (0017h), loaded during load protocol	TX_PWM_ MODE_RM	0b	0b	1b	1b

Note: *Recommendation is to use all the settings configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.*

Table 15. Antenna EEPROM configuration

EEPROM (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2	Single-Ended TX1 driving	Single-Ended TX2 driving
TX_SHAPING_ CONFIG (0x17)	0	0	0	1	1
RM_GLOBAL_TX_ SHAPING. bTX_INV_ RM (0x18)	-	0x02	0x00	do not care, leave default 0x02	do not care, leave default 0x02

9.20 Antenna tuning with variable capacitors

The PN5190B1 allows the tuning of the connected antenna based on variable capacitors.

Variable capacitors are devices which allow to change their capacity dependent on a supplied control voltage. Typically, these capacitors are used as serial and parallel capacitors in an antenna matching network.

The PN5190B1 allows to measure a detuning of the connected antenna caused e.g. by surrounding metal and correct the actual detuning by applying an appropriate control voltage on 2 analog outputs.

To correct a potential detuning of the connected antenna, a phase measurement needs to be performed. The following sequence is required to read out the phase information:

Step 1: Disable DPC

Step 2: Perform Type A-106 load protocol

Step 3: Set the VDDPA Voltage as $V_(Vddpa_AAT)$

Step 4: Perform RF ON

Step 5: Read out RXM phase

Step 6: Perform RF OFF

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Step 7: Enable DPC

For reading the RXM phase, refer to the related application note. Based on the phase information, a host is able to calculate the DAC output voltages to correct a detuning.

The antenna tuning requires the DPC to be disabled, and is typically not suitable for dynamic tuning e.g. during card communication.

Note:

Since disabling of the DPC requires a modification of the EEPROM is required, care must be taken not to exceed the maximum permitted number of Erase/Write cycles.

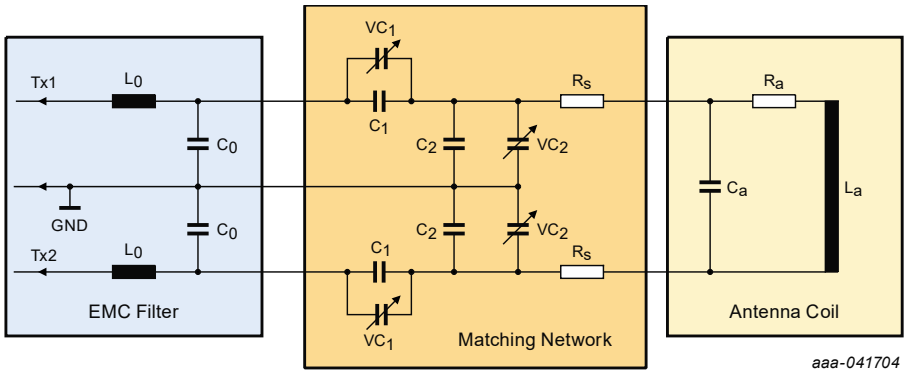


Figure 32. Antenna connection using variable capacitors

9.21 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN5190B1. The commands CONFIGURE_TESTBUS_DIGITAL (12h) and CONFIGURE_TESTBUS_ANALOG (13h) are used to configure the dedicated signal on an output pin.

If used, **ADC-Q needs to be routed always to AUX1, ADC-I needs to be routed always to AUX2**.

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

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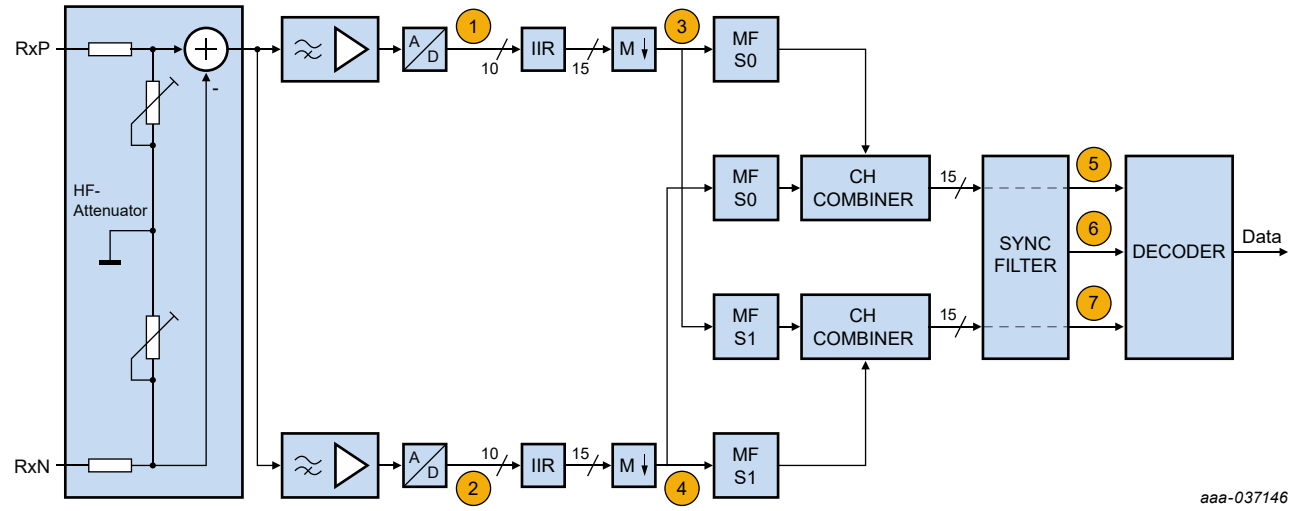


Figure 33. Receiver block diagram

Table 16. DEBUG SIGNALS

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_ tbcontrol_ patchbox0	adc_ data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
	obs_clif_ tbcontrol_ patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_ tbcontrol_ patchbox2	adc_ data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_ tbcontrol_ patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_ rm0	rm_cor_ adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_ rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_ rm2	rm_cor_ adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_ rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling
Output MF S0 (5)	obs_clif_sigpro_ rm4	mf_pt_ s0_d	14:8	Delayed matched filter S0 output, after CH combiner

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Table 16. DEBUG SIGNALS *...continued*

Signal	REGISTER	SIGNAL NAME	BITS	Description
				upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_rm6	mf_pt_s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106
Output Synchronization Filter (7)	obs_clif_sigpro_rm8	sync_filt_out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_sigpro		0	

Table 17. TRIGGER SIGNALS

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.

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Table 17. TRIGGER SIGNALS...*continued*

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
RX Enable	obs_clif_sigpro_rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

9.22 Secure firmware update

The PN5190B1 supports a secure update of the implemented firmware.

The secure firmware download mode is using dedicated commands, but does not require a dedicated physical handling of the SPI interface lines.

The secure firmware download mode is entered by setting a register in non-volatile memory followed by a trigger of the VEN pin.

The firmware binary file which is used to update the PN5190B1 is protected with an RSA signature and AES encryption.

The key length of the RSA is 2048 bits, the public exponent supports any 32-bit integer value.

A pre-computed Montgomery format of signature is used, and the signature hash computation is based on SHA256 algorithm.

This prevents a download of any other software which is not released by NXP.

An anti-tearing function is implemented in order to detect supply voltage removal or memory fault.

During the secure firmware download, the NFC operation is not available, only the command set defined for the secure firmware download is valid.

Updating the PN5190B1 with the default firmware binaries programs the memories for user configuration with default values. Any previous user configuration is overwritten. The user has to take care to restore the data of these memories after a secure firmware update.

If this is not intended, special firmware versions are available which do not overwrite the configuration. If the standard firmware file is named e.g. FW XX.YY, the name of the firmware which does not overwrite existing settings is then FW XX.FY. (The "F" is indicating the non-overwrite version)

The PN5190B1 checks if the new major version number is equal or higher than the current one. In case the major version number of the new firmware to be installed is smaller than the already installed version number of the firmware, the secure firmware update is rejected. Downgrading major firmware versions is therefore not possible. Upgrading and therefore increasing major firmware versions is always possible.

In case of any failure or exception during the download (e.g. caused by a communication error or power off), the PN5190B1 remains in the secure firmware download mode until a complete and valid NXP firmware is available in the device.

Features of the automatic secure firmware update:

- Works without download request pin
- No special implementation of SPI interface handling
- Maximum integrity: Only encrypted and signed firmware images download possible via the secure firmware update functionality

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- Updating the firmware overwrites existing all previous EEPROM configurations, unless a special version of the firmware was used.

9.23 SPI host interface

The interface of the PN5190B1 to a host microcontroller is based on a SPI interface.

The maximum SPI speed is 15 Mbit/s and fixed to CPOL = 0 and CPHA = 0. Only a half-duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer shall be written at once as well. No NSS assertion is allowed during data transfer.

The SPI host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of CPUs. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (pin VDDIO).

There is no external pull-up / pull-down resistor required, the SPI pads are automatically configured by the PN5190B1.

Only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.4 V.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

Controller in target out (MISO)

The MISO line is configured as an output in a target device. It is used to transfer data from the target to the controller, with the most significant bit sent first. The MISO signal is put into 3-state mode when NSS is high.

Controller out target in (MOSI)

The MOSI line is configured as an input in a target device. It is used to transfer data from the controller to a target, with the most significant bit sent first.

Serial clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

Not target select (NSS)

The target select input (NSS) line is used to select a target device. It shall be set to low before any data transaction starts and must stay low during the transaction.

9.24 Host interface commands

9.24.1 Logical command layer

PN5190B1 has two main modes of operation to communicate with the host controller:

1. TLV-command response-based communication

2. HDLL-based communication, used when device is triggered to enter the “download mode”, to update its firmware.

The description of the transport layer in the next chapters is limited to TLV-based command-response communication.

For more information, see ref.[3].

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9.24.1.1 Logical frame definition

A SPI frame starts with the falling edge of NSS and ends with the rising edge of NSS.

SPI is per physical definition full duplex but PN5190B1 uses SPI in a half-duplex mode.

SPI mode is limited to CPOL 0 and CPHA 0 with a max clock speed of 15 MHz.

Every SPI frame is composed of a 1-byte header and n-bytes of body.

9.24.1.2 Logical flow definition

The HOST always sends as a first byte the flow indication byte whether it wants to write or read data from the PN5190B1.

In case of a read request and no data is available, the response contains 0xFF.

The data after the flow indication byte is one or several messages.

For every NSS assertion, the first byte is always a HEADER (flow indication byte), it can be either 0x7F/0xFF with respect to write/read operation.

9.24.1.3 Logical message type definition

A host controller communicates with PN5190B1 using messages which are transported within SPI frames.

There are three different message types:

- Command
- Response
- Event

Commands are only sent from host controller to PN5190B1 responses.

Events are only sent from PN5190B1 to host controller.

Allowed sequences and rules:

- Command is always acknowledged by a response
- Host Controller is not allowed to send another command before receiving a response to a previous command, except in concatenation
- Events may be sent asynchronously at any time (NOT interleaved within a command/response pair)
- EVENT messages are never combined with the RESPONSE messages within one frame.

9.24.1.4 Logical message format

Type (T) => 1 byte

Bit[7] Message Type

0: COMMAND or RESPONSE message

1: EVENT message

Bit[6:0]: Instruction Code

Length (L) => 2 bytes (large endian format)

Length of the message body

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Value (V) => N bytes

Value/data of the TLV (Command Parameters / Response data) based on Length field (Large endian format)

9.24.1.5 Split frame definition

COMMAND message must be sent in one SPI frame RESPONSE and EVENT messages can be read in multiple SPI frames, e.g., to read out the length byte.

RESPONSE and EVENT messages can be read in single SPI frame but delayed by NO-CLOCK in between, e.g., to read out the length byte.

9.24.2 Host interface command list

PN5190B1 command/response list

Table 18. Host interface commands

Command code	PN5180 legacy command	Command
0x00	Yes	WRITE_REGISTER
0x01	Yes	WRITE_REGISTER_OR_MASK
0x02	Yes	WRITE_REGISTER_AND_MASK
0x03	Yes	WRITE_REGISTER_MULTIPLE
0x04	Yes	READ_REGISTER
0x05	Yes	READ_REGISTER_MULTIPLE
0x06	Yes	WRITE_EEPROM
0x07	Yes	READ_EEPROM
0x08	No	TRANSMIT_RF_DATA
0x09	No	RETRIEVE_RF_DATA
0x0A	No	EXCHANGE_RF_DATA
0x0B	Yes	MFC_AUTHENTICATE
0x0C	Yes	EPC_GEN2_INVENTORY
0x0D	Yes	LOAD_RF_CONFIGURATION
0x0E	Yes	UPDATE_RF_CONFIGURATION
0x0F	Yes	GET_ RF_CONFIGURATION
0x10	Yes	RF_ON
0x11	Yes	RF_OFF
0x12	Yes	CONFIGURE_ TESTBUS_DIGITAL (not available for engineering samples)
0x13	Yes	CONFIGURE_TESTBUS_ANALOG (not available for engineering samples)
0x14	No	CTS_ENABLE
0x15	No	CTS_CONFIGURE
0x16	No	CTS_RETRIEVE_LOG
0x17 - 0x18	-	RFU

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Table 18. Host interface commands*...continued*

Command code	PN5180 legacy command	Command
0x19	No	up to FW 2.01: RFU
		from FW2.03 onwards: RETRIEVE_RF_FELICA_EMD_DATA
0x1A	No	RECEIVE_RF_DATA
0x1B-0x1F	-	RFU
0x20	Yes	SWITCH_MODE_NORMAL
0x21	Yes	SWITCH_MODE_AUTOCOLL
0x22	Yes	SWITCH_MODE_STANDBY
0x23	No	SWITCH_MODE_LPCD
0x24	No	SWITCH_MODE_SUSPEND
0x25	No	SWITCH_MODE_DOWNLOAD
0x26	No	GET_DIE_ID
0x27	No	GET_VERSION
0x28	-	RFU
0x29	No	GET_CRC_USER_AREA (available from FW 2.6 onwards)
0x2A	-	up to FW 2.03: RFU
	No	available from FW 2.05 onwards: CONFIGURE_MULTIPLE_TESTBUS_DIGITAL
0x2B - 0x3F	-	RFU
0x40	-	RFU
0x41	No	PRBS_TEST
0x41 - 0x50	-	RFU

Below is a list of CLIF registers that are changed by the firmware between an RF Exchange followed by an RF Reset command:

Table 19. Register values changed by firmware between RF Exchange - RF Reset

Register name	After first exchange	RF Reset after first exchange	Changes done in RF-ON
CLIF_STATUS_REG (Read-Only)	04000001	04000000	NA
CLIF_CONTROL_REG	00000003	00000000	Command bit is set to IDLE
CLIF_CRC_RX_CONFIG_REG	00000008	00000009	RX CRC Is enabled
CLIF_CRC_TX_CONFIG_REG	00000008	00000009	TX CRC is enabled
CLIF_RXCTRL_STATUS_REG (Read-Only)	07758704	077D8704	NA

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Table 19. Register values changed by firmware between RF Exchange - RF Reset *...continued*

Register name	After first exchange	RF Reset after first exchange	Changes done in RF-ON
CLIF_DCOC_ STATUS_REG (Read-Only)	002607C8	001807B5	NA
CLIF_TIMER0_ CONFIG_REG	00000000	0000007D	Timer0 Configuration changes. But Timer not started
CLIF_TIMER0_ RELOAD_REG	00000000	00000109	Timer0 Configuration changes.
CLIF_TIMER3_ OUTPUT_REG	01000018	00000000	Timer3 Configuration changes.
CLIF_ANA_ STATUS_REG (Read-Only)	001E404B	001D9831	NA
CLIF_INT_ STATUS_REG (Read-Only)	00000000	00000004	NA
CLIF_INT_ ENABLE_REG (Read-Only)	00060F21	00068F21	NA

9.24.3 EVENTS INDICATED BY INTERRUPT

Normal events are indicated over IRQ.

The availability of a message (either RESPONSE or EVENT) is signalized with the IRQ going high, from low. IRQ stays high until all the response or event frame is read. Only after IRQ signal is low, the host can send the next command.

These normal events can be either

- always enabled - Host is always notified
- controlled by Host – Host is notified if the respective Event Enable bit is set in the register (EVENT_ENABLE).

Low-level interrupts from the peripheral IPs including the CLIF are completely handled within the firmware and the host will be notified only of the events listed in the events section.

The firmware implements two event registers as RAM registers that can be written / read using WRITE_REGISTER / READ_REGISTER commands.

Two registers do exist to handle the events from a host microcontroller: EVENT_ENABLE and EVENT_STATUS:

- EVENT_ENABLE => register, enables/disables specific event notifications
- EVENT_STATUS => content of this register is part of the event message payload

Events are autocleared once the event message is read-out by the host.

Events are asynchronous in nature and are notified to the host if they are enabled within the event register.

Following is the list of events available to the host as part of the event message:

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Table 20. IRQ EVENT LIST

BIT	EVENT	Always enabled	Value/Description
31..12	RFU	-	-
11	CTS_EVENT	N	
10	IDLE_EVENT	Y	
9	LP_CALIBRATION_EVENT	Y	
8	LPCD_EVENT	Y	
7	AUTOCOLL_EVENT	Y	
6	TIMER0_EVENT	N	
5	TX_OVERCURRENT_EVENT	N	
4	RFON_DET_EVENT	N	
3	RFOFF_DET_EVENT	N	
2	STANDBY_PREV_EVENT	Y	
1	GENERAL_ERROR_EVENT	Y	
0	BOOT_EVENT	Y	

Note that no two events are clubbed except in case of errors. In case of errors during the operation, functional event (e.g. BOOT_EVENT, AUTOCOLL_EVENT etc.) and GENERAL_ERROR_EVENT will be set.

9.24.4 EVENTS INDICATED ON GPIO

Temperature events are possible to be indicated by a GPIO to speed up the notification to a host.

The EEPROM register ENABLE_GPIO0_ON_OVERTEMP (0016h) allows enabling the indication of a temperature event on GPIO0.

No other event can be routed to a GPIO.

9.25 Register description

The default setting of a bit within a register is indicated by the "*". Value indicates the allowed range for the bits of a symbol.

Note, that some registers change its content by the firmware between an RF Exchange followed by an RF Reset command.

9.25.1 Register overview

Table 21. Register overview

Address (hex)	Address (decimal)	Name
0	0	SYSTEM_CONFIG
1	1	EVENT_ENABLE
2	2	EVENT_STATUS
3	3	EMD_CONTROL
4	4	FELICA_EMD_CONTROL

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Table 21. Register overview*...continued*

Address (hex)	Address (decimal)	Name
5	5	RX_STATUS
6	6	RX_STATUS_ERROR
7	7	CLIF_STATUS
8	8	TRANSCEIVE_CONTROL
9	9	TX_SYMBOL01_MOD
A	10	TX_SYMBOL1_DEF
B	11	TX_SYMBOL0_DEF
C	12	TX_SYMBOL23_MOD
D	13	TX_SYMBOL23_DEF
E	14	TX_SYMBOL_CONFIG
F	15	TX_FRAME_CONFIG
10	16	TX_DATA_MOD
11	17	TX_WAIT
12	18	TX_CRC_CONFIG
13	19	RFU
14	20	RFU
15	21	SS_TX_CONFIG
16	22	SS_TX1_RMCFG
17	23	SS_TX2_RMCFG
18	24	RFU
19	25	SS_TX_TRANS_CFG
1A-1C	26-28	RFU
1D	29	SIGPRO_CONFIG
1E	30	RFU
1F	31	PUBLIC_RESERVED
20	32	SIGPRO_RM_PATTERN
21	33	PUBLIC RESERVED
22	34	RFU
23-24	35-36	PUBLIC RESERVED
25	37	RX_PROTOCOL_CONFIG
26	38	RX_FRAME_LENGTH
27	39	RFU
28	40	RX_CTRL_STATUS
29	41	PUBLIC RESERVED
2A	42	SIGPRO_IIR_CONFIG0
2B-2C	43-44	PUBLIC RESERVED

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Table 21. Register overview*...continued*

Address (hex)	Address (decimal)	Name
2D	45	DGRM_BBA
2E	46	PUBLIC RESERVED
2F	47	RFU
30	48	DGRM_RSSI
31	49	RX_CRC_CONFIG
32	50	RX_WAIT
33	51	DCOC_CONFIG
34	52	RFU
35	53	RXM_CTRL
36	54	ANA_AGC_DCO_CTRL
37	55	RFU
38-3A	56-58	PUBLIC RESERVED
3B	59	SS_TX1_CMCFG
3C	60	SS_TX2_CMCFG
3D	61	TIMER0_CONFIG
3E	62	TIMER0_RELOAD
3F	63	RFU
40	64	RFU
41	65	ANA_STATUS
42	66	RFU
43	67	ANA_RX_CTRL
44	68	ANACTRL_TX_CONFIG
45-46	69-70	RFU
47	71	EMD_1_CONFIG
48	72	EMD_0_CONFIG
49-4F	73-79	RFU
50	80	LPCD_CALIBRATE_CTRL
51	81	IQ_CHANNEL_VALS
52	82	PAD_CONFIG
53	83	CALIBRATE_STATUS
54	84	TXLDO_VDDPA_CONFIG
55	85	GENERAL_ERROR_STATUS
56	86	TXLDO_VOUT_CURR
57	87	DAC
58	88	RFU
59	89	RXM_FREQ

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Table 21. Register overview*...continued*

Address (hex)	Address (decimal)	Name
5A	90	RXM_RSSI
5B	91	TEMP_SENSOR
5D	93	TX_NOV_CALIBRATE_AND_STORE
5E	94	DPC_CONFIFG
5F	95	TIMER0_OUTPUT (from FW 2.05 onwards)
60	96	TIMER1_OUTPUT (from FW 2.05 onwards)
61	97	TIMER2_CONFIG (from FW 2.05 onwards)
62	98	TIMER2_RELOAD (from FW 2.05 onwards)
63	99	TIMER2_OUTPUT (from FW 2.05 onwards)
64	100	Up to FW2.8 RFU DYNAMIC_POWERLEVEL_REDUCTION Available from FW2.9 onwards.
80	128	SS_TX1_RTRANS0
81	129	SS_TX1_RTRANS1
82	130	SS_TX1_RTRANS2
83	131	SS_TX1_RTRANS3
84	132	SS_TX1_RTRANS4
85	133	SS_TX1_RTRANS5
86	134	SS_TX1_RTRANS6
87	135	SS_TX1_RTRANS7
88	136	SS_TX1_RTRANS8
89	137	SS_TX1_RTRANS9
8A	138	SS_TX1_RTRANS10
8B	139	SS_TX1_RTRANS11
8C	140	SS_TX1_RTRANS12
8D	141	SS_TX1_RTRANS13
8E	142	SS_TX1_RTRANS14
8F	143	SS_TX1_RTRANS15

9.25.2 SYSTEM_CONFIG (0000h)

Table 22. SYSTEM_CONFIG register (address 0000h) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r/w	0*,1	-
8	TX_NOV_CALIBRATION	r/w	0*,1	One time calibration when the host writes a 1 into this register, a one time calibration is performed. ***Note:***

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Table 22. SYSTEM_CONFIG register (address 0000h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				The calibration is resulting a short RF-on. All the power configurations shall the configured before setting this bit.
7	RFU	r/w	0	-
6:5	15693_CHANGE_DATARATE	r/w	0*,1	15693_changedatarate 0 - RFU 1 - Change data rate to 53kB/sec 2 - Change data rate to 106kB/sec 3 - Change data rate to 212kB/sec By default, the basic data rate of 26kB/sec is loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers are updated automatically.
4	up to FW 2.03: RFU	r/w	0*,1	-
	from FW 2.05 onwards: FAST_FIELD_ON	r/w	0*,1	0 - Field ON Duration includes time interval to start TXLDO and DC-DC as part of RF ON 1 - Field ON Duration is reduced as TXLDO and DC-DC remains ON and only TX Driver is Enabled/ Disabled as part of RF ON
3	AUTOCOLL STATE A	r/w	0*,1	0: TypeA Card mode: Autocoll entry with IDLE state of the card 1: TypeA Card mode: Autocoll entry with HALT state of the card
2	SOFT RESET	r/w	0*,1	Performs a soft reset of the system, all registers are set to default values
1	MF CRYPTO ON	r/w	0*,1	If set to 1 the MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption
0	RFU	r/w	0*,1	-

Note: *For firmware versions up to V2.02, the SYSTEM_CONFIG register requires to be initialized with value 0x00 upon every Power-On Reset. This initialization is not required for firmware versions V2.03 or higher.*

9.25.3 EVENT_ENABLE (0001h)

Table 23. EVENT_ENABLE register (address 0001h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	r	0*,1	-
11	CTS_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
10	IDLE_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
9	LP_CALIBRATION_EVENT_ ENABLE	r/w	0*,1	Enable the corresponding event
8	LPCD_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
7	AUTOCOLL_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
6	TIMER0_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event

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Table 23. EVENT_ENABLE register (address 0001h) bit description...*continued*

Bit	Symbol	Access	Value	Description
5	TX_OVERCURRENT_ERROR_ EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
4	RFON_DET_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
3	RFOFF_DET_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
2	STANDBY_PREV_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event
1	GENERAL_ERROR_EVENT_ ENABLE	r/w	0*,1	Enable the corresponding event
0	BOOT_EVENT_ENABLE	r/w	0*,1	Enable the corresponding event

9.25.4 EVENT_STATUS (0002h)

Table 24. EVENT_STATUS register (address 0002h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	r	0*,1	-
11	CTS_EVENT	r	0*,1	Indicated the availability of CTS Event
10	IDLE_EVENT	r	0*,1	Indicated the availability of IDLE event.
9	LP_CALIBRATION_EVENT	r	0*,1	Indicated the availability of LP Calibration event
8	LPCD_EVENT	r	0*,1	Indicated the availability of LPCD event.
7	AUTOCOLL_EVENT	r	0*,1	Indicated the availability of Autocoll event
6	TIMER0_EVENT	r	0*,1	Indicated the availability of Timer0 event
5	TX_OVERCURRENT_ERROR_ EVENT	r	0*,1	Indicated the availability of transmitter over current error. This bit is set, when the current on the TX driver is higher than the defined threshold in the EEPROM. Upon this condition, the field is automatically switched OFF before the notification to the host.
4	RFON_DET_EVENT	r	0*,1	Indicated the availability of RF ON detected.
3	RFOFF_DET_EVENT	r	0*,1	Indication of external RF OFF detected
2	STANDBY_PREV_EVENT	r	0*,1	Indicated the availability of Standby Prevention reason.
1	GENERAL_ERROR_EVENT	r	0*,1	Indicated the availability of General Error event.
0	BOOT_EVENT	r	0*,1	Indicated the availability of Boot event.

9.25.5 EMD_CONTROL (0003h)

To activate the EMVCo EMD handling of the PN5190B1, the following bits of the register need to be set as follows:

0001b: EMD_ENABLE

1b: EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD

0001b: EMD_NOISE_BYTES_THRESHOLD

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Table 25. EMD_CONTROL register (address 0003h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	rw	0*,1	-
11:10	EMD_RM_EMD_SENSITIVITY	rw	0*,1	RM EMD SENSITIVITY value that will be applied to SIGPRO_RM_CONFIG, At layer 4, when EMD is enabled, the value of EMD_RM_SENSITIVITY can be lowered to ensure robust EMD suppression, if during the layer 3 activation, the value of EMD_RM_SENSITIVITY in the protocol area is set to a high value to ensure collision detection and resolution when multiple typeA cards are presented at close distance to the antenna.
9:8	EMD_TRANSMISSION_TIMER_USED	rw	0*,1	Timer used for RF communication.
7	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B	rw	0*,1	Missing CRC treated as protocol error in » case of Type B based communication P » case of Type B based communication
6	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A	rw	0*,1	Missing CRC treated as protocol error in » case of Type A based communication P » case of Type A based communication
5:2	EMD_NOISE_BYTES_THRESHOLD	rw	0*,1	Defines the threshold under which transmission errors are treated as noise. Note: CRC bytes are NOT included/counted!
1	EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD	rw	0*,1	Transmission errors with received byte length >= EMD_NOISE_BYTES_THRESHOLD is never treated as EMD (can be used for versions below EMVCo3.0)
0	EMD_ENABLE	rw	0*,1	EMD handling enabled If this register is enabled by setting EMVCO_EMD_ENABLE=1, the registers EMD_0_CONFIG and EMD_1_CONFIG is ignored for the EMVCO_EMD function.

9.25.6 FELICA_EMD_CONTROL (0004h)

Table 26. FELICA_EMD_CONTROL register (address 0004h) bit description

Bit	Symbol	Access	Setting for FeliCa EMD handling	Value	Description
31:24	FELICA_EMD_RC_BYTE_VALUE	rw	0	0*,1	FeliCa RC byte value that needs to be received does not treat the frame as EMD
23:16	FELICA_EMD_LENGTH_BYTE_MAX	rw	0	0*,1	Maximum Length byte value that needs to be received does not treat the frame as EMD
15:8	FELICA_EMD_LENGTH_BYTE_MIN	rw	0	0*,1	Minimum Length byte value that needs to be received does not treat the frame as EMD
7:5	RESERVED	rw	0	0*,1	-

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Table 26. FELICA_EMD_CONTROL register (address 0004h) bit description...*continued*

Bit	Symbol	Access	Setting for FeliCa EMD handling	Value	Description
6	FELICA_EMD_LOG_ENABLE	rw	0 or 1	0*1	Log Enable bit to send RX Status during EMD
5	FELICA_EMD_RC_CHECK_ ON_CRC_CORRECT_ENABLE	rw	0 or 1	0*1	RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed
4	FELICA_EMD_INTEGRITY_ ERR_CHECK_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled when integrity error is set
3	FELICA_EMD_PROTOCOL_ ERR_CHECK_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled when protocol error is set
2	FELICA_EMD_RC_CHECK_ ENABLE	rw	0	0*,1	FeliCa RC byte check enabled for FeliCa EMD handling
1	FELICA_EMD_LEN_CHECK_ ENABLE	rw	0	0*,1	FeliCa Length byte check enabled for FeliCa EMD handling
0	FELICA_EMD_ENABLE	rw	1	0*,1	FeliCa EMD handling enabled

Recommended value for FeliCa EMD handling: 00FF0019h

9.25.7 RX_STATUS (0005h)

Table 27. RX_STATUS register (address 0005h) bit description

Bit	Symbol	Access	Value	Description
31:27	RFU	r	0*,1	-
26:20	RX_COLL_POS	r	0*,1	Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken into account (RX_ COLL_POS = physical bit position in the flow + RX_ BIT_ALIGN value). Indicates the collision position in the first 8 bytes only. Can be used during the TypeA/ICODE/EPC anti-collision procedure.0x00 - first bit 0x01 - second bit... 0x7F - 128th bit. The status register is not updated by the collision detected on stop or parity bit.
19:17	RX_NUM_LAST_BITS	r	0*,1	Indicating the number of valid bits in the last byte received. 0: all bits are valid 1: 1 bit is valid …. 7: - 7 bits are valid This is generally used during ISO/IEC14443 type A anti-collision
16:13	RX_NUM_FRAMES_RECEIVED	r	0*,1	Indicates the number of frames received. The value is updated after every normal frame reception in RX_ MULTIPLE mode.

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Table 27. RX_STATUS register (address 0005h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				The value is valid only if the bit RX_MULTIPLE_ ENABLE==’1’.
12:0	RX_NUM_BYTES_RECEIVED	r	0*,1	Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ ENABLE=='1'.

9.25.8 RX_STATUS_ERROR (0006h)

Table 28. RX_STATUS_ERROR register (address 0006h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU	r	0*,1	
29	EMD_DETECTED_IN_RXDEC	r	0*,1	The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception.
28	EMD_DETECTED_IN_SIGPRO	r	0*,1	The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception.
27	EXT_RFOFF_DETECTED	r	0*,1	The high level indicates that the external RF-field vanished during the reception
26	RX_FRAME_MAXLEN_VIOL	r	0*,1	The high level indicates that the received frame length violated the configured maximum limit
25	RX_FRAME_MINLEN_VIOL	r	0*,1	The high level indicates that the received frame length violated the configured minimum limit.
24	RX_FRAME_LE_CRC	r	0*,1	The high level indicates that the received frame length is less or equal to the expected CRC field length.
23	RX_NOT_FULL_BYTE	r	0*,1	The high level indicates that the last received character in the frame has less than 8 bits.
22	RX_MISSING_PARBIT_ DETECTED	r	0*,1	The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent.
21	RX_MISSING_STOPBIT_ DETECTED	r	0*,1	The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent.
20	RX_COLLISION_PARBIT_ DETECTED	r	0*,1	The high level indicates that the collision was detected on the parity bit position.
19	RX_COLLISION_STOPBIT_ DETECTED	r	0*,1	The high level indicates that the collision was detected on the stop bit position.
18	RX_COLLISION_DETECTED	r	0*,1	The high level indicates that the collision was detected during the frame reception.
17	RX_STOP_ON_RXOVER	r	0*,1	The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception.
16	RX_STOP_ON_RFOFF	r	0*,1	The high level indicates that the frame reception was interrupted by external RF-field vanishing event.

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Table 28. RX_STATUS_ERROR register (address 0006h) bit description*...continued*

Bit	Symbol	Access	Value	Description
15	RX_STOP_ON_ERR	r	0*,1	The high level indicates that the frame reception was stopped by detected communication error event.
14	RX_STOP_ON_LEN	r	0*,1	The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM).
13	RX_STOP_ON_INVPAR	r	0*,1	The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212-848 kbit/s modes.
12	RX_STOP_ON_PATTERN	r	0*,1	The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.
11	RX_STOP_ON_ANTICOLL	r	0*,1	The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbit/s mode during the anti-collision procedure.
10	RX_CRC_ERROR	r	0*,1	The high level indicates that the CRC error is detected in the received frame.
9	RX_LEN_ERROR	r	0*,1	The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_FRAME_MAX LEN] limits. Can assert only in the mode where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM).
8	RX_SIGPRO_ERROR	r	0*,1	The high level indicates that the communication error/errors were detected during the frame reception on physical layer(in the SigPro).
7	RX_PARITY_ERROR	r	0*,1	The high level indicates that the parity error was detected during the frame reception.
6	RX_STOPBIT_ERROR	r	0*,1	The high level indicates that the stop bit error (‘0’ level instead of ‘1’ on the stop bit position) was detected during the frame reception.
5	RX_WRITE_ERROR	r	0*,1	The high level indicates that the error acknowledge status was received on the CLIF-system interface during the received frame transmission to the System RAM.
4	RX_BUFFER_OVFL_ERROR	r	0*,1	The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the FeliCa RM mode only.
3	RX_LATENCY_ERROR	r	0*,1	The high level indicates that the write request flow was corrupted due to traffic congestion on

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Table 28. RX_STATUS_ERROR register (address 0006h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				the system interface during the received frame transmission to the System RAM.
2	RX_DATA_INTEGRITY_ERROR	r	0*,1	The high level indicates that the data integrity corruption (parity/CRC/etc error) was detected in the received frame.
1	RX_PROTOCOL_ERROR	r	0*,1	The high level indicates that the protocol requirements violation (stop bit error, missing parity bit, not full byte received, etc.) was detected in the received frame.
0	RX_CL_ERROR	r	0*,1	The high level indicates that some protocol/data integrity erorr/errors were detected during the frame reception

9.25.9 CLIF_STATUS (0007h)

Table 29. CLIF_STATUS register (address 0007h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU	r	0*,1	-
29	CRC_OK	r	0*,1	This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only be evaluated at the end of a communication
28	RX_SC_DETECTED	r	0*,1	Status signal indicating that a subcarrier is detected.
27	RX_SOF_DETECTED	r	0*,1	Status signal indicating that a SOF has been detected.
26	TX_RF_STATUS	r	0*,1	If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself.
25	RF_DET_STATUS	r	0*,1	If set to 1 this bit indicates that an external RF-Field is detected by the RF level detectors (after digital filtering)
24	ADC_Q_CLIPPING	r	0*,1	Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
23	ADC_I_CLIPPING	r	0*,1	Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
22:12	RFU	r	0*,1	-
11	TX_NO_DATA_ERROR	r	0*,1	This error flag is set to 1. in case a transmission is started but no data is available (register NumBytes ToSend == 0).
10:8	RF_ACTIVE_ERROR_CAUSE	r	0*,1	This status flag indicates the cause of an NFC-Active error. Note: These bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1. 0*

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Table 29. CLIF_STATUS register (address 0007h) bit description*...continued*

Bit	Symbol	Access	Value	Description
				No Error. reset value 1 External field was detected on within TIDT timing 2 External field was detected on within TADT timing 3 No external field was detected within TADT timings 4 Peer did switch off RF Field without but no RX event was raised (no data received) 5 - 7 Reserved.
7:6	RFU	r	0*,1	-
5	RX_ENABLE	r	0*,1	This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled and is now ready for data reception
4	TX_ACTIVE	r	0*,1	This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state.
3	RX_ACTIVE	r	0*,1	This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state.
2:0	RF_EXCHANGE_STATE	r	0*,1	These registers hold the command bits 0* IDLE state 1 WaitTransmit state 2 Transmitting state 3 WaitReceive state 4 WaitForData state 5 Receiving state 6 LoopBack state 7 reserved

9.25.10 TRANSCEIVE_CONTROL (0008h)

To meet the ISO14443A FDT with an accuracy of 1 carrier clock cycle, there is support implemented to synchronize the guard time prescaler to the modified Miller envelope pulses (end of pulse). For adjustment, there is a 7-bit wide configuration register - TX_BITPHASE - which allows to adjust the FDT in the range of 0 to 128 carrier clock cycles. As defined in the ISO14443 the adjustment is different, depending on the data bit value of the data stream. For correct bit grid calculation, the prescaler must be set to a value corresponding exactly to one etu - for 106 kbit/s this corresponds to 0x7F. Otherwise the FdT will be incorrect.

Table 30. TRANSCEIVE_CONTROL register (address 0008h) bit description

Bit	Symbol	Access	Value	Description
31:16	RFU	r	0*,1	-
15:8	TX_BITPHASE	r/w	0*,1	Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is applicable for CardMode only.
7:3	RFU	r/w	0*,1	-
2	RX_MULTIPLE_ENABLE	r/w	0*,1	If this bit is set to 1. the receiver is reactivated after the end of a reception.
1:0	RFU	r/w	0*,1	-

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9.25.11 TX_SYMBOL01_MOD (0009h)

Table 31. TX_SYMBOL01_MOD register (address 0009h) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	rw	0*,1	-
23:16	TX_S01_MODWIDTH	rw	0*,1	Specifies the length of a pulse for sending data of symbol 0/1. The length is given by the number of carrier clocks + 1.
15:9	RFU	rw	0*,1	-
8	TX_S01_MILLER_ENABLE	rw	0*,1	If set to 1. pulse modulation is applied according to modified miller coding.
7	TX_S01_INV_ENV	rw	0*,1	If set to 1. the output envelope is inverted.
6:4	TX_S01_ENV_TYPE	rw	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU.
3	TX_S01_SC_FREQ	rw	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_S01_BIT_FREQ	rw	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.25.12 TX_SYMBOL1_DEF (000Ah)

Table 32. TX_SYMBOL1_DEF register (address 000Ah) bit description

Bit	Symbol	Access	Value	Description
31:0	TX_SYMBOL1_DEF	rw	0*,1	Pattern definition for Symbol1

9.25.13 TX_SYMBOL0_DEF (000Bh)

Table 33. TX_SYMBOL0_DEF register (address 000Bh) bit description

Bit	Symbol	Access	Value	Description
31:0	TX_SYMBOL0_DEF	rw	0*,1	Pattern definition for Symbol0

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9.25.14 TX_SYMBOL23_MOD (000Ch)

Table 34. TX_SYMBOL23_MOD register (address 000Ch) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r	0*,1	-
23:16	TX_S23_MODWIDTH	r/w	0*,1	Specifies the length of a pulse for sending data of symbol 2/3. The length is given by the number of carrier clocks + 1.
15:9	RFU	r/w	0*,1	-
8	TX_S23_MILLER_ENABLE	r/w	0*,1	If set to 1 pulse modulation is applied according to modified miller coding
7	TX_S23_INV_ENV	r/w	0*,1	If set to 1 the output envelope is inverted.
6:4	TX_S23_ENV_TYPE	r/w	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU
3	TX_S23_SC_FREQ	r/w	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_S23_BIT_FREQ	r/w	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.25.15 TX_SYMBOL23_DEF (000Dh)

Table 35. TX_SYMBOL23_DEF register (address 000Dh) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r	0*,1	-
23:16	TX_SYMBOL3_DEF	r/w	0*,1	Pattern definition for Symbol3
15:8	RFU	r/w	0*,1	-
7:0	TX_SYMBOL2_DEF	r/w	00000h* - FFFFFh	Pattern definition for Symbol2

9.25.16 TX_SYMBOL_CONFIG (000Eh)

Table 36. TX_SYMBOL_CONFIG register (address 000Eh) bit description

Bit	Symbol	Access	Value	Description
31	RFU		0*,1	-
30:27	TX_SYMBOL1_BURST_LEN	r/w	00000h* - FFFFFh	Specifies the number of bits issued for symbol 1 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit

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Table 36. TX_SYMBOL_CONFIG register (address 000Eh) bit description...*continued*

Bit	Symbol	Access	Value	Description
26	TX_SYMBOL1_BURST_TYPE	r/w	0*,1	Specifies the type of the burst of Symbol1 (logical zero / logical one)
25	TX_SYMBOL1_BURST_ONLY	r/w	0*,1	If set to 1. Symbol1 consists only of a burst and no symbol pattern
24	TX_SYMBOL1_BURST_ ENABLE	r/w	0*,1	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL1_BURST_LEN is enabled
23	RFU	r	0*,1	-
22:19	TX_SYMBOL0_BURST_LEN	r/w	0*,1	Specifies the number of bits issued for symbol 0 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit
18	TX_SYMBOL0_BURST_TYPE	r/w	0*,1	Specifies the type of the burst of Symbol0 (logical zero / logical one)
17	TX_SYMBOL0_BURST_ONLY	r/w	0*,1	If set to 1. Symbol0 consists only of a burst and no symbol pattern
16	TX_SYMBOL0_BURST_ ENABLE	r/w	0*,1	If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL0_BURST_LEN is enabled
15:13	TX_SYMBOL3_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol3. The range is from 1 bit (value 0000) to 8 bit (value 111)
12:10	TX_SYMBOL2_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol2. The range is from 1 bit (value 0000) to 8 bit (value 111)
9:5	TX_SYMBOL1_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol1. The range is from 1 bit (value 0000) to 31 bits (value 11110)
4:0	TX_SYMBOL0_LEN	r/w	0*,1	Specifies the number of valid bits of the symbol definition of Symbol0. The range is from 1 bit (value 0000) to 31 bits (value 11110)

9.25.17 TX_FRAME_CONFIG (000Fh)

Table 37. TX_FRAME_CONFIG register (address 000Fh) bit description

Bit	Symbol	Access	Value	Description
31:19	RFU	r	0*,1	-
18:16	TX_DATA_CODE_TYPE	r/w	0*,1	Specifies the type of encoding of data to be used 000b No special code 001b 1 out of 4 code [ICODE SLI] 010b 1 out of 256 code [ICODE SLI] 011b Pulse interval encoding (PIE) [ICODE EPC-V2] 100b 2bit tupple code (intended only for test purpose) 101-111b Reserved
15:13	TX_STOPBIT_TYPE	r/w	0*,1	Enables the stop bit (logic 1) and extra guard time (logic 1). The value 0 disables transmission of stop-bits. 000b no stop-bit. no EGT 001b stop-bit. no EGT

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Table 37. TX_FRAME_CONFIG register (address 000Fh) bit description...*continued*

Bit	Symbol	Access	Value	Description
				010b stop-bit + 1 EGT 011b stop-bit + 2 EGT 100b stop-bit + 3 EGT 101b stop-bit + 4 EGT 110b stop-bit + 5 EGT 111b stop-bit + 6 EGT
12	TX_STARTBIT_ENABLE	r/w	0*,1	If set to 1. a start-bit (logic 0) will be sent
11	TX_MSB_FIRST	r/w	0*,1	If set to 1. data bytes are interpreted MSB first for data transmission
10	TX_PARITY_LAST_INV_ ENABLE	r/w	0*,1	If set to 1. the parity bit of last sent data byte is inverted
9	TX_PARITY_TYPE	r/w	0*,1	Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated
8	TX_PARITY_ENABLE	r/w	0*,1	If set to 1. a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero. then a NO_DATA_ERROR occurs.
7:5	RFU	r	0*,1	-
4	TX_DATA_ENABLE	r/w	0*,1	If set to 1. transmission of data is enabled otherwise only symbols are transmitted.
3:2	TX_STOP_SYMBOL	r/w	0*,1	Defines which pattern symbol is sent as frame stop-symbol 00b No symbol is sent 01b Symbol1 is sent 10b Symbol2 is sent 11b Symbol3 is sent
1:0	TX_START_SYMBOL	r/w	0*,1	Defines which symbol pattern is sent as frame start-symbol 00b No symbol pattern is sent 01b Symbol0 is sent 10b Symbol1 is sent 11b Symbol2 is sent

9.25.18 TX_DATA_MOD (0010h)

Table 38. TX_DATA_MOD register (address 0010h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24	TX_ICODE_DATA_MODWIDTH_ ENABLE	r/w	0*,1	Enables modulation width of icode data. Width of modulation is defined by the TX_DATA_MODWIDTH field. When 1, we should have TX_DATA_ENV_ TYPE=0 and TX_DATA_INV_ENV=0
23:16	TX_DATA_MODWIDTH	r/w	0*,1	Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1.
15:9	RFU	r	0*,1	-
8	TX_DATA_MILLER_ENABLE	r/w	0*,1	If set to 1 pulse modulation is applied according to modified miller coding
7	TX_DATA_INV_ENV	r/w	0*,1	If set to 1 the output envelope is inverted
6:4	TX_DATA_ENV_TYPE	r/w	0*,1	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ

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Table 38. TX_DATA_MOD register (address 0010h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				(pulse of half bit length at beginning of bit) 110b Manchester tupple coding 111b RFU
3	TX_DATA_SC_FREQ	r/w	0*,1	Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz
2:0	TX_DATA_BIT_FREQ	r/w	0*,1	Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.

9.25.19 TX_WAIT (0011h)

To guarantee correct protocol timing a guard period timer is implemented for the RF_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time TX_WAIT is started after the end of a reception no matter if the frame is correct or erroneous.

It is not started in case the reception is restarted because of an EMD-event or in case the RX_MULTIPLE_ENABLE bit is set to 1 the TX_WAIT.

In case the register flag TX_WAIT_RFON_ENABLE is set to 1 the guard time timer is started when the devices own RF-Field was switched on.

It is possible to disable the guard time tx_wait by setting the register TX_WAIT_VALUE to 00h.

TX_WAIT can be used for 2 different purposes:

1. It can be used to prevent start of transmission before a certain period has expired - even if FW already finished data processing and set the START_SEND bit. This behavior is mainly intended for reader mode to guaranteed PICC to PCD frame delay time (FDT).

2. TX_WAIT time can be used to start the transmission at an exactly defined time.

Table 39. TX_CLIF_WAIT register (address 0011h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU	r	0*,1	-
27:8	TX_WAIT_VALUE	r/w	0*,1	Defines the tx_wait timer reload value. Note: If set to 00000h the tx_wait timer guard time is disabled Note: This bit is set by HW a protocol is detected in automatic mode detection
0	TX_WAIT_PRESCALER	r/w	0*,1	Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detection

9.25.20 TX_CRC_CONFIG (0012h)

Table 40. TX_CRC_CONFIG (address 0012h) bit description

Bit	Symbol	Access	Value	Description
31:16	TX_CRC_PRESET_VALUE	r/w	0*-FFFFh	Arbitrary preset value for the TX-Encoder CRC calculation.

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Table 40. TX_CRC_CONFIG (address 0012h) bit description...*continued*

Bit	Symbol	Access	Value	Description
15:7	RFU	r/w	0	Reserved
6	TX_CRC_BYTE2_ENABLE	r/w	0*,1	If set; the CRC is calculated from the second byte onwards (intended for HID). This option is used in the TX-Encoder.
5:3	TX_CRC_PRESET_SEL	r/w	000-101b	Preset values of the CRC register for the TX-Encoder. For a CRC calculation using 5 bits, only the LSByte is used.
			000b*	0000h, reset value
			001b	6363h
			010b	A671h
			011b	FFFFh
			100b	0012h
			101b	E012h
			110b	RFU
			111b	Use arbitrary preset value TX_CRC_PRESET_ VALUE
2	TX_CRC_TYPE	r/w	0*,1	Controls the type of CRC calculation for the TX-Encoder
			0*	16-bit CRC calculation, reset value
			1	5-bit CRC calculation
1	TX_CRC_INV	r/w	0*,1	Controls the sending of an inverted CRC value by the TX-Encoder
			0*	Not inverted CRC checksum, reset value
			1	Inverted CRC checksum
0	TX_CRC_ENABLE	r/w	0*, 1	If set to one, the TX-Encoder computes and transmits a CRC.

9.25.21 SS_TX_CONFIG (0015h)

Table 41. SS_TX_CONFIG register (address 0015h) bit description

Bit	Symbol	Access	Value	Description
31:14	RFU	r	0*,1	-
13	TX2_USE_TX1_CONF	r/w	0*,1	When 1, the tx1 configuration is used also for tx2: all SS_TX2_* registers are discarded and configurations from corresponding SS_TX1_* register is used.
12:6	RFU	r/w	0*,1	-
5:3	TX2_CLK_MODE_DEFAULT	r/w	0*,1	TX2 clk mode without field (RM and CM)
2:0	TX1_CLK_MODE_DEFAULT	r/w	0*,1	TX1 clk mode without field (RM and CM)

There are 5 choices for the RF output stage behavior during 100 % modulation, and one setting for 10 % modulation. The antenna driver TX1 clk mode and TX2 clk mode are possible to be configured as such:

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Table 42. Settings for Antenna drivers TX1 and TX2

TX_CLK_MODE_RM (binary)	Tx1 and TX2 output	Remarks
000	High-impedance	High-impedance of the transmitters (field-off)
001	0	Output pulled to 0 in any case
010	1	Output pulled to 1 in any case
110	RF high side push	Open-drain, only high side (push) MOS supplied with clock
101	RF low side pull	Open-drain, only low side (pull) MOS supplied with clock
111	13.56 MHz clock	Push/pull operation

9.25.22 SS_TX1_RMCFG (0016h)

Table 43. SS_TX1_RMCFG register (address 0016h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24:22	TX1_CLK_MODE_TRANS_RM	r/w	0*,1	TX1 clock mode in RM during transition
21:19	TX1_CLK_MODE_MOD_RM	r/w	0*,1	TX1 clock mode of modulated wave in RM 000: TX1=High-Z 001: TX1=VSS_PA 010 - 110: RFU 111: TX1 clocked normal operation
18:16	TX1_CLK_MODE_CW_RM	r/w	0*,1	TX1 clock mode of modulated wave in RM 000: TX1=High-Z 001: TX1=VSS_PA 010 - 110: RFU 111: TX1 clocked normal operation
15:8	TX1_AMP_MOD_RM	r/w	0*,1	TX1 amplitude of modulated wave in RM (0x00 = 0% modulaton, 0xFF: 100% modulation)
7:0	TX1_AMP_CW_RM	r/w	0*,1	TX1 amplitude of unmodulated wave in RM (0x00 = 0% signal, 0xFF: 100% signal)

9.25.23 SS_TX2_RMCFG (0017h)

These settings for TX_2 are only applied, if the bit 13 in TX_CONFIG (TX2_USE_TX1_CONF is set to 0.

Table 44. SS_TX2_RMCFG register (address 0017h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24:22	TX2_CLK_MODE_TRANS_RM	r/w	0*,1	TX2 clock mode in RM during transition
21:19	TX2_CLK_MODE_MOD_RM	r/w	0*,1	TX2 clock mode of modulated wave in RM 000: TX2=High-Z 001: TX2=VSS_PA 010 - 110: RFU 111: TX2 clocked normal operation
18:16	TX2_CLK_MODE_CW_RM	r/w	0*,1	TX2 clock mode of modulated wave in RM

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Table 44. SS_TX2_RMCFG register (address 0017h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				000: TX2=High-Z 001: TX2=VSS_PA 010 - 110: RFU 111: TX2 clocked normal operation
15:8	TX2_AMP_MOD_RM	r/w	0*,1	TX2 amplitude of modulated wave in RM (0x00 = 0% modulaton, 0xFF: 100% modulation)
7:0	TX2_AMP_CW_RM	r/w	0*,1	TX2 amplitude of unmodulated wave in RM (0x00 = 0% signal, 0xFF: 100% signal)

9.25.24 SS_TX_TRANS_CFG (0019h)

Table 45. SS_TX_TRANS_CFG register (address 0019h) bit description

Bit	Symbol	Access	Value	Description
31:12	RFU	rw	0*,1	-
11	TX2_SS_TRANS_RATE	rw	0*,1	TX2 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM.
10	TX1_SS_TRANS_RATE	rw	0*,1	TX1 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM
9:5	TX2_SS_TRANS_LENGTH	rw	0*,1	TX2 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid
4:0	TX1_SS_TRANS_LENGTH	rw	0*,1	TX1 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid

9.25.25 SIGPRO_CONFIG (001Dh)

Table 46. SIGPRO_CONFIG register (address 001Dh) bit description

Bit	Symbol	Access	Value	Description
31	DGRM_SOFT_RESET	r/w	0*,1	When high (1) resets the DGRM block.
30...0	RFU	r/w	0*,1	-

9.25.26 SIGPRO_RM_PATTERN (0020h)

Table 47. SIGPRO_RM_PATTERN register (address 0020h) bit description

Bit	Symbol	Access	Value	Description
31:16	RM_SYNC_PATTERN	r/w	0*,1	Sync pattern for FeliCa. LSB transmitted last
15	RM_SYNC_PATTERN_EXT4	r/w	0*,1	Extend FeliCa sync pattern with 16 leading 0s
14	RM_SYNC_PATTERN_EXT2	r/w	0*,1	Extend FeliCa sync pattern with 8 leading 0s
13	RM_RECEIVE_TILL_END	r/w	0*,1	Do not stop the reception before RxDecoder sends a stop command.
12	RFU	r	0*,1	-
11:0	RM_SOF_PATTERN	r/w	0*,1	SOF pattern for Type B. LSB transmitted last or Start Byte pattern for NFC passive.

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9.25.27 SIGPRO_RM_TECH (0022h)

Table 48. SIGPRO_RM_TECH register (address 0022h) bit description

Bit	Symbol	Access	Value	Description
31:17	RFU	rw	0	-
16:15	RM_MF_GAIN	rw	0	Defines the gain of the Matched-Filters 00: Minimum Gain, 11: Maximum Gain
14:0	RFU	rw	0	-

9.25.28 RX_PROTOCOL_CONFIG (0025h)

Table 49. RX_PROTOCOL_CONFIG register (address 0025h) bit description

Bit	Symbol	Access	Value	Description
31:6	RFU	r	0*,1	-
5:3	RX_BIT_ALIGN	r/w	0*,1	Defines the position of the 1st received data bit in the formed data byte.000b - 0 position...111b - 7th position
2	RX_PARITY_TYPE	r/w	0*,1	0 - data + parity bits contain even number of “1”. 1 - data + parity bits contain odd number of “1”. Valid if cfg_rx_parity_enable_i ==1.
1	RX_PARITY_ENABLE	r/w	0*,1	If set to ‘1’, the bit following last data bit in the frame character is considered as parity bit.
0	RFU	r/w	0*,1	-

9.25.29 RX_FRAME_LENGTH (0026h)

Table 50. RX_FRAME_LENGTH register (address 0026h) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30:16	RX_FRAME_MAXLEN	r/w	0*,1	Maximal number of received [DATA + CRC] bits in the frame. The violation of the maximum length limit can be also configured as an Error/EMD condition. If the max length violation is configured as error - the frame reception is stopped in case of maximum length limit exceeding. Otherwise the reception is continued. 0x0000 - 1 bit...0x7FFF - 32 kbit
15	RFU	r	0*,1	-
14:0	RX_FRAME_MINLEN	r/w	0*,1	Minimal number of received [DATA + CRC] bits in the frame. The violation of the minimum length limit can be also configured as an Error/EMD condition. The parameter also defines the number of received[DATA + CRC] bits before which any of the EOF patterns or INVPAR stop condition events are ignored.0x0000 - 1 bit...0x7FFF - 32 kbit

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9.25.30 RX_CTRL_STATUS (0028h)

Table 51. RX_CTRL_STATUS register (address 0028h) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r	dyn	-
8:3	RXCTRL_HF_ATT_VAL	r	dyn	HF attenuator value
2:0	RFU	r	dyn	-

9.25.31 SIGPRO_IIR_CONFIG0 (002Ah)

Table 52. SIGPRO_IIR_CONFIG0 register (address 002Ah) bit description

Bit	Symbol	Access	Value	Description
31:1	RFU	rw	0*,1	-
0	IIR_ENABLE	rw	0*,1	Enable the IIR filter

9.25.32 DGRM_BBA (002Dh)

Table 53. DGRM_BBA register (address 002Dh) bit description

Bit	Symbol	Access	Value	Description
31:17	RFU	r	0*,1	-
16:14	DGRM_BBA_MIN_VAL	r/w	0*,1	Defines the minimum value of BBA gain: 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB 0: -6dB
13:11	DGRM_BBA_MAX_VAL	r/w	0*,1	Defines the maximum value of BBA gain. 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB 0: -6dB
10:8	DGRM_BBA_INIT_VAL	r/w	0*,1	Defines initial value of BBA gain. 5: +24dB 4: +18dB 3: +12dB 2: +6dB 1: 0dB 0: -6dB
7:0	RFU	r	0*,1	-

9.25.33 DGRM_RSSI (0030h)

This register is updated dynamically by the firmware if the DPC is enabled.

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Table 54. DGRM_RSSI register (address 0030h) bit description

Bit	Symbol	Access	Value	Description
31:30	RFU			-
29	DGRM_SIGNAL_DETECT_TH_OVR	r/w	0*,1	Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL.
28:23	RFU	r/w	0*,1	-
22:17	DGRM_RSSI_HYST	r/w	0*,1	Hysteresis value for RSSI target
16:7	DGRM_RSSI_TARGET	r/w	0*,1	RSSI target value
6:0	DGRM_SIGNAL_DETECT_TH_OVR_VAL	r/w	0*,1	Defines the override value for signal detect threshold when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage. Only if the ARC is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session.

9.25.34 RX_CRC_CONFIG (0031h)

Table 55. RX_CRC_CONFIG register (address 0031h) bit description

Bit	Symbol	Access	Value	Description
31:16	RX_CRC_PRESET_VALUE	r	0*,1	Arbitrary preset value for the Rx-Decoder CRC calculation.
15:8	RFU	r/w	0*,1	-
7	RX_FORCE_CRC_WRITE	r/w	0*,1	If set. the Rx-Decoder will send to the RAM the CRC bits as well.
6	RX_CRC_ALLOW_BITS	r/w	0*,1	If activated the frame with length =< CRC_length will be always sent to the System RAM as is, without CRC bits removal.
5:3	RX_CRC_PRESET_SEL	r/w	0*,1	Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSByte is used. 000b* 0000h reset value. Note that this configuration is set by the Mode detector for FeliCa. 001b 6363h Note that this configuration is set by the Mode detector for ISO14443 type A. 010b A671h 011b FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B. 100b 0012h 101b E012h 110b RFU 111b Use arbitrary preset value RX_CRC_PRESET_VALUE
2	RX_CRC_TYPE	r/w	0*,1	Controls the type of CRC calculation for the Rx-Decoder 0* 16bit CRC calc
1	RX_CRC_INV	r/w	0*,1	Controls the comparison of the CRC checksum for the Rx-Decoder

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Table 55. RX_CRC_CONFIG register (address 0031h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				0*: Not inverted CRC value: 0000h reset value. Note that this bit is cleared by the Mode detector for ISO14443 type A and FeliCa. 1: Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B
0	RX_CRC_ENABLE			If set. the Rx-Decoder will check the CRC for correctness. Note that this bit is set by the Mode Detector when ISO14443 type B. or FeliCa (212 kBd or 424 kBd) is detected.

9.25.35 RX_WAIT (0032h)

To guarantee correct protocol timing a guard period timer is implemented for the RF_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time RX_WAIT is started after the end of a transmission. The guard time RX_WAIT can be disabled by setting the register RX_WAIT_VALUE to 00h meaning the receiver is immediately enabled.

Table 56. RX_WAIT register (address 0032h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU	r	0*,1	-
27:8	RX_WAIT_VALUE	r/w	0*,1	Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled
7:0	RX_WAIT_PRESCALER	r/w	0*,1	Defines the prescaler reload value for the rx_wait timer.

9.25.36 DCOC_CONFIG (0033h)

Table 57. DCOC_CONFIG register (address 0033h) bit description

Bit	Symbol	Access	Value	Description
31:22	RFU	rw	0*,1	-
21	DCOC_CAL_DONE_FORCE	rw	0*,1	forces the signal dcoc_cal_done to 1
20:0	RFU	rw	0*,1	-

9.25.37 RXM_CTRL (0035h)

Table 58. RXM_CTRL register (address 0035h) bit description

Bit	Symbol	Access	Value	Description
31:3	RFU			-
2	RXM_FRQ_CHECK_PCRM_ ENABLE	r/w		enable frequency check from PCRM
1	RXM_FRQ_CHECK_CORDIC_ ENABLE	r/w		enable precise frequency check from cordic phase (+/- 1.7 MHz multiples)
0	RXM_ENABLE	r/w		enable the all RxMeasure module

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9.25.38 ANA_AGC_DCO_CTRL (0036h)

Table 59. ANA_AGC_DCO_CTRL register (address 0036h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	rw	0*,1	-
24	RX_DCO_C_EN	rw	0*,1	Enable signal for the DCO coarse DAC
23:4	RFU	rw	0*,1	-
3	RX_DCO_F_EN	rw	0*,1	enable signal for the DCO fine DAC
2:0	RFU	rw	0*,1	-

9.25.39 SS_TX1_CMCFG (0003Bh)

Table 60. SS_TX1_CMCFG register (address 003Bh) bit description

Bit	Symbol	Access	Reset Value	Description
31:22	RFU	rw	0	-
21:19	TX1_CLK_MODE_MOD_CM	rw	0	TX1 clock mode of modulated wave in CM
18:16	TX1_CLK_MODE_CW_CM	rw	0	TX1 clock mode of unmodulated wave in CM
15:8	TX1_AMP_MOD_CM	rw	0	TX1 clock mode of modulated wave in CM
7:0	TX1_AMP_CW_CM	rw	0xFF	TX1 clock mode of unmodulated wave in CM

9.25.40 SS_TX2_CMCFG (0003Ch)

Table 61. SS_TX2_CMCFG register (address 003Ch) bit description

Bit	Symbol	Access	Reset Value	Description
31:22	RFU	rw	0	-
21:19	TX2_CLK_MODE_MOD_CM	rw	0	TX2 clock mode of modulated wave in CM
18:16	TX2_CLK_MODE_CW_CM	rw	0	TX2 clock mode of unmodulated wave in CM
15:8	TX2_AMP_MOD_CM	rw	0	TX2 clock mode of modulated wave in CM
7:0	TX2_AMP_CW_CM	rw	0xFF	TX2 clock mode of unmodulated wave in CM

9.25.41 TIMER0_CONFIG (003Dh)

Table 62. TIMER0_CONFIG register (address 003Dh) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	r	0*,1	-
8	T0_START_NOW	r/w	0*,1	T0_START_EVENT: If set. the timer T0 is started immediately
7	RFU	r	0*,1	-
6	T0_ONE_SHOT_MODE	r/w	0*,1	When set to 1, the counter value does not reload again until the counter value has reached zero
5:3	T0_PRESCALE_SEL	r/w	0*,1	Controls input frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL.

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Table 62. TIMER0_CONFIG register (address 003Dh) bit description *...continued*

Bit	Symbol	Access	Value	Description
				000b - 6.78 MHz counter 001b - 3.39 MHz counter 010b - 1.70 MHz counter 011b - 848 kHz counter 100b - 424 kHz counter 101b - 212 kHz counter 110b - 106 kHz counter 111b - 53 kHz counter
2	T0_MODE_SEL	r/w	0*,1	Configuration of the timer T0 clock. 0b - Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b - Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_PRESCALE_SEL).
1	T0_RELOAD_ENABLE	r/w	0*,1	If set to 0b - the timer T0 will stop on expiration. 0* After expiration the timer T0 will stop counting. i.e. remain zero. reset value. 1b - After expiration the timer T0 will reload its preset value and continue counting down.
0	T0_ENABLE	r/w	0*,1	Enables the timer T0

9.25.42 TIMER0_RELOAD (003Eh)

Table 63. TIMER0_RELOAD register (address 003Eh) bit description

Bit	Symbol	Access	Value	Description
31:20	RFU	r	0*,1	-
19:0	T0_RELOAD_VALUE	r/w	0*,1	Reload value of the timer T0.

9.25.43 TIMER1_CONFIG (003Fh)

Timer 1 is typically used for the FDT configuration. Configuration can be done from the host but the associated IRQ is handled by the firmware of the PN5190B1.

Table 64. TIMER1_CONFIG register (address 003Fh) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30	T1_STOP_ON_RX_STARTED	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when a data reception begins (1st bit is received).
29	T1_STOP_ON_TX_STARTED	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when a data transmission begins.
28	T1_STOP_ON_RF_ON_EXT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field is detected.
27	T1_STOP_ON_RF_OFF_EXT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field vanishes.

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Table 64. TIMER1_CONFIG register (address 003Fh) bit description *...continued*

Bit	Symbol	Access	Value	Description
26	T1_STOP_ON_RF_ON_INT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on.
25	T1_STOP_ON_RF_OFF_INT	r/w	0*,1	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off.
24	T1_STOP_ON_RX_ENDED	r/w	0*,1	T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected.
23:18	RFU	r	0*,1	-
17	T1_START_ON_RX_STARTED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received).
16	T1_START_ON_RX_ENDED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data reception ends.
15	T1_START_ON_TX_STARTED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data transmission begins.
14	T1_START_ON_TX_ENDED	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when a data transmission ends.
13	T1_START_ON_RF_ON_EXT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when the external RF field is detected.
12	T1_START_ON_RF_OFF_EXT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected anymore.
11	T1_START_ON_RF_ON_INT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on.
10	T1_START_ON_RF_OFF_INT	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off.
9	T1_START_ON_TX_ FRAMESTEP	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started when an activity on Frame step is detected.
8	T1_START_NOW	r/w	0*,1	T1_START_EVENT: If set. the timer T1 is started immediately.
7	RFU	r	0*,1	-
6	T1_ONE_SHOT_MODE	r/w	0*,1	When set to 1, the counter value does not reload again until the counter value has reached zero
5:3	T1_PRESCALE_SEL	r/w	0*,1	Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL. 000b - 6.78 MHz counter 001b - 3.39 MHz counter 010b - 1.70 MHz counter 011b - 848 kHz counter 100b - 424 kHz counter 101b - 212 kHz counter 110b - 106 kHz counter 111b - 53 kHz counter
2	T1_MODE_SEL	r/w	0*,1	If set. the timer T1 is started the prescaler for the timer T1 is enabled. 0* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1 Prescaler is enabled: the timer operates

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Table 64. TIMER1_CONFIG register (address 003Fh) bit description *...continued*

Bit	Symbol	Access	Value	Description
				on the prescaler signal frequency (chosen by T1_PRESCALE_SEL).
1	T1_RELOAD_ENABLE	r/w	0*,1	If set to 0.the timer T1 will stop on expiration. 0* After expiration the timer T1 will stop counting. i.e. remain zero. reset value. 1 After expiration the timer T1 will reload its preset value and continue counting down.
0	T1_ENABLE	r/w	0*,1	Enables the timer T1

9.25.44 TIMER1_RELOAD (0040h)

Table 65. TIMER1_RELOAD register (address 0040h) bit description

Bit	Symbol	Access	Value	Description
31:20	RFU	r	0*,1	-
19:0	T1_RELOAD_VALUE	r/w	0*,1	Reload value of the timer T1.

9.25.45 ANA_STATUS (0041h)

Table 66. ANA_STATUS register (address 0041h) bit description

Bit	Symbol	Access	Value	Description
31:21	RFU	rw	0.1	-
20:11	ADC_DATA_I	rw	0.1	RX adc I output for validation purposes
10:1	ADC_DATA_Q	rw	0.1	RX adc Q output for validation purposes
0	PLL_LOCK_STATUS	rw	0.1	PLL lock status indicator

9.25.46 ANA_RX_CTRL (0043h)

Table 67. ANA_RX_CTRL register (address 00434h) bit description

Bit	Symbol	Access	Value	Description
31:7	RFU	rw	0.1	-
6	RX_MIXER_SE_MODE_EN	rw	0.1	enable signal for selecting single ended mode
5:0	RFU	rw	0.1	-

9.25.47 ANACTRL_TX_CONFIG (0044h)

Table 68. ANACTRL_TX_CONFIG register (address 0044h) bit description

Bit	Symbol	Access	Value	Description
31:6	RFU	rw	0.1	-
5:4	TX_INVP_RM	rw	0.1	shift driver waves of 180 degrees in RM. Index 0: TX1; index 1: TX2 This value is initialized with data from TX_INV_RM (address 0018h) EEPROM bit 0.1 during Load protocol.

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Table 68. ANACTRL_TX_CONFIG register (address 0044h) bit description...*continued*

Bit	Symbol	Access	Value	Description
3:2	RFU	rw	0.1	-
1	TX_PWM_MODE_RM	rw	0.1	PWM scheme for RM: 0: TX1/2 3-levels (If at least either clk_mode_tx1 or clk_mode_tx2 is set on a clocked mode) 1: TX1/2 2-levels with differentiated pulses This value is initialized with data from TX_SHAPING_CONFIG (address 0017h) EEPROM bit 0 during Load protocol.
0	RFU	rw	0.1	-

9.25.48 EMD_1_CFG (0047h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 69. EMD_1_CFG register (address 0047h) bit description

Bit	Symbol	Access	Value	Description
31:0	EMD_1_Configuration	r/w		0000 FF03h EMD ISO 0000 FF04h EMD NFC Forum

9.25.49 EMD_0_CONFIG (0048h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 70. EMD_0_CONFIG register (address 0048h) bit description

Bit	Symbol	Access	Value	Description
31:0	EMD_0_Configuration	r/w		176003FFh EMD ISO14443 1F6003FFh EMD NFC Forum

9.25.50 LPCD_CALIBRATE_CTRL (0050h)

This register is used for LPCD semi autonomous mode. Writing to this register triggers the LPCD calibration with the RSSI_HYSTERESIS and RSSI_TARGET values as given in bits 23:16 and 15:0. After calibration is completed, calibration status is available in LPCD_CALIBRATE_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ_CHANNEL_VALS (51h).

Table 71. LPCD_CALIBRATE_CTRL register (address 0050h) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30	FREEZE_VALUE	r/w	0*,1	Write RSSI_TARGET and RSSI_HYSTERESIS into LPCD_CALIBRATE_CTRL: 1. **FREEZE_VALUE = 0:** This calibrates the Semi autonomous LPCD. The calibration status can be checked in bit 31 of CALIBRATE_STATUS register (0x53). 2. **FREEZE_VALUE = 1:** This writes the RSSI_TARGET and RSSI_HYSTERESIS into the EEPROM

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Table 71. LPCD_CALIBRATE_CTRL register (address 0050h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				LPCD_RSSI_TARGET (0x494) and LPCD_RSSI_HYSTERESIS (0x496).
29:24	RFU	r	0*,1	-
23:16	RSSI_HYSTERESIS	r/w	0*,1	Value to be set in DGRM_RSSI_HYST used for calibration
15:0	RSSI_TARGET	r/w	0*,1	Value to be set in DGRM_RSSI_TARGET used for calibration

9.25.51 IQ_CHANNEL_VALS (0051h)

Table 72. IQ_CHANNEL_VALS register (address 0051h) bit description

Bit	Symbol	Access	Value	Description
31:16	Q_CHANNEL_VAL	r	-	Q Channel value
15:0	I_CHANNEL_VAL	r	-	I Channel value

9.25.52 PAD_CONFIG (0052h)

Table 73. PAD_CONFIG register (address 0052h) bit description

Bit	Symbol	Access	Value	Description
31:7	RFU	rw		-
6	AUX3_OUTPUT_VAL	rw		Output value for AUX3 0: Low 1: High
5	AUX2_OUTPUT_VAL	rw		Output value for AUX2 0: Low 1: High
4	AUX1_OUTPUT_VAL	rw		Output value for AUX1 0: Low 1: High
3	GPIO3_OUTPUT_VAL	rw		Output value for GPIO3 0: Low 1: High
2	GPIO2_OUTPUT_VAL	rw		Output value for GPIO2 0: Low 1: High
1	GPIO1_OUTPUT_VAL	rw		Output value for GPIO1 0: Low 1: High
0	GPIO0_OUTPUT_VAL	rw		Output value for GPIO0 0: Low 1: High

On PN5190B1 only output functionality is available on GPIO's.

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9.25.53 CALIBRATE_STATUS (0053h)

Table 74. CALIBRATE_STATUS register (address 0053h) bit description

Bit	Symbol	Access	Value	Description
31	LPCD_CALIBRATION_STATUS	r	-	Calibration Status 0 - Calibration Not Done, 1- Calibration Done
30:1	RFU	r	-	-
0	TXNOV_CALIBRATION_STATUS			Calibration Status 0 - Calibration Not Done, 1- Calibration Done

9.25.54 TXLDO_VDDPA_CONFIG (0054h)

If DPC is disabled, the VDDPA supply voltage can be set with this register. These register settings are overruled by the DPC.

This register does allow to read the actual VDDPA supply voltage independent from having the DPC enabled/ disabled, this allows to read-out the actual transmitter supply voltage.

Table 75. TXLDO_VDDPA_CONFIG register (address 0054h) bit description

Bit	Symbol	Access	Value	Description
31:8	RFU	rw		-
7:0	VDDPA CONFIG	rw		TX_LDO output voltage VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */ VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */ VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */ VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */

9.25.55 GENERAL_ERROR_STATUS (0055h)

Table 76. GENERAL_ERROR_STATUS register (address 0055h) bit description

Bit	Symbol	Access	Value	Description
31:3	RFU	r	0*,1	-

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Table 76. GENERAL_ERROR_STATUS register (address 0055h) bit description...*continued*

Bit	Symbol	Access	Value	Description
2	TXLDO_ERROR	r	0*,1	TXLDO does not start
1	CLOCK_ERROR	r	0*,1	XTAL or PLL does not start
0	GPADC_ERROR	r	0*,1	GPADC initialization fail

9.25.56 TXLDO_VOUT_CURR (0056h)

Table 77. TXLDO_VOUT_CURR register (address 0056h) bit description

Bit	Symbol	Access	Value	Description
31:24	RFU	r		-
23:8	TXLDO_CURRENT	r		Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA)
7:0	VDDPA_VOUT	r		VDDPA output voltage VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */ VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */ VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */ VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */

9.25.57 DAC (0057h)

This register allows configuring the output voltage of VTUNE1, VTUNE2.

Table 78. DAC register (address 0057h) bit description

Bit	Symbol	Access	Value	Description
31:28	RFU			-
27:24	TUNING_DAC_2_RANGE			Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111. Available range: 0000=2 V 0001=3 V 0011=3.45 V

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Table 78. DAC register (address 0057h) bit description...*continued*

Bit	Symbol	Access	Value	Description
				0111=3.8 V If the VDDIO is 1.8 V, then configuration 000 shall be used. This applies only to DAC2.
23:17	TUNING_DAC_2_VALUE			Output voltage of DAC2 according to 1/128 *<TUNING_DAC_2_VALUE> * <Range in V>
16	TUNING_DAC_2_PD			0=DAC Turned off, 1=DAC enabled
15:12	RFU			-
11:8	TUNING_DAC_1_RANGE			Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111. Available range: 0000=2 V 0001=3 V 0011=3.45 V 0111=3.8 V
7:1	TUNING_DAC_1_VALUE			Output voltage of DAC1 according to 1/128 * <TUNING_DAC_1_VALUE> * <Range in V>
0	TUNING_DAC_1_PD			0=DAC Turned off, 1=DAC enabled

9.25.58 RXM_FREQ (0059h)

Table 79. RXM_FREQ register (address 0059h) bit description

Bit	Symbol	Access	Value	Description
31	RXM_FREQ_REG_VALID	r	-	CLIF_RXM_FREQ_REG fields are valid
30:25	RFU	r	-	-
24:16	RXM_FREQ	r	-	frequence difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded
15:9	RFU	r	-	-
0:8	RXM_PHASE	r	-	phase value

9.25.59 RXM_RSSI (005Ah)

Table 80. RXM_RSSI register (address 005Ah) bit description

Bit	Symbol	Access	Reset Value	Description
31:23	RFU	r	-	-
22	RXM_RSSI_FROZEN	r	-	The RSSI value is not currently updated
21	RXM_FRQ_OK	r	-	The carrier frequency detected is OK.
20	RXM_RSSI_REG_VALID	r	-	CLIF_RXM_RSSI_REG fields are valid
19:14	RXM_HFATT	r	-	HFAtt latched with RSSI
13:0	RXM_RSSI	r	-	RSSI value

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9.25.60 TEMP_SENSOR (005Bh)

Table 81. TEMP_SENSOR register (address 005Bh) bit description

Bit	Symbol	Access	Value	Description
31:16	-	r	0*,1	RFU
15-0	TEMP_SENSOR_DATA	r	0*,1	Indicates the current temperature of the chip in degree celsius. This is the actual temperature data of the sensor which is used for the overheat protection. Maximum temperature readable will be the maximum temperature threshold configured in EEPROM TEMP_WARNING address 0x14.

9.25.61 TX_NOV_CALIBRATE_AND_STORE (005Dh)

Table 82. TX_NOV_CALIBRATE_AND_STORE register (address 005Dh) bit description

Bit	Symbol	Access	Value	Description
31:29	RFU	rw	0*,1	-
1:0	TX_NOV_CALIBRATE_AND_STORE_VAL	rw		Calibrates the TX NOV and stores the resulting value in EEPROM

9.25.62 DPC_CONFIG (005Eh)

Table 83. DPC_CONFIG register (address 005Eh) bit description

Bit	Symbol	Access	Value	Description
31	DPC_REG_ACCESS	r/w	0*,1	This bit is used to enable the DPC enable / disable control via register. 1: DPC enabled / disabled via register. 0: DPC enabled / disabled via EEPROM (default) This bit needs to be SET to enable/disable the functionality of bit 0.
30:1	RFU	r/w	0*,1	-
0	ENABLE_DISABLE_DPC	r/w	0*,1	1: DPC enabled, if bit 31 is enabled. 0: DPC disabled, if bit 31 is enabled. The DPC can only be enabled or disabled during RF off.

9.25.63 TIMER0_OUTPUT (005Fh)

Available from firmware version 2.05 onwards:

Table 84. TIMER0_OUTPUT register (address 005Fh) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24	T0_RUNNING	r	0*,1	Indicates that timer T0 is running (busy)
23:20	RFU	r	0*,1	-
19:0	T0_VALUE	r/w	0*,1	Value of 20bit counter in timer T0

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9.25.64 TIMER1_OUTPUT (0060h)

Available from firmware version 2.05 onwards:

Table 85. TIMER1_OUTPUT register (address 0060h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24	T1_RUNNING	r	0*,1	Indicates that timer T1 is running (busy)
23:20	RFU	r	0*,1	-
19:0	T1_VALUE	r/w	0*,1	Value of 20bit counter in timer T1

9.25.65 TIMER2_CONFIG (0061h)

Available from firmware version 2.05 onwards:

Timer 2 is typically used for the FDT measurement.

Table 86. TIMER2_CONFIG register (address 0061h) bit description

Bit	Symbol	Access	Value	Description
31	RFU	r	0*,1	-
30	T2_STOP_ON_RX_STARTED	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when a data reception begins (1st bit is received).
29	T2_STOP_ON_TX_STARTED	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when a data transmission begins.
28	T2_STOP_ON_RF_ON_EXT	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when the external RF field is detected.
27	T2_STOP_ON_RF_OFF_EXT	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when the external RF field vanishes.
26	T2_STOP_ON_RF_ON_INT	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when the internal RF field is turned on.
25	T2_STOP_ON_RF_OFF_INT	r/w	0*,1	T2_STOP_EVENT: If set. the timer T2 is stopped when the internal RF field is turned off.
24	T2_STOP_ON_RX_ENDED	r/w	0*,1	T2_STOP_EVENT: If set the timer T2 is stopped when an activity on RX is detected.
23:18	RFU	r	0*,1	-
17	T2_START_ON_RX_STARTED	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when a data reception begins (1st bit is received).
16	T2_START_ON_RX_ENDED	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when a data reception ends.
15	T2_START_ON_TX_STARTED	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when a data transmission begins.
14	T2_START_ON_TX_ENDED	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when a data transmission ends.
13	T2_START_ON_RF_ON_EXT	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when the external RF field is detected.
12	T2_START_ON_RF_OFF_EXT	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when the external RF field is not detected anymore.

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Table 86. TIMER2_CONFIG register (address 0061h) bit description *...continued*

Bit	Symbol	Access	Value	Description
11	T2_START_ON_RF_ON_INT	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned on.
10	T2_START_ON_RF_OFF_INT	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned off.
9	T2_START_ON_TX_ FRAMESTEP	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started when an activity on Frame step is detected.
8	T2_START_NOW	r/w	0*,1	T2_START_EVENT: If set. the timer T2 is started immediately.
7	RFU	r	0*,1	-
6	T2_ONE_SHOT_MODE	r/w	0*,1	When set to 1, the counter value does not reload again until the counter value has reached zero
5:3	T2_PRESCALE_SEL	r/w	0*,1	Controls input frequency/period of the timer T0 when the prescaler is activated in T2_MODE_SEL. 000b - 6.78 MHz counter 001b - 3.39 MHz counter 010b - 1.70 MHz counter 011b - 848 kHz counter 100b - 424 kHz counter 101b - 212 kHz counter 110b - 106 kHz counter 111b - 53 kHz counter
2	T2_MODE_SEL	r/w	0*,1	If set. the timer T2 is started the prescaler for the timer T2 is enabled. 0* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1 Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T2_ PRESCALE_SEL).
1	T2_RELOAD_ENABLE	r/w	0*,1	If set to 0, the timer T2 stops on expiration. 0* After expiration the timer T2 stops counting. i.e. remain zero. reset value. 1 After expiration the timer T2 reloads its preset value and continue counting down.
0	T2_ENABLE	r/w	0*,1	Enables the timer T2

9.25.66 TIMER2_RELOAD (0062h)

Available from firmware version 2.05 onwards:

Table 87. TIMER2_RELOAD register (address 0062h) bit description

Bit	Symbol	Access	Value	Description
31:20	RFU	r	0*,1	-
19:0	T2_RELOAD_VALUE	r/w	0*,1	Reload value of the timer T2.

9.25.67 TIMER2_OUTPUT (0063h)

Available from firmware version 2.05 onwards:

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Table 88. TIMER2_OUTPUT register (address 0063h) bit description

Bit	Symbol	Access	Value	Description
31:25	RFU	r	0*,1	-
24	T2_RUNNING	r	0*,1	Indicates that timer T2 is running (busy)
23:20	RFU	r	0*,1	-
19:0	T2_VALUE	r/w	0*,1	Value of 20bit counter in timer T2

9.25.68 DYNAMIC_POWERLEVEL_REDUCTION (0064h)

Up to FW2.8 RFU

Available from FW2.9 onwards: DYNAMIC_POWERLEVEL_REDUCTION

Table 89. DYNAMIC_POWERLEVEL_REDUCTION (address 0064h) configuration bit description

Address (hex)	Function	Bit	Description
0064h	DPR: Dyanmic Power reduction value	7:0	bits[7:0] are used for reducing the power level. Procedure steps: 1. Perform an RF OFF 2. Write the dynamic power reduction level into the register 3. Perform an RF On (In case RF was already ON, a soft reset is mandatory.) 4. The new power level will be applied.

Be aware of the Target current and Current reduction LUT entries: The DPR value shall not be higher than target current + (hysteresis + largest current reduction value).

A too high DPR value, which could result a “negative current”, causes the DPC to freeze.

9.25.69 SS_TX1_RTRTRANS0 (0080h)

Table 90. SS_TX1_RTRTRANS0 register (address 0080h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS3	rw		TX1 rising transition value 3
23:16	TX1_SS_RTRANS2	rw		TX1 rising transition value 2
15:8	TX1_SS_RTRANS1	rw		TX1 rising transition value 1
7:0	TX1_SS_RTRANS0	rw		TX1 rising transition value 0

9.25.70 SS_TX1_RTRTRANS1 (0081h)

Table 91. SS_TX1_RTRTRANS1 register (address 0081h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS7	rw		TX1 rising transition value 7
23:16	TX1_SS_RTRANS6	rw		TX1 rising transition value 6
15:8	TX1_SS_RTRANS5	rw		TX1 rising transition value 5
7:0	TX1_SS_RTRANS4	rw		TX1 rising transition value 4

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9.25.71 SS_TX1_RTRTRANS2 (0082h)

Table 92. SS_TX1_RTRTRANS2 register (address 0082h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS11	rw		TX1 rising transition value 11
23:16	TX1_SS_RTRANS10	rw		TX1 rising transition value 10
15:8	TX1_SS_RTRANS9	rw		TX1 rising transition value 9
7:0	TX1_SS_RTRANS8	rw		TX1 rising transition value 8

9.25.72 SS_TX1_RTRTRANS3 (0083h)

Table 93. SS_TX1_RTRTRANS3 register (address 0083h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_RTRANS15	rw		TX1 rising transition value 15
23:16	TX1_SS_RTRANS14	rw		TX1 rising transition value 14
15:8	TX1_SS_RTRANS13	rw		TX1 rising transition value 13
7:0	TX1_SS_RTRANS12	rw		TX1 rising transition value 12

9.25.73 SS_TX2_RTRTRANS0 (0084h)

Table 94. SS_TX2_RTRTRANS0 register (address 0084h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS3	rw	0*,1	TX2 rising transition value 3
23:16	TX2_SS_RTRANS2	rw	0*,1	TX2 rising transition value 2
15:8	TX2_SS_RTRANS1	rw	0*,1	TX2 rising transition value 1
7:0	TX2_SS_RTRANS0	rw	0*,1	TX2 rising transition value 0

9.25.74 SS_TX2_RTRTRANS1 (0085h)

Table 95. SS_TX2_RTRTRANS1 register (address 0085h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS7	rw		TX2 rising transition value 7
23:16	TX2_SS_RTRANS6	rw		TX2 rising transition value 6
15:8	TX2_SS_RTRANS5	rw		TX2 rising transition value 5
7:0	TX2_SS_RTRANS4	rw		TX2 rising transition value 4

9.25.75 SS_TX2_RTRTRANS2 (0086h)

Table 96. SS_TX2_RTRTRANS2 register (address 0086h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS11	rw		TX2 rising transition value 11
23:16	TX2_SS_RTRANS10	rw		TX2 rising transition value 10
15:8	TX2_SS_RTRANS9	rw		TX2 rising transition value 9

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Table 96. SS_TX2_RTRTRANS2 register (address 0086h) bit description...*continued*

Bit	Symbol	Access	Value	Description
7:0	TX2_SS_RTRANS8	rw		TX2 rising transition value 8

9.25.76 SS_TX2_RTRTRANS3 (0087h)

Table 97. SS_TX2_RTRTRANS3 register (address 0087h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_RTRANS15	rw		TX2 rising transition value 15
23:16	TX2_SS_RTRANS14	rw		TX2 rising transition value 14
15:8	TX2_SS_RTRANS13	rw		TX2 rising transition value 13
7:0	TX2_SS_RTRANS12	rw		TX2 rising transition value 12

9.25.77 SS_TX1_FTRTRANS0 (0088h)

Table 98. SS_TX1_FTRTRANS0 register (address 0088h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS3	rw	0*,1	TX1 falling transition value 3
23:16	TX1_SS_FTRANS2	rw	0*,1	TX1 falling transition value 2
15:8	TX1_SS_FTRANS1	rw	0*,1	TX1 falling transition value 1
7:0	TX1_SS_FTRANS0	rw	0*,1	TX1 falling transition value 0

9.25.78 SS_TX1_FTRTRANS1 (0089h)

Table 99. SS_TX1_FTRTRANS1 register (address 0089h) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS7	rw		TX1 falling transition value 7
23:16	TX1_SS_FTRANS6	rw		TX1 falling transition value 6
15:8	TX1_SS_FTRANS5	rw		TX1 falling transition value 5
7:0	TX1_SS_FTRANS4	rw		TX1 falling transition value 4

9.25.79 SS_TX1_FTRTRANS2 (008Ah)

Table 100. SS_TX1_FTRTRANS2 register (address 008Ah) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS11	rw		TX1 rising transition value 11
23:16	TX1_SS_FTRANS10	rw		TX1 rising transition value 10
15:8	TX1_SS_FTRANS9	rw		TX1 rising transition value 9
7:0	TX1_SS_FTRANS8	rw		TX1 rising transition value 8

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9.25.80 SS_TX1_FTRTRANS3 (008Bh)

Table 101. SS_TX1_FTRTRANS3 register (address 008Bh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX1_SS_FTRANS15	rw		TX1 rising transition value 15
23:16	TX1_SS_FTRANS14	rw		TX1 rising transition value 14
15:8	TX1_SS_FTRANS13	rw		TX1 rising transition value 13
7:0	TX1_SS_FTRANS12	rw		TX1 rising transition value 12

9.25.81 SS_TX2_FTRTRANS0 (008Ch)

Table 102. SS_TX2_FTRTRANS0 register (address 008Ch) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS3	rw		TX2 falling transition value 3
23:16	TX2_SS_FTRANS2	rw		TX2 falling transition value 2
15:8	TX2_SS_FTRANS1	rw		TX2 falling transition value 1
7:0	TX2_SS_FTRANS0	rw		TX2 falling transition value 0

9.25.82 SS_TX2_FTRTRANS1 (008Dh)

Table 103. SS_TX2_FTRTRANS1 register (address 008Dh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS7	rw		TX2 falling transition value 7
23:16	TX2_SS_FTRANS6	rw		TX2 falling transition value 6
15:8	TX2_SS_FTRANS5	rw		TX2 falling transition value 5
7:0	TX2_SS_FTRANS4	rw		TX2 falling transition value 4

9.25.83 SS_TX2_FTRTRANS2 (008Eh)

Table 104. SS_TX2_FTRTRANS2 register (address 008Eh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS11	rw		TX2 falling transition value 11
23:16	TX2_SS_FTRANS10	rw		TX2 falling transition value 10
15:8	TX2_SS_FTRANS9	rw		TX2 falling transition value 9
7:0	TX2_SS_FTRANS8	rw		TX2 falling transition value 8

9.25.84 SS_TX2_FTRTRANS3 (008Fh)

Table 105. SS_TX2_FTRTRANS3 register (address 008Fh) bit description

Bit	Symbol	Access	Value	Description
31:24	TX2_SS_FTRANS15	rw		TX2 falling transition value 15
23:16	TX2_SS_FTRANS14	rw		TX2 falling transition value 14
15:8	TX2_SS_FTRANS13	rw		TX2 falling transition value 13

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Table 105. SS_TX2_FTRTRANS3 register (address 008Fh) bit description...*continued*

Bit	Symbol	Access	Value	Description
7:0	TX2_SS_FTRANS12	rw		TX2 falling transition value 12

9.26 EEPROM configuration description

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power off.

This section describes the EEPROM configuration of the PN5190B1.

Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.

The detailed description of the EEPROM is available in the User API documentation.

9.26.1 EEPROM configuration overview

Table 106. EEPROM CONFIGURATION REGISTER

Address (hex)	Name
0	DCDC_PWR_CONFIG
1	DCDC_CONFIG
2	TXLDO_CONFIG
6	TXLDO_VDDPA_HIGH
7	RFU
8	TXLDO_VDDPA_MAX_RDR
9	RFU
A	BOOST_DEFAULT_VOLTAGE
B-F	RFU
10	XTAL_CONFIG
11	XTAL_TIMEOUT
12	CLK_INPUT_FREQ
13	XTAL_CHECK_DELAY
14	TEMP_WARNING
15	RFU
16	ENABLE_GPIO0_ON_OVERTEMP
17	TX_SHAPING_CONFIG
18	TX_INV_RM
19	TX_CLK_MODE_1
1A	TX_CLK_MODE_2
1B	RFU

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
1C	RFU
1D	RFU
1E	RFU
1F	RFU
20	RFU
21	RFU
22	RESIDUAL_AMP_LEVEL_A106
23	EDGE_TYPE_A106
24	EDGE_STYLE_A106
25	EDGE_LENGTH_A106
26	RESIDUAL_AMP_LEVEL_A212
27	EDGE_TYPE_A212
28	EDGE_STYLE_A212
29	EDGE_LENGTH_A212
2A	RESIDUAL_AMP_LEVEL_A424
2B	EDGE_TYPE_A424
2C	EDGE_STYLE_A424
2D	EDGE_LENGTH_A424
2E	RESIDUAL_AMP_LEVEL_A848
2F	EDGE_TYPE_A848
30	EDGE_STYLE_A848
31	EDGE_LENGTH_A848
32	RESIDUAL_AMP_LEVEL_B106
33	EDGE_TYPE_B106
34	EDGE_STYLE_B106
35	EDGE_LENGTH_B106
36	RESIDUAL_AMP_LEVEL_B212
37	EDGE_TYPE_B212
38	EDGE_STYLE_B212
39	EDGE_LENGTH_B212
3A	RESIDUAL_AMP_LEVEL_B424
3B	EDGE_TYPE_B424
3C	EDGE_STYLE_B424
3D	EDGE_LENGTH_B424
3E	RESIDUAL_AMP_LEVEL_B848
3F	EDGE_TYPE_A848

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
40	EDGE_STYLE_A848
41	EDGE_LENGTH_A848
42	RESIDUAL_AMP_LEVEL_F212
43	EDGE_TYPE_F212
44	EDGE_STYLE_F212
45	EDGE_LENGTH_F212
46	RESIDUAL_AMP_LEVEL_F424
47	EDGE_TYPE_F424
48	EDGE_STYLE_F424
49	EDGE_LENGTH_F424
4A	RESIDUAL_AMP_LEVEL_V100_26
4B	EDGE_TYPE_V100_26
4C	EDGE_STYLE_V100_26
4D	EDGE_LENGTH_V100_26
4E	RESIDUAL_AMP_LEVEL_V100_53
4F	EDGE_TYPE_V100_53
50	EDGE_STYLE_V100_53
51	EDGE_LENGTH_V100_53
52	RESIDUAL_AMP_LEVEL_V100_106
53	EDGE_TYPE_V100_106
54	EDGE_STYLE_V100_106
55	EDGE_LENGTH_V100_106
56	RESIDUAL_AMP_LEVEL_V100_212
57	EDGE_TYPE_V100_212
58	EDGE_STYLE_V100_212
59	EDGE_LENGTH_V100_212
5A	RESIDUAL_AMP_LEVEL_V10_26
5B	EDGE_TYPE_V10_26
5C	EDGE_STYLE_V10_26
5D	EDGE_LENGTH_V10_26
5E	RESIDUAL_AMP_LEVEL_V10_53
5F	EDGE_TYPE_V10_53
60	EDGE_STYLE_V10_53
61	EDGE_LENGTH_V10_53
62	RESIDUAL_AMP_LEVEL_V10_106
63	EDGE_TYPE_V10_106

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
64	EDGE_STYLE_V10_106
65	EDGE_LENGTH_V10_106
66	RESIDUAL_AMP_LEVEL_V10_212
67	EDGE_TYPE_V10_212
68	EDGE_STYLE_V10_212
69	EDGE_LENGTH_V10_212
66	RESIDUAL_AMP_LEVEL_V10_212
67	EDGE_TYPE_V10_212
68	EDGE_STYLE_V10_212
69	EDGE_LENGTH_V10_212
6A	RESIDUAL_AMP_LEVEL_180003m3_tari18p88
6B	EDGE_TYPE_180003m3_tari18p88
6C	EDGE_STYLE_180003m3_tari18p88
6D	EDGE_LENGTH_180003m3_tari18p88
6E	RESIDUAL_AMP_LEVEL_180003m3_tari9p44
6F	EDGE_TYPE_180003m3_tari9p44
70	EDGE_STYLE_180003m3_tari9p44
71	EDGE_LENGTH_180003m3_tari9p44
72	RESIDUAL_AMP_LEVEL_B_PRIME_106
73	EDGE_TYPE_B_PRIME_106
74	EDGE_STYLE_B_PRIME_106
75	EDGE_LENGTH_B_PRIME_106
76	DPC_CONFIG
77	DPC_TARGET_CURRENT
79	DPC_HYSTERESIS_LOADING
7A	RFU
7B	RFU
7C	DPC_HYSTERESIS_UNLOADING
7D	DPC_TXLDOVDDPALow
7E	DPC_TXGSN
7F	DPC_RDON_Control
80	DPC_InitialRDOn_RFOn
81	DPC_TXLDO_MAX_DROP
83	RFU
85	RFU
87	DPC_GUARD_TIME

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
88	DPC_ENABLE_DURING_FDT
89	DPC_GUARD_TIME_AFTER_RX
8A	RFU
8B	DPC_LOOKUP_TABLE
137	ARC_CONFIG
139	ARC_VDDPA
13E	ARC_RM_A106
148	ARC_RM_A212
152	ARC_RM_A424
15C	ARC_RM_A848
166	ARC_RM_B106
170	ARC_RM_B212
17A	ARC_RM_B424
184	ARC_RM_B848
18E	ARC_RM_F212
198	ARC_RM_F424
1A2	ARC_RM_V6p6
1AC	ARC_RM_V26
1B6	ARC_RM_V53
1C0	ARC_RM_V106
1CA	ARC_RM_V212
1D4	ARC_RM_18003m3_SC424_4MAN
1DE	ARC_RM_18003m3_SC848_2MAN
1E8	ARC_RM_18003m3_SC848_4MAN
1F2	ARC_RM_18003m3_SC848_2MAN
1FC	ARC_RM_AI106
206	ARC_RM_AI212
210	ARC_RM_AI424
2B2	RF_DEBOUNCE_TIMEOUT
2B3	SENSE_RES
2B5	NFC_ID1
2B8	SEL_RES
2B9	FELICA_POLL_RES
2CB	RANDOM_UID_ENABLE
2CC	MFC_AUTH_TIMEOUT
2DA	RSSI_TIMER

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
2DC	RSSI_TIMER_FIRST_PERIOD
2DE	RSSI_CTRL_00_AB
2DF	RSSI_NB_ENTRIES_AB
2E0	RSSI_THRESHOLD_PHASE_TABLE
3A2	TX_PARAM_ENTRY_TABLE
492	LPCD_AVG_SAMPLES
493	RFU
494	LPCD_RSSI_TARGET
496	LPCD_RSSI_HYST
497-499	RFU
49A	LPCD_THRESHOLD
49B-4AA	RFU
4AB	WAIT_RX_SETTLE
4AC-4AD	RFU
4AF	LPCD_VDDPA
4BD	XTAL_CONTROL
4BF	ULPCD_VDDPA_CTRL
4C2	ULPCD_TIMING_CTRL
4C6	ULPCD_VOLTAGE_CTRL
4C7	RFU
4C9	ULPCD_RSSI_GUARD_TIME
4CA	ULPCD_RSSI_SAMPLE_CFG
4CB	ULPCD_THRESH_LVL
4CC	ULPCD_GPIO3
559	TXIRQ_GUARDTIME
55D	FDT_DEFAULTVAL
561	RXIRQ_GUARDTIME
562-6D2	RFU
6D3	NFCLD_RFLD_Valid
6D4-ABB	RFU
ABC	RFU
ABD-BD9	RFU
BAD	CORRECTION_ENTRY_TABLE
C03	RTRANS_FRTANS_TABLE
C83	CFG_NOV_CAL
C84	NOV_CAL_VAL1

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
C85	NOV_CAL_VAL2
C86	NOV_CAL_THRESHOLD
C87	NOV_CAL_OFFSET1
C8B	NOV_CAL_OFFSET2
C8F	VDDPA_DISCHARGE
C9D	ARC_RM_A106_FDT
CA8-CC4	RFU
CC5	Tx_Symbol23_Mod_Reg_BR_53
CC9	Tx_Data_Mod_Reg_BR_53
CCD	Tx_Symbol23_Mod_Reg_BR_106
CD1	Tx_Data_Mod_Reg_BR_106
CD5	Tx_Symbol23_Mod_Reg_BR_212
CD9	Tx_Data_Mod_Reg_BR_212
CDA-CDE	RFU
CDF	CardModeUltraLowPowerEnabled
CE0	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_ENABLE
CE1	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON
CE2	Up to FW2.01: RFU from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON
CE3-CE7	DO NOT MODIFY - INTERNAL SETTINGS
CE8	RxGuardTO_Multiple
CE9	up to FW 2.03: RFU from FW2.05 onwards: DigitalTBSignalIndex
CEA	up to FW 2.03: RFU from FW2.05 onwards: DigitalTBSignalBit
CEB	up to FW 2.03: RFU from FW2.05 onwards: AnalogTBSignal
CEC	up to FW 2.06: RFU from FW 2.07 onwards: ENABLE_ULFO_TRIM_CALIBRATION
CED	up to FW2.8: RFU from FW2.9 onwards: ENABLE_LFO_TRIM_CALIBRATION
CEE	up to FW 2.09: RFU from FE 2.0A onwards: LpcdWithAutocollExpiryInterval
CEF	up to FW 2.09: RFU from FE 2.0A onwards: EnableHIFPadsReConfig
CF0	up to FW 2.09: RFU

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Table 106. EEPROM CONFIGURATION REGISTER*...continued*

Address (hex)	Name
	from FE 2.0A onwards: SPIPadReConfig
CF4-D2C	RFU
D2D-D3C	up to FW 2.03: RFU from FW2.05 onwards: USER DATA
D3Dh-1400h	DO NOT MODIFY - INTERNAL SETTINGS

9.26.2 DCDC_PWR_CONFIG (0000h)

Table 107. DCDC_PWR_CONFIG (address 0000h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0	DC-DC usage in card mode	7	0b: DC-DC is disabled 1b: DC-DC is enabled
	DC-DC usage in reader mode	6	0b: DC-DC is disabled 1b: DC-DC is enabled
	RFU	5	Do not touch, default value 01b
	VUP input voltage	4..0	0x00: Not connected or 0 V 0x01: Internal VDDPA_LDO used, internal DC-DC not used: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR) 0x02: Internal DC-DC: with fixed VDDBOOST 0x03: RFU 0x04: Internal DC-DC used: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V. 0x05 - 0x09: RFU 0x10: Internal VDDPA_LDO used, internal DC-DC not used: VUP supplied by external LDO (not connected to VBAT)

9.26.3 DCDC_CONFIG (0001h)

Table 108. DCDC_CONFIG (address 0001h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	DC-DC configuration	7:5	RFU
		4	DC-DC passthrough feature is: 0: Not supported (Vout = 0v or +5v) 1: Supported (Vout = 0v, Vin or +5v)
		3	Use of DC-DC for LPCD (attention: not ULPCD) 1: enabled 0: disabled
		2:0	RFU

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9.26.4 TXLDO_CONFIG (0002h)

Table 109. TXLDO_CONFIG (address 0002h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2	TX_LDO Configuration	31:2	RFU
		1	Overcurrent protection (0: Disable, 1: Enable)
		0	Enable TXLDO 0b: disabled - no voltage output of the TXLDO 1b: enabled - regulated output of the TXLDO

9.26.5 TXLDO_VDDPA_HIGH (0006h)

Table 110. TXLDO_VDDPA_HIGH (address 0006h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
6	TX_LDO output: initial voltage in case the DPC is used. Applies directly at the beginning of the RF-field-on before any DPC regulation takes place. (Initial VDDPA Voltage at RF ON). These values define as well the TX_LDO output voltage in case the DPC is disabled and not used.	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70

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Table 110. TXLDO_VDDPA_HIGH (address 0006h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.26.6 TXLDO_VDDPA_MAX_RDR (0008h)

Table 111. TXLDO_VDDPA_MAX_RDR (address 0008h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
8	VDDPA maximum output voltage in case the DPC is enabled in reader mode. This is used only when DPC is enabled. This ensures the Maximum Voltage up to which VDDPA reached during DPC Regulation.	7:0	0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50

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Table 111. TXLDO_VDDPA_MAX_RDR (address 0008h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

9.26.7 BOOST_DEFAULT_VOLTAGE (000Ah)

Table 112. BOOST_DEFAULT_VOLTAGE (address 000Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0A	DC-DC configuration This Field is Used only in case of Fixed BOOST. In case of Variable BOOST the value is calculated based on the VDDPA.	7:0	VDDBOOST output voltage in case of DC-DC with fixed VDDBOOST is enabled (PWR_CONFIG) 0x00: 3.1 V 0x01: 3.2 V 0x02: 3.3 V 0x03: 3.4 V 0x04: 3.5 V 0x05: 3.6 V 0x06: 3.7 V 0x07: 3.8 V 0x08: 3.9 V 0x09: 4.0 V 0x0A: 4.1 V 0x0B: 4.2 V 0x0C: 4.3 V 0x0D: 4.4 V 0x0E: 4.5 V 0x0F: 4.6 V 0x10: 4.7 V 0x11: 4.8 V 0x12: 4.9 V 0x13: 5.0 V 0x14: 5.1 V 0x15: 5.2 V 0x16: 5.3 V 0x17: 5.4 V 0x18: 5.5 V 0x19: 5.6 V 0x1A: 5.7 V

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Table 112. BOOST_DEFAULT_VOLTAGE (address 000Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			0x1B: 5.8 V 0x1C: 5.9 V 0x1D: 6.0 V all other values: RFU

9.26.8 XTAL_CONFIG (0010h)

Table 113. XTAL_CONFIG (address 0010h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
10	Configuration for the XTAL startup procedure	7:1	RFU
		0	Crystal recalibration start after wake-up from standby 1: enable 0: disable

9.26.9 XTAL_TIMEOUT (0011h)

Table 114. XTAL_TIMEOUT (address 0011h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
11	Configuration for the XTAL startup procedure	7:0	Timeout for XTAL to be ready (in *128us), if the timeout happens, an XTAL error event will be raised. This configuration does not speed up the boot time.

9.26.10 CLK_INPUT_FREQ (0012h)

Table 115. CLK_INPUT_FREQ (address 0012h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
12	Configuration for the PLL input clock frequency	7:4	RFU
		3:0	0011b: 24 MHz 0100b: 32 MHz 0101b: 48 MHz 1000b: XTAL 27.12 MHz All others: RFU

9.26.11 XTAL_CHECK_DELAY (0013h)

Correct Crystal clocking is detected by locking the crystal to the PLL. This allows the system to start quick independent from the crystal startup time. High-quality crystals will start up typically fast and allow by this optimized current consumption, e.g, during ULPCD.

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A user needs to find an optimized balance between retry numbers of checking for a proper locking and the interval for checking for a locked PLL.

This allows to configure a timeout value for locking the crystal to the PLL. The timeout value is defined by **Retry_number** x **Interval**. If the timeout is reached, a clock error is raised.

Table 116. XTAL_CHECK_DELAY (address 0013h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
13	**Retry_number**	7:5	Max Number of retries before a clock error is raised
	Interval	4:0	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval. This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD and ULPCD.

9.26.12 TEMP_WARNING (0014h)

Table 117. TEMP_WARNING (address 0014h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
14	CLIF and PMU temperature warning	7:6	PMU high threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)
		5:4	PMU low threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)
		3:2	high threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) - in case temp sensor is triggered, transmitter and TX_LDO are shut down, system goes in low-power mode - default is 130 °C. This event is not indicated by an IRQ to the host, instead GPIO0 is used to indicate this critical event (Register PAD_CONFIG 0x52). GPIO0 is set from LOW to HIGH before the IC enters standby. To enable this event on GPIO0, the EEPROM configuration ENABLE_GPIO0_ON_OVERTEMP (0016h) must be set. **Remark:** As soon as the chip enters standby, the GPIO0 will go to LOW
		1:0	low threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) - in case temperature sensed is lower than threshold, system wakes up from low-power mode indicated by an IRQ - default is 114 °C. As soon as the chip wakes up, the wake-up source shall be checked to ensure a wake-up due to the low threshold sensing.

9.26.13 ENABLE_GPIO0_ON_OVERTEMP (0016h)

Table 118. ENABLE_GPIO0_ON_OVERTEMP (address 0016h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
16	RFU	7..1	-
	Set/Clear GPIO0 during over temperature.	0	If set, the GPIO0 is used to indicate a temperature event. The temperature warning levels are configured in the Register TEMP_WARNING (0014h).

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9.26.14 TX_SHAPING_CONFIG (0017h)

Table 119. TX_SHAPING_CONFIG (address 0017h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
17		7:1	RFU
		0	PWM scheme for RM 0: defining 3-levels for drivers TX1/2 - required for balanced antenna (default) 1: defining 2-levels for drivers TX1/2 - required for single ended antenna This value is written into CLIF_ANACTROL_TX_CONFIG_REG during Load protocol.

9.26.15 TX_INV_RM (0018h)

Table 120. TX_INV_RM (address 0018h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
18	Transmitter configuration	7:6	RFU
		5	0: TX1 non-inverted output (output zero remains zero) 1: TX1 inverted output (common mode operation, output zero becomes one) This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		4	0: TX2 non-inverted output (output zero remains zero) 1: TX2 inverted output (common mode operation, output zero becomes one) This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		3:2	RFU
		1	0: TX1 no phase shift, 0° 1: TX1 phase shifted by 180° This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.
		0	0: TX2 no phase shift, 0° 1: TX2 phase shifted by 180° This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.

9.26.16 TX_CLK_MODE_1 (0019h)

Table 121. TX_CLK_MODE_1 (address 0019h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
19	Transmitter clock configuration	7	RFU
		6:4	CLK_MODE_CW_RM
		3	RFU
		2:0	CLK_MODE_MOD_RM

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9.26.17 TX_CLK_MODE_2 (001Ah)

Table 122. TX_CLK_MODE_2 (address 001Ah) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
1A	Transmitter clock configuration	7	RFU
		6:4	CLK_MODE_DEFAULT
		3	RFU
		2:0	CLK_MODE_TRANS_RM

9.26.18 RESIDUAL_AMP_LEVEL_A106 (0022h)

Table 123. RESIDUAL_AMP_LEVEL_A106 (address 0022h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0% carrier FF: 100% carrier

9.26.19 EDGE_TYPE_A106 (0023h)

Table 124. EDGE_TYPE_A106 (address 0023h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 124. EDGE_TYPE_A106 (address 0023h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.20 EDGE_STYLE_A106 (0024h)

Table 125. EDGE_STYLE_A106 (address 0024h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.21 EDGE_LENGTH_A106 (0025h)

Table 126. EDGE_LENGTH_A106 (address 0025h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.22 RESIDUAL_AMP_LEVEL_A212 (0026h)

Table 127. RESIDUAL_AMP_LEVEL_A212 (address 0026h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.23 EDGE_TYPE_A212 (0027h)

Table 128. EDGE_TYPE_A212 (address 0027h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.24 EDGE_STYLE_A212 (0028h)

Table 129. EDGE_STYLE_A212 (address 0028h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.25 EDGE_LENGTH_A212 (0029h)

Table 130. EDGE_LENGTH_A212 (address 0029h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.26 RESIDUAL_AMP_LEVEL_A424 (002Ah)

Table 131. RESIDUAL_AMP_LEVEL_A424 (address 002Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2A	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.27 EDGE_TYPE_A424 (002Bh)

Table 132. EDGE_TYPE_A424 (address 002Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 132. EDGE_TYPE_A424 (address 002Bh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.28 EDGE_STYLE_A424 (002Ch)

Table 133. EDGE_STYLE_A424 (address 002Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.29 EDGE_LENGTH_A424 (002Dh)

Table 134. EDGE_LENGTH_A424 (address 002Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.30 RESIDUAL_AMP_LEVEL_A848 (002Eh)

Table 135. RESIDUAL_AMP_LEVEL_A848 (address 002Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.31 EDGE_TYPE_A848 (002Fh)

Table 136. EDGE_TYPE_A848 (address 002Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.32 EDGE_STYLE_A848 (0030h)

Table 137. EDGE_STYLE_A848 (address 0030h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.33 EDGE_LENGTH_A848 (0031h)

Table 138. EDGE_LENGTH_A848 (address 0031h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.34 RESIDUAL_AMP_LEVEL_B106 (0032h)

Table 139. RESIDUAL_AMP_LEVEL_B106 (address 0032h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.35 EDGE_TYPE_B106 (0033h)

Table 140. EDGE_TYPE_B106 (address 0033h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 140. EDGE_TYPE_B106 (address 0033h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.36 EDGE_STYLE_B106 (0034h)

Table 141. EDGE_STYLE_B106 (address 0034h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.37 EDGE_LENGTH_B106 (0035h)

Table 142. EDGE_LENGTH_B106 (address 0035h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.38 RESIDUAL_AMP_LEVEL_B212 (0036h)

Table 143. RESIDUAL_AMP_LEVEL_B212 (address 0036h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.39 EDGE_TYPE_B212 (0037h)

Table 144. EDGE_TYPE_B212 (address 0037h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.40 EDGE_STYLE_B212 (0038h)

Table 145. EDGE_STYLE_B212 (address 0038h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.41 EDGE_LENGTH_B212 (0039h)

Table 146. EDGE_LENGTH_B212 (address 0039h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.42 RESIDUAL_AMP_LEVEL_B424 (003Ah)

Table 147. RESIDUAL_AMP_LEVEL_B424 (address 003Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.43 EDGE_TYPE_B424 (003Bh)

Table 148. EDGE_TYPE_B424 (address 003Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 148. EDGE_TYPE_B424 (address 003Bh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.44 EDGE_STYLE_B424 (003Ch)

Table 149. EDGE_STYLE_B424 (address 003Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1,2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1,2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.45 EDGE_LENGTH_B424 (003Dh)

Table 150. EDGE_LENGTH_B424 (address 003Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.46 RESIDUAL_AMP_LEVEL_B848 (003Eh)

Table 151. RESIDUAL_AMP_LEVEL_B848 (address 003Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.47 EDGE_TYPE_B848 (003Fh)

Table 152. EDGE_TYPE_B848 (address 003Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.48 EDGE_STYLE_B848 (0040h)

Table 153. EDGE_STYLE_B848 (address 0040h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.49 EDGE_LENGTH_B848 (0041h)

Table 154. EDGE_LENGTH_B848 (address 0041h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.50 RESIDUAL_AMP_LEVEL_F212 (0042h)

Table 155. RESIDUAL_AMP_LEVEL_F212 (address 0042h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.51 EDGE_TYPE_F212 (0043h)

Table 156. EDGE_TYPE_F212 (address 0043h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 156. EDGE_TYPE_F212 (address 0043h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.52 EDGE_STYLE_F212 (0044h)

Table 157. EDGE_STYLE_F212 (address 0044h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.53 EDGE_LENGTH_F212 (0045h)

Table 158. EDGE_LENGTH_F212 (address 0045h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.54 RESIDUAL_AMP_LEVEL_F424 (0046h)

Table 159. RESIDUAL_AMP_LEVEL_F424 (address 0046h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.55 EDGE_TYPE_F424 (0047h)

Table 160. EDGE_TYPE_F424 (address 0047h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.56 EDGE_STYLE_F424 (0048h)

Table 161. EDGE_STYLE_F424 (address 0048h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.57 EDGE_LENGTH_F424 (0049h)

Table 162. EDGE_LENGTH_F424 (address 0049h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.58 RESIDUAL_AMP_LEVEL_V100_26 (004Ah)

Table 163. RESIDUAL_AMP_LEVEL_V100_26 (address 004Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.59 EDGE_TYPE_V100_26 (004Bh)

Table 164. EDGE_TYPE_V100_26 (address 004Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 164. EDGE_TYPE_V100_26 (address 004Bh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.60 EDGE_STYLE_V100_26 (004Ch)

Table 165. EDGE_STYLE_V100_26 (address 004Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.61 EDGE_LENGTH_V100_26 (004Dh)

Table 166. EDGE_LENGTH_V100_26 (address 004Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.62 RESIDUAL_AMP_LEVEL_V100_53 (004Eh)

Table 167. RESIDUAL_AMP_LEVEL_V100_53 (address 004Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.63 EDGE_TYPE_V100_53 (004Fh)

Table 168. EDGE_TYPE_V100_53 (address 004Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.64 EDGE_STYLE_V100_53 (0050h)

Table 169. EDGE_STYLE_A106 (address 0050h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.65 EDGE_LENGTH_V100_53 (0051h)

Table 170. EDGE_LENGTH_V100_53 (address 0051h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.66 RESIDUAL_AMP_LEVEL_V100_106 (0052h)

Table 171. RESIDUAL_AMP_LEVEL_V100_106 (address 0052h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.67 EDGE_TYPE_V100_106 (0053h)

Table 172. EDGE_TYPE_V100_106 (address 0053h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 172. EDGE_TYPE_V100_106 (address 0053h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.68 EDGE_STYLE_V100_106 (0054h)

Table 173. EDGE_STYLE_V100_106 (address 0054h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.69 EDGE_LENGTH_V100_106 (0055h)

Table 174. EDGE_LENGTH_V100_106 (address 0055h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.70 RESIDUAL_AMP_LEVEL_100_212 (0056h)

Table 175. RESIDUAL_AMP_LEVEL_100_212 (address 0056h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.71 EDGE_TYPE_V100_212 (0057h)

Table 176. EDGE_TYPE_V100_212 (address 0057h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.72 EDGE_STYLE_V100_212 (0058h)

Table 177. EDGE_STYLE_V100_212 (address 0058h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.73 EDGE_LENGTH_V100_212 (0059h)

Table 178. EDGE_LENGTH_V100_212 (address 0059h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.74 RESIDUAL_AMP_LEVEL_V10_26 (005Ah)

Table 179. RESIDUAL_AMP_LEVEL_V10_26 (address 005Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.75 EDGE_TYPE_V10_26 (005Bh)

Table 180. EDGE_TYPE_V10_26 (address 005Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 180. EDGE_TYPE_V10_26 (address 005Bh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.76 EDGE_STYLE_V10_26 (005Ch)

Table 181. EDGE_STYLE_V10_26 (address 005Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.77 EDGE_LENGTH_V10_26 (005Dh)

Table 182. EDGE_LENGTH_V10_26 (address 005Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.78 RESIDUAL_AMP_LEVEL_V10_53 (005Eh)

Table 183. RESIDUAL_AMP_LEVEL_V10_53 (address 005Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.79 EDGE_TYPE_V10_53 (005Fh)

Table 184. EDGE_TYPE_V10_53 (address 005Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.80 EDGE_STYLE_V10_53 (0060h)

Table 185. EDGE_STYLE_V10_53 (address 0060h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.81 EDGE_LENGTH_V10_53 (0061h)

Table 186. EDGE_LENGTH_V10_53 (address 0061h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.82 RESIDUAL_AMP_LEVEL_V10_106 (0062h)

Table 187. RESIDUAL_AMP_LEVEL_V10_106 (address 0062h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.83 EDGE_TYPE_V10_106 (0063h)

Table 188. EDGE_TYPE_V10_106 (address 0063h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction

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Table 188. EDGE_TYPE_V10_106 (address 0063h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.84 EDGE_STYLE_V10_106 (0064h)

Table 189. EDGE_STYLE_V100_212 (address 0064h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.85 EDGE_LENGTH_V10_106 (0065h)

Table 190. EDGE_LENGTH_V10_106 (address 0065h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.86 RESIDUAL_AMP_LEVEL_V10_212 (0066h)

Table 191. RESIDUAL_AMP_LEVEL_V10_212 (address 0066h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.87 EDGE_TYPE_V10_212 (0067h)

Table 192. EDGE_TYPE_V10_212 (address 0067h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.88 EDGE_STYLE_V10_212 (0068h)

Table 193. EDGE_STYLE_V10_212 (address 0068h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.89 EDGE_LENGTH_V10_212 (0069h)

Table 194. EDGE_LENGTH_V100_212 (address 0069h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.90 RESIDUAL_AMP_LEVEL_180003m3_tari18p88 (006Ah)

Table 195. RESIDUAL_AMP_LEVEL_180003m3_tari18p88 (address 006Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.91 EDGE_TYPE_180003m3_tari18p88 (006Bh)

Table 196. EDGE_TYPE_180003m3_tari18p88 (address 006Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA

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Table 196. EDGE_TYPE_180003m3_tari18p88 (address 006Bh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.92 EDGE_STYLE_180003m3_tari18p88 (006Ch)

Table 197. EDGE_STYLE_180003m3_tari18p88 (address 006Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.93 EDGE_LENGTH_180003m3_tari18p88 (006Dh)

Table 198. EDGE_LENGTH_180003m3_tari18p88 (address 006Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.94 RESIDUAL_AMP_LEVEL_180003m3_tari9p44 (006Eh)

Table 199. RESIDUAL_AMP_LEVEL_180003m3_tari9p44 (address 006Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

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9.26.95 EDGE_TYPE_180003m3_tari9p44 (006Fh)

Table 200. EDGE_TYPE_180003m3_tari9p44 (address 006Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.96 EDGE_STYLE_180003m3_tari9p44 (0070h)

Table 201. EDGE_STYLE_180003m3_tari9p44 (address 0070h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

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9.26.97 EDGE_LENGTH_180003m3_tari9p44 (0071h)

Table 202. EDGE_LENGTH_180003m3_tari9p44 (address 0071h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.98 RESIDUAL_AMP_LEVEL_B_PRIME_106 (0072h)

Table 203. RESIDUAL_AMP_LEVEL_180003m3_tari18p88 (address 0072h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
22	Transmitter shaping configuration	7:0	Residual amplitude level 00: 0 % carrier FF: 100 % carrier

9.26.99 EDGE_TYPE_B_PRIME_106 (0073h)

Table 204. EDGE_TYPE_B_PRIME_106 (address 0073h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
23	Transmitter shaping configuration	7:4	Definition of edge transition style of falling edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU
		3:0	Definition of edge transition style of rising edge Defines style of edge transition: Firmware based shaping: 1: linear transition between two amplitude levels 2: two linear transitions between amplitude levels 3: three linear transitions between amplitude levels Others: RFU Lookup table based shaping: 4: lookup table-based transition, no automatic adaptation based on VDDPA

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Table 204. EDGE_TYPE_B_PRIME_106 (address 0073h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction others: RFU

9.26.100 EDGE_STYLE_B_PRIME_106 (0074h)

Table 205. EDGE_STYLE_B_PRIME_106 (address 0074h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
24	RFU	7	-
	Transmitter shaping configuration falling edge	6:4	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of falling edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
	RFU	3	-
	Transmitter shaping configuration rising edge	2:0	If EDGE_TYPE is 1, 2 or 3: Time constant configuration of rising edge (depends on edge style) If EDGE_TYPE is 4,5,6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

9.26.101 EDGE_LENGTH_B_PRIME_106 (0075h)

Table 206. EDGE_LENGTH_B_PRIME_106 (address 0075h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
25	Transmitter shaping configuration	7	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) 0=disabled (1 transition state = one carrier cycle) 1=enabled (1 transition state = two carrier cycles)
		6:5	RFU
		4:0	Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

9.26.102 DPC_CONFIG (0076h)

Table 207. DPC_CONFIG (address 0076h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
76	DPC Configuration	7:3	RFU
		2	DPC in Active Target Mode: 0: disabled, 1: enabled

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Table 207. DPC_CONFIG (address 0076h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
		1	DPC in Active Initiator Mode: 0: disabled, 1: enabled
		0	DPC in Reader/ Passive Initiator Mode: 0: disabled, 1: enabled

9.26.103 DPC_TARGET_CURRENT (077h)

Table 208. DPC_TARGET_CURRENT (address 077h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
77	DPC Configuration	15:0	VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC. This configuration shall not exceed 350 mA - hysteresis.

Note: *The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.*

9.26.104 DPC_HYSTERESIS_LOADING (079h)

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

Table 209. DPC_HYSTERESIS_LOADING (address 079h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
79	DPC Configuration	7:0	Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during loading.

Note: *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

Note: *In most application, the default values work well and do not need to be modified.*

9.26.105 DPC_HYSTERESIS_UNLOADING (07Ch)

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

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Table 210. DPC_HYSTERESIS_UNLOADING (address 07Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
7C	DPC Configuration	7:0	Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during unloading.

Note: *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

Note: *In most application, the default values work well and do not need to be modified.*

9.26.106 DPC_TXLDOVDDPALow (007Dh)

Table 211. DPC_TXLDOVDDPALow (address 007Dh) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
7D	DPC Configuration	7:0	VDDPA Low Limit for RDON

9.26.107 DPC_TXGSN (007Eh)

Table 212. DPC_TXGSN (address 007Eh) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
7E	DPC Configuration	7:0	for tx1_gsn < 20: resistance = 10 Ohm / (tx1_gsn + 1) for tx1_gsn >= 20: resistance = 0.5 Ohm

9.26.108 DPC_RDON_Control (007Fh)

Table 213. DPC_RDON_Control (address 007Fh) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
7F	DPC Configuration	7:0	00: Disabled 01: RdON Control 02-FF: RFU

9.26.109 DPC_InitialRDOn_RFOn (0080h)

Table 214. DPC_InitialRDOn_RFOn (address 0080h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
80	DPC Configuration	7:0	Initial GSP TX1/TX2 value during FieldON

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9.26.110 DPC_TXLDO_MAX_DROP (0081h)

Table 215. DPC_TXLDO_MAX_DROP (address 0081h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
81	DPC Configuration		At DPC start (on initial RF ON), if TXLDO drop out is higher to this value then VDDPA is reduced to: eVddpaSafe if no boost bypass on going else Vddpa is stopped. Unit is mV. Default = E10h = 3600mV

9.26.111 DPC_GUARD_TIME (087h)

Table 216. DPC_GUARD_TIME (address 087h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
87	DPC guard time configuration	7:0	Guard time before TX and after RX. 1unit = 1us. The DPC regulation is done once before TX and once after RX. The guard time parameter is the time between DPC regulation completion and TX start. The guard time parameter is the time between RX stop and DPC regulation start. The guard time is always enabled for TX

Note: *Recommendation is not to modify the default value.*

9.26.112 DPC_ENABLE_DURING_FDT (088h)

Table 217. DPC_ENABLE_DURING_FDT (address 088h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
88	RFU	7-1	-
	DPC Configuration	0	DPC regulation enable during FDT 0: DPC disabled during FDT (debug purpose only) 1: DPC enabled during FDT (recommendation)

9.26.113 DPC_GUARD_TIME_AFTER_RX (089h)

Table 218. DPC_GUARD_TIME_AFTER_RX (address 089h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
89	RFU	7:1	-
89	DPC Configuration	0	Enable DPC guard time after RX 0: disable (debug purposes) 1: enable (recommended) The guard time can be configured in register DPC_GUARD_TIME

Note: *The guard time is always enabled for TX and cannot be disabled.*

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9.26.114 DPC_LOOKUP_TABLE (008Bh-0133h)

Table 219. DPC_LOOKUP_TABLE (008Bh-0133h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
	ENTRY 0	31:0	This is the entry for 1.5 V
08B	Target current reduction	31:24	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
08C	AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
08D	AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
08E	AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)
08F	ENTRY 1	31:0	This is the entry for 1.6 V
….			….
093	ENTRY 2	31:0	This is the entry for 1.7 V
…..			….
….			This is the entry for 5.6 V
0133	ENTRY 42	31:0	This is the entry for 5.7 V

9.26.115 ARC_CONFIG (0137h)

Table 220. ARC_CONFIG (address 0137h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
137	ARC Setting configuration	7	ARC algorithm enable 0: Disable 1: Enable
		6:3	RFU
		2:0	Number of entries in ARC table. (value between 0 to 4) 0: one entry 1: two entries 2: three entries 3: four entries 4: five entries

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9.26.116 ARC_VDDPA (0139h)

Table 221. ARC_VDDPA (0139Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
13D	VDDPA_4	7:0	Byte[4] = VDDPA range_index 4: if VDDPA voltage between VDDPA_3 to ARC_ VDDPA_4
13C	VDDPA_3	7:0	Byte[3] = VDDPA_range_index 3: if VDDPA voltage between VDDPA_2 to ARC_ VDDPA_3 - 0.1
13B	VDDPA_2	7:0	Byte[2] = VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_ VDDPA_2 - 0.1
13A	VDDPA_1	7:0	Byte[1] = VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_ VDDPA_1 - 0.1)
139	VDDPA_0	7:0	Byte[0] = VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1)

Note: *VDDPA setting for Bytes 0...4:*

0x00: 1V50

0x01: 1V60

0x02: 1V70

0x03: 1V80

0x04: 1V90

0x05: 2V00

0x06: 2V10

0x07: 2V20

0x08: 2V30

0x09: 2V40

0x0A: 2V50

0x0B: 2V60

0x0C: 2V70

0x0D: 2V80

0x0E: 2V90

0x0F: 3V00

0X10: 3V10

0x11: 3V20

0x12: 3V30

0x13: 3V40

0x14: 3V50

0x15: 3V60

0x16: 3V70

0x17: 3V80

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0x18: 3V90

0x19: 4V00

0x1A: 4V10

0x1B: 4V20

0x1C: 4V30

0x1D: 4V40

0x1E: 4V50

0x1F: 4V60

0x20: 4V70

0x21: 4V80

0x22: 4V90

0x23: 5V00

0x24: 5V10

0x25: 5V20

0x26: 5V30

0x27: 5V40

0x28: 5V50

0x29: 5V60

0x2A: 5V70

9.26.117 ARC_RM_A106 (013Eh)

This is the setting for type A-106.

Table 222. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
146	RM_RX_ARC_4	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
144	RM_RX_ARC_3	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used

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Table 222. ARC_RM_A106 (address 013Eh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
142	RM_RX_ARC_2	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
140	RM_RX_ARC_1	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
13E	RM_RX_ARC_0	15:0	Bit[15] This setting is only taken into account if bit 14 of address 13E is set. 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used Bit [14]: 1: ARC enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

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9.26.118 ARC_RM_A212 (0148h)

This is the setting for type A-212.

Table 223. ARC_RM_A212 (address 0148h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
150	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14E	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14C	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
14A	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
148	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT

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Table 223. ARC_RM_A212 (address 0148h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.119 ARC_RM_A424 (0152h)

This is the setting for type A-424.

Table 224. ARC_RM_A424 (address 0152h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
15A	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
158	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
156	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

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Table 224. ARC_RM_A424 (address 0152h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
154	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
152	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.120 ARC_RM_A848 (015Ch)

This is the setting for type A-848.

Table 225. ARC_RM_A848 (address 015Ch) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
164	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
162	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used

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Table 225. ARC_RM_A848 (address 015Ch) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
160	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
15E	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
15C	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.121 ARC_RM_B106 (0166h)

This is the setting for type B-106.

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Table 226. ARC_RM_B106 (address 0166h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
16E	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
16C	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
16A	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
168	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
166	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter.

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Table 226. ARC_RM_B106 (address 0166h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.122 ARC_RM_B212 (0170h)

This is the setting for type B-212.

Table 227. ARC_RM_B212 (address 0170h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
178	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
176	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
174	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
172	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used

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Table 227. ARC_RM_B212 (address 0170h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
170	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.123 ARC_RM_B424 (017Ah)

This is the setting for type B-424.

Table 228. ARC_RM_B424 (address 017Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
182	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
180	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

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Table 228. ARC_RM_B424 (address 017Ah) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17E	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17C	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
17A	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.124 ARC_RM_B848 (0184h)

This is the setting for type B-848.

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Table 229. ARC_RM_B848 (address 0184h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
18C	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
18A	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
188	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
186	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
184	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter.

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Table 229. ARC_RM_B848 (address 0184h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.125 ARC_RM_F212 (018Eh)

This is the setting for type F-212.

Table 230. ARC_RM_F212 (address 018Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
196	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
194	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
192	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
190	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F212 are used

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Table 230. ARC_RM_F212 (address 018Eh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
18E	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.126 ARC_RM_F424 (0198h)

This is the setting for type F-424.

Table 231. ARC_RM_F424 (address 0198h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1A0	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19E	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

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Table 231. ARC_RM_F424 (address 0198h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19C	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
19A	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_F424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
198	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.127 ARC_RM_V_6p6 (01A2h)

This is the setting for type A-106.

Table 232. ARC_RM_V_6p6 (address 01A2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1AA	RM_RX_ARC_4	15:0	Bit[15]

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Table 232. ARC_RM_V_6p6 (address 01A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A8	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A6	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A4	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1A2	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

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Table 232. ARC_RM_V_6p6 (address 01A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.128 ARC_RM_V_26 (01ACh)

This is the setting for type V 26.

Table 233. ARC_RM_V_26 (address 01ACh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1B4	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B2	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B0	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1AE	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used

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Table 233. ARC_RM_V_26 (address 01ACh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1AC	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.129 ARC_RM_V53 (01B6h)

This is the setting for type V53.

Table 234. ARC_RM_V53(address 01B6h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1BE	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1BC	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

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Table 234. ARC_RM_V53(address 01B6h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1BA	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B8	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V53 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1B6	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.130 ARC_RM_V106 (01C0h)

This is the setting for type V106.

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Table 235. ARC_RM_V106(address 01C0h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1C8	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C6	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C4	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C2	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1C0	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter.

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Table 235. ARC_RM_V106(address 01C0h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.131 ARC_RM_V212 (01CAh)

This is the setting for type V212.

Table 236. ARC_RM_V212(address 01CAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1D2	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D0	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CE	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CC	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_V212 are used

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Table 236. ARC_RM_V212(address 01CAh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1CA	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.132 ARC_RM_180003m3_SC424_4Man (01D4h)

This is the setting for type 180003m3_SC424_4Man.

Table 237. ARC_RM_180003m3_SC424_4Man (address 01D4h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1DC	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4 MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1DA	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used

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Table 237. ARC_RM_180003m3_SC424_4Man (address 01D4h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4 MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_ 4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D8	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_ SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4 MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_ 4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D6	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_ SC424_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4 MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_ 4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1D4	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

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9.26.133 ARC_RM_180003m3_SC424_2Man (01DEh)

This is the setting for type 180003m3_SC424_2Man.

Table 238. ARC_RM_180003m3_SC424_2Man (address 01DEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1E6	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E4	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E2	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:9] = RFU Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E0	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

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Table 238. ARC_RM_180003m3_SC424_2Man (address 01DEh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1DE	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.134 ARC_RM_180003m3_SC848_4Man (01E8h)

This is the setting for type 180003m3_SC848_4Man.

Table 239. ARC_RM_180003m3_SC848_4Man (address 01E8h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1F0	RM_RX_ ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_ 180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003 M3_SC848_4MAN are used, else settings will be used from Load Protocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_ TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EE	RM_RX_ ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_ 180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003 M3_SC848_4MAN are used, else settings will be used from Load Protocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_ TECH register, applies as soon as the ARC is enabled)

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Table 239. ARC_RM_180003m3_SC848_4Man (address 01E8h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EC	RM_RX_ ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_ 180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003 M3_SC848_4MAN are used, else settings will be used from Load Protocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_ TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1EA	RM_RX_ ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_ 180003M3_SC848_4MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003 M3_SC848_4MAN are used, else settings will be used from Load Protocol 180003M3_SC848_4MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_ TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1E8	RM_RX_ ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_ TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.135 ARC_RM_180003m3_SC848_2Man (01F2h)

This is the setting for type 180003m3_SC848_2Man.

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Table 240. ARC_RM_180003m3_SC848_2Man (address 01F2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1FA	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F8	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F6	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1F4	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

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Table 240. ARC_RM_180003m3_SC848_2Man (address 01F2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
1F2	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.136 ARC_RM_AI106 (01FCh)

This is the setting for type AI106.

Table 241. ARC_RM_AI106 (address 01FCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
204	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
202	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
200	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU

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Table 241. ARC_RM_AI106 (address 01FCh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
			Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1FE	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
1FC	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.137 ARC_RM_AI212 (0206h)

This is the setting for type AI212.

Table 242. ARC_RM_AI212 (0206h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
20E	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

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Table 242. ARC_RM_AI212 (0206h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
20C	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
20A	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
208	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI212 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
206	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

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9.26.138 ARC_RM_AI424 (0210h)

This is the setting for type AI424.

Table 243. ARC_RM_AI424 (0210h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
218	RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
216	RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
214	RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
212	RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used 1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424 Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
210	RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change

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Table 243. ARC_RM_AI424 (0210h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

Note: *Bit15 of all RM_RX_ARC_n is recommended to be "0" always.*

9.26.139 RF_DEBOUNCE_TIMEOUT (02B2h)

Table 244. RF_DEBOUNCE_TIMEOUT (address 02B2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B2	DEBOUNCE_ TIMEOUT	7:0	Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF Value is entered in micro seconds, each bit represents 1 micro second

9.26.140 SENSE_RES (02B3h)

Table 245. SENSE_RES (address 02B3) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B3	AUTOCOLL configuration	16:0	ATQA in order byte 0, byte 1
		16:8	Byte1
		7:0	Byte0

9.26.141 NFC_ID1 (02B5h)

Table 246. NFC_ID1 (address 2B5h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B5	AUTOCOLL configuration		If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID. The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically
		23:16	Byte2
		15:8	Byte1:
		7:0	Byte0:

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9.26.142 SEL_RES (02B8h)

Table 247. SEL_RES (address 2B8h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B8	AUTOCOLL configuration	7:0	Response to Select: SAK

9.26.143 FELICA_POLL_RES (02B9h)

The FeliCa response is configured by 18 bytes.

Table 248. FELICA_POLL_RES (address 02B9) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2B9	AUTOCOLL configuration	15:0	FeliCa polling response: shall be 01h, FEh (2 bytes)
2BB		47:0	FeliCa polling response: NFCID2 (6 bytes)
2C1		63:0	FeliCa polling response: PAD (8 bytes)
2C9		15:0	FeliCa polling response: system code (2 bytes)

9.26.144 RANDOM_UID_ENABLE (02CBh)

Table 249. RANDOM_UID_ENABLE (address 2CBh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2CB	RFU	7:1	-
	Random UID Enable	0	0: Use UID stored in EEPROM 1: Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random A new random number is generated after each RF-OFF to RF-ON.

9.26.145 MFC_AUTH_TIMEOUT (02CCh)

Table 250. MFC_AUTH_TIMEOUT (address 2CCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2CC	RFU	15:0	Timeout value in micro seconds used for Auth1 and Auth2 stages during MIFARE Classic Authenticate

9.26.146 RSSI_TIMER (02DAh)

Configuration for Card Emulation mode only.

Table 251. RSSI_TIMER (address 2DAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DA	RSSI_TIMER	15:0	Default: 423

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9.26.147 RSSI_TIMER_FIRST_PERIOD (02DCh)

Table 252. RSSI_TIMER_FIRST_PERIOD (address 2DCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DC	RSSI	15:0	First period duration after Rffield ON. Unit is 128/fc (106 kHz) if set to 0 it means that feature is not used 0D2 => ~2 ms

9.26.148 RSSI_CTRL_00_AB (02DEh)

Table 253. RSSI_CTRL_00_AB (address 2DEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DE	RSSI	7:6	Bits [6:7] = RFU
		5:0	Bits [0:5] = (APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB)

9.26.149 RSSI_NB_ENTRIES_AB (02DFh)

Table 254. RSSI_NB_ENTRIES_AB (address 2DFh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2DF	RSSI	7:5	RFU
		4:0	For Initial RF ON, CEA and CEB Number of entries in RSSI lookup table (it refers to dwRssiEntryAB_01 to dwRssiEntry AB_X);

9.26.150 RSSI_THRESHOLD_PHASE_TABLE (02E0h)

Table 255. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
2E0	wRssiThresholdF_01	15:0	bit[0:12] - RSSI Value bit[13:15] - RFU Note: dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)
2E2	ArbPhaseF_01	15:0	wArbPhaseF_xx: Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)
	RssiThresholdF_02	15:0	-
	ArbPhaseF_02	15:0	-
	RssiThresholdF_03	15:0	-
	ArbPhaseF_03	15:0	-
	RssiThresholdF_04	15:0	-
	ArbPhaseF_04	15:0	-
	RssiThresholdF_05	15:0	-
	ArbPhaseF_05	15:0	-
	RssiThresholdF_06	15:0	-

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Table 255. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
	ArbPhaseF_06	15:0	-
	RssiThresholdF_07	15:0	-
	ArbPhaseF_07	15:0	-
	RssiThresholdF_08	15:0	-
	ArbPhaseF_08	15:0	-
	RssiThresholdF_09	15:0	-
	ArbPhaseF_09	15:0	-
	RssiThresholdF_0A	15:0	-
	ArbPhaseF_0A	15:0	-
	RssiThresholdF_0B	15:0	-
	ArbPhaseF_0B	15:0	-
	RssiThresholdF_0C	15:0	-
	ArbPhaseF_0C	15:0	-
	RssiThresholdF_0D	15:0	-
	ArbPhaseF_0D	15:0	-
	RssiThresholdF_0E	15:0	-
	ArbPhaseF_0E	15:0	-
	RssiThresholdF_0F	15:0	-
	ArbPhaseF_0F	15:0	-
	RssiThresholdF_10	15:0	-
	ArbPhaseF_10	15:0	-
	RssiThresholdF_11	15:0	-
	ArbPhaseF_11	15:0	-
	RssiThresholdF_12	15:0	-
	ArbPhaseF_12	15:0	-
	RssiThresholdF_13	15:0	-
	ArbPhaseF_13	15:0	-
	RssiThresholdF_14	15:0	-
	ArbPhaseF_14	15:0	-
	RssiThresholdF_15	15:0	-
	ArbPhaseF_15	15:0	-
	RssiThresholdF_16	15:0	-
	ArbPhaseF_16	15:0	-
	RssiThresholdF_17	15:0	-
	ArbPhaseF_17	15:0	-
	RssiThresholdF_18	15:0	-

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Table 255. RSSI_THRESHOLD_PHASE_TABLE (address 2E0h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
	ArbPhaseF_18	15:0	-

9.26.151 TX_PARAM_ENTRY_TABLE (03A2h)

Table 256. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
3A2	TxParamEntry_00_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_00_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_00_Tx2	7:0	Scaling factor for TX1 and TX2
3A5	TxParamEntry_01_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_01_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_01_Tx2	7:0	Scaling factor for TX1 and TX2
3A8	TxParamEntry_02_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID

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Table 256. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	bTxParamEntry_02_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_02_Tx2	7:0	Scaling factor for TX1 and TX2
3AB	TxParamEntry_03_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_03_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_03_Tx2	7:0	Scaling factor for TX1 and TX2
3AE	TxParamEntry_04_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_04_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_04_Tx2	7:0	Scaling factor for TX1 and TX2
3B1	TxParamEntry_05_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID

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Table 256. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	bTxParamEntry_05_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_05_Tx2	7:0	Scaling factor for TX1 and TX2
3B4	TxParamEntry_06_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_06_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_06_Tx2	7:0	Scaling factor for TX1 and TX2
3B7	TxParamEntry_07_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_07_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_07_Tx2	7:0	Scaling factor for TX1 and TX2
3BA	TxParamEntry_08_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID

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Table 256. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
	bTxParamEntry_08_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_08_Tx2	7:0	Scaling factor for TX1 and TX2
3BD	TxParamEntry_09_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_09_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_09_Tx2	7:0	Scaling factor for TX1 and TX2
3C1	TxParamEntry_0A_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID
	bTxParamEntry_0A_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_0A_Tx2	7:0	Scaling factor for TX1 and TX2
3C3	TxParamEntry_0B_ID	7	bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): 0 - Dual driver, 1 - Single driver
		6	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): 0 - Disabled, 1 - Enabled
		5:0	ID

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Table 256. TX_PARAM_ENTRY_TABLE (address 3A2h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
	bTxParamEntry_0B_Tx1	7:6	RFU
		5:0	PMU VDDPA setting: VDDPA(v) = (val*10)+1,5 0 = 1.50 V ... 2Ah = 5.70 V
	bTxParamEntry_0B_Tx2	7:0	Scaling factor for TX1 and TX2

9.26.152 LPCD_AVG_SAMPLES (0492h)

Configuration for the Switch mode LPCD

Table 257. LPCD_AVG_SAMPLES (address 0492h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
492	LPCD setting	7:0	Defining how many samples of the I and Q values are used for the averaging. Average of samples in power of 2 0->1 sample 1->2 samples 2->4 samples 3->8 samples 4->16 samples 5-> 32 samples 6-> 64 samples

9.26.153 LPCD_RSSI_TARGET (0494h)

Table 258. LPCD_RSSI_TARGET (address 0494h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
494	RFU	15:10	-
	LPCD setting	9:0	This value is used for the LPCD as DGRM_RSSI_TARGET. Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used.

9.26.154 LPCD_RSSI_HYST (0496h)

Table 259. LPCD_RSSI_HYST (address 0496h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
496	LPCD setting	7:0	This value is used for the LPCD as DGRM_RSSI_HYST Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used

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9.26.155 LPCD_CONFIG (0497h)

Table 260. LPCD_CONFIG (address 0497h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
497	RFU	15:6	-
		5	Immediate RF OFF before TXLDO shutdown to save power 0 - Disable 1 - Enable
		4	VDDPA fast discharge 0 - Disable 1 - Enable
		3	TX Drivers 0 - Enable Single driver 1 - Enable both drivers
	Acquisition channels:	2:0	0:1 = RFU 2 = Magnitude 3 = I and Q 4 =M, I and Q 5:7 = RFU

9.26.156 LPCD_THRESHOLD_COARSE (049Ah)

Table 261. LPCD_THRESHOLD_COARSE (address 049Ah) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
49A	LPCD Q channel threshold	31:16	ADC LSB granularity of threshold depends on avg_samples_meas value 5: unit 1/32; 4: unit 1/16; 3: unit 1/8; 2: unit 1/4; 1: unit 1/2; 0: unit 1
	LPCD I channel threshold	0:15	ADC LSB granularity of threshold depends on avg_samples_meas value 5: unit 1/32; 4: unit 1/16; 3: unit 1/8; 2: unit 1/4; 1: unit 1/2; 0: unit 1

Note: *If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.*

9.26.157 WAIT_RX_SETTLE (04ABh)

Table 262. WAIT_RX_SETTLE (address 04ABh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4AB	LPCD Delay	7:0	Delay between Field-On and starting ADC data averaging for the LPCD. Value in us, default 14h = 20us

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9.26.158 LPCD_VDDPA (04AFh)

Table 263. LPCD_VDDPA (address 04AFh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4AF	VDDPA voltage during LPCD when DC-DC (internal or external) or external power source is used to feed TXLDO	7:0	TXLDO output voltage: 0x00: 1V50 0x01: 1V60 0x02: 1V70 0x03: 1V80 0x04: 1V90 0x05: 2V00 0x06: 2V10 0x07: 2V20 0x08: 2V30 0x09: 2V40 0x0A: 2V50 0x0B: 2V60 0x0C: 2V70 0x0D: 2V80 0x0E: 2V90 0x0F: 3V00 0X10: 3V10 0x11: 3V20 0x12: 3V30 0x13: 3V40 0x14: 3V50 0x15: 3V60 0x16: 3V70 0x17: 3V80 0x18: 3V90 0x19: 4V00 0x1A: 4V10 0x1B: 4V20 0x1C: 4V30 0x1D: 4V40 0x1E: 4V50 0x1F: 4V60 0x20: 4V70 0x21: 4V80 0x22: 4V90 0x23: 5V00 0x24: 5V10 0x25: 5V20 0x26: 5V30 0x27: 5V40 0x28: 5V50 0x29: 5V60 0x2A: 5V70

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9.26.159 XTAL_CONTROL (04BDh)

Table 264. XTAL_CONTROL (address 04BDh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
04BD	Configuration for the electrical XTAL startup conditions	15:7	Must not be changed
		6	XTAL_OVER_BOOST_EN
		5:0	XTAL_AMP_CTRL

Note: *This settings may help to reduce the current consumption in ULPCD mode, particularly when a fast XTAL is used.*

9.26.160 ULPCD_VDDPA_CTRL (04BFh)

Table 265. ULPCD_VDDPA_CTRL (address 4BFh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
	RFU	15:9	-
	LDO_VDDPA_VOUT_SEL	8:3	TXLDO output voltage during ULPCD polling VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */ VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */ VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */ VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */ VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */ VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */ VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */ VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */ VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */ VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */ VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */ VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */ VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */ VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */

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Table 265. ULPCD_VDDPA_CTRL (address 4BFh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */ VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */ VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */ VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */ VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */ VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */ VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */ VDDPA_5V70, /* 0x2A */
4BF	RFU	2:0	-

9.26.161 ULPCD_TIMING_CTRL (04C2h)

Table 266. ULPCD_TIMING_CTRL (address 4C2h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C2	RFON_GUARD_TIME	7:4	RFON guard time: (RFON_GUARD_TIME + 2) * LFO-Freq (380 kHz) Guard time: Time between RF-ON and first sampling of data
	RFU	3:0	-

9.26.162 ULPCD_VOLTAGE_CTRL (04C6h)

Table 267. ULPCD_VOLTAGE_CTRL (address 4C6h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C6	ULPCD configuration	7:5	RFU
		4:2	RFU
		1	TX_SUPPLY by VUP_TX 0: VUP externally supplied (2.8 V to 6.0 V) 1: VUP supplied by PN5190B1 itself (pin VUP_TX connected to VBAT/VBATPWR)
		0	RFU

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9.26.163 ULPCD_RSSI_GUARD_TIME (04C9h)

Table 268. ULPCD_RSSI_GUARD_TIME (address 4C9h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4C9	ULPCD RSSI sampling guard time	15	RFU
		14:0	This is the time between consecutive RSSI samples: Range: 0 - 127 in micro seconds

9.26.164 ULPCD_RSSI_SAMPLE_CFG (04CAh)

Table 269. ULPCD_RSSI_SAMPLE_CFG (address 4CAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CA	ULPCD configuration	7:0	Number of RSSI Samples which are internally averaged: 0: 4 samples, 1: 8 samples 2: 16 samples 3: 32 samples

9.26.165 ULPCD_THRESH_LVL(04CBh)

Table 270. ULPCD_THRESH_LVL (address 4CBh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CB	ULPCD configuration	8:0	RSSI Threshold level Range 0 - 31 If the difference between the measured RSSI value and the reference (which is derived during calibration) is greater than the threshold, then a card is detected.

9.26.166 ULPCD_GPIO3 (04CCh)

Table 271. ULPCD_GPIO3 (address 4CCh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
4CC	RFU	7:1	-
4CC	ULPCD GPIO3 configuration	0	GPIO3 abort polarity configuration. If PN5190B1 is using the ULPCD, GPIO3 cannot be used for any other purpose than aborting the ULPCD. 1: high-level aborts ULPCD 0: low-level aborts ULPCD

9.26.167 TXIRQ_GuardTime (0559h)

Table 272. TXIRQ_GuardTime (address 0559) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
559	TXIRQ_Guard Time	31:0	0 - Disabled 0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s

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9.26.168 FDT_default_val (055Dh)

Table 273. FDT_default_val (address 055D) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
55D	FDT_default_val	31:0	0x00 - Disabled others - enabled (1 unit is 18.86us) Default fixed to 5.5 secs

9.26.169 RXIRQ_GuardTime (0561h)

Table 274. RXIRQ_GuardTime (address 0561h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
55D	RXIRQ_Guard Time	31:0	0x00 Disabled 0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s Default value = 0xF4240 (1 s)

9.26.170 NFCLD_RFLD_Valid (006D3h)

Table 275. NFCLD_RFLD_Valid (address 06D3h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
6D3	RFU	7:1	-
	RFLD_ CALIBRATE	0	This bit allows to calibrate the RFLD / NFCLD. This calibration is required only once in the lifetime of the chip for increased RFLD / NFCLD accuracy, independent from the value of this bit (0 or 1). Clearing this bit (0) will calibrate the RFLD /RFLD during the next boot-up, precondition for the proper calibration is an unloaded condition and no external field applied. After calibration this bit is set (1) and indicates that the RFLD /RFLD Threshold is a valid data.

9.26.171 CORRECTION_ENTRY_TABLE (0BADh)

Table 276. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0BAD	sCorrection_Entry0	15:0	The correction that is applied when lookup table based shaping with scaling is enabled. Range is -128 to +127, sCorrection_Entry0 corresponds to correction applied at VDDPA = 1V5, Correction_Entry42 corresponds to correction applied at VDDPA = 5V7 For each entry: BYTE 0: Bits[7:0] = define the correction which is applied for ASK100 BYTE 1: Bits[15:8] = define the correction which is applied for ASK10
BAF	sCorrection_Entry1	15:0	-

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Table 276. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
BB1	sCorrection_Entry2	15:0	-
BB3	sCorrection_Entry3	15:0	-
BB5	sCorrection_Entry4	15:0	-
BB7	sCorrection_Entry5	15:0	-
BB9	sCorrection_Entry6	15:0	-
BBB	sCorrection_Entry7	15:0	-
BBD	sCorrection_Entry8	15:0	-
BBF	sCorrection_Entry9	15:0	-
BC1	sCorrection_Entry10	15:0	-
BC3	sCorrection_Entry11	15:0	-
BC5	sCorrection_Entry12	15:0	-
BC7	sCorrection_Entry13	15:0	-
BC9	sCorrection_Entry14	15:0	-
BCB	sCorrection_Entry15	15:0	-
BCD	sCorrection_Entry16	15:0	-
BCF	sCorrection_Entry17	15:0	-
BD1	sCorrection_Entry18	15:0	-
BD3	sCorrection_Entry19	15:0	-
BD5	sCorrection_Entry20	15:0	-
BD7	sCorrection_Entry21	15:0	-
BD9	sCorrection_Entry22	15:0	-
BDB	sCorrection_Entry23	15:0	-
BDD	sCorrection_Entry24	15:0	-
BDF	sCorrection_Entry25	15:0	-
BE1	sCorrection_Entry26	15:0	-
BE3	sCorrection_Entry27	15:0	-
BE5	sCorrection_Entry28	15:0	-
BE7	sCorrection_Entry29	15:0	-
BE9	sCorrection_Entry30	15:0	-
BEB	sCorrection_Entry31	15:0	-
BED	sCorrection_Entry32	15:0	-
BEF	sCorrection_Entry33	15:0	-
BF1	sCorrection_Entry34	15:0	-
BF3	sCorrection_Entry35	15:0	-
BF5	sCorrection_Entry36	15:0	-
BF7	sCorrection_Entry37	15:0	-

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Table 276. CORRECTION_ENTRY_TABLE (address 0BADh) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
BF9	sCorrection_Entry38	15:0	-
BFB	sCorrection_Entry39	15:0	-
BFD	sCorrection_Entry40	15:0	-
BFF	sCorrection_Entry41	15:0	-
C01	sCorrection_Entry42	15:0	-

9.26.172 TX_SHAPING_PROPRIETARY_1 (0C03h)

This EEPROM content serves as look-up input for the TX Shaping registers based on edge type and edge style setting.

The description of the functionality of the dedicated entries can be found in the description for the TX Shaping.

This table is valid for a protocol only, in case edge type is 4, 5,or 6 AND the edge style 0.

Table 277. TX_SHAPING_PROPRIETARY_1 (0C03h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0C03	RTRANS0	31:0	Rising Edge content for register RTRANS0
0C07	RTRANS1	31:0	Rising Edge content for register RTRANS1
0C0B	RTRANS2	31:0	Rising Edge content for register RTRANS2
0C0F	RTRANS3	31:0	Rising Edge content for register RTRANS3
0C13	FTRANS0	31:0	Falling Edge content for register FTRANS0
0C17	FTRANS1	31:0	Falling Edge content for register FTRANS1
0C1B	FTRANS2	31:0	Falling Edge content for register FTRANS2
0C1F	FTRANS3	31:0	Falling Edge content for register FTRANS3

9.26.173 TX_SHAPING_PROPRIETARY_2 (0C23h)

This EEPROM content serves as look-up input for the TX Shaping registers based on edge type and edge style setting.

The description of the functionality of the dedicated entries can be found in the description for the TX Shaping.

This table is valid for a protocol only, in case edge type is 4,5,or 6 AND the edge style 1.

Table 278. TX_SHAPING_PROPRIETARY_1 (0C23h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0C23	RTRANS0	31:0	Rising Edge content for register RTRANS0
0C27	RTRANS1	31:0	Rising Edge content for register RTRANS1
0C2B	RTRANS2	31:0	Rising Edge content for register RTRANS2
0C2F	RTRANS3	31:0	Rising Edge content for register RTRANS3
0C23	FTRANS0	31:0	Falling Edge content for register FTRANS0

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Table 278. TX_SHAPING_PROPRIETARY_1 (0C23h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
0C37	FTRANS1	31:0	Falling Edge content for register FTRANS1
0C3B	FTRANS2	31:0	Falling Edge content for register FTRANS2
0C3F	FTRANS3	31:0	Falling Edge content for register FTRANS3

9.26.174 TX_SHAPING_PROPRIETARY_3 (0C43h)

This EEPROM content serves as look-up input for the TX Shaping registers based on edge type and edge style setting.

The description of the functionality of the dedicated entries can be found in the description for the TX Shaping.

This table is valid for a protocol only, in case edge type is 4,5,or 6 AND the edge style 2.

Table 279. TX_SHAPING_PROPRIETARY_1 (0C43h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0C43	RTRANS0	31:0	Rising Edge content for register RTRANS0
0C47	RTRANS1	31:0	Rising Edge content for register RTRANS1
0C4B	RTRANS2	31:0	Rising Edge content for register RTRANS2
0C4F	RTRANS3	31:0	Rising Edge content for register RTRANS3
0C53	FTRANS0	31:0	Falling Edge content for register FTRANS0
0C57	FTRANS1	31:0	Falling Edge content for register FTRANS1
0C5B	FTRANS2	31:0	Falling Edge content for register FTRANS2
0C5F	FTRANS3	31:0	Falling Edge content for register FTRANS3

9.26.175 TX_SHAPING_PROPRIETARY_4 (0C63h)

This EEPROM content serves as look-up input for the TX Shaping registers based on edge type and edge style setting.

The description of the functionality of the dedicated entries can be found in the description for the TX Shaping.

This table is valid for a protocol only, in case edge type is 4,5,or 6 AND the edge style 3.

Table 280. TX_SHAPING_PROPRIETARY_1 (0C63h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0C63	RTRANS0	31:0	Rising Edge content for register RTRANS0
0C67	RTRANS1	31:0	Rising Edge content for register RTRANS1
0C6B	RTRANS2	31:0	Rising Edge content for register RTRANS2
0C6F	RTRANS3	31:0	Rising Edge content for register RTRANS3
0C73	FTRANS0	31:0	Falling Edge content for register FTRANS0
0C77	FTRANS1	31:0	Falling Edge content for register FTRANS1
0C7B	FTRANS2	31:0	Falling Edge content for register FTRANS2

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Table 280. TX_SHAPING_PROPRIETARY_1 (0C63h) EEPROM configuration bit description...*continued*

Address (hex)	Function	Bit	Description
0C7F	FTRANS3	31:0	Falling Edge content for register FTRANS3

9.26.176 CFG_NOV_CAL (0C83h)

TX non-overlap feature - defines the non-overlap time of TX1, TX2.

Table 281. CFG_NOV_CAL (address 0083h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	RFU	7:2	-
	CALIBRATION_TYPE	1:0	00 = No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed 01 = Enable FW calibration after every cold boot 10 = Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2 **(Default)** 11 = RFU

9.26.177 NOV_CAL_VAL1 (0C84h)

Table 282. NOV_CAL_VAL1 (address 0C84h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	VddpaCalVal1	7:0	It defines the VDDPA value that FW uses to perform NOV calibration group #1. value = 03h (1.8 V) value = 0Dh (2.8 V) See "TxLdoVddpaHigh" parameter for list of voltage

9.26.178 NOV_CAL_VAL2 (0C85h)

Table 283. NOV_CAL_VAL2 (0C85h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	VddpaCalVal2	7:0	It defines the VDDPA value that FW uses to perform NOV calibration group #2. default value = 15h (3.6 V) default value = 24h (5.1 V) See "TxLdoVddpaHigh" parameter for list of voltage

9.26.179 NOV_CAL_THRESHOLD (0C86h)

Table 284. NOV_CAL_THRESHOLD (address 0C86h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
1	CfgThreshold	7:0	It defines VDDPA threshold that FW will use to select Group #1 or Group #2 NOV offset values. default value = 08h (2.3 V) default value = 16h (3.7 V)

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Table 284. NOV_CAL_THRESHOLD (address 0C86h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
			See "TxLdoVddpaHigh" parameter for list of voltage

9.26.180 NOV_CAL_OFFSET1 (0C87h)

Table 285. NOV_CAL_OFFSET1 (address 0C87h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C87	RFU	31:29	-
	UserOffsets1	28:0	It defines user static offsets applied if CFG_NOV_CAL[1:0] = 10b bits[04:00] Group #1 (CfgThreshold to VDDPA max), offset_3l bits[12:08] Group #1 (CfgThreshold to VDDPA max), offset_3l_p2 bits[20:16] Group #1 (CfgThreshold to VDDPA max), offset_2l<0> bits[28:24] Group #1 (CfgThreshold to VDDPA max), offset_2l<1>

9.26.181 NOV_CAL_OFFSET2 (0C8Bh)

Table 286. NOV_CAL_OFFSET1 (address 0C8Bh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C8B	RFU	31:29	-
	UserOffsets2	28:0	It defines user static offsets applied if CFG_NOV_CAL1:0] = 10b bits[04:00] Group #2 (CfgThreshold to VDDPA max), offset_3l bits[12:08] Group #2 (CfgThreshold to VDDPA max), offset_3l_p2 bits[20:16] Group #2 (CfgThreshold to VDDPA max), offset_2l<0> bits[28:24] Group #2 (CfgThreshold to VDDPA max), offset_2l<1>

9.26.182 VDDPA_DISCHARGE (0C8Fh)

Table 287. VDDPA_DISCHARGE (address 0C8Fh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
C8F	RFU	7:1	RFU
	EnableFast VDDPADischarge	0	1 - Enables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF (default) 0 - Disables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF

9.26.183 ARC_RM_A106_FDT (0C9Dh)

This is the setting for type A-106.

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Table 288. ARC_RM_A106_FDT (address 0C9Dh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CA5	RM_RX_ARC_FDT_4	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
CA3	RM_RX_ARC_FDT_3	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
CA1	RM_RX_ARC_FDT_2	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
C9F	RM_RX_ARC_FDT_1	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
C9D	RM_RX_ARC_FDT_0	15:0	Bit[15]: RFU Bit [14]: Has to be always "0" Bits[13:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

Note: *The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.*

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9.26.184 Tx_Symbol23_Mod_Reg_BR_53 (0CC5h)

Table 289. Tx_Symbol23_Mod_Reg_BR_53 (0CC5Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CC5	15693_BR_CFG	31:0	CLIF_TX_SYMBOL23_MOD_REG value loaded for 15693 BR 53 kbit/s

9.26.185 Tx_Data_Mod_Reg_BR_53 (0CC9h)

Table 290. Tx_Data_Mod_Reg_BR_53 (0CC9Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CC9	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 53 kbit/s

9.26.186 Tx_Symbol23_Mod_Reg_BR_106 (0CCDh)

Table 291. Tx_Symbol23_Mod_Reg_BR_106 (0CCDEh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CCD	15693_BR_CFG	31:0	CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 106 kbit/s

9.26.187 Tx_Data_Mod_Reg_BR_106 (0CD1h)

Table 292. Tx_Data_Mod_Reg_BR_106 (0CD1Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD1	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 106 kbit/s

9.26.188 Tx_Symbol23_Mod_Reg_BR_212 (0CD5h)

Table 293. Tx_Symbol23_Mod_Reg_BR_212 (0CD5Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD5	15693_BR_CFG	31:0	CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 212 kbit/s

9.26.189 Tx_Data_Mod_Reg_BR_212 (0CD9h)

Table 294. Tx_Data_Mod_Reg_BR_212 (0CD9Eh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CD9	15693_BR_CFG	31:0	CLIF_TX_Data_MOD_REG value loaded for 15693 BR 212 kbit/s

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9.26.190 CardModeUltraLowPowerEnabled (0CDFh)

Table 295. CardModeUltraLowPowerEnabled (address 00DFh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CDF	RFU	7:1	-
	CALIBRATION_ TYPE	0	Enable Ultra Low-Power standby for CardMode.

Note: *Note: When bit 0 = 1, Switch Standby instruction with ULP mode cannot be used*

9.26.191 LPCD_EXT_DCDC_ENABLE (0CE0h)

Table 296. LPCD_EXT_DCDC_ENABLE (0CE0h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
CE0	up to FW 2.02: RFU	7:0	-
	from FW 2.03. onwards: RFU	7:1	-
	from FW 2.03. onwards: GPIO1 configuration for LPCD	0	Enables the use of GPIO to wake up EXT DC-DC from power saving during LPCD. This function is not available for the ULPCD.

9.26.192 LPCD_EXT_DCDC_DELAY_TO_ON (0CE1h)

Table 297. LPCD_EXT_DCDC_DELAY_TO_ON (0CE1h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
CE1	up to FW 2.02: RFU	7:0	-
	from FW 2.03. onwards: GPIO1 configuration for LPCD	7:0	The value defines the time between setting GPIO1 until Field is switched on. Time in us * 8 to wait for the Ext DC-DC to be started

9.26.193 LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h)

Table 298. LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h) EEPROM configuration register bit description

Address (hex)	Function	Bit	Description
CE2	until FW2.02: RFU	7:0	-
	from FW 2.03. onwards:	7:0	Value defines the time between Field Off and clear GPIO1. Time in us * 8 to wait for the Ext DC-DC to be shut down

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Table 298. LPCD_EXT_DCDC_DELAY_TO_OFF (0CE2h) EEPROM configuration register bit description...*continued*

Address (hex)	Function	Bit	Description
	GPIO1 configuration for LPCD		

9.26.194 RxGuardTO_Multiple (0CE8h)

Table 299. RxGuardTO_Multiple (address 00CE8h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
0CE8	RxGuardTO_ Multiple	7:0	This field configures the RxGuard Timeout configuration in multiple of Timeout configured using RXIRQ_GuardTime EEPROM Field (Address 0561h). Default value is 1. Indicating RX_TIMEOUT shall be triggered due to expiry of RXIRQ_GUARD first time only.

9.26.195 DigitalTBSignalIndex (0CE9h)

Available from FW 2.05 onwards:

Test bus number to be configured. Selected from the list of exposed test busses described in Instruction layer document.

Table 300. DigitalTBSignalIndex (address 0CE9h) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CE9	TB signal index	7:0	Digital signal test bus number from table "CTS and test bus signals" in instruction layer document Valid data as described in table, all others: RFU

9.26.196 DigitalTBSignalBit (0CEAh)

Available from FW 2.05 onwards:

Test bus bit number to be configured. Selected from the list of exposed test busses described in Instruction layer document.

Table 301. DigitalTBSignalBit (address 0CEAh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CEA	TB signal bit	7:0	Digital signal test bus bit number from table "CTS and test bus signals" in instruction layer document Valid data as described in table, all others: RFU

9.26.197 AnalogTBSignalIndex (0CEBh)

Available from FW 2.05 onwards:

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Analog test bus to be configured. Selected from the list of exposed test busses described in Instruction layer document.

Table 302. AnalogTBSignalIndex (address 0CEBh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CEB		7:0	Analog signal test bus number: 0x78 - obs_clif_tbcontrol_patchbox0 0x79 - obs_clif_tbcontrol_patchbox1 0x7A - obs_clif_tbcontrol_patchbox2 0x7B - obs_clif_tbcontrol_patchbox3 all others: RFU

9.26.198 ENABLE_ULFO_TRIM_CALIBRATION (0CECh)

Up to FW2.6 RFU

Available from FW2.7 onwards: ENABLE_LFO_TRIM_CALIBRATION

Table 303. ENABLE_ULFO_TRIM_CALIBRATION (address 0CECh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CEC	ENABLE_ ULFO_TRIM_ CALIBRATION	7:1	RFU
		0	1: Enable 0: Disable The internal calibration of the wake-up counter value is done based on the ULFO accuracy measured with Xtal as reference clock and the entered wake-up time. The calibration is done each time when the ULPCD mode is entered and the bit 1 is set. Note: This feature shall be used only when Xtal is available on the board, otherwise an accurate reference clock for the ULFO accuracy measurement is not available. No other user input is required to achieve a higher accuracy of the ULFO.

9.26.199 ENABLE_LFO_TRIM_CALIBRATION (0CEDh)

Up to FW2.7: RFU

Available from FW2.9 onwards: ENABLE_LFO_TRIM_CALIBRATION

Table 304. ENABLE_LFO_TRIM_CALIBRATION (0CEDh) EEPROM configuration bit description

Address (hex)	Function	Bit	Description
CED	ENABLE_ LFO_TRIM_ CALIBRATION	7:1	RFU
		0	until FW 2.07: RFU from FW 2.09 onwards: 1: Enable 0: Disable The internal calibration of wake-up Counter value will be done based on the LFO accuracy measured with Xtal as reference clock and the entered wake-up time.

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Table 304. ENABLE_LFO_TRIM_CALIBRATION (0CEDh) EEPROM configuration bit description*...continued*

Address (hex)	Function	Bit	Description
			The calibration is done each time when the LPCD mode is entered and the bit 1 is set. Note: This feature shall be used only when Xtal is available on the board, otherwise an accurate reference clock for the LFO accuracy measurement is not available. No other user input is required to achieve a higher accuracy of the LFO.

9.26.200 LpcdWithAutocollExpiryInterval (0CEEh)

Table 305. LpcdWithAutocollExpiryInterval (0CEEh) EEPROM configuration bit description (available from FW 2.0A onwards)

Address (hex)	Function	Bit	Description
CEE	Autocoll expiration time	7:0	This field is the time before Autocoll expires when LPCD is used with Autocoll option. 1 unit = 100 ms. Default value: 0x0A (10 ms)

9.26.201 EnableHIFPadsReConfig (0CEDh)

Table 306. EnableHIFPadsReConfig (0CEDh) EEPROM configuration bit description (available from FW 2.0A onwards)

Address (hex)	Function	Bit	Description
0CEDh	RFU	7:1	-
	EnableHIFPadsReConfig	0	Reconfigure the HIF Pads configuration. 0:->Disabled; 1-> enabled This bit enables/disables the function of EEPROM configuration SPIPadReConfig (0CF0h)

9.26.202 SPIPadReConfig (0CF0h)

Table 307. SPIPadReConfig (0CF0h) EEPROM configuration bit description (available from FW 2.0A onwards)

Address (hex)	Function	Bit	Description
CF3	RFU	7:2	-
	NSS Pad	0:1	00: Weak pulldown 01: No Pull 10: Bus Keeper 11: Weak pullup (default)
CF2	RFU	7:2	-
	MOSI Pad	0:1	00: Weak pulldown 01: No Pull; (default) 10: Bus Keeper 11: Weak pullup
CF1	RFU	7:2	-
	MISO Pad	0:1	00: Weak pulldown 01: No Pull; (default)

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Table 307. SPIPadReConfig (0CF0h) EEPROM configuration bit description (available from FW 2.0A onwards)*...continued*

Address (hex)	Function	Bit	Description
			10: Bus Keeper 11: Weak pullup
CF0	RFU	7:2	-
	SCK Pad	0:1	00: Weak pulldown 01: No Pull (default) 10: Bus Keeper 11: Weak pullup

9.26.203 USER_DATA (0D2Dh)

Table 308. USER_DATA (0D2Dh) EEPROM configuration bit description

available only from FW 2.5 onwards

Address (hex)	Function	Bit	Description
0D2D	USER_DATA Byte1	7:0	Custom defined R/W user data. Content does not have any impact on the functionality of the device. Note that frequent (e.g. automatic triggered) R/W cycles to this DWORD have an impact on the lifetime of the EEPROM as described in the chapter "EEPROM characteristics". ATTENTION: Any user data will be erased during a Firmware update.
	USER_DATA Byte2	7:0	
	USER_DATA Byte3	7:0	
	USER_DATA Byte4	7:0	
	USER_DATA Byte5	7:0	
	USER_DATA Byte6	7:0	
	USER_DATA Byte7	7:0	
	USER_DATA Byte8	7:0	
	USER_DATA Byte9	7:0	
	USER_DATA Byte10	7:0	
	USER_DATA Byte11	7:0	
	USER_DATA Byte12	7:0	
	USER_DATA Byte13	7:0	
	USER_DATA Byte14	7:0	

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Table 308. USER_DATA (0D2Dh) EEPROM configuration bit description...*continued*

available only from FW 2.5 onwards

Address (hex)	Function	Bit	Description
	USER_DATA Byte15	7:0	
	USER_DATA Byte16	7:0	

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10 Limiting values

Table 309. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	+ 2.0	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	+ 2.0	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	+500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

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11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

11.1 Thermal characteristics

Table 310. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	+25	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	+25	+105	°C

Table 311. Thermal characteristics VFLGA40 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFLGA40	44.2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	24.2	K/W

Table 312. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	22	K/W

Table 313. Junction Temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T_{j_max}	maximum junction temperature	-	-	+125	°C

Table 314. Thermal Shutdown Temperature

Symbol	Parameter	Conditions	Typ	Unit
$T_{shutdown}$	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

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11.2 Static characteristics

Table 315. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT_PWR)}$	supply voltage on pin VBAT_PWR (DC-DC input pin) $V_{DD(VBAT_PWR)}$ needs to be connected to $V_{DD(VBAT)}$	DC-DC disabled	2.4	-	5.5	V
		DC-DC enabled	2.8	-	4.8	V
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX (TX_LDO input pin)	Remark: If DC-DC is used, its output $V_{DD(BOOST)}$ Min is limited to 3.1 V	2.4	-	6.0	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT >= VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
$V_{I(RXP)}$	input voltage on pin RXP	-	-0.5	-	1.8	V
$V_{I(RXN)}$	input voltage on pin RXN	-	-0.5	-	1.8	V

Note: The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT

Note: $V_{DD(VBAT_PWR)}$ needs to be connected to $V_{DD(VBAT)}$

Table 316. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VBAT)}$	system supply		-	-	20	mA
$I_{DD(VDDIO)}$		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)}$ max	-	-	30	mA
$I_{DD(BOOST_IN)}$	DC-DC boost supply	average input current	-	-	1.0	A
		peak input current (short peak)	-	-	1.7	A
$I_{DD(VUP_TX)}$	input supply for transmitter LDO	-	-	-	350	mA
$I_{DD(VDDPA)}$	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA

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Table 316. Current consumption in active mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		supplied without DC-DC and without TXLDO active	-	-	400	mA

Table 317. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF\ Plus\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	µA
$I_{OFF\ Plus\ ULFO\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode, ULFO active (ULPCD during RF-OFF)	25 °C ambient operating temperature	-	5	-	µA
$I_{hard\ power\ down\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	µA
$I_{standby\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	µA
$I_{suspend\ (VBAT)}$	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
$I_{ULPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in ULPCD (Ultra Low-Power Card Detection) mode	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	22	-	µA
$I_{LPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	240	-	µA

Table 318. Overcurrent detection function [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VUP_TX)}$	current of overcurrent detection becoming active	-	450	550	650	mA

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[1] Refer to the Errata sheet. In normal operation within spec limits, this flag shall not be triggered under any circumstances. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active. The overcurrent protection shall be treated as an additional safety feature only.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 319. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$	0.7 * $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		0	-	0.3 * $V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(VBAT)}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	µA
C_i	input capacitance		-	5	-	pF
$t_{(ULPCD_abort)}$	VEN time required to abort ULPCD		5	-	-	ms

Table 320. GPIO input / output pins (GPIO_0 - 5, SWDIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65x VDDIO	-	VDDIO+0.5	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V 2.4 <= VDDIO <= 3.6	-	-	3	mA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ

Table 321. XTAL1, XTAL2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	VI= 1.65 V, no power saving, active mode	-	-	5	µA
I_{IL}	LOW-level input current	VI = 0 V, no power saving, active mode	-	-	1	µA

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Table 321. XTAL1, XTAL2 pins *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF

Table 322. IRQ pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	$V_{DD(VDDIO)}$ -0.4	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns
R_{pd}	pull-down resistance		40	-	62	kΩ

Table 323. ATX_B, ATX_C, ATX_D pins (SPI (SCLK, COTI, NTS))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.65 x $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		- 0.5	-	0.35 x $V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{VDDIO}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
R_{PU}	Weak pullup resistor		40	50	62	kΩ
R_{PD}	Weak pulldown resistor		40	50	62	kΩ
C_i	input capacitance		-	5	-	pF

Table 324. ATX_A pin (SPI (CITO))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	$V_{DD(VDDIO)}$ -0.4	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V

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Table 324. ATX_A pin (SPI (CITO))*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns

Table 325. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(dyn)}$	dynamic input voltage		-	-	1.8	V
C_i	input capacitance		-	1	-	pF
Z_i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 326. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDPA)}$=5.0 V; with internal VDDPA LDO	-	$V_{DD(VDDPA)}$ -150 mV	$V_{DD(VDDPA)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(VDDPA)}$=5.0 V;with internal VDDPA LDO	0	200	-	m

Table 327. AUX1, AUX2, AUX3 pins (Debug output)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AUX_OH}	HIGH-level output voltage	pin used as debug signal output	VDDIO -0.4	-	VDDIO	V
V_{AUX_OL}	LOW-level output voltage	pin used as debug signal output	0	-	0.4	V
I_{AUX_OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3.0	mA
I_{AUX_OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3.0	mA
C_{O_LOAD}	output capacitance load of pin		-	5	10	pF

Table 328. VTUNE0 and VTUNE1 output pins (Tuning DAC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O_VTUNE1_max}$	HIGH-level maximum output voltage VTUNE1	connected to a variable capacitor (varicap), VDDIO = 3.3 V Remark: Output voltage is limited by VDDIO and cannot be higher than this supply.	-	$V_{DD(VDDIO)}$	3.65	V

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Table 328. VTUNE0 and VTUNE1 output pins (Tuning DAC)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O_VTUNE0_max}$	HIGH-level maximum output voltage VTUNE0	connected to a variable capacitor (varicap), VBAT = 3.3 V Remark: Output voltage is limited by VBAT and cannot be higher than this supply.	-	$V_{DD(VBAT)}$	3.65	V
V_{O_min}	LOW-level minimum output voltage	connected to a variable capacitor (varicap)	- 0.3	0	200	mV
	DAC resolution		-	-	8	bits
C_{O_LOAD}	output capacitance load of pin		0	-	4	nF

11.3 Timing characteristics

Table 329. Power supply connection timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rise_vbat}	VBAT supply ramp	VEN = LOW	2.5	-	5000	µs
t_{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	VDDIO condition: VBAT > 2.4 V, VDDIO supply (external), hpd_off_sel = x	0	-	1000	ms
t_{boot}	startup time[1]	VDDIO condition: VBAT > 2.4 V, VDDIO supply (external), hpd_off_sel = x	-	-	Dependent on the configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals, which allow a fast settling. This allows to optimize the average current consumption during ULPCD.	ms
t_{vddio_ven}	startup sequence A: t_{vddio_ven} >= 25 ms time from VDDIO HIGH TO VEN HIGH	-	25	-	-	ms
	startup sequence B: t_{vddio_ven} < 25 ms time from VDDIO HIGH TO VEN HIGH	-	-	-	25	ms
	startup sequence C: VBAT = VDDIO = VEN	A VBAT power cycle is required to reset the IC.	0	-	0	ms

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Table 329. Power supply connection timing *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{sw_cmd}	time between VEN and host sending the SWITCH_MODE_ NORMAL command	-	1300	-	-	µs
$t_{ven_Boot_POR}$	reset time to get BOOT_ POR, if t_{vddio_ven} < 25 ms	-	25	-	-	ms

[1] (PN5190B1 ready to receive commands on the host interface). For ULPCD, the PN5190B1 indicates the ability to receive commands from a host after raising an IDLE IRQ.

Note: *Switching OFF VBAT during TX ON, might damage the IC - ensure to switch RF OFF before the power supply VBAT is disconnected.*

Note: *For details on BOOT_POR refer to the user manual.*

Information: *The first boot after production or FW update writes automatically calibration data to the EEPROM. If the chip is started up the first time after receiving the chip from NXP or after a firmware update, a reset (VEN toggling) shall only been performed after sending a SWITCH_MODE_NORMAL command and having received the response.*

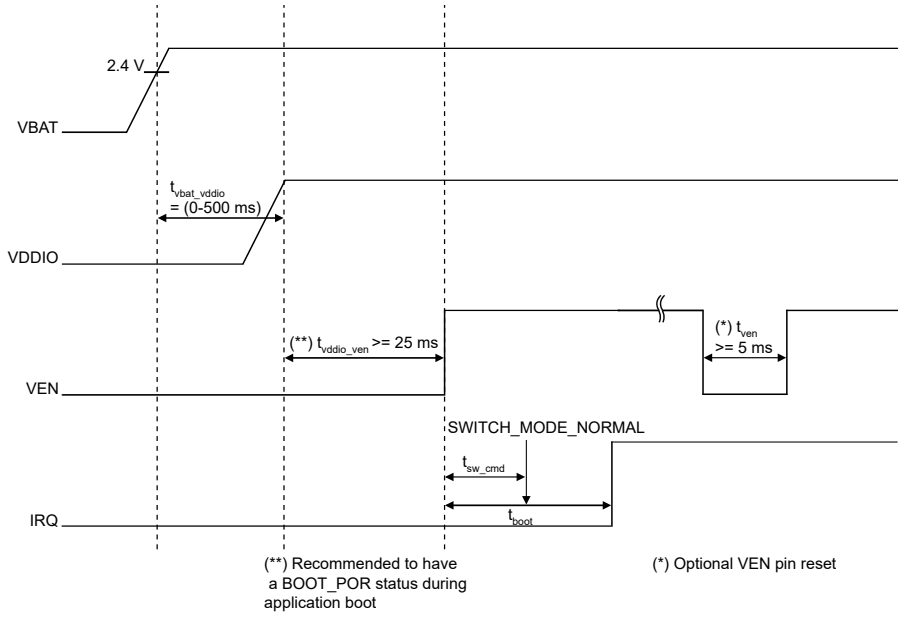


Figure 34. Startup sequence A (recommended)

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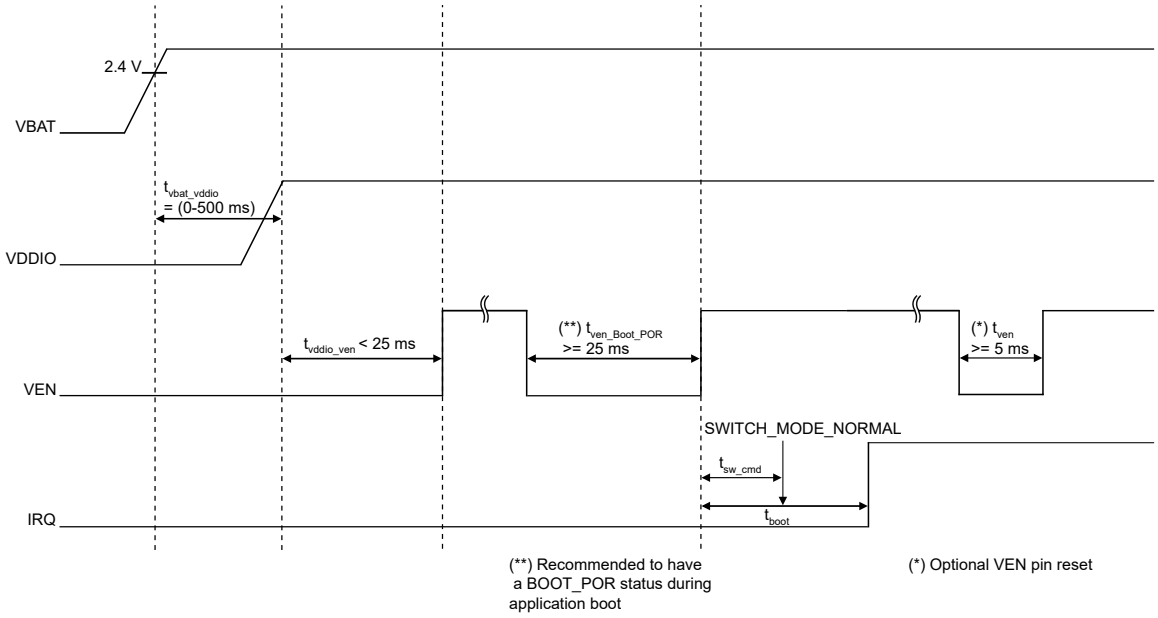


Figure 35. Startup sequence B

Note: *With FW version 2.09 (or higher), a missing BOOT_POR requires a manual initialization of the DPR register value, before the first RF_ON.*

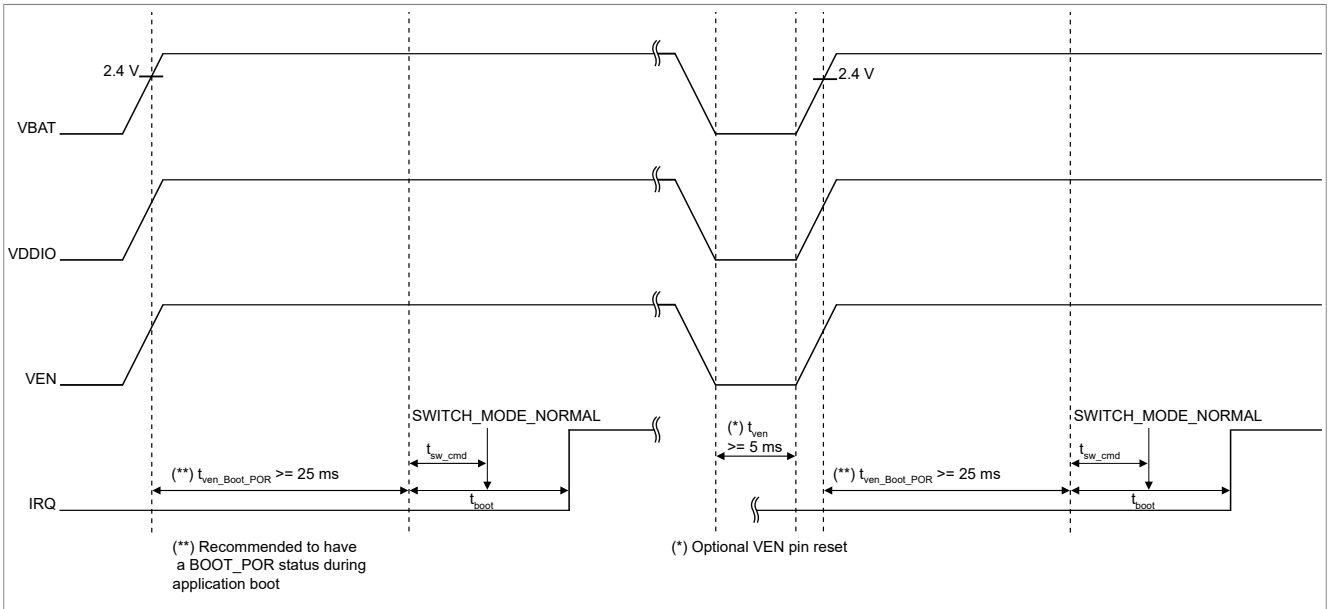


Figure 36. Startup sequence C

Note: *If VBAT = VDDIO = VEN (all connected together), then a VBAT power cycle is required to reset the IC.*

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Table 330. Pulse length

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(VEN)}$	on Pin VEN, pulse width to reset the chip or exit from ULPCD / Hard power-down state	-	5	-	-	ms
$t_{(wake-up)}$	on pin GPIOx, pulse width to wake up	-	1	-	-	µs
$t_{VEN(GPIO)}$	time from VEN HIGH to GPIOs available for use	-	100	-	-	ms

Table 331. DAC1, DAC2 conversion timing (Tuning DAC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{conversion}$	Conversion speed of 8-bit DAC1, DAC2	1 LSB rising falling, (depends on capacitive load) RF cut resistance: 100k Ohm (max), Cin: 8 nF (max)	-	-	0.15	ms
		Full signal rising from 0.0 V to 3 V, (depends on capacitive load) RF cut resistance: 100k Ohm (max), Cin: 8 nF (max)	-	-	0.15	ms
		falling from 3 V to 300 mV, (depends on capacitive load) RF cut resistance: 100k Ohm (max), Cin: 8 nF (max)	-	-	2	ms

Table 332. SPI interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	33.3	-	-	ns
t_{SCKH}	SCK HIGH time	33.3	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	16.65	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	16.65	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NTS HIGH time	0	-	-	ns
t_{NSSH}	NTS HIGH time	33.3	-	-	ns

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Table 333. RF_ON command timing following a previous RF_OFF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(RF_OFF-RF_ON)}$	RF_ON command timing	guard time between command sends for RF_OFF and command send for RF_ON, capacitors on the transmitter must be fully de-charged before the RF_ON command is sent	5.1	5.6	-	ms

11.4 DPC characteristics

Table 334. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (address 079h)	Depends on application target current	ApplicationTargetCurrent * 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_ CURRENT (077h)	Hysteresis as configured in DPC_ HYSTERESIS (address 079h)		-	350-Hysteresis	mA

11.5 Clock input

Table 335. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
delta f_{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C_L	load capacitance	-	6	8	10	pF
$t_{startup}$	crystal startup time	-	-	-	1	ms
P_{xtal}	crystal power dissipation	-	-	-	100	µW

Table 336. Recommended additional crystal requirements for ISO/IEC14443 compliant and ULPCD operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_L	Load capacitance	ULPCD	6	7	8	pF
C_m	Motion Capacitance	-	0.8	1	1.5	fF

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Table 336. Recommended additional crystal requirements for ISO/IEC14443 compliant and ULPCD operation*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{shunt}	Shunt Capacitance	Standard Operation	0.1	0.6	1	pF
		ULPCD	0.1	0.3	0.5	pF
$t_{startup}$ULPCD	Crystal start time	a fast startup of the crystal is recommended in ULPCD mode to achieve best power saving figures. This can be achieved by e.g. using a crystal with low shunt capacity.	-	-	0.4	ms

Note: *Refer to AN14518 Crystal Oscillator Design Guide ref.[4] for further consideration to design and tuning crystal oscillator for NFC design.*

11.6 EEPROM characteristics

Table 337. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu(W)}$	write endurance	at ambient temperature T_a = +25 °C	100	-	-	K cycles
t_{ret}	retention time	at ambient temperature T_a =+25 °C	25	-	-	years

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12 Package outline

12.1 VFBGA64 package

Table 338. Package outline VFBGA64 (SOT1307-2)

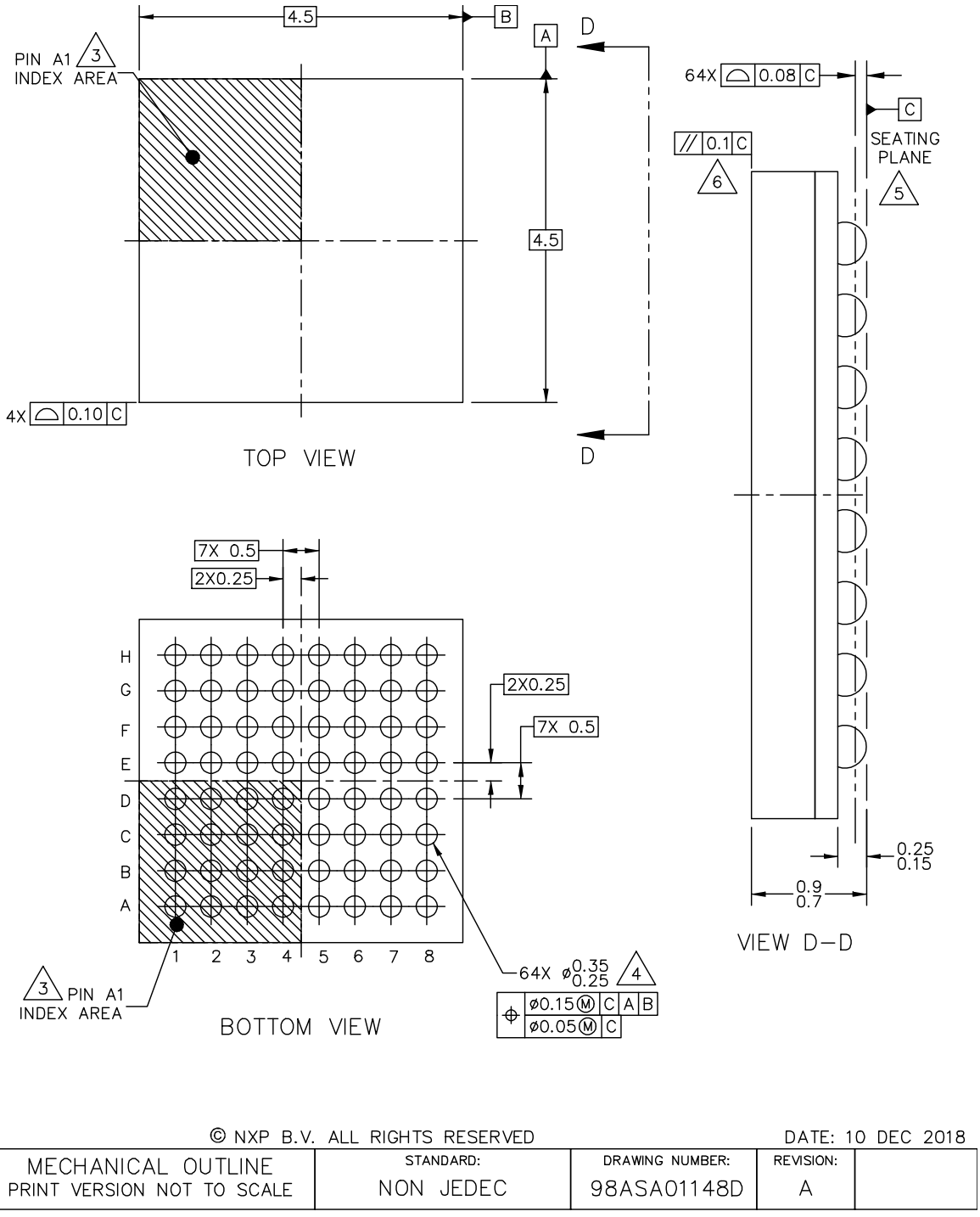


Figure 37. Package outline VFBGA64 (SOT1307-2)

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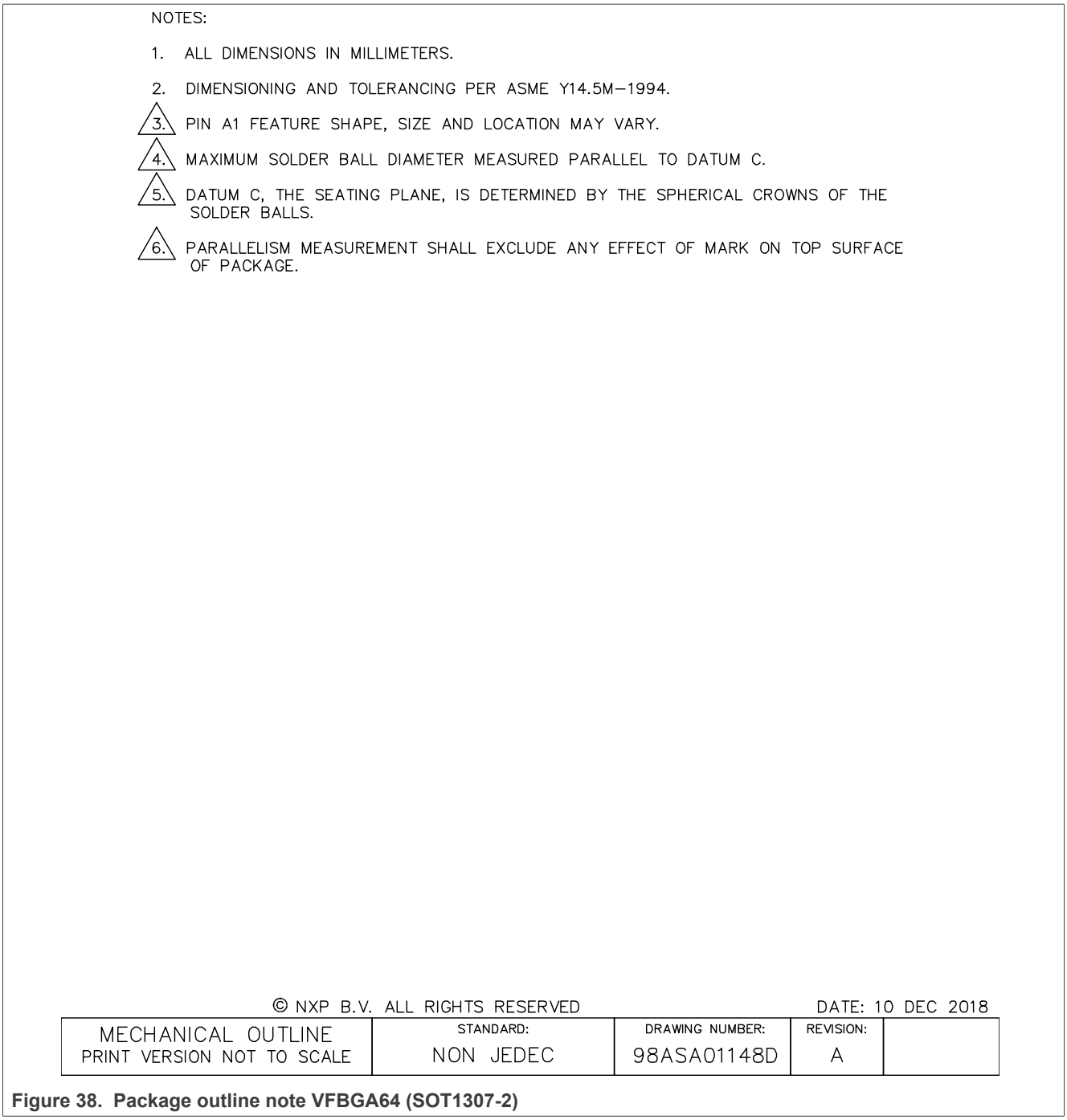


Figure 38. Package outline note VFBGA64 (SOT1307-2)

12.2 VFLGA40 package

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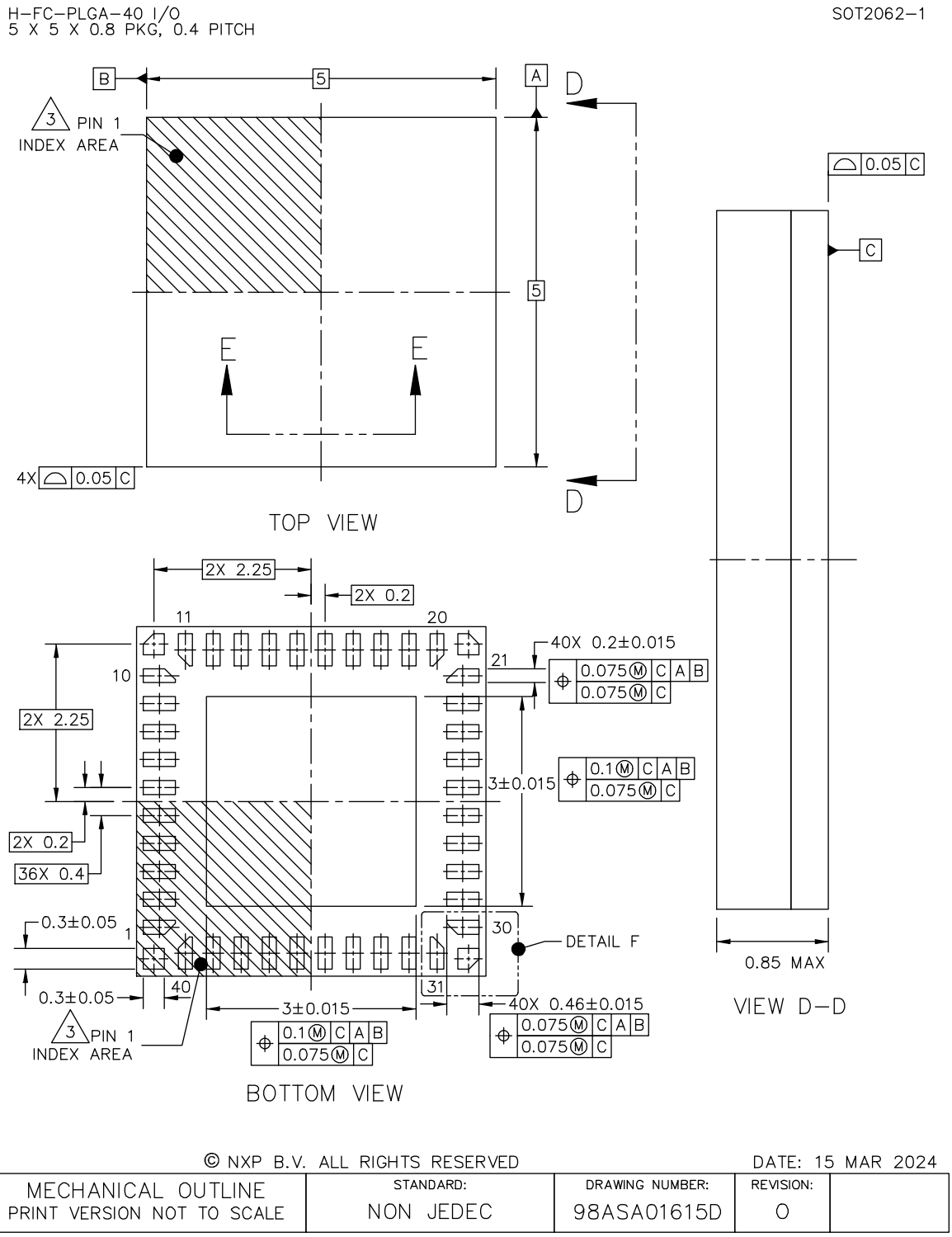


Figure 39. Package outline VFLGA40, SOT2062-1

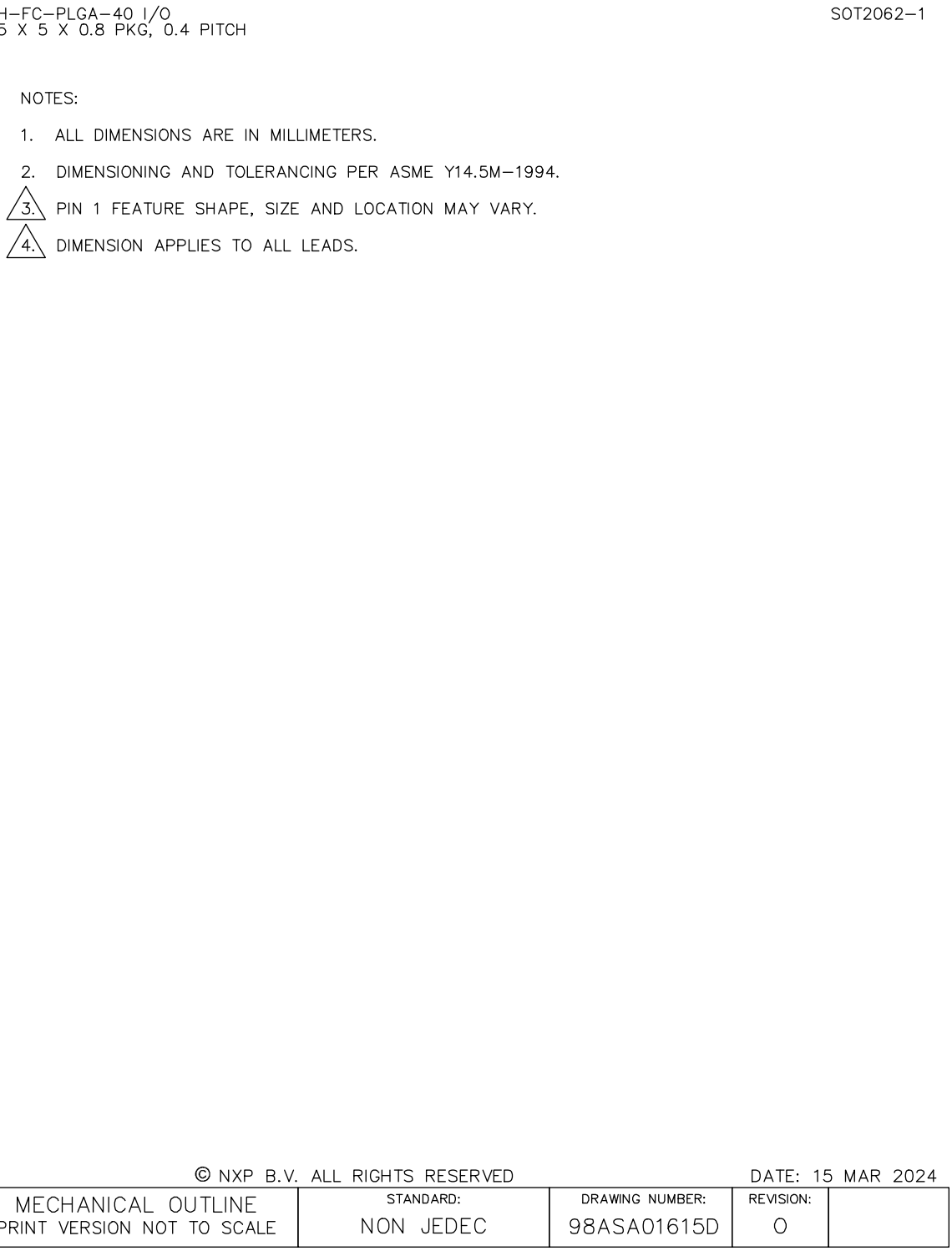


Figure 40. Package outline detail VFLGA40, SOT2062-1

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13 Package marking

13.1 Package marking drawing VFBGA64

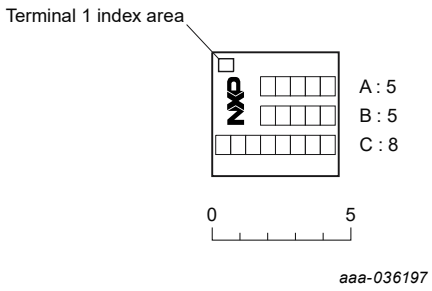


Figure 41. VFBGA64 Package 3 line marking

Line A: 5 characters; "PN5190D" (FW 2.0) or "5190E" (FW 2.1, FW 2.7)

Line B: 5 characters; contains the DB ID and AS ID

Line C: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level (“X” = engineering samples, “ “ = released product)

13.2 Package marking drawing VFLGA40

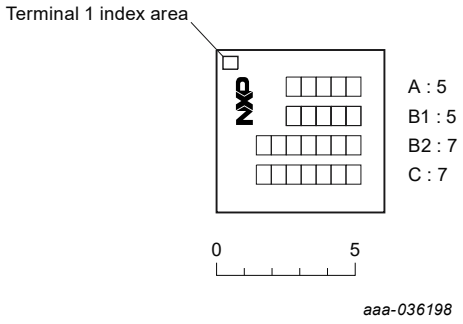


Figure 42. Marking VFLGA40 package SOT2062-1

Line A: 5 characters; "5190D" (FW 2.0) or "5190E" (FW 2.1, FW 2.7)

Line B1: 5 characters; contains the DB ID

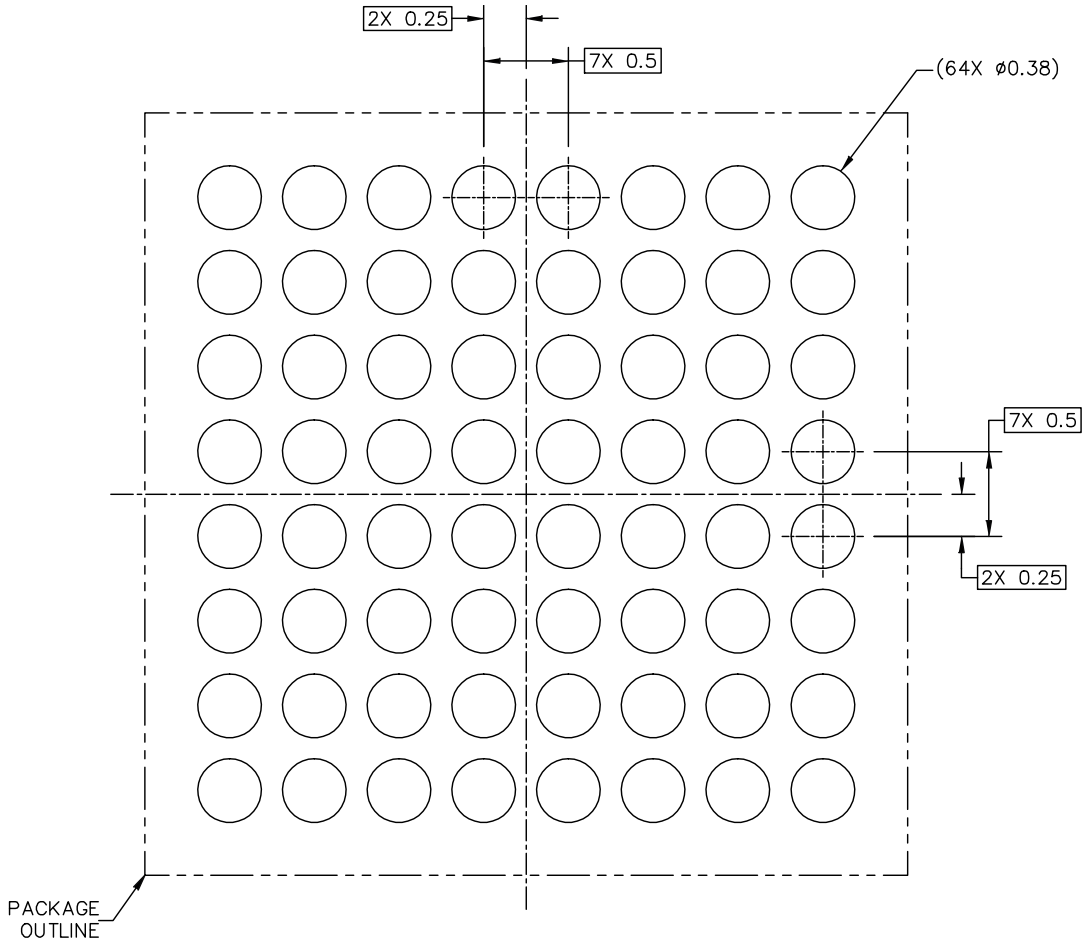
Line B2: 7 characters; contains the DB ID (continued) and AS ID (2 digits)

Line C: 7 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level (“X” = engineering samples, “Y” = customer qualification samples, “ “ = released product)

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14 Reflow soldering footprint VFBGA64



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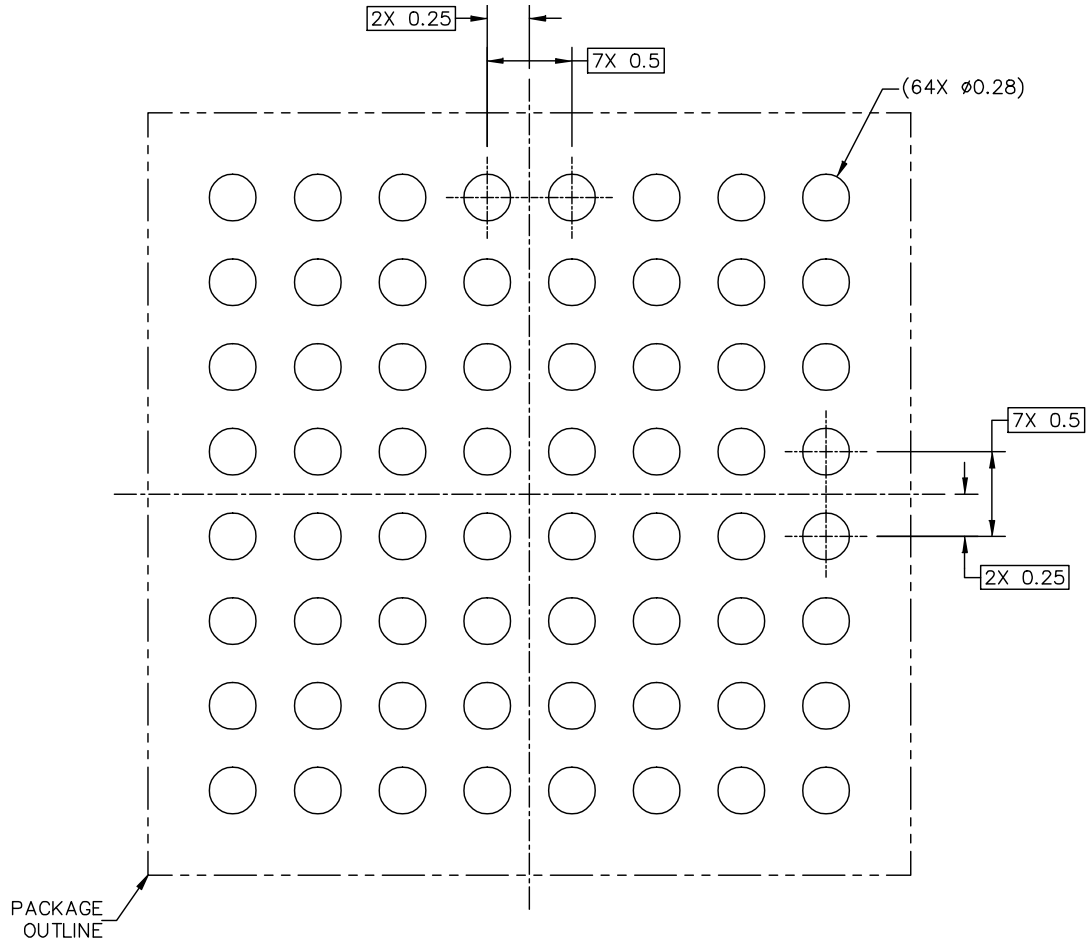
DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 43. Reflow soldering footprint part1 for VFBGA64 (SOT1307-2)

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

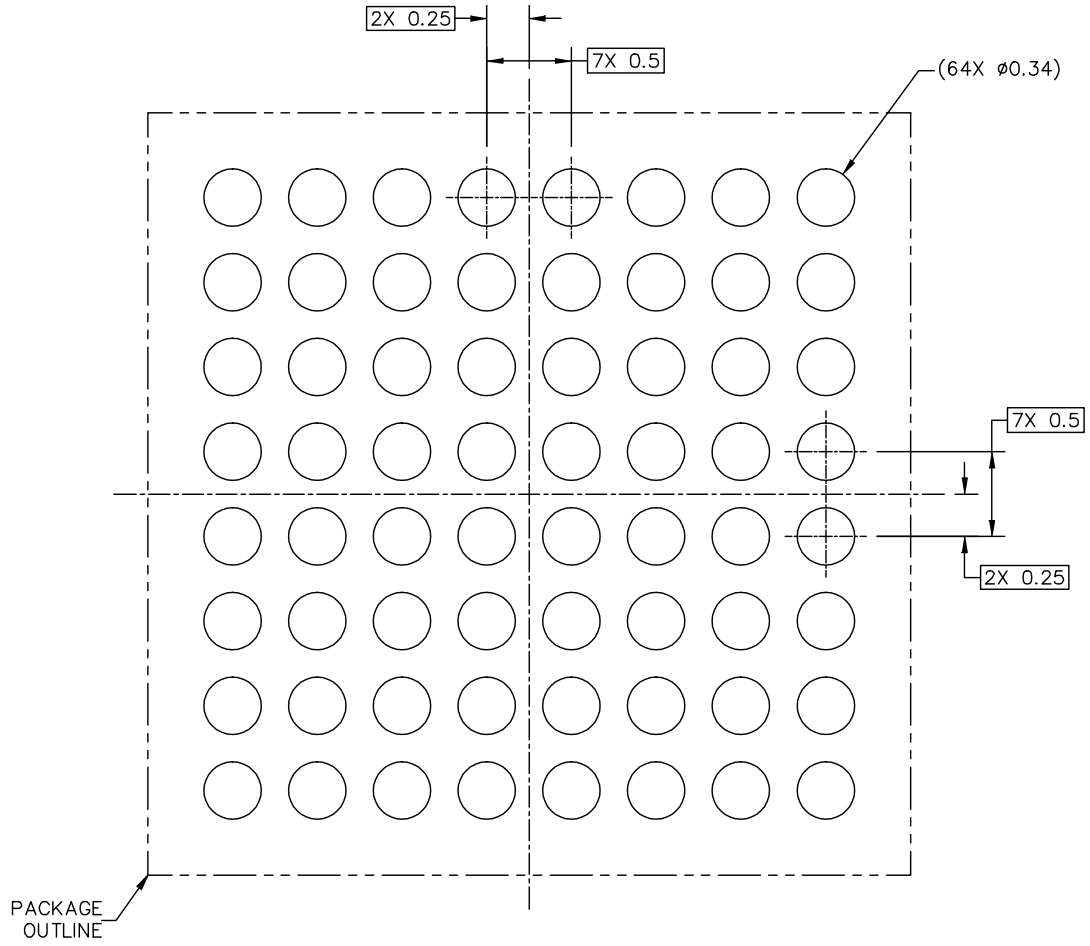
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Figure 44. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	

Figure 45. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)

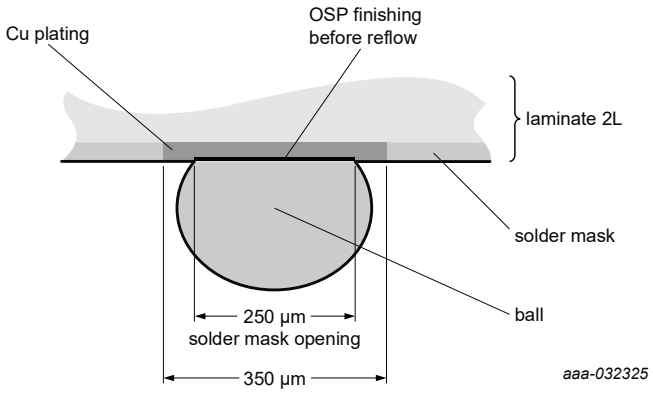


Figure 46. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)

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15 Reflow soldering footprint VFLGA40

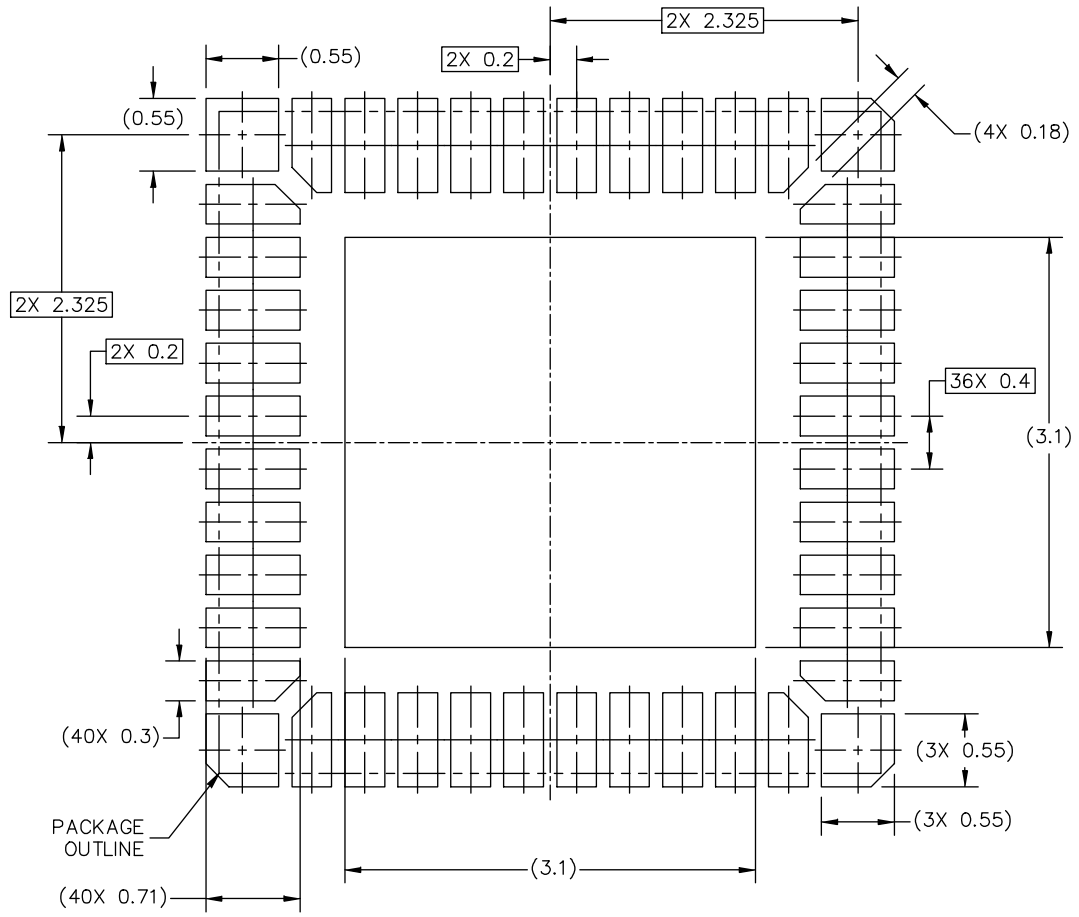
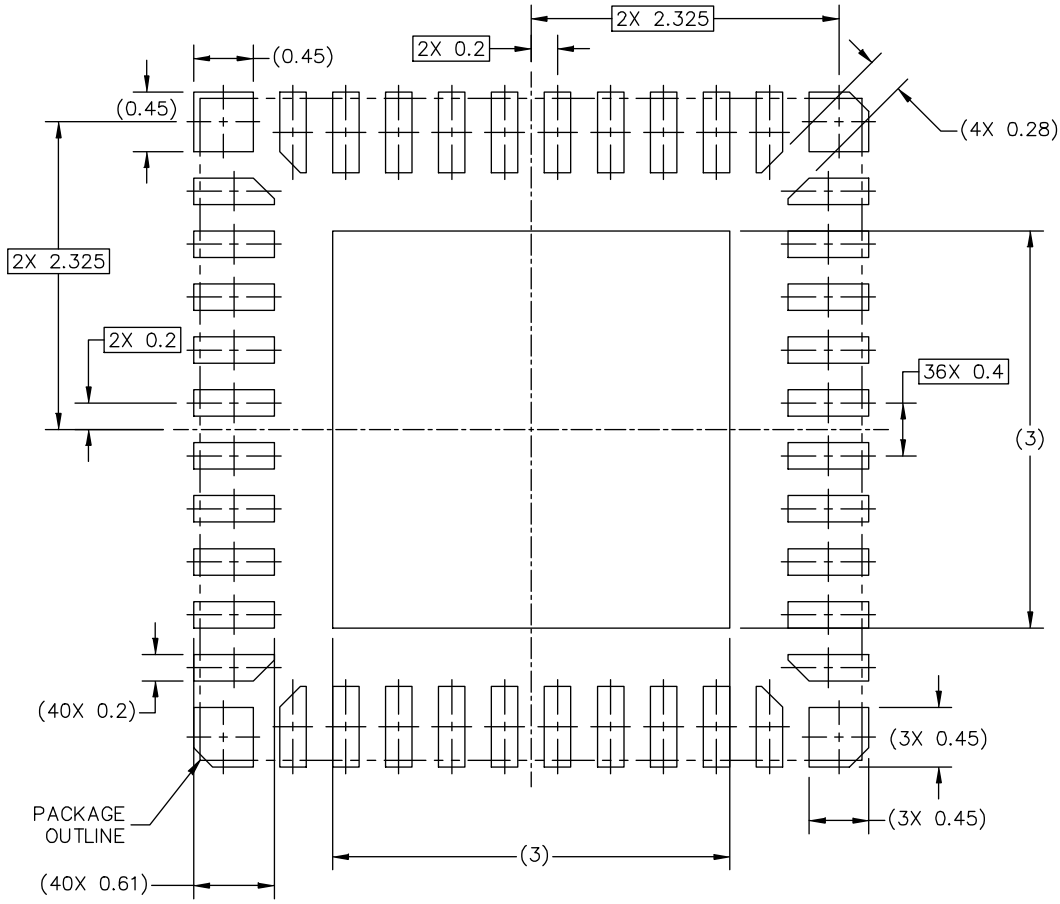


Figure 47. Package outline VFLGA40, SOT2062-1

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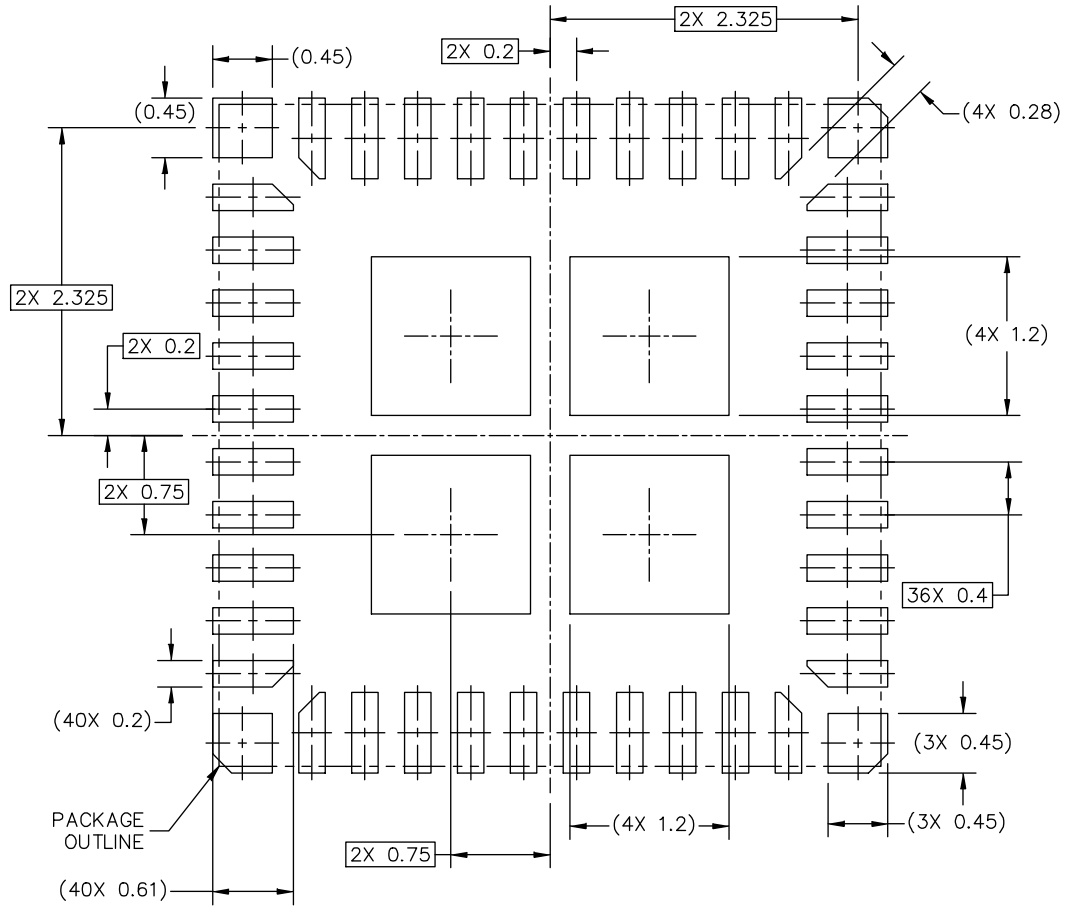
DATE: 15 MAR 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01615D	REVISION: O	

Figure 48. Package outline VFLGA40, SOT2062-1

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RECOMMENDED STENCIL THICKNESS 0.1

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DATE: 15 MAR 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01615D	REVISION: O	

Figure 49. Package outline VFLGA40, SOT2062-1

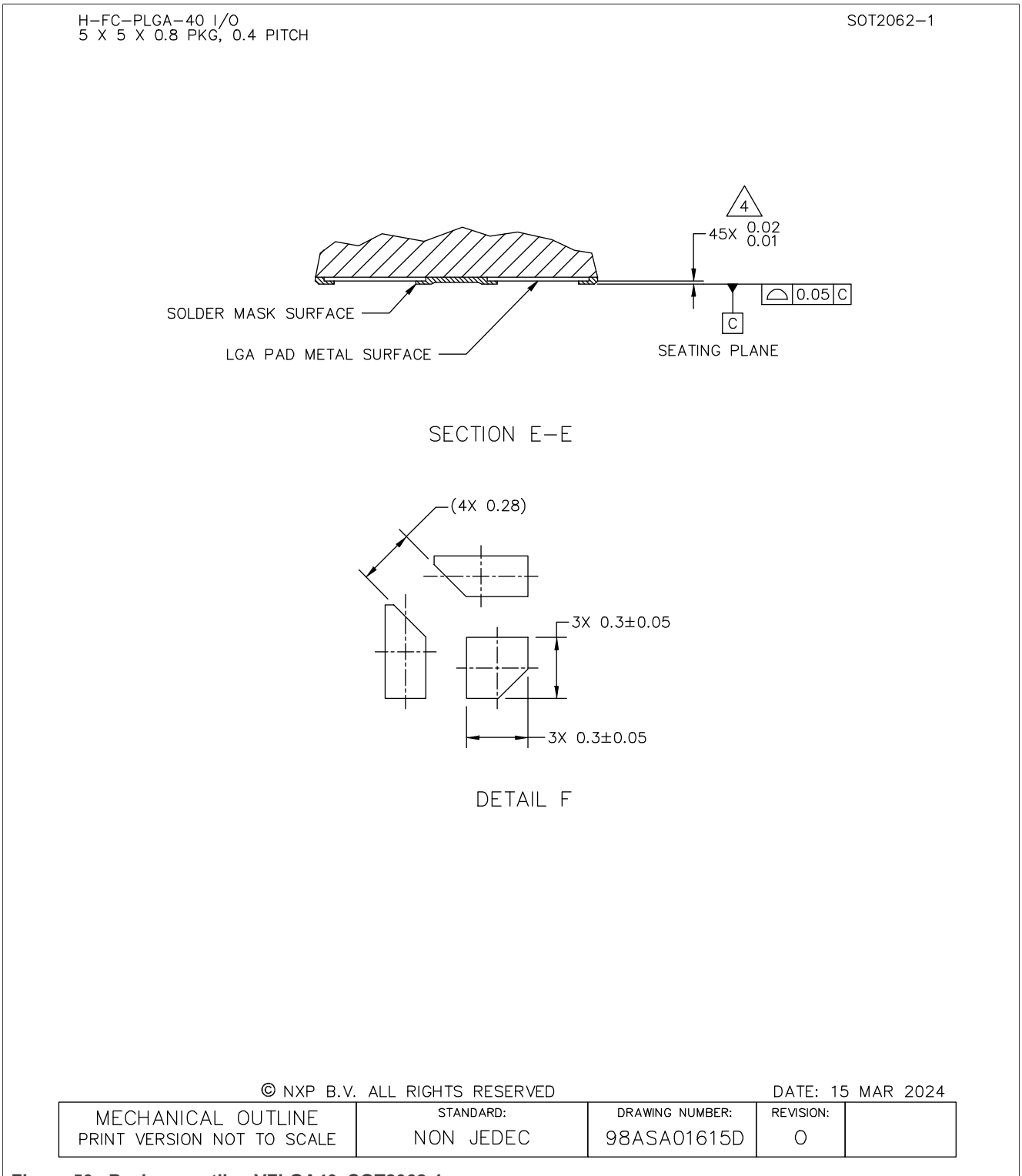


Figure 50. Package outline VFLGA40, SOT2062-1

16 Surface mount reflow soldering

For information on surface mount, reflow soldering and component handling please refer to the related application note.

This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages:

https://www.nxp.com/docs/en/application-note/AN10365.pdf

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17 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, in order to remove any moisture that might have soaked into the package.

For MSL3:

168h out-of-pack floor life at maximum ambient temperature, conditions < 30 °C / 60 % RH.

For MSL2:

- 1 year out-of-pack floor life at maximum ambient temperature, conditions < 30 °C° / 60 % RH.

For MSL1:

- No out-of-pack floor live spec. required. Conditions: <30 °C° / 85 % RH.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

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18 Abbreviations

Table 339. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CITO	controller input target output (previously master input slave output)
CLIF	contactless interface
COTI	controller output target input (previously master output slave input)
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN5190B1 integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine

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Table 339. Abbreviations...*continued*

Acronym	Description
GND	Ground
GPIO	general-purpose input output
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPCD	low-power card detection
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NTS	not target select (previously not slave select)
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PCD	power card detection
PICC	proximity inductive coupling card
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory

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Table 339. Abbreviations...*continued*

Acronym	Description
RF	radio frequency
RNG	random number generator
ROM	read-only memory
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I^2C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
ULPCD	ultra low-power card detection
USB	universal serial bus
VREF	voltage reference

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19 References

[1] Application note - AN12551 - PN5190 design-in recommendations (link)
[2] Application note - AN12549 - PN5190 antenna design guide (link)
[3] User manual - UM11942 - PN5190 instruction layer (link)
[4] Application note - AN14518 - Crystal Oscillator Design Guide (link)

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21 Revision history

Table 340. Revision history

Document ID	Release date	Data sheet status	Supersedes
PN5190B1 v.4.3	11 May 2026	Product data sheet	PN5190B1 v.4.2
Modifications:	• Section 4 "Firmware versions": updated. • Section 8.1 "Pin description VFBGA64": updated description for pin C2. • Section 9.5.3.3 "DC-DC (boost) supply": updated. • Section 9.5.3.4 "Configuration example 1: TX_LDO transmitter supply - DC-DC active": updated. • Section 9.5.3.5 "Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed": updated. • Section 9.5.3.6 "Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC": updated. • Section 9.5.3.7 "Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC": updated. • Section 9.5.3.8 "Configuration example 5: TX_LDO not used - no DC-DC": updated. • Section 9.5.3.9 "Supply voltage range for transmitter supply configuration examples": Table 7: updated VBAT maximum for Config1 (5.5 V → 4.8 V). • Section 9.11.1 "DPC algorithm": corrected bits for target current reduction (31:24). • Section 9.12 "Adaptive waveshape control (AWC)": updated Figure 21 title. • Section 9.15.3 "Ultra low-power card detection (ULPCD)": added note. • Section 9.26.1 "EEPROM configuration overview": added XTAL_CONTROL (4BD). • Section 11.3 "Timing characteristics": updated, added note, clarifications on start-up timing added. • Section 11.5 "Clock input ": removed Table "Frequency requirements for a direct clock input (no crystal)". • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.06" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.03" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.06 - EMVCo optimized" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.05" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.01" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.00" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.07, FW2.08, FW2.09 - EMVCo optimized" removed. • Section "Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.07, FW2.08, FW2.09" removed. • Section 20 "Note about the source code in the document ": updated.	

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Table 340. Revision history...*continued*

Document ID	Release date	Data sheet status	Supersedes
PN5190B1 v.4.2	18 November 2025	Product data sheet	PN5190B1 v.4.1
Modifications:	• Section 6 "Ordering information": updated. • Section 9.3 "Initial calibration ": updated. • Section 9.4 "System power states": updated. • Section 9.5.3 "Transmitter power supply ": removed TXLDO_VDDPA_HIGH_MAX_CARD description • Section 9.19 "Antenna connection": Table 14: updated description for ANACTRL_TX_CONFIG.TX_INVP_RM (0x44) and ANACTRL_TX_CONFIG.TX_PWM_MODE_RM (0x44) • Section 9.24.4 "EVENTS INDICATED ON GPIO": updated EEPROM register address (0054h → 0016h). • Section 9.25.68 "DYNAMIC_POWERLEVEL_REDUCTION (0064h)": updated. • Section 9.26 "EEPROM configuration description": – Section 9.26.1 "EEPROM configuration overview": Table 106: updated entry for "Address (hex) 9": TXLDO_VDDPA_HIGH_MAX_CARD → RFU – Section 9.26.114 "DPC_LOOKUP_TABLE (008Bh-0133h)": updated. – Section 9.26.199 "ENABLE_LFO_TRIM_CALIBRATION (0CEDh)": updated. – Description for Section 9.26.172 "TX_SHAPING_PROPRIETARY_1 (0C03h)", Section 9.26.173 "TX_SHAPING_PROPRIETARY_2 (0C23h)", Section 9.26.174 "TX_SHAPING_PROPRIETARY_3 (0C43h)", and Section 9.26.175 "TX_SHAPING_PROPRIETARY_4 (0C63h)": added. – Removed Section "TXLDO_VDDPA_MAX_CARD (0009h)". – Removed Section "RTRANS_FTRANS_TABLE (0C03h)". • Section 11.3 "Timing characteristics": updated.	
PN5190B1 v.4.1	9 December 2024	Product data sheet	PN5190B1 v.4.0
Modifications:	• Section 4 "Firmware versions": added description for Firmware version 2.0A • Section 9.26.200 "LpcdWithAutocollExpiryInterval (0CEEh)": added • Section 9.26.201 "EnableHIFPadsReConfig (0CEDh)": added • Section 9.26.202 "SPIPadReConfig (0CF0h)": added		
PN5190B1 v.4.0	11 November 2024	Product data sheet	PN5190B1 v.3.10
Modifications:	• Section 9.26.2 "DCDC_PWR_CONFIG (0000h)": added RFU to the description of VUP input voltage • TXLDO_VDDPA_MAX_CARD (0009h): updated description • Section 11.3 "Timing characteristics": added information about startup timing • Section 13.2 "Package marking drawing VFLGA40": added FW 2.7 • Added a section for Recommended additional crystal requirements in chapter Clock Input		
PN5190B1 v.3.10	25 July 2024	Product data sheet	PN5190B1 v.3.9
Modifications:	• Section 9.11 "Dynamic power control (DPC)": EEPROM settings updated.		

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Table 340. Revision history...*continued*

Document ID	Release date	Data sheet status	Supersedes
PN5190B1 v.3.9	27 June 2024	Product data sheet	PN5190B1 v.3.8
Modifications:	• Section 9.5.3 "Transmitter power supply ": Wording of DCDC_PWR_CONFIG (0000h) updated. • Section 9.5.3.9 "Supply voltage range for transmitter supply configuration examples" updated. • Section 9.11 "Dynamic power control (DPC)": Figure 19 "System overview: DPC, AWC and ARC" updated. • Section 9.24.3 "EVENTS INDICATED BY INTERRUPT": updated with clarification on IQR handling. • Section 9.25.1 "Register overview": Register address 0x64 added due to new Firmware feature DYNAMIC_POWERLEVEL_REDUCTION. • Section 9.26 "EEPROM configuration description": Editorial change to Section 9.26.18 "RESIDUAL_AMP_LEVEL_A106 (0022h)", Section 9.26.22 "RESIDUAL_AMP_LEVEL_A212 (0026h)", etc.: Section titles updated. • Section 9.26.1 "EEPROM configuration overview": EEPROM adress 0xCED added due to new Firmware feature LFO calibration. • Section 11.2 "Static characteristics": Table 323 "ATX_B, ATX_C, ATX_D pins (SPI (SCLK, COTI, NTS))": Description for weak pull-up and pull-down resisitors added. • Section 12.2 "VFLGA40 package": updated. • Section 15 "Reflow soldering footprint VFLGA40": updated. • Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.07, FW2.08, FW2.09: Section title updated according to latest firmware releases. • Appendix: EEPROM LOAD_RF_CONFIGURATION FW2.07, FW2.08, FW2.09 - EMVCo optimized: Section title updated according to latest firmware releases.	
PN5190B1 v.3.8	20 November 2023	Product data sheet	PN5190B1 v.3.7
Modifications:	• Register description for PMU_ANA_SMPS_CTRL_REG (00058h) removed • Section 9.25.3, Section 9.25.59 and Section 9.25.61: some bit fields updated		
PN5190B1 v.3.7	06 November 2023	Product data sheet	PN5190B1 v.3.6
Modifications:	• Section 19 "References": PN5190 instruction layer ref.[3]: Document type changed from product data sheet addendum to user manual • New register added: ENABLE_ULFO_TRIM_CALIBRATION (0CECh) • Section 6 "Ordering information": updated • Section 4 "Firmware versions" updated • New appendixes added • Section 20 "Note about the source code in the document ": added		
PN5190B1 v.3.6	15 May 2023	Product data sheet	PN5190B1 v.3.5
Modifications:	• New firmware versions 2.6 added, new registers and description added • Register description for SIGPRO_CONFIG (001Dh) added • Host interface command list updated with command 0x29 • CLK_INPUT_FREQ (0012h): Table for frequencies updated • $V_{DD(VUP_TX)}$ Absolute Limiting Value increased to 6.3 V • Package marking drawing VFBGA64 updated with new FW version information • Package marking drawing VFLGA40 updated with new FW version information • Initial calibration: Value to write for calibration updated • Supply voltage range for transmitter supply configuration examples: updated • DWL_REQ pin description: Recommendation added • Table 327 "AUX1, AUX2, AUX3 pins (Debug output) ": V_{AUX_OL} mV corrected to V • Various typos corrected and descriptions improved		

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Table 340. Revision history...*continued*

Document ID	Release date	Data sheet status	Supersedes
PN5190B1 v.3.5	19 October 2022	Product data sheet	PN5190B1 v.3.4
Modifications:	• Package type HVQFN40 udpated to official naming VFLGA40 • Section 6 "Ordering information": updated • The replacement of "master/slave" by "controller/target" in this document follows the recommendation of the NXP - I^2C and JEDEC SPI standards organizations. • Pin description in static characteristics corrected. CLK → XTAL Table 321 "XTAL1, XTAL2 pins " • Pin name in Table 3 "Pin description VFBGA64" and Table 4 "Pin description VFLGA40" corrected. VBATPWR → VBAT_PWR • Pin name in Table 328 "VTUNE0 and VTUNE1 output pins (Tuning DAC)" corrected. DAC → VTUNE • Register RX_STATUS_ERROR: Bit description corrected • RX_ERROR_CONFIG register (address 0027h) description updated • Pin description VFLGA40: ATX Input / output corrected. • Chapter antenna connection: added remark: Stored as part of the RF protocol configuration, added RM_GLOBAL_TX_SHAPING. bTX_INV_RM (0x18) • Register description for RX_ERROR_CONFIG removed, there is nothing to be configured/modified - default values work under all conditions. • EEPROM description DPC_TXLDO_MAX_DROP (0081h) added • TXLDO_CONFIG (0002h) description updated • TXLDO_VDDPA_HIGH (0006h) description updated • TxLdoVddpaLow (adr 0x07) description removed and changed to RFU- no useful function linked to this address. • TX_SHAPING_CONFIG (address 0017h): description updated • Small editorial changes	
PN5190B1 v.3.4	01 July 2022	Product data sheet	PN5190B1 v.3.3
Modifications:	• Figure 31 "Two antennas connected to TX1, TX2 each": corrected • EEPROM 0C55h: DWORD for USER_DATA storage had been added • EEPROM TEMP_WARNING (address 0014h): description updated in Table 81 • Updated Antenna register configuration Table 14 (added "do not care" for TX2_CLK_MODE_ TRANS_RM, TX2_CLK_MODE_MOD_RM, TX2_CLK_MODE_CW_RM; TX2_USE_TX1_CONF for single ended TX2 is "0b") • Updated Antenna EEPROM configuration in Table 15 (removed the EEPROM modification of 0x19 and 0x1A, since that must done via register update after Load Protocol) • GPIO0: Pin function description changed from I/O to Input only in Section 8.2. • SPI interface timing updated for 15 MHz SPI clock frequency • Vtune1 comment removed in description for VFBGA description • Description of FW2.05 • Description EXT_RFOFF_DETECTED corrected • Description RX_FRAME_MAXLEN_VIOL corrected • Description RX_COLLISION_STOPBIT_DETECTED corrected • Description RFOFF_DET_EVENT corrected • EEPROM configuration TX_SHAPING_CONFIG description updated • EEPROM configuration VDDPA_DISCHARGE description updated • System power supply clarification: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in power off mode. • RX_PROTOCOL_CONFIG (0025h) bit description updated, bist which should not be used set to RFU	

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Table 340. Revision history...*continued*

Document ID	Release date	Data sheet status	Supersedes
PN5190B1 v.3.3	19 April 2022	Product data sheet	PN5190B1 v.3.2
Modifications:	Section 9.25.62 "DPC_CONFIG (005Eh)": Description improved. Table 328 "VTUNE0 and VTUNE1 output pins (Tuning DAC)": Condition for max output voltage updated: VDDIO = 3.3 V Table 78 "DAC register (address 0057h) bit description": TUNING_DAC_2_RANGE description improved Table 55 "RX_CRC_CONFIG register (address 0031h) bit description": Register description added Table 3 "Pin description VFBGA64" and Table 4 "Pin description VFLGA40": Pin VEN - remark added: "Avoid a floating or unexpected toggling of the pin." Section 9.26.156 "LPCD_THRESHOLD_COARSE (049Ah)": Address corrected to 49Ah Table 257 "LPCD_AVG_SAMPLES (address 0492h) EEPROM configuration bit description": Updated description **0 to 6**		
PN5190B1 v.3.2	17 November 2021	Product data sheet	PN5190B1 v.3.1
Modifications:	• Section 9.8: TEMP_WARNING address corrected to 14h • Section 9.26.4: TXLDO_CONFIG description updated with Overcurrent enable and TxLdo current limiter • Section 9.25.4: EVENT_STATUS and Section 9.25.3 EVENT_ENABLE register: TEMP_ERROR_EVENT corrected to / replaced by TX_OVERCURRENT_ERROR_EVENT (bit 5) • Section 9.5.3.9: Power configuration corrected		
PN5190B1 v.3.1	07 September 2021	Product data sheet	PN5190B1 v.3.0
Modifications:	• Description for FW2.3 added • General update and clarifications added • Description for SE antenna configurations added		
PN5190B1 v.3.0	21 April 2021	Product data sheet	PN5190B1 v.1.0
Modifications:	• General update • Data sheet status changed to "Product data sheet"		
PN5190B1 v.1.0	22 March 2021	Objective data sheet	-
Modifications:	• First official released version		

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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