LA1238_B0

Layerscape Access LA1216, LA1218, LA1236, and LA1238 Family Data Sheet

Rev. 2 — April 2024

Data Sheet: Technical Data

- Eight Vector Signal Processing Acceleration (VSPA) core Complexes, each consisting of:
  - VSPA3-16SP running up-to 614.4 MHz (VSPA3 ISA, Arithmetic Units capable of 128 Multiply Accumulate per clock cycle)
  - 140 KB VCPU plus IPPU combined program memory
  - 320 KB VCPU plus IPPU combined data memory
  - Support for program memory overlay
  - DMA
- Forward Error Correction Accelerators (FECA)
  - 3GPP 5G/NR 38.212 compliant, gNB and UE modes
  - Polar decoder/encoder
  - LDPC decoder/encoder
  - 6MB of HARQ RAM (HRAM)
- Six e200 Power® Architecture core complexes, each consisting of:
  - e200z7 core running up-to 614.4 MHz
  - 32-bit PowerPC Book E compliant
  - 64 KB Local Data Memory
  - 16 KB Instruction Cache
  - 16 KB Data Cache
  - Memory Protection Unit (MPU) with 24-entry descriptor table
  - Embedded Floating-point APU (EFPU2) supporting scalar and SIMD single-precision floating-point operations
  - Signal Processing Extension (SPE2) APU supporting SIMD fixed-point operations.
  - Performance Monitor APU supporting execution profiling
- High Speed Data Conversion Subsystem (HS_DCS)
  - Two IQ ADC Blocks
- Low Speed Data Conversion Subsystem (LS_DCS)
  - Four IQ ADC blocks
  - Four IQ ADC blocks
- Two PCIe Gen3 interfaces
  - PCIe1 supporting x8/x4/x2/x1 lane operation in Endpoint (EP) mode only
  - PCIe2 supporting x4/x2/x1 lane operation in both Root Complex (RC) and Endpoint (EP) mode
- One eight lane SerDes
- Multiple on chip memory
  - 512 KB Core SRAM, primarily used as Layer 2 memory for all the e200z7 cores.
  - 2MB Packet Express Buffer Memory (PEBM)
- I/O
  - Six I2C interface
  - Six Serial Peripheral Interface (SPI) controllers
  - Flexible Serial Peripheral Interface (FlexSPI)
  - General Purpose IO (GPIO) interface
  - Four UART interfaces
  - Universal Subscriber Identity interface (USIM)
  - Two Light-Weight LVDS communication protocol (LLCP) interfaces to control RFIC chip
- Standard 5-pin JTAG
- Multi-Processor Interrupt Controller (MPIC)
- Two Timebase Generator (TBGen)
  - 64-bit master counter
  - On-chip and off-chip system timing generation including timing advance/delay compensation
- 621 FC-PBGA package, 21 mm x 21 mm

NXP reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 Introduction

The Layerscape® Access LA1238 family of products are based on an integrated programmable baseband processor architecture for 5G or proprietary wireless connectivity applications. This family includes versions with integrated high speed and/or low speed data converters to support FR1/sub-6GHz as well as FR2/mmWave antenna subsystems for multiple applications including Radio Units (RU), fixed wireless and Customer Premise Equipment (CPE) and Integrated Small Cell (ISC) or Femto Cells.

The main processing unit of the LA1238 family consists of a Vector Signal Processing Accelerator (VSPA) DSP complex with up to eight programmable vector engines which deliver over 1.3 teraflops of Single Precision Floating Point (SP FP) performance, ideal for offloading PHY processing applications freeing up CPU cycles and saving cost and power. The LA1238 family supports a high performance integrated Forward Error Correction Accelerator (FECA) with a powerful integrated acceleration engine supporting both LDPC and Polar encoding and decoding for fixed wireless and small cell applications

The LA1238 family integrates e200 Power® Architecture RISC cores for control, large on-chip SRAMs and operates without any external DRAM to save system cost. The device supports boot from an external host over PCIe or can boot standalone from a serial Flash memory. High-speed digital I/O to a host processor is supported with up to eight lanes PCIe Gen3. The LA1238 family supports integrated ADCs and DACs which enables developers a choice of low power NXP ecosystem, partner or custom RF solutions.

The Layerscape Access products are supported by proven NXP CodeWarrior development tools and enablement applications. NXP also fosters a variety of third party ecosystem partner for product-ready software stacks and integration services.

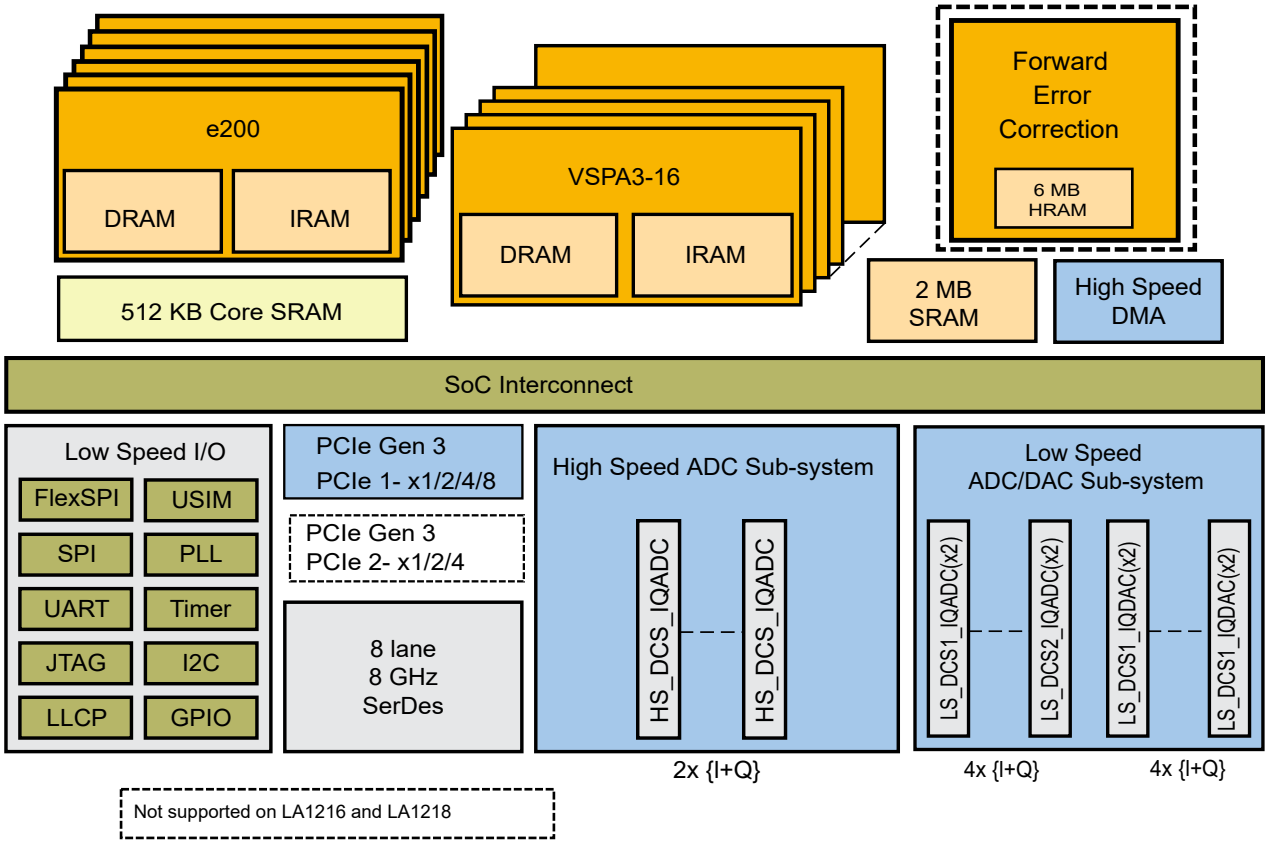


Figure 1. LA1216, LA1218, LA1236 and LA1238 Rev. B0 block diagram

2 Pin assignments

2.1 Pinout list

This table provides the pinout listing for the LA1238 silicon Rev. B0 by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
Clocking					
CLKOUT	122.88 MHz CLKOUT	R23	O	OV_{DD}	2
CLKOUT_TBGen_PLL_N	Diff Clock test point of TBGen PLL output clock	B2	O	CG_SV_{DD}	---
CLKOUT_TBGen_PLL_P	Diff Clock test point of TBGen PLL output clock	A2	O	CG_SV_{DD}	---
SYSCLK_N	TBGen PLL and PLATFORM PLL Reference Clock - (122.88 MHz)	B4	I	CG_SV_{DD}	---
SYSCLK_P	TBGen PLL and PLATFORM PLL Reference Clock + (122.88 MHz)	A4	I	CG_SV_{DD}	---
High-Speed DCS					
HS_DCS_REXT	Analog Current Reference	L3	I	$HS_DCS_AV_{DD}H$	18
HS_DCS_RXQ1_N	Analog Receive - (rxi1_n)	D2	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXQ1_P	Analog Receive + (rxi1_p)	D1	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXI2_N	Analog Receive - (rxi2_n)	H2	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXI2_P	Analog Receive + (rxi2_p)	H1	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXI1_N	Analog Receive - (rxq1_n)	F2	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXI1_P	Analog Receive + (rxq1_p)	F1	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXQ2_N	Analog Receive - (rxq2_n)	K2	I	$HS_DCS_AV_{DD}$	---
HS_DCS_RXQ2_P	Analog Receive + (rxq2_p)	K1	I	$HS_DCS_AV_{DD}$	---
HS_DCS_VCM	ADC Common Mode output Reference Voltage (vcm)	G3	O	$HS_DCS_AV_{DD}$	---
HS_DCS_VREF	ADC/DAC Reference Voltage (vref)	J3	I	$HS_DCS_AV_{DD}$	---
LLCP1					
LLCP1_DIN_N	LVDS Receive Data In -	AD5	I	OV_{DD}	---
LLCP1_DIN_P	LVDS Receive Data In +	AE5	I	OV_{DD}	---
LLCP1_DOUT_N	LVDS Transmit Data -	AD7	O	OV_{DD}	---
LLCP1_DOUT_P	LVDS Transmit Data +	AE7	O	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LLCP1_STIN_N	LVDS Strobe In -	AB6	I	OV_{DD}	---
LLCP1_STIN_P	LVDS Strobe In +	AC6	I	OV_{DD}	---
LLCP1_STOUT_N	LVDS Strobe Out -	AB8	O	OV_{DD}	---
LLCP1_STOUT_P	LVDS Strobe Out +	AC8	O	OV_{DD}	---
LLCP2					
LLCP2_DIN_N	LVDS Receive Data In -	AD6	I	OV_{DD}	---
LLCP2_DIN_P	LVDS Receive Data In+	AE6	I	OV_{DD}	---
LLCP2_DOUT_N	LVDS Transmit Data -	AD8	O	OV_{DD}	---
LLCP2_DOUT_P	LVDS Transmit Data +	AE8	O	OV_{DD}	---
LLCP2_STIN_N	LVDS Strobe In -	AA7	I	OV_{DD}	---
LLCP2_STIN_P	LVDS Strobe In +	AB7	I	OV_{DD}	---
LLCP2_STOUT_N	LVDS Strobe Out -	AB9	O	OV_{DD}	---
LLCP2_STOUT_P	LVDS Strobe Out +	AC9	O	OV_{DD}	---
GPIO1					
GPIO_1_0 /TBGEN1_GPO32	General Purpose Input/Output	R24	IO	OV_{DD}	---
GPIO_1_1 /TBGEN1_GPO33	General Purpose Input/Output	R25	IO	OV_{DD}	---
GPIO_1_2 /TBGEN1_SYNC_IN /TBGEN1_GPO34	General Purpose Input/Output	P19	IO	OV_{DD}	---
GPIO_1_3 /TBGEN1_GPO35	General Purpose Input/Output	P20	IO	OV_{DD}	---
GPIO_1_4 /TBGEN1_GPO36	General Purpose Input/Output	P21	IO	OV_{DD}	---
GPIO_1_5 /TBGEN1_GPO37	General Purpose Input/Output	P22	IO	OV_{DD}	---
GPIO_1_6 /TBGEN1_GPO38	General Purpose Input/Output	P23	IO	OV_{DD}	---
WDOG_TOUT /GPIO_1_7 / TBGEN1_GPO39	WDOG Interrupt to Host	P24	IO	OV_{DD}	---
GPIO2					
GPIO_2_0 /RSTOUT_TR3_B / TBGEN1_GPO0	General Purpose Input/Output	P25	IO	OV_{DD}	---
GPIO_2_1 /RSTOUT_TR4_B / TBGEN1_GPO1	General Purpose Input/Output	N22	IO	OV_{DD}	---
GPIO_2_2 /TBGEN1_GPO2	General Purpose Input/Output	N23	IO	OV_{DD}	---
GPIO_2_3 /TBGEN1_GPO3	General Purpose Input/Output	N19	IO	OV_{DD}	---
GPIO_2_4 /TBGEN1_GPO4	General Purpose Input/Output	N20	IO	OV_{DD}	---
GPIO_2_5 /TBGEN1_GPO5	General Purpose Input/Output	K25	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO_2_6 /TBGEN1_GPO6	General Purpose Input/Output	M21	IO	OV_{DD}	---
GPIO_2_7 /TBGEN1_GPO7 / CFG_spare_sr5_0	General Purpose Input/Output	M22	IO	OV_{DD}	4
GPIO_2_8 /TBGEN1_GPO8 / CFG_spare_sr5_1	General Purpose Input/Output	K23	IO	OV_{DD}	4
GPIO_2_9 /TBGEN1_GPO9 / CFG_spare_sr5_2	General Purpose Input/Output	L23	IO	OV_{DD}	4
GPIO_2_10 /TBGEN1_ GPO10 /cfg_spare_sr2	General Purpose Input/Output	K22	IO	OV_{DD}	4
GPIO_2_11 /TBGEN1_ GPO11 /cfg_pcie_lrev_b	General Purpose Input/Output	L21	IO	OV_{DD}	4
GPIO_2_12 /TBGEN1_ GPO12 /cfg_sd_prtcl0	General Purpose Input/Output	L22	IO	OV_{DD}	4
GPIO_2_13 /TBGEN1_ GPO13 /cfg_sd_prtcl1	General Purpose Input/Output	H25	IO	OV_{DD}	4
GPIO_2_14 /TBGEN1_ GPO14 /cfg_sd_prtcl2	General Purpose Input/Output	J25	IO	OV_{DD}	4
GPIO_2_15 /TBGEN1_ GPO15 /cfg_sd_pll_ref_clk	General Purpose Input/Output	L19	IO	OV_{DD}	4
GPIO_2_16 /TBGEN1_ GPO16 /cfg_test_port_dis	General Purpose Input/Output	L20	IO	OV_{DD}	4
GPIO_2_17 /TBGEN1_ GPO17 /cfg_test_port_sel	General Purpose Input/Output	J24	IO	OV_{DD}	4
GPIO_2_18 /TBGEN1_ GPO18 /cfg_pcie2_rc_ep	General Purpose Input/Output	K20	IO	OV_{DD}	4
GPIO_2_19 /TBGEN1_ GPO19 /cfg_test_sysclk_sel	General Purpose Input/Output	J23	IO	OV_{DD}	4
GPIO_2_20 /TBGEN1_ GPO20 /cfg_sysclk_sel1	General Purpose Input/Output	K19	IO	OV_{DD}	4
GPIO_2_21 /TBGEN1_GPO21	General Purpose Input/Output	J22	IO	OV_{DD}	---
GPIO_2_22 /TBGEN1_ GPO22 /cfg_TBGen_pll0	General Purpose Input/Output	H24	IO	OV_{DD}	4
GPIO_2_23 /TBGEN1_ GPO23 /cfg_TBGen_pll1	General Purpose Input/Output	F25	IO	OV_{DD}	4
GPIO_2_24 /TBGEN1_ GPO24 /cfg_TBGen_pll2	General Purpose Input/Output	G25	IO	OV_{DD}	4
GPIO_2_25 /TBGEN1_ GPO25 /cfg_TBGen_pll3	General Purpose Input/Output	J20	IO	OV_{DD}	4

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Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO_2_26 /TBGEN1_GPO26 /cfg_sysclk_sel	General Purpose Input/Output	J21	IO	OV_{DD}	4
GPIO_2_27 /TBGEN1_GPO27 /cfg_sys_pll	General Purpose Input/Output	H23	IO	OV_{DD}	4
GPIO_2_28 /TBGEN1_GPO28 /cfg_boot_src1	General Purpose Input/Output	F24	IO	OV_{DD}	4
GPIO_2_29 /TBGEN1_GPO29 /cfg_boot_src0	General Purpose Input/Output	H22	IO	OV_{DD}	4
GPIO_2_30 /TBGEN1_GPO30 /cfg_boot_ho_b	General Purpose Input/Output	J19	IO	OV_{DD}	4
GPIO_2_31 /TBGEN1_SYNC_IN /TBGEN1_GPO31 /cfg_spare	General Purpose Input/Output	G23	IO	OV_{DD}	4
GPIO3					
GPIO_3_0 /RSTOUT_TR1_B / TBGEN2_GPO0	General Purpose Input/Output	V3	IO	OV_{DD}	---
GPIO_3_1 /RSTOUT_TR2_B / TBGEN2_GPO1	General Purpose Input/Output	Y1	IO	OV_{DD}	---
GPIO_3_2 /TBGEN2_GPO2	General Purpose Input/Output	AA1	IO	OV_{DD}	---
GPIO_3_3 /TBGEN2_GPO3	General Purpose Input/Output	Y2	IO	OV_{DD}	---
GPIO_3_4 /TBGEN2_GPO4	General Purpose Input/Output	W3	IO	OV_{DD}	---
GPIO_3_5 /TBGEN2_GPO5	General Purpose Input/Output	V4	IO	OV_{DD}	---
GPIO_3_6 /TBGEN2_GPO6	General Purpose Input/Output	U5	IO	OV_{DD}	---
GPIO_3_7 /TBGEN2_GPO7	General Purpose Input/Output	T6	IO	OV_{DD}	---
GPIO_3_8 /TBGEN2_GPO8	General Purpose Input/Output	U4	IO	OV_{DD}	---
GPIO_3_9 /TBGEN2_GPO9	General Purpose Input/Output	AB1	IO	OV_{DD}	---
GPIO_3_10 /TBGEN2_GPO10	General Purpose Input/Output	AA2	IO	OV_{DD}	---
GPIO_3_11 /TBGEN2_GPO11	General Purpose Input/Output	Y3	IO	OV_{DD}	---
GPIO_3_12 /TBGEN2_GPO12	General Purpose Input/Output	W4	IO	OV_{DD}	---
GPIO_3_13 /TBGEN2_GPO13	General Purpose Input/Output	AC1	IO	OV_{DD}	---
GPIO_3_14 /TBGEN2_GPO14	General Purpose Input/Output	V5	IO	OV_{DD}	---
GPIO_3_15 /TBGEN2_GPO15	General Purpose Input/Output	AA3	IO	OV_{DD}	---
GPIO_3_16 /TBGEN2_GPO16	General Purpose Input/Output	U6	IO	OV_{DD}	---
GPIO_3_17 /TBGEN2_GPO17	General Purpose Input/Output	Y4	IO	OV_{DD}	---
GPIO_3_18 /TBGEN2_GPO18	General Purpose Input/Output	AC2	IO	OV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO_3_19 /TBGEN2_GPO19	General Purpose Input/Output	T7	IO	OV_{DD}	---
GPIO_3_20 /TBGEN2_GPO20	General Purpose Input/Output	AB3	IO	OV_{DD}	---
GPIO_3_21 /TBGEN2_GPO21	General Purpose Input/Output	AB5	IO	OV_{DD}	---
GPIO_3_22 /TBGEN2_GPO22	General Purpose Input/Output	AA4	IO	OV_{DD}	---
GPIO_3_23 /TBGEN2_GPO23	General Purpose Input/Output	V6	IO	OV_{DD}	---
GPIO_3_24 /TBGEN2_GPO24	General Purpose Input/Output	AC3	IO	OV_{DD}	---
GPIO_3_25 /TBGEN2_GPO25	General Purpose Input/Output	Y5	IO	OV_{DD}	---
GPIO_3_26 /TBGEN2_GPO26	General Purpose Input/Output	AB4	IO	OV_{DD}	---
GPIO_3_27 /TBGEN2_GPO27	General Purpose Input/Output	AA6	IO	OV_{DD}	---
GPIO_3_28 /TBGEN2_GPO28	General Purpose Input/Output	Y7	IO	OV_{DD}	---
GPIO_3_29 /TBGEN2_GPO29	General Purpose Input/Output	U7	IO	OV_{DD}	---
GPIO_3_30 /TBGEN2_GPO30	General Purpose Input/Output	W6	IO	OV_{DD}	---
GPIO_3_31 /TBGEN2_GPO31	General Purpose Input/Output	AC4	IO	OV_{DD}	---
GPIO4					
GPIO_4_0 /RSTOUT_TR1_B	General Purpose Input/Output/ Reset out to transceiver	V7	IO	OV_{DD}	---
GPIO_4_1 /RSTOUT_TR2_B	General Purpose Input/Output/ Reset out to transceiver	Y6	IO	OV_{DD}	---
GPIO_4_2 /TBGEN2_SYNC_IN	General Purpose Input/Output/ TBGEN2 SYNC IN	W7	IO	OV_{DD}	---
IRQ External Interrupt					
IRQ_0 /GPIO_4_3	External Interrupt	AD2	I	OV_{DD}	1
IRQ_1 /GPIO_4_4	External Interrupt	AD3	I	OV_{DD}	1
IRQ_2 /GPIO_4_5	External Interrupt	AE3	I	OV_{DD}	1
IRQ_3 /GPIO_4_6	External Interrupt	AD4	I	OV_{DD}	1
IRQ_4 /GPIO_4_7	External Interrupt	AE4	I	OV_{DD}	1
I2C controller					
IIC1_SCL /GPIO_1_18	Serial Clock	Y23	IO	OV_{DD}	7, 8
IIC1_SDA /GPIO_1_19	Serial Data	W24	IO	OV_{DD}	7, 8
IIC2_SCL /GPIO_1_20	Serial Clock	W23	IO	OV_{DD}	7, 8
IIC2_SDA /GPIO_1_21	Serial Data	V23	IO	OV_{DD}	7, 8
IIC3_SCL /GPIO_1_22	Serial Clock	W25	IO	OV_{DD}	7, 8
IIC3_SDA /GPIO_1_23	Serial Data	Y25	IO	OV_{DD}	7, 8

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
IIC4_SCL /GPIO_4_26	Serial Clock	Y10	IO	OV_{DD}	7, 8
IIC4_SDA /GPIO_4_27	Serial Data	W10	IO	OV_{DD}	7, 8
IIC5_SCL /GPIO_4_28	Serial Clock	Y9	IO	OV_{DD}	7, 8
IIC5_SDA /GPIO_4_29	Serial Data	W9	IO	OV_{DD}	7, 8
IIC6_SCL /GPIO_4_30	Serial Clock	Y8	IO	OV_{DD}	7, 8
IIC6_SDA /GPIO_4_31	Serial Data	Y11	IO	OV_{DD}	7, 8
Low Speed DCS1 and DCS2					
LS_DCS1_RXI1_N	Analog Receive - (rxi1_n)	B7	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXI1_P	Analog Receive + (rxi1_p)	A7	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXI2_N	Analog Receive - (rxi2_n)	B11	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXI2_P	Analog Receive + (rxi2_p)	A11	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXQ1_N	Analog Receive - (rxq1_n)	B9	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXQ1_P	Analog Receive + (rxq1_p)	A9	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXQ2_N	Analog Receive - (rxq2_n)	B13	I	LS_DCS_AV_{DD}	---
LS_DCS1_RXQ2_P	Analog Receive + (rxq2_p)	A13	I	LS_DCS_AV_{DD}	---
LS_DCS1_TXI1_N	Analog Transmit - (txi1_n)	E7	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXI1_P	Analog Transmit + (txi1_p)	D7	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXI2_N	Analog Transmit - (txi2_n)	E11	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXI2_P	Analog Transmit + (txi2_p)	D11	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXQ1_N	Analog Transmit - (txq1_n)	E9	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXQ1_P	Analog Transmit + (txq1_p)	D9	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXQ2_N	Analog Transmit - (txq2_n)	E13	O	LS_DCS_AV_{DD}H	---
LS_DCS1_TXQ2_P	Analog Transmit + (txq2_p)	D13	O	LS_DCS_AV_{DD}H	---
LS_DCS_VREF_P	Analog Rx Voltage Ref (vref)	C12	I	LS_DCS_AV_{DD}	22
LS_DCS_VREF_N	Analog Rx Voltage Ref (vref_n)	C16	---	LS_DCS_AV_{DD}	22
LS_DCS2_RXI1_N	Analog Receive - (rxi1_n)	B15	I	LS_DCS_AV_{DD}	---
LS_DCS2_RXI1_P	Analog Receive + (rxi1_p)	A15	I	LS_DCS_AV_{DD}	---
LS_DCS2_RXI2_N	Analog Receive - (rxi2_n)	B19	I	LS_DCS_AV_{DD}	---
LS_DCS2_RXI2_P	Analog Receive + (rxi2_p)	A19	I	LS_DCS_AV_{DD}	---
LS_DCS2_RXQ1_N	Analog Receive - (rxq1_n)	B17	I	LS_DCS_AV_{DD}	---
LS_DCS2_RXQ1_P	Analog Receive + (rxq1_p)	A17	I	LS_DCS_AV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LS_DCS2_RXQ2_N	Analog Receive - (rxq2_n)	B21	I	$LS_DCS_AV_{DD}$	---
LS_DCS2_RXQ2_P	Analog Receive + (rxq2_p)	A21	I	$LS_DCS_AV_{DD}$	---
LS_DCS2_TXI1_N	Analog Transmit - (txi1_n)	E15	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXI1_P	Analog Transmit + (txi1_p)	D15	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXI2_N	Analog Transmit - (txi2_n)	E19	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXI2_P	Analog Transmit + (txi2_p)	D19	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXQ1_N	Analog Transmit - (txq1_n)	E17	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXQ1_P	Analog Transmit + (txq1_p)	D17	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXQ2_N	Analog Transmit - (txq2_n)	E21	O	$LS_DCS_AV_{DD}H$	---
LS_DCS2_TXQ2_P	Analog Transmit + (txq2_p)	D21	O	$LS_DCS_AV_{DD}H$	---
SIM Card Interface					
SIM_CLK	Clock for SIM Card	U23	O	OV_{DD}	---
SIM_PD	Card Insertion detect signal	T25	I	OV_{DD}	---
SIM_RST_B	Reset signal for SIM Card	V25	O	OV_{DD}	---
SIM_SVEN	Power Enable Signal	U25	O	OV_{DD}	---
SIM_TRXD	Data Port	U24	IO	OV_{DD}	---
DUART					
UART1_CTS_B /GPIO_1_31 / UART3_SIN	Clear To Send	V22	I	OV_{DD}	1
UART1_RTS_B /GPO_1_30 / UART3_SOUT /cfg_pcie2_gen	Ready to Send	Y21	O	OV_{DD}	5
UART1_SIN /GPO_1_29	Receive Data	W22	I	OV_{DD}	1
UART1_SOUT /GPO_1_28 / cfg_pcie1_gen	Transmit Data	W21	O	OV_{DD}	2, 4
UART2_CTS_B /GPIO_1_27 / UART4_SIN	Clear To Send	U22	I	OV_{DD}	1
UART2_RTS_B /GPIO_1_26 / UART4_SOUT /cfg_sd_pll_pd_plls_b	Ready to Send	U21	O	OV_{DD}	1, 5
UART2_SIN /GPIO_1_25	Receive Data	U20	I	OV_{DD}	1
UART2_SOUT /GPIO_1_24 / cfg_sd_pll_pd_pllf_b	Transmit Data	T20	O	OV_{DD}	1, 4
System Control					
HRESET_B	Hard Reset	W20	IO	OV_{DD}	6, 7

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
PORESET_B	Power On Reset	V20	I	OV_{DD}	---
JTAG					
TCK	Test Clock	R21	I	OV_{DD}	---
TDI	Test Data In	T22	I	OV_{DD}	9
TDO	Test Data Out	T23	O	OV_{DD}	2
TMS	Test Mode Select	R22	I	OV_{DD}	9
TRST_B	Test Reset	U19	I	OV_{DD}	9
SerDes					
SD_IMP_CAL_RX	SerDes Receive Impedance Calibration	AA12	I	SD_SV_{DD}	16
SD_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y18	I	SD_OV_{DD}	11
SD_PLLF_REF_CLK_N	SerDes PLL Fast Reference Clock Complement	AA16	I	SD_SV_{DD}	---
SD_PLLF_REF_CLK_P	SerDes PLL Fast Reference Clock	Y16	I	SD_SV_{DD}	---
SD_PLLF_TPA	SerDes PLL Fast Analog Test Point	Y14	O	AVDD_SD_PLLF	12
SD_PLLF_TPD	SerDes PLL Fast Digital Test Point	AA24	O	SD_SV_{DD}	12
SD_PLLS_TPA	SerDes PLL Slow Analog Test Point	AA20	O	AVDD_SD_PLLS	12
SD_PLLS_TPD	SerDes PLL Slow Digital Test Point	AA22	O	SD_SV_{DD}	12
SD_RX0_N	SerDes Receive Data (negative)	AE10	I	SD_SV_{DD}	---
SD_RX0_P	SerDes Receive Data (positive)	AD10	I	SD_SV_{DD}	---
SD_RX1_N	SerDes Receive Data (negative)	AE12	I	SD_SV_{DD}	---
SD_RX1_P	SerDes Receive Data (positive)	AD12	I	SD_SV_{DD}	---
SD_RX2_N	SerDes Receive Data (negative)	AE14	I	SD_SV_{DD}	---
SD_RX2_P	SerDes Receive Data (positive)	AD14	I	SD_SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_RX3_N	SerDes Receive Data (negative)	AE16	I	SD_SV_{DD}	---
SD_RX3_P	SerDes Receive Data (positive)	AD16	I	SD_SV_{DD}	---
SD_RX4_N	SerDes Receive Data (negative)	AE18	I	SD_SV_{DD}	---
SD_RX4_P	SerDes Receive Data (positive)	AD18	I	SD_SV_{DD}	---
SD_RX5_N	SerDes Receive Data (negative)	AE20	I	SD_SV_{DD}	---
SD_RX5_P	SerDes Receive Data (positive)	AD20	I	SD_SV_{DD}	---
SD_RX6_N	SerDes Receive Data (negative)	AE22	I	SD_SV_{DD}	---
SD_RX6_P	SerDes Receive Data (positive)	AD22	I	SD_SV_{DD}	---
SD_RX7_N	SerDes Receive Data (negative)	AE24	I	SD_SV_{DD}	---
SD_RX7_P	SerDes Receive Data (positive)	AD24	I	SD_SV_{DD}	---
SD_TX0_N	SerDes Transmit Data (negative)	AC11	O	SD_OV_{DD}	---
SD_TX0_P	SerDes Transmit Data (positive)	AB11	O	SD_OV_{DD}	---
SD_TX1_N	SerDes Transmit Data (negative)	AC13	O	SD_OV_{DD}	---
SD_TX1_P	SerDes Transmit Data (positive)	AB13	O	SD_OV_{DD}	---
SD_TX2_N	SerDes Transmit Data (negative)	AC15	O	SD_OV_{DD}	---
SD_TX2_P	SerDes Transmit Data (positive)	AB15	O	SD_OV_{DD}	---
SD_TX3_N	SerDes Transmit Data (negative)	AC17	O	SD_OV_{DD}	---
SD_TX3_P	SerDes Transmit Data (positive)	AB17	O	SD_OV_{DD}	---
SD_TX4_N	SerDes Transmit Data (negative)	AC19	O	SD_OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_TX4_P	SerDes Transmit Data (positive)	AB19	O	SD_OV_{DD}	---
SD_TX5_N	SerDes Transmit Data (negative)	AC21	O	SD_OV_{DD}	---
SD_TX5_P	SerDes Transmit Data (positive)	AB21	O	SD_OV_{DD}	---
SD_TX6_N	SerDes Transmit Data (negative)	AC23	O	SD_OV_{DD}	---
SD_TX6_P	SerDes Transmit Data (positive)	AB23	O	SD_OV_{DD}	---
SD_TX7_N	SerDes Transmit Data (negative)	AC25	O	SD_OV_{DD}	---
SD_TX7_P	SerDes Transmit Data (positive)	AB25	O	SD_OV_{DD}	---
Analog Signals					
CG_CAL	ClockGenerator RX Impedance Calibration	A5	IO	CG_SVDD	16
TD1_ANODE	Thermal diode anode	F16	IO	-	17
TD1_CATHODE	Thermal diode cathode	G16	IO	-	17
Alternate GPIO1					
WDOG_TOUT /GPIO_1_7 / TBGEN1_GPO39	GPIO/General Purpose Output	P24	O	OV_{DD}	1
GPIO_1_10/ **SPI3_CS0_B** / TBGEN1_GPO42	GPIO/General Purpose Output	F20	IO	OV_{DD}	---
GPIO_1_11/ **SPI3_CS1_B** / TBGEN1_GPO43	GPIO/General Purpose Output	G21	IO	OV_{DD}	---
GPIO_1_12/ **SPI3_CS2_B** / TBGEN1_GPO44	GPIO/General Purpose Output	G19	IO	OV_{DD}	---
GPIO_1_13/ **SPI3_CS3_B** / TBGEN1_GPO45	GPIO/General Purpose Output	H19	IO	OV_{DD}	---
GPIO_1_14/ **SPI3_CLK** / TBGEN1_GPO46	GPIO/General Purpose Output	G20	IO	OV_{DD}	---
GPIO_1_17/ **MODEM1_ SYNC_OUT**	General Purpose Input/Output	R20	IO	OV_{DD}	---
GPO_1_18/ **IIC1_SCL**	General Purpose Output	Y23	O	OV_{DD}	1
GPO_1_18/ **MODEM1_SYNC_ IN**	General Purpose Output	R19	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPO_1_19/ **IIC1_SDA**	General Purpose Output	W24	O	OV_{DD}	1
GPO_1_19/ **SPI2_CS1_B**	General Purpose Output	C24	O	OV_{DD}	1
GPIO_1_20/ **IIC2_SCL**	General Purpose Input/Output	W23	IO	OV_{DD}	---
GPIO_1_15/ **SPI2_CS2_B**	General Purpose Input/Output	C22	IO	OV_{DD}	---
GPIO_1_21/ **IIC2_SDA**	General Purpose Input/Output	V23	IO	OV_{DD}	---
GPIO_1_16/ **SPI2_CS3_B**	General Purpose Input/Output	C23	IO	OV_{DD}	---
GPIO_1_22/ **IIC3_SCL**	General Purpose Input/Output	W25	IO	OV_{DD}	---
GPIO_1_23/ **IIC3_SDA**	General Purpose Input/Output	Y25	IO	OV_{DD}	---
GPIO_1_24/ **UART2_SOUT** / cfg_sd_pll_pd_pllf_b	General Purpose Input/Output/ Power-On-Reset Configuration Signal	T20	IO	OV_{DD}	4
GPIO_1_25/ **UART2_SIN**	General Purpose Input/Output	U20	IO	OV_{DD}	---
GPIO_1_26/ **UART2_RTS_B** / UART4_SOUT /cfg_sd_pll_pd_plls_b	General Purpose Input/Output/ Transmit Data/ Power-On-Reset Configuration Signal	U21	IO	OV_{DD}	5
GPIO_1_27/ **UART2_CTS_B** / UART4_SIN	General Purpose Input/Output/ Receive Data	U22	IO	OV_{DD}	---
GPO_1_28/ **SPI1_CS2_B**	General Purpose Output	D25	O	OV_{DD}	1
GPO_1_28/ **UART1_SOUT** / cfg_pcie1_gen	General Purpose Output/ Power-On-Reset Configuration Signal	W21	O	OV_{DD}	1, 4
GPO_1_29/ **SPI1_CS3_B**	General Purpose Output	E24	O	OV_{DD}	1
GPO_1_29/ **UART1_SIN**	General Purpose Output	W22	O	OV_{DD}	1
GPO_1_30/ **SPI1_CS1_B**	General Purpose Output	E23	O	OV_{DD}	1
GPO_1_30/ **UART1_RTS_B** / UART3_SOUT /cfg_pcie2_gen	General Purpose Output/ Transmit Data/ Power-On-Reset Configuration Signal	Y21	O	OV_{DD}	1, 5
GPIO_1_31/ **UART1_CTS_B** / UART3_SIN	General Purpose Input/Output/ Receive Data	V22	IO	OV_{DD}	---
GPIO_1_7/ **WDOG_TOUT** / TBGEN1_GPO39	General Purpose Input/Output/ General Purpose Output	P24	IO	OV_{DD}	1
GPIO_1_8/ **SPI3_MOSI** / TBGEN1_GPO40	General Purpose Input/Output/ General Purpose Output	H20	IO	OV_{DD}	---
GPIO_1_9/ **SPI3_MISO** / TBGEN1_GPO41	General Purpose Input/Output/ General Purpose Output	G22	IO	OV_{DD}	---
Alternate GPIO4					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO_4_10/ **SPI6_CS0_B**	General Purpose Input/Output	U3	IO	OV_{DD}	---
GPIO_4_11/ **SPI6_CS1_B**	General Purpose Input/Output	V2	IO	OV_{DD}	---
GPIO_4_12/ **SPI6_CS2_B**	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO_4_13/ **SPI6_CS3_B**	General Purpose Input/Output	W1	IO	OV_{DD}	---
GPIO_4_14/ **SPI6_CLK**	General Purpose Input/Output	T3	IO	OV_{DD}	---
GPIO_4_15/ **SPI4_CS2_B**	General Purpose Input/Output	P1	IO	OV_{DD}	---
GPIO_4_16/ **SPI5_MOSI**	General Purpose Input/Output	R4	IO	OV_{DD}	---
GPIO_4_17/ **SPI5_MISO**	General Purpose Input/Output	P6	IO	OV_{DD}	---
GPIO_4_18/ **SPI5_CS0_B**	General Purpose Input/Output	R6	IO	OV_{DD}	---
GPIO_4_19/ **SPI5_CS1_B**	General Purpose Input/Output	R7	IO	OV_{DD}	---
GPIO_4_20/ **SPI5_CS2_B**	General Purpose Input/Output	R5	IO	OV_{DD}	---
GPIO_4_21/ **SPI5_CS3_B**	General Purpose Input/Output	T4	IO	OV_{DD}	---
GPIO_4_22/ **SPI5_CLK**	General Purpose Input/Output	P7	IO	OV_{DD}	---
GPIO_4_23/ **SPI4_CS3_B**	General Purpose Input/Output	R3	IO	OV_{DD}	---
GPIO_4_24/ **MODEM2_ SYNC_OUT**	General Purpose Input/Output	AA9	IO	OV_{DD}	---
GPIO_4_25/ **MODEM2_ SYNC_IN**	General Purpose Input/Output	AA10	IO	OV_{DD}	---
GPIO_4_26/ **IIC4_SCL**	General Purpose Input/Output	Y10	IO	OV_{DD}	---
GPIO_4_27/ **IIC4_SDA**	General Purpose Input/Output	W10	IO	OV_{DD}	---
GPIO_4_28/ **IIC5_SCL**	General Purpose Input/Output	Y9	IO	OV_{DD}	---
GPIO_4_29/ **IIC5_SDA**	General Purpose Input/Output	W9	IO	OV_{DD}	---
GPIO_4_3/ **IRQ_0**	General Purpose Input/Output	AD2	IO	OV_{DD}	---
GPIO_4_30/ **IIC6_SCL**	General Purpose Input/Output	Y8	IO	OV_{DD}	---
GPIO_4_31/ **IIC6_SDA**	General Purpose Input/Output	Y11	IO	OV_{DD}	---
GPIO_4_4/ **IRQ_1**	General Purpose Input/Output	AD3	IO	OV_{DD}	---
GPIO_4_5/ **IRQ_2**	General Purpose Input/Output	AE3	IO	OV_{DD}	---
GPIO_4_6/ **IRQ_3**	General Purpose Input/Output	AD4	IO	OV_{DD}	---
GPIO_4_7/ **IRQ_4**	General Purpose Input/Output	AE4	IO	OV_{DD}	---
GPIO_4_8/ **SPI6_MOSI**	General Purpose Input/Output	U2	IO	OV_{DD}	---
GPIO_4_9/ **SPI6_MISO**	General Purpose Input/Output	V1	IO	OV_{DD}	---
TBGen2					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TBGEN2_GPO0/ **GPIO_3_0** / RSTOUT_TR1_B	General Purpose Output/ Reset out to transceiver	V3	O	OV_{DD}	1
TBGEN2_GPO1/ **GPIO_3_1** / RSTOUT_TR2_B	General Purpose Output/ Reset out to transceiver	Y1	O	OV_{DD}	1
TBGEN2_GPO10/ **GPIO_3_10**	General Purpose Output	AA2	O	OV_{DD}	1
TBGEN2_GPO11/ **GPIO_3_11**	General Purpose Output	Y3	O	OV_{DD}	1
TBGEN2_GPO12/ **GPIO_3_12**	General Purpose Output	W4	O	OV_{DD}	1
TBGEN2_GPO13/ **GPIO_3_13**	General Purpose Output	AC1	O	OV_{DD}	1
TBGEN2_GPO14/ **GPIO_3_14**	General Purpose Output	V5	O	OV_{DD}	1
TBGEN2_GPO15/ **GPIO_3_15**	General Purpose Output	AA3	O	OV_{DD}	1
TBGEN2_GPO16/ **GPIO_3_16**	General Purpose Output	U6	O	OV_{DD}	1
TBGEN2_GPO17/ **GPIO_3_17**	General Purpose Output	Y4	O	OV_{DD}	1
TBGEN2_GPO18/ **GPIO_3_18**	General Purpose Output	AC2	O	OV_{DD}	1
TBGEN2_GPO19/ **GPIO_3_19**	General Purpose Output	T7	O	OV_{DD}	1
TBGEN2_GPO2/ **GPIO_3_2**	General Purpose Output	AA1	O	OV_{DD}	1
TBGEN2_GPO20/ **GPIO_3_20**	General Purpose Output	AB3	O	OV_{DD}	1
TBGEN2_GPO21/ **GPIO_3_21**	General Purpose Output	AB5	O	OV_{DD}	1
TBGEN2_GPO22/ **GPIO_3_22**	General Purpose Output	AA4	O	OV_{DD}	1
TBGEN2_GPO23/ **GPIO_3_23**	General Purpose Output	V6	O	OV_{DD}	1
TBGEN2_GPO24/ **GPIO_3_24**	General Purpose Output	AC3	O	OV_{DD}	1
TBGEN2_GPO25/ **GPIO_3_25**	General Purpose Output	Y5	O	OV_{DD}	1
TBGEN2_GPO26/ **GPIO_3_26**	General Purpose Output	AB4	O	OV_{DD}	1
TBGEN2_GPO27/ **GPIO_3_27**	General Purpose Output	AA6	O	OV_{DD}	1
TBGEN2_GPO28/ **GPIO_3_28**	General Purpose Output	Y7	O	OV_{DD}	1
TBGEN2_GPO29/ **GPIO_3_29**	General Purpose Output	U7	O	OV_{DD}	1
TBGEN2_GPO3/ **GPIO_3_3**	General Purpose Output	Y2	O	OV_{DD}	1
TBGEN2_GPO30/ **GPIO_3_30**	General Purpose Output/ General Purpose Output	W6	O	OV_{DD}	1
TBGEN2_GPO31/ **GPIO_3_31**	General Purpose Output/ General Purpose Output	AC4	O	OV_{DD}	1
TBGEN2_GPO4/ **GPIO_3_4**	General Purpose Output	W3	O	OV_{DD}	1
TBGEN2_GPO5/ **GPIO_3_5**	General Purpose Output	V4	O	OV_{DD}	1
TBGEN2_GPO6/ **GPIO_3_6**	General Purpose Output	U5	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TBGEN2_GPO7/ **GPIO_3_7**	General Purpose Output	T6	O	OV_{DD}	1
TBGEN2_GPO8/ **GPIO_3_8**	General Purpose Output	U4	O	OV_{DD}	1
TBGEN2_GPO9/ **GPIO_3_9**	General Purpose Output	AB1	O	OV_{DD}	1
TBGen1					
TBGEN1_GPO0/ **GPIO_2_0** / RSTOUT_TR3_B	General Purpose Output/ Reset out to transceiver	P25	O	OV_{DD}	1
TBGEN1_GPO1/ **GPIO_2_1** / RSTOUT_TR4_B	General Purpose Output/ Reset out to transceiver	N22	O	OV_{DD}	1
TBGEN1_GPO10/ **GPIO_2_10** /cfg_spare_sr2	General Purpose Output	K22	O	OV_{DD}	1, 4
TBGEN1_GPO11/ **GPIO_2_11** /cfg_pcie_lrev_b	General Purpose Output	L21	O	OV_{DD}	1, 4
TBGEN1_GPO12/ **GPIO_2_12** /cfg_sd_prtcl0	General Purpose Output	L22	O	OV_{DD}	1, 4
TBGEN1_GPO13/ **GPIO_2_13** /cfg_sd_prtcl1	General Purpose Output	H25	O	OV_{DD}	1, 4
TBGEN1_GPO14/ **GPIO_2_14** /cfg_sd_prtcl2	General Purpose Output	J25	O	OV_{DD}	1, 4
TBGEN1_GPO15/ **GPIO_2_15** /cfg_sd_pll_ref_clk	General Purpose Output	L19	O	OV_{DD}	1, 4
TBGEN1_GPO16/ **GPIO_2_16** /cfg_test_port_dis	General Purpose Output	L20	O	OV_{DD}	1, 4
TBGEN1_GPO17/ **GPIO_2_17** /cfg_test_port_sel	General Purpose Output	J24	O	OV_{DD}	1, 4
TBGEN1_GPO18/ **GPIO_2_18** /cfg_pcie2_rc_ep	General Purpose Output	K20	O	OV_{DD}	1, 4
TBGEN1_GPO19/ **GPIO_2_19** /cfg_test_sysclk_sel	General Purpose Output	J23	O	OV_{DD}	1, 4
TBGEN1_GPO2/ **GPIO_2_2**	General Purpose Output	N23	O	OV_{DD}	1
TBGEN1_GPO20/ **GPIO_2_20** /cfg_sysclk_sel1	General Purpose Output	K19	O	OV_{DD}	1, 4
TBGEN1_GPO21/ **GPIO_2_21**	General Purpose Output	J22	O	OV_{DD}	1
TBGEN1_GPO22/ **GPIO_2_22** /cfg_TBGen_pll0	General Purpose Output	H24	O	OV_{DD}	1, 4
TBGEN1_GPO23/ **GPIO_2_23** /cfg_TBGen_pll1	General Purpose Output	F25	O	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TBGEN1_GPO24/ **GPIO_2_24** /cfg_TBGen_pll2	General Purpose Output	G25	O	OV_{DD}	1, 4
TBGEN1_GPO25/ **GPIO_2_25** /cfg_TBGen_pll3	General Purpose Output	J20	O	OV_{DD}	1, 4
TBGEN1_GPO26/ **GPIO_2_26** /cfg_sysclk_sel	General Purpose Output	J21	O	OV_{DD}	1, 4
TBGEN1_GPO27/ **GPIO_2_27** /cfg_sys_pll	General Purpose Output	H23	O	OV_{DD}	1, 4
TBGEN1_GPO28/ **GPIO_2_28** /cfg_boot_src1	General Purpose Output	F24	O	OV_{DD}	1, 4
TBGEN1_GPO29/ **GPIO_2_29** /cfg_boot_src0	General Purpose Output	H22	O	OV_{DD}	1, 4
TBGEN1_GPO3/ **GPIO_2_3**	General Purpose Output	N19	O	OV_{DD}	1
TBGEN1_GPO30/ **GPIO_2_30** /cfg_boot_ho_b	General Purpose Output	J19	O	OV_{DD}	1, 4
TBGEN1_GPO31/ **GPIO_2_31** /TBGEN1_SYNC_IN /cfg_spare	General Purpose Output/ TBGEN1 SYNC IN	G23	O	OV_{DD}	1, 4
TBGEN1_GPO32/ **GPIO_1_0**	General Purpose Output	R24	O	OV_{DD}	1
TBGEN1_GPO33/ **GPIO_1_1**	General Purpose Output	R25	O	OV_{DD}	1
TBGEN1_GPO34/ **GPIO_1_2** / TBGEN1_SYNC_IN	General Purpose Output/ TBGEN1 SYNC IN	P19	O	OV_{DD}	1
TBGEN1_GPO35/ **GPIO_1_3**	General Purpose Output	P20	O	OV_{DD}	1
TBGEN1_GPO36/ **GPIO_1_4**	General Purpose Output	P21	O	OV_{DD}	1
TBGEN1_GPO37/ **GPIO_1_5**	General Purpose Output	P22	O	OV_{DD}	1
TBGEN1_GPO38/ **GPIO_1_6**	General Purpose Output	P23	O	OV_{DD}	1
TBGEN1_GPO39/ **WDOG_TOUT** /GPIO_1_7	General Purpose Output	P24	O	OV_{DD}	1
TBGEN1_GPO4/ **GPIO_2_4**	General Purpose Output	N20	O	OV_{DD}	1
TBGEN1_GPO40/ **SPI3_MOSI** /GPIO_1_8	General Purpose Output	H20	O	OV_{DD}	1
TBGEN1_GPO41/ **SPI3_MISO** /GPIO_1_9	General Purpose Output	G22	O	OV_{DD}	1
TBGEN1_GPO42/ **SPI3_CS0_B** /GPIO_1_10	General Purpose Output	F20	O	OV_{DD}	1
TBGEN1_GPO43/ **SPI3_CS1_B** /GPIO_1_11	General Purpose Output	G21	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TBGEN1_GPO44/ **SPI3_CS2_B** /GPIO_1_12	General Purpose Output	G19	O	OV_{DD}	1
TBGEN1_GPO45/ **SPI3_CS3_B** /GPIO_1_13	General Purpose Output	H19	O	OV_{DD}	1
TBGEN1_GPO46/ **SPI3_CLK** / GPIO_1_14	General Purpose Output	G20	O	OV_{DD}	1
TBGEN1_GPO5/ **GPIO_2_5**	General Purpose Output	K25	O	OV_{DD}	1
TBGEN1_GPO6/ **GPIO_2_6**	General Purpose Output	M21	O	OV_{DD}	1
TBGEN1_GPO7/ **GPIO_2_7** / CFG_spare_sr5_0	General Purpose Output	M22	O	OV_{DD}	1, 4
TBGEN1_GPO8/ **GPIO_2_8** / CFG_spare_sr5_1	General Purpose Output	K23	O	OV_{DD}	1, 4
TBGEN1_GPO9/ **GPIO_2_9** / CFG_spare_sr5_2	General Purpose Output	L23	O	OV_{DD}	1, 4
TBGEN2_SYNC_IN/ **GPIO_4_2**	TBGEN2 SYNC IN	W7	I	OV_{DD}	1
Reset to RF Transceivers RSTOUT					
RSTOUT_TR1_B/ **GPIO_3_0** / TBGEN2_GPO0	Reset out to transceiver	V3	O	OV_{DD}	1
RSTOUT_TR1_B/ **GPIO_4_0**	Reset out to transceiver	V7	O	OV_{DD}	1
RSTOUT_TR2_B/ **GPIO_3_1** / TBGEN2_GPO1	Reset out to transceiver	Y1	O	OV_{DD}	1
RSTOUT_TR2_B/ **GPIO_4_1**	Reset out to transceiver	Y6	O	OV_{DD}	1
RSTOUT_TR3_B/ **GPIO_2_0** / TBGEN1_GPO0	Reset out to transceiver	P25	O	OV_{DD}	1
RSTOUT_TR4_B/ **GPIO_2_1** / TBGEN1_GPO1	Reset out to transceiver	N22	O	OV_{DD}	1
Modem2 Timing Sync Signals					
MODEM2_SYNC_IN /GPIO_4_25	Modem2 Timing Sync signal	AA10	I	OV_{DD}	1
MODEM2_SYNC_OUT / GPIO_4_24	MODEM2 Sync out	AA9	O	OV_{DD}	1
Modem1 Timing Sync Signals					
MODEM1 SYNC_IN /GPIO_1_18	Modem1 Timing Sync signal	R19	I	OV_{DD}	1
MODEM1_SYNC_OUT / GPIO_1_17	MODEM1_ Sync out	R20	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI1 Controller					
SPI1_CLK	SPI Clock	D23	O	OV_{DD}	2
SPI1_CS0_B	Chip Select 0	F23	O	OV_{DD}	2
SPI1_CS1_B /GPIO_1_30	Chip Select 1	E23	O	OV_{DD}	2
SPI1_CS2_B /GPIO_1_28	Chip Select 0	D25	O	OV_{DD}	1
SPI1_CS3_B /GPIO_1_29	Chip Select 1	E24	O	OV_{DD}	2
SPI1_MISO	Master In / Slave Out	F22	I	OV_{DD}	---
SPI1_MOSI	Master Out / Slave In	E25	O	OV_{DD}	2
SPI2 Controller					
SPI2_CLK	SPI Clock	A23	O	OV_{DD}	2
SPI2_CS0_B	Chip Select 0	B24	O	OV_{DD}	2
SPI2_CS1_B /GPIO_1_19	Chip Select 1	C24	O	OV_{DD}	2
SPI2_CS2_B /GPIO_1_15	Chip Select 2	C22	O	OV_{DD}	1
SPI2_CS3_B /GPIO_1_16	Chip Select 3	C23	O	OV_{DD}	1
SPI2_MISO	Master In / Slave Out	B23	I	OV_{DD}	---
SPI2_MOSI	Master Out / Slave In	C25	O	OV_{DD}	2
SPI3 Controller					
SPI3_CLK /GPIO_1_14 / TBGEN1_GPO46	SPI Clock	G20	O	OV_{DD}	1
SPI3_CS0_B /GPIO_1_10 / TBGEN1_GPO42	Chip Select 0	F20	O	OV_{DD}	1
SPI3_CS1_B /GPIO_1_11 / TBGEN1_GPO43	Chip Select 1	G21	O	OV_{DD}	1
SPI3_CS2_B /GPIO_1_12 / TBGEN1_GPO44	Chip Select 2	G19	O	OV_{DD}	1
SPI3_CS3_B /GPIO_1_13 / TBGEN1_GPO45	Chip Select 3	H19	O	OV_{DD}	1
SPI3_MISO /GPIO_1_9 / TBGEN1_GPO41	Master In / Slave Out	G22	I	OV_{DD}	1
SPI3_MOSI /GPIO_1_8 / TBGEN1_GPO40	Master Out / Slave In	H20	O	OV_{DD}	1
SPI4 controller					
SPI4_CLK	SPI Clock	T1	O	OV_{DD}	2
SPI4_CS0_B	Chip Select 0	P3	O	OV_{DD}	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI4_CS1_B	Chip Select 1	R2	O	OV_{DD}	2
SPI4_CS2_B /GPIO_4_15	Chip Select 2	P1	O	OV_{DD}	1
SPI4_CS3_B /GPIO_4_23	Chip Select 3	R3	O	OV_{DD}	1
SPI4_MISO	Master In / Slave Out	P2	I	OV_{DD}	---
SPI4_MOSI	Master Out / Slave In	R1	O	OV_{DD}	2
SPI5 Controller					
SPI5_CLK /GPIO_4_22	SPI Clock	P7	O	OV_{DD}	1
SPI5_CS0_B /GPIO_4_18	Chip Select 0	R6	O	OV_{DD}	1
SPI5_CS1_B /GPIO_4_19	Chip Select 1	R7	O	OV_{DD}	1
SPI5_CS2_B /GPIO_4_20	Chip Select 2	R5	O	OV_{DD}	1
SPI5_CS3_B /GPIO_4_21	Chip Select 3	T4	O	OV_{DD}	1
SPI5_MISO /GPIO_4_17	Master In / Slave Out	P6	I	OV_{DD}	1
SPI5_MOSI /GPIO_4_16	Master Out / Slave In	R4	O	OV_{DD}	1
SPI6 Controller					
SPI6_CLK /GPIO_4_14	SPI Clock	T3	O	OV_{DD}	1
SPI6_CS0_B /GPIO_4_10	Chip Select 0	U3	O	OV_{DD}	1
SPI6_CS1_B /GPIO_4_11	Chip Select 1	V2	O	OV_{DD}	1
SPI6_CS2_B /GPIO_4_12	Chip Select 2	U1	O	OV_{DD}	1
SPI6_CS3_B /GPIO_4_13	Chip Select 3	W1	O	OV_{DD}	1
SPI6_MISO /GPIO_4_9	Master In / Slave Out	V1	I	OV_{DD}	1
SPI6_MOSI /GPIO_4_8	Master Out / Slave In	U2	O	OV_{DD}	1
Power-On-Reset Configuration					
cfg_boot_ho_b/ **GPIO_2_30** / TBGEN1_GPO30	Power-on-Reset Configuration	J19	I	OV_{DD}	1, 4
cfg_boot_src0/ **GPIO_2_29** / TBGEN1_GPO29	Power-on-Reset Configuration	H22	I	OV_{DD}	1, 4
cfg_boot_src1/ **GPIO_2_28** / TBGEN1_GPO28	Power-on-Reset Configuration	F24	I	OV_{DD}	1, 4
cfg_TBGen_pll0/ **GPIO_2_22** / TBGEN1_GPO22	Power-on-Reset Configuration	H24	I	OV_{DD}	1, 4
cfg_TBGen_pll1/ **GPIO_2_23** / TBGEN1_GPO23	Power-on-Reset Configuration	F25	I	OV_{DD}	1, 4
cfg_TBGen_pll2/ **GPIO_2_24** / TBGEN1_GPO24	Power-on-Reset Configuration	G25	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
cfg_TBGen_pll3/ **GPIO_2_25** / TBGEN1_GPO25	Power-on-Reset Configuration	J20	I	OV_{DD}	1, 4
cfg_pcie1_gen/ **UART1_SOUT** /GPIO_1_28	Power-on-Reset Configuration	W21	I	OV_{DD}	1, 4
cfg_pcie2_gen/ **UART1_RTS_B** /GPIO_1_30 /UART3_SOUT	Power-on-Reset Configuration	Y21	I	OV_{DD}	1, 5
cfg_pcie2_rc_ep/ **GPIO_2_18** / TBGEN1_GPO18	Power-on-Reset Configuration	K20	I	OV_{DD}	1, 4
cfg_pcie_lrev_b/ **GPIO_2_11** / TBGEN1_GPO11	Power-on-Reset Configuration	L21	I	OV_{DD}	1, 4
cfg_sd_pll_pd_pllf_b/ **UART2_SOUT** /GPIO_1_24	Power-on-Reset Configuration	T20	I	OV_{DD}	1, 4
cfg_sd_pll_pd_plls_b/ **UART2_RTS_B** /GPIO_1_26 /UART4_SOUT	Power-on-Reset Configuration	U21	I	OV_{DD}	1, 5
cfg_sd_pll_ref_clk/ **GPIO_2_15** /TBGEN1_GPO15	Power-on-Reset Configuration	L19	I	OV_{DD}	1, 4
cfg_sd_prtcl0/ **GPIO_2_12** / TBGEN1_GPO12	Power-on-Reset Configuration	L22	I	OV_{DD}	1, 4
cfg_sd_prtcl1/ **GPIO_2_13** / TBGEN1_GPO13	Power-on-Reset Configuration	H25	I	OV_{DD}	1, 4
cfg_sd_prtcl2/ **GPIO_2_14** / TBGEN1_GPO14	Power-on-Reset Configuration	J25	I	OV_{DD}	1, 4
CFG_spare_sr5_0/ **GPIO_2_7** /TBGEN1_GPO7	Power-on-Reset Configuration	M22	I	OV_{DD}	1, 4
CFG_spare_sr5_1/ **GPIO_2_8** /TBGEN1_GPO8	Power-on-Reset Configuration	K23	I	OV_{DD}	1, 4
CFG_spare_sr5_2/ **GPIO_2_9** /TBGEN1_GPO9	Power-on-Reset Configuration	L23	I	OV_{DD}	1, 4
cfg_spare/ **GPIO_2_31** / TBGEN1_SYNC_IN / TBGEN1_GPO31	Power-on-Reset Configuration	G23	I	OV_{DD}	1, 4
cfg_spare_sr2/ **GPIO_2_10** / TBGEN1_GPO10	Power-on-Reset Configuration	K22	I	OV_{DD}	1, 4
cfg_sys_pll/ **GPIO_2_27** / TBGEN1_GPO27	Power-on-Reset Configuration	H23	I	OV_{DD}	1, 4
cfg_sysclk_sel/ **GPIO_2_26** / TBGEN1_GPO26	Power-on-Reset Configuration	J21	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
cfg_sysclk_sel1/ **GPIO_2_20** / TBGEN1_GPO20	Power-on-Reset Configuration	K19	I	OV_{DD}	1, 4
cfg_test_port_dis/ **GPIO_2_16** /TBGEN1_GPO16	Power-on-Reset Configuration	L20	I	OV_{DD}	1, 4
cfg_test_port_sel/ **GPIO_2_17** /TBGEN1_GPO17	Power-on-Reset Configuration	J24	I	OV_{DD}	1, 4
cfg_test_sysclk_sel/ **GPIO_2_19** /TBGEN1_GPO19	Power-on-Reset Configuration	J23	I	OV_{DD}	1, 4
FlexSPI					
XSPI_CS0_B	Chip Select (Port A)	L25	O	OV_{DD}	2
XSPI_DATA_0	Data (Port A)	M25	IO	OV_{DD}	---
XSPI_DATA_1	Data (Port A)	M24	IO	OV_{DD}	---
XSPI_DATA_2	Data (Port A)	M23	IO	OV_{DD}	---
XSPI_DATA_3	Data (Port A)	N25	IO	OV_{DD}	---
XSPI_SCK	Clock (Port A)	L24	O	OV_{DD}	1
DFT					
SCAN_B_MODE	Internal use only	V19	I	OV_{DD}	10
Power and Ground Signals					
GND01	GND - SoC Common ground	A24	---	---	---
GND02	GND - SoC Common ground	B25	---	---	---
GND03	GND - SoC Common ground	D24	---	---	---
GND04	GND - SoC Common ground	G14	---	---	---
GND05	GND - SoC Common ground	G18	---	---	---
GND06	GND - SoC Common ground	G24	---	---	---
GND07	GND - SoC Common ground	H16	---	---	15
GND08	GND - SoC Common ground	H18	---	---	15
GND09	GND - SoC Common ground	H21	---	---	15
GND10	GND - SoC Common ground	J9	---	---	15
GND11	GND - SoC Common ground	J11	---	---	15
GND12	GND - SoC Common ground	J13	---	---	15
GND13	GND - SoC Common ground	J15	---	---	15
GND14	GND - SoC Common ground	J17	---	---	15
GND15	GND - SoC Common ground	K10	---	---	15

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND16	GND - SoC Common ground	K12	---	---	15
GND17	GND - SoC Common ground	K14	---	---	15
GND18	GND - SoC Common ground	K16	---	---	15
GND19	GND - SoC Common ground	K21	---	---	15
GND20	GND - SoC Common ground	K24	---	---	15
GND21	GND - SoC Common ground	L9	---	---	15
GND22	GND - SoC Common ground	L11	---	---	15
GND23	GND - SoC Common ground	L13	---	---	15
GND24	GND - SoC Common ground	L15	---	---	15
GND25	GND - SoC Common ground	L17	---	---	15
GND26	GND - SoC Common ground	M10	---	---	15
GND27	GND - SoC Common ground	M12	---	---	15
GND28	GND - SoC Common ground	M14	---	---	15
GND29	GND - SoC Common ground	M16	---	---	15
GND30	GND - SoC Common ground	M20	---	---	15
GND31	GND - SoC Common ground	N9	---	---	15
GND32	GND - SoC Common ground	N11	---	---	15
GND33	GND - SoC Common ground	N13	---	---	15
GND34	GND - SoC Common ground	N15	---	---	15
GND35	GND - SoC Common ground	N17	---	---	15
GND36	GND - SoC Common ground	N21	---	---	15
GND37	GND - SoC Common ground	N24	---	---	15
GND38	GND - SoC Common ground	P10	---	---	15
GND39	GND - SoC Common ground	P12	---	---	15
GND40	GND - SoC Common ground	P14	---	---	15
GND41	GND - SoC Common ground	P16	---	---	15
GND42	GND - SoC Common ground	R9	---	---	15
GND43	GND - SoC Common ground	R11	---	---	15
GND44	GND - SoC Common ground	R13	---	---	15
GND45	GND - SoC Common ground	R15	---	---	15
GND46	GND - SoC Common ground	R17	---	---	15
GND47	GND - SoC Common ground	T2	---	---	15

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND48	GND - SoC Common ground	T5	---	---	15
GND49	GND - SoC Common ground	T10	---	---	15
GND50	GND - SoC Common ground	T12	---	---	15
GND51	GND - SoC Common ground	T14	---	---	15
GND52	GND - SoC Common ground	T16	---	---	15
GND53	GND - SoC Common ground	T19	---	---	15
GND54	GND - SoC Common ground	T21	---	---	15
GND55	GND - SoC Common ground	T24	---	---	15
GND56	GND - SoC Common ground	U9	---	---	15
GND57	GND - SoC Common ground	U11	---	---	15
GND58	GND - SoC Common ground	V21	---	---	15
GND59	GND - SoC Common ground	V24	---	---	15
GND60	GND - SoC Common ground	W2	---	---	15
GND61	GND - SoC Common ground	W5	---	---	15
GND62	GND - SoC Common ground	W8	---	---	15
GND63	GND - SoC Common ground	W11	---	---	15
GND64	GND - SoC Common ground	AA5	---	---	15
GND65	GND - SoC Common ground	AA8	---	---	15
GND66	GND - SoC Common ground	AB2	---	---	15
GND67	GND - SoC Common ground	AC5	---	---	15
GND68	GND - SoC Common ground	AC7	---	---	15
GND69	GND - SoC Common ground	AD1	---	---	15
CG_GND1	Clock Gen GND	A3	---	---	---
CG_GND2	Clock Gen GND	B1	---	---	---
CG_GND3	Clock Gen GND	B3	---	---	---
CG_GND4	Clock Gen GND	B5	---	---	---
CG_GND5	Clock Gen GND	H8	---	---	---
CG_GND6	Clock Gen GND	J8	---	---	---
LS_DCS_AGND1	LS DCS Analog GND	A6	---	---	---
LS_DCS_AGND2	LS DCS Analog GND	A8	---	---	---
LS_DCS_AGND3	LS DCS Analog GND	A10	---	---	---
LS_DCS_AGND4	LS DCS Analog GND	A12	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LS_DCS_AGND5	LS DCS Analog GND	A14	---	---	---
LS_DCS_AGND6	LS DCS Analog GND	A16	---	---	---
LS_DCS_AGND7	LS DCS Analog GND	A18	---	---	---
LS_DCS_AGND8	LS DCS Analog GND	A20	---	---	---
LS_DCS_AGND9	LS DCS Analog GND	A22	---	---	---
LS_DCS_AGND10	LS DCS Analog GND	B6	---	---	---
LS_DCS_AGND11	LS DCS Analog GND	B8	---	---	---
LS_DCS_AGND12	LS DCS Analog GND	B10	---	---	---
LS_DCS_AGND13	LS DCS Analog GND	B12	---	---	---
LS_DCS_AGND14	LS DCS Analog GND	B14	---	---	---
LS_DCS_AGND15	LS DCS Analog GND	B16	---	---	---
LS_DCS_AGND16	LS DCS Analog GND	B18	---	---	---
LS_DCS_AGND17	LS DCS Analog GND	B20	---	---	---
LS_DCS_AGND18	LS DCS Analog GND	B22	---	---	---
LS_DCS_AGND19	LS DCS Analog GND	C7	---	---	---
LS_DCS_AGND20	LS DCS Analog GND	C8	---	---	---
LS_DCS_AGND21	LS DCS Analog GND	C9	---	---	---
LS_DCS_AGND22	LS DCS Analog GND	C11	---	---	---
LS_DCS_AGND23	LS DCS Analog GND	C13	---	---	---
LS_DCS_AGND24	LS DCS Analog GND	C15	---	---	---
LS_DCS_AGND25	LS DCS Analog GND	C17	---	---	14
LS_DCS_AGND26	LS DCS Analog GND	C18	---	---	14
LS_DCS_AGND27	LS DCS Analog GND	C19	---	---	14
LS_DCS_AGND28	LS DCS Analog GND	C20	---	---	14
LS_DCS_AGND29	LS DCS Analog GND	C21	---	---	14
LS_DCS_AGND30	LS DCS Analog GND	D6	---	---	14
LS_DCS_AGND31	LS DCS Analog GND	D8	---	---	14
LS_DCS_AGND32	LS DCS Analog GND	D10	---	---	14
LS_DCS_AGND33	LS DCS Analog GND	D12	---	---	14
LS_DCS_AGND34	LS DCS Analog GND	D14	---	---	14
LS_DCS_AGND35	LS DCS Analog GND	D16	---	---	14
LS_DCS_AGND36	LS DCS Analog GND	D18	---	---	14

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LS_DCS_AGND37	LS DCS Analog GND	D20	---	---	14
LS_DCS_AGND38	LS DCS Analog GND	D22	---	---	14
LS_DCS_AGND39	LS DCS Analog GND	E6	---	---	14
LS_DCS_AGND40	LS DCS Analog GND	E8	---	---	14
LS_DCS_AGND41	LS DCS Analog GND	E10	---	---	14
LS_DCS_AGND42	LS DCS Analog GND	E12	---	---	14
LS_DCS_AGND43	LS DCS Analog GND	E14	---	---	14
LS_DCS_AGND44	LS DCS Analog GND	E16	---	---	14
LS_DCS_AGND45	LS DCS Analog GND	E18	---	---	14
LS_DCS_AGND46	LS DCS Analog GND	E20	---	---	14
LS_DCS_AGND47	LS DCS Analog GND	E22	---	---	14
LS_DCS_AGND48	LS DCS Analog GND	F7	---	---	14
LS_DCS_AGND49	LS DCS Analog GND	F9	---	---	14
LS_DCS_AGND50	LS DCS Analog GND	F11	---	---	14
LS_DCS_AGND51	LS DCS Analog GND	F13	---	---	14
LS_DCS_AGND52	LS DCS Analog GND	F15	---	---	14
LS_DCS_AGND53	LS DCS Analog GND	F17	---	---	14
LS_DCS_AGND54	LS DCS Analog GND	F19	---	---	14
LS_DCS_AGND55	LS DCS Analog GND	F21	---	---	14
LS_DCS_AGND56	LS DCS Analog GND	H9	---	---	14
LS_DCS_AGND57	LS DCS Analog GND	H10	---	---	14
LS_DCS_AGND58	LS DCS Analog GND	H11	---	---	14
LS_DCS_AGND59	LS DCS Analog GND	H12	---	---	14
HS_DCS_AGND1	HS DCS Analog GND	C1	---	---	---
HS_DCS_AGND2	HS DCS Analog GND	C2	---	---	---
HS_DCS_AGND3	HS DCS Analog GND	C4	---	---	---
HS_DCS_AGND4	HS DCS Analog GND	C5	---	---	---
HS_DCS_AGND5	HS DCS Analog GND	D3	---	---	---
HS_DCS_AGND6	HS DCS Analog GND	E1	---	---	---
HS_DCS_AGND7	HS DCS Analog GND	E2	---	---	---
HS_DCS_AGND8	HS DCS Analog GND	E3	---	---	---
HS_DCS_AGND9	HS DCS Analog GND	E4	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
HS_DCS_AGND10	HS DCS Analog GND	E5	---	---	---
HS_DCS_AGND11	HS DCS Analog GND	F3	---	---	---
HS_DCS_AGND12	HS DCS Analog GND	F6	---	---	---
HS_DCS_AGND13	HS DCS Analog GND	G1	---	---	---
HS_DCS_AGND14	HS DCS Analog GND	G2	---	---	---
HS_DCS_AGND15	HS DCS Analog GND	G4	---	---	---
HS_DCS_AGND16	HS DCS Analog GND	G5	---	---	---
HS_DCS_AGND17	HS DCS Analog GND	H3	---	---	---
HS_DCS_AGND18	HS DCS Analog GND	H6	---	---	---
HS_DCS_AGND19	HS DCS Analog GND	J1	---	---	---
HS_DCS_AGND20	HS DCS Analog GND	J2	---	---	---
HS_DCS_AGND21	HS DCS Analog GND	J4	---	---	---
HS_DCS_AGND22	HS DCS Analog GND	J5	---	---	---
HS_DCS_AGND23	HS DCS Analog GND	K3	---	---	---
HS_DCS_AGND24	HS DCS Analog GND	K6	---	---	---
HS_DCS_AGND25	HS DCS Analog GND	L1	---	---	---
HS_DCS_AGND26	HS DCS Analog GND	L2	---	---	---
HS_DCS_AGND27	HS DCS Analog GND	L4	---	---	---
HS_DCS_AGND28	HS DCS Analog GND	L5	---	---	---
HS_DCS_AGND29	HS DCS Analog GND	L7	---	---	---
HS_DCS_AGND30	HS DCS Analog GND	L8	---	---	---
HS_DCS_AGND31	HS DCS Analog GND	M3	---	---	---
HS_DCS_AGND32	HS DCS Analog GND	M6	---	---	---
HS_DCS_AGND33	HS DCS Analog GND	N1	---	---	---
HS_DCS_AGND34	HS DCS Analog GND	N2	---	---	---
HS_DCS_AGND35	HS DCS Analog GND	N4	---	---	---
HS_DCS_AGND36	HS DCS Analog GND	N5	---	---	---
SD_GND01	SerDes core logic ground	V12	---	---	---
SD_GND02	SerDes core logic ground	V13	---	---	---
SD_GND03	SerDes core logic ground	V14	---	---	---
SD_GND04	SerDes core logic ground	V15	---	---	---
SD_GND05	SerDes core logic ground	V16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND06	SerDes core logic ground	V17	---	---	---
SD_GND07	SerDes core logic ground	V18	---	---	---
SD_GND08	SerDes core logic ground	Y13	---	---	---
SD_GND09	SerDes core logic ground	Y15	---	---	---
SD_GND10	SerDes core logic ground	Y17	---	---	---
SD_GND11	SerDes core logic ground	Y20	---	---	---
SD_GND12	SerDes core logic ground	Y22	---	---	---
SD_GND13	SerDes core logic ground	Y24	---	---	---
SD_GND14	SerDes core logic ground	AA11	---	---	---
SD_GND15	SerDes core logic ground	AA13	---	---	---
SD_GND16	SerDes core logic ground	AA15	---	---	---
SD_GND17	SerDes core logic ground	AA17	---	---	---
SD_GND18	SerDes core logic ground	AA19	---	---	---
SD_GND19	SerDes core logic ground	AA21	---	---	---
SD_GND20	SerDes core logic ground	AA23	---	---	---
SD_GND21	SerDes core logic ground	AA25	---	---	---
SD_GND22	SerDes core logic ground	AB10	---	---	---
SD_GND23	SerDes core logic ground	AB12	---	---	---
SD_GND24	SerDes core logic ground	AB14	---	---	---
SD_GND25	SerDes core logic ground	AB16	---	---	---
SD_GND26	SerDes core logic ground	AB18	---	---	---
SD_GND27	SerDes core logic ground	AB20	---	---	---
SD_GND28	SerDes core logic ground	AB22	---	---	---
SD_GND29	SerDes core logic ground	AB24	---	---	---
SD_GND30	SerDes core logic ground	AC10	---	---	---
SD_GND31	SerDes core logic ground	AC12	---	---	---
SD_GND32	SerDes core logic ground	AC14	---	---	---
SD_GND33	SerDes core logic ground	AC16	---	---	---
SD_GND34	SerDes core logic ground	AC18	---	---	---
SD_GND35	SerDes core logic ground	AC20	---	---	---
SD_GND36	SerDes core logic ground	AC22	---	---	---
SD_GND37	SerDes core logic ground	AC24	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND38	SerDes core logic ground	AD9	---	---	---
SD_GND39	SerDes core logic ground	AD11	---	---	---
SD_GND40	SerDes core logic ground	AD13	---	---	---
SD_GND41	SerDes core logic ground	AD15	---	---	---
SD_GND42	SerDes core logic ground	AD17	---	---	---
SD_GND43	SerDes core logic ground	AD19	---	---	---
SD_GND44	SerDes core logic ground	AD21	---	---	---
SD_GND45	SerDes core logic ground	AD23	---	---	---
SD_GND46	SerDes core logic ground	AD25	---	---	---
SD_GND47	SerDes core logic ground	AE9	---	---	---
SD_GND48	SerDes core logic ground	AE11	---	---	---
SD_GND49	SerDes core logic ground	AE13	---	---	---
SD_GND50	SerDes core logic ground	AE15	---	---	---
SD_GND51	SerDes core logic ground	AE17	---	---	---
SD_GND52	SerDes core logic ground	AE19	---	---	---
SD_GND53	SerDes core logic ground	AE21	---	---	---
SD_GND54	SerDes core logic ground	AE23	---	---	---
OVDD01	OVDD supply	J18	---	OV_{DD}	---
OVDD02	OVDD supply	K18	---	OV_{DD}	---
OVDD03	OVDD supply	L18	---	OV_{DD}	---
OVDD04	OVDD supply	M18	---	OV_{DD}	---
OVDD05	OVDD supply	N18	---	OV_{DD}	---
OVDD06	OVDD supply	P8	---	OV_{DD}	---
OVDD07	OVDD supply	P18	---	OV_{DD}	---
OVDD08	OVDD supply	R8	---	OV_{DD}	---
OVDD09	OVDD supply	R18	---	OV_{DD}	---
OVDD10	OVDD supply	T8	---	OV_{DD}	---
OVDD11	OVDD supply	T18	---	OV_{DD}	---
OVDD12	OVDD supply	U8	---	OV_{DD}	---
OVDD13	OVDD supply	V8	---	OV_{DD}	---
OVDD14	OVDD supply	V10	---	OV_{DD}	---
OVDD15	OVDD supply	V11	---	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD01	Supply for cores, platform,HS DCS and LS DCS	H15	---	V_{DD}	---
VDD02	Supply for cores, platform,HS DCS and LS DCS	H17	---	V_{DD}	---
VDD03	Supply for cores, platform,HS DCS and LS DCS	J10	---	V_{DD}	---
VDD04	Supply for cores, platform,HS DCS and LS DCS	J12	---	V_{DD}	---
VDD05	Supply for cores, platform,HS DCS and LS DCS	J14	---	V_{DD}	---
VDD06	Supply for cores, platform,HS DCS and LS DCS	J16	---	V_{DD}	---
VDD07	Supply for cores, platform,HS DCS and LS DCS	K9	---	V_{DD}	---
VDD08	Supply for cores, platform,HS DCS and LS DCS	K11	---	V_{DD}	---
VDD09	Supply for cores, platform,HS DCS and LS DCS	K13	---	V_{DD}	---
VDD10	Supply for cores, platform,HS DCS and LS DCS	K15	---	V_{DD}	---
VDD11	Supply for cores, platform,HS DCS and LS DCS	K17	---	V_{DD}	---
VDD12	Supply for cores, platform,HS DCS and LS DCS	L10	---	V_{DD}	---
VDD13	Supply for cores, platform,HS DCS and LS DCS	L12	---	V_{DD}	---
VDD14	Supply for cores, platform,HS DCS and LS DCS	L14	---	V_{DD}	---
VDD15	Supply for cores, platform,HS DCS and LS DCS	L16	---	V_{DD}	---
VDD16	Supply for cores, platform,HS DCS and LS DCS	M9	---	V_{DD}	---
VDD17	Supply for cores, platform,HS DCS and LS DCS	M11	---	V_{DD}	---
VDD18	Supply for cores, platform,HS DCS and LS DCS	M13	---	V_{DD}	---
VDD19	Supply for cores, platform,HS DCS and LS DCS	M15	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD20	Supply for cores, platform,HS DCS and LS DCS	M17	---	V_{DD}	---
VDD21	Supply for cores, platform,HS DCS and LS DCS	N10	---	V_{DD}	---
VDD22	Supply for cores, platform,HS DCS and LS DCS	N12	---	V_{DD}	---
VDD23	Supply for cores, platform,HS DCS and LS DCS	N14	---	V_{DD}	---
VDD24	Supply for cores, platform,HS DCS and LS DCS	N16	---	V_{DD}	---
VDD25	Supply for cores, platform,HS DCS and LS DCS	P9	---	V_{DD}	---
VDD26	Supply for cores, platform,HS DCS and LS DCS	P11	---	V_{DD}	---
VDD27	Supply for cores, platform,HS DCS and LS DCS	P13	---	V_{DD}	---
VDD28	Supply for cores, platform,HS DCS and LS DCS	P15	---	V_{DD}	---
VDD29	Supply for cores, platform,HS DCS and LS DCS	P17	---	V_{DD}	---
VDD30	Supply for cores, platform,HS DCS and LS DCS	R10	---	V_{DD}	---
VDD31	Supply for cores, platform,HS DCS and LS DCS	R12	---	V_{DD}	---
VDD32	Supply for cores, platform,HS DCS and LS DCS	R14	---	V_{DD}	---
VDD33	Supply for cores, platform,HS DCS and LS DCS	R16	---	V_{DD}	---
VDD34	Supply for cores, platform,HS DCS and LS DCS	T9	---	V_{DD}	---
VDD35	Supply for cores, platform,HS DCS and LS DCS	T11	---	V_{DD}	---
VDD36	Supply for cores, platform,HS DCS and LS DCS	T13	---	V_{DD}	---
VDD37	Supply for cores, platform,HS DCS and LS DCS	T15	---	V_{DD}	---
VDD38	Supply for cores, platform,HS DCS and LS DCS	T17	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD39	Supply for cores, platform,HS DCS and LS DCS	U10	---	V_{DD}	---
AVDD_SD_PLLF	SerDes Analog PLL fast supply	AA14	---	AVDD_SD_PLLF	---
AVDD_SD_PLLS	SerDes Analog PLL slow supply	AA18	---	AVDD_SD_PLLS	---
SD_SVDD1	SerDes core logic supply	U12	---	SD_SV_{DD}	---
SD_SVDD2	SerDes core logic supply	U13	---	SD_SV_{DD}	---
SD_SVDD3	SerDes core logic supply	U14	---	SD_SV_{DD}	---
SD_SVDD4	SerDes core logic supply	U15	---	SD_SV_{DD}	---
SD_SVDD5	SerDes core logic supply	U16	---	SD_SV_{DD}	---
SD_SVDD6	SerDes core logic supply	U17	---	SD_SV_{DD}	---
SD_SVDD7	SerDes core logic supply	U18	---	SD_SV_{DD}	---
SD_OVDD01	SerDes transceiver supply	W12	---	SD_OV_{DD}	---
SD_OVDD02	SerDes transceiver supply	W13	---	SD_OV_{DD}	---
SD_OVDD03	SerDes transceiver supply	W14	---	SD_OV_{DD}	---
SD_OVDD04	SerDes transceiver supply	W15	---	SD_OV_{DD}	---
SD_OVDD05	SerDes transceiver supply	W16	---	SD_OV_{DD}	---
SD_OVDD06	SerDes transceiver supply	W17	---	SD_OV_{DD}	---
SD_OVDD07	SerDes transceiver supply	W18	---	SD_OV_{DD}	---
SD_OVDD08	SerDes transceiver supply	W19	---	SD_OV_{DD}	---
SD_OVDD09	SerDes transceiver supply	Y12	---	SD_OV_{DD}	---
SD_OVDD10	SerDes transceiver supply	Y19	---	SD_OV_{DD}	---
CG_AVDD	ClockGen PLL analog Supply	H7	---	CG_AV_{DD}	---
CG_OVDD	ClockGen transceiver supply	J7	---	CG_OV_{DD}	---
CG_SVDD1	ClockGen Core supply	G6	---	CG_SV_{DD}	---
CG_SVDD2	ClockGen Core supply	G7	---	CG_SV_{DD}	---
AVDD_PLAT	Platform PLL supply	G15	---	AVDD_PLAT	---
LS_DCS_CVDD1	0.8 V LS DCS Analog Supply	F8	---	$LS_DCS_CV_{DD}$	20
LS_DCS_CVDD2	0.8 V LS DCS Analog Supply	G8	---	$LS_DCS_CV_{DD}$	20
LS_DCS_CVDD3	0.8 V LS DCS Analog Supply	G9	---	$LS_DCS_CV_{DD}$	20
LS_DCS_AVDD1	0.8 V LS DCS Analog Supply	F12	---	$LS_DCS_AV_{DD}$	20
LS_DCS_AVDD2	0.8 V LS DCS Analog Supply	G11	---	$LS_DCS_AV_{DD}$	20

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LS_DCS_AVDD3	0.8 V LS DCS Analog Supply	G12	---	LS_DCS_AV_{DD}	20
LS_DCS_AVDDH1	1.8 V LS DCS Analog Supply	F10	---	LS_DCS_AV_{DD}H	21
LS_DCS_AVDDH3	1.8 V LS DCS Analog Supply	G10	---	LS_DCS_AV_{DD}H	21
LS_DCS_AVDDH2	1.8 V LS DCS Analog Supply	F14	---	LS_DCS_AV_{DD}H	21
LS_DCS_AVDDH4	1.8 V LS DCS Analog Supply	G13	---	LS_DCS_AV_{DD}H	21
LS_DCS_AVDDH5	1.8 V LS DCS Analog Supply	H13	---	LS_DCS_AV_{DD}H	21
HS_DCS_AVDD1	1.2 V HS DCS Analog Supply	J6	---	HS_DCS_AV_{DD}	---
HS_DCS_AVDD2	1.2 V HS DCS Analog Supply	K7	---	HS_DCS_AV_{DD}	---
HS_DCS_AVDD3	1.2 V HS DCS Analog Supply	L6	---	HS_DCS_AV_{DD}	---
HS_DCS_AVDD4	1.2 V HS DCS Analog Supply	M7	---	HS_DCS_AV_{DD}	---
HS_DCS_AVDDH	1.8 V HS DCS Analog Supply	K8	---	HS_DCS_AV_{DD}H	---
RSVD_M8	Reserved	M8	---	HS_DCS_AVNN	15
TH_VDD	Thermal Monitor Unit supply	F18	---	TH_V_{DD}	---
No Connection / DEPOP / Reserved Pins					
NC_H14	No Connection	H14	---	---	12
NC_C14	No Connection	C14	---	---	12
NC_C10	No Connection	C10	---	---	12
NC_AE2	No Connection	AE2	---	---	12
NC_M2	No Connection	M2	---	---	12
NC_M1	No Connection	M1	---	---	12
NC_M5	No Connection	M5	---	---	12
NC_M4	No Connection	M4	---	---	12
DEPOP1	Depopulate BGA pin	A1	---	---	---
DEPOP2	Depopulate BGA pin	A25	---	---	---
DEPOP3	Depopulate BGA pin	AE1	---	---	---
DEPOP4	Depopulate BGA pin	AE25	---	---	---
RSVD_P5	Reserved	P5	---	---	15
RSVD_N8	Reserved	N8	---	---	15
RSVD_N7	Reserved	N7	---	-	15
RSVD_N6	Reserved	N6	---	---	15
RSVD_G17	Reserved	G17	---	---	12
RSVD_M19	Reserved	M19	---	I	15

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_V9	Reserved	V9	---	---	15
RSVD_P4	Reserved	P4	---	---	15
RSVD_N3	Reserved	N3	---	---	15
RSVD_C6	Reserved	C6	IO	-	12
RSVD_C3	Reserved	C3	O	---	12
RSVD_D4	Reserved	D4	O	---	12
RSVD_H5	Reserved	H5	O	---	12
RSVD_H4	Reserved	H4	O	---	12
RSVD_F5	Reserved	F5	O	---	12
RSVD_F4	Reserved	F4	O	---	12
RSVD_K5	Reserved	K5	O	---	12
RSVD_K4	Reserved	K4	O	---	12
RSVD_D5	Reserved	D5	O	---	12

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

4. This pin is a reset configuration pin. It has a weak internal pull-up that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an externalresistor. See Design Checklist for details.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100 Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 1.5 kΩ pull-up to respective power-supply.

12. No connection. These pins should be left floating.

14. This pins must be tied to anlog ground (AGND).

15. This pin must be tied to ground (GND).

16. This pin requires a 200 Ω pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. This pin requires an external resistor 2.5 kΩ to respective analog GND.

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
20. This pin must be tied to 0.8 V filtered supply. Refer LA1238 design checklist (AN13410) for recommended pin termination. 21. This pin must be tied to 1.8 V filtered supply. Refer LA1238 design checklist (AN13410) for recommended pin termination. 22. Common LS_DCS_VREF_P and LS_DCS_VREF_N input reference voltage pin for LS_DCS1 and LS_DCS2.					

Warning

See **"Connection Recommendations"**for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic	Symbol	Min	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3	0.88	V	
Platform PLL supply voltage	AV_{DD}_PLAT	-0.3	1.98	V	
SerDes analog PLL fast and PLL slow supply voltage	AV_{DD}_SD_PLLF AV_{DD}_SD_PLLS	-0.3	0.99	V	
SerDes core logic supply	SD_SV_{DD}	-0.3	0.99	V	
SerDes transceiver supply	SD_OV_{DD}	-0.3	1.98	V	
Clock Gen Core supply	CG_SV_{DD}	-0.3	0.99	V	
Clock Gen PLL analog supply	CG_AV_{DD}	-0.3	0.99	V	
Clock Gen transceiver supply	CG_OV_{DD}	-0.3	1.98	V	
Low-Speed ADC/DAC high analog supply	LS_DCS_AV_{DD}_H	-0.3	1.98	V	
Low-Speed ADC/DAC analog supply	LS_DCS_AV_{DD}	-0.3	0.88	V	

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic	Symbol	Min	Max Value	Unit	Notes
Low-Speed ADC/DAC analog supply	LS_DCS_CV_{DD}	-0.3	0.88	V	
High-Speed ADC/DAC analog supply	HS_DCS_AV_{DD}	-0.3	1.32	V	
High-Speed ADC/DAC high analog supply	HS_DCS_AV_{DD}_H	-0.3	1.98	V	
General I/O supply (System Control, FlexSPI, I2C1, I2C2,I2C3, SPI1, SPI2, SPI3,SPI4, SPI5, SPI6, I2C4, I2C5, I2C6, GPIO_1[0:6], GPIO_2[0:31], GPIO_3[0:31], GPIO_4[0:2], IRQ, USIM, UART1, UART2, JTAG, LLCP1, LLCP2, MODEM1 & MODEM2)	OV_{DD}	-0.3	1.98	V	
Input voltage for General I/O supply (System Control, FlexSPI, I2C1, I2C2,I2C3, SPI1, SPI2, SPI3,SPI4, SPI5, SPI6, I2C4, I2C5, I2C6, GPIO_1[0:6], GPIO_2[0:31], GPIO_3[0:31], GPIO_4[0:2], IRQ, USIM, UART1, UART2, JTAG, LLCP1, LLCP2, MODEM1 & MODEM2)	OV_{IN}	-0.3	OV_{DD} + 0.3	V	
Input voltage for HS DCS signals	HS_DCS_AV_{in}	-0.3	Vcm_max+200mV	V	
Storage temperature range	T_{STG}	-55	150	°C	

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operations at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

WARNING

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit	Note
Core and platform supply voltage	V_{DD}	0.8 -24mV	0.8	0.8 +24mV	V	1
Platform PLL supply voltage	AV_{DD}_PLAT	1.8 -90mV	1.8	1.8 +90mV	V	1

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Min	Typ	Max	Unit	Note
SerDes analog PLL fast and PLL slow supply voltage		AV_{DD}_SD_PLLF AV_{DD}_SD_PLLS	0.9 -30mV	0.9	0.9 +50mV	V	
SerDes core logic supply		SD_SV_{DD}	0.9 -30mV	0.9	0.9 +50mV		
SerDes transceiver supply		SD_OV_{DD}	1.8 -90mV	1.8	1.8 +90mV	V	
Clock Gen Core supply		CG_SV_{DD}	0.9 -27mV	0.9	0.9 +45mV	V	
Clock Gen PLL analog supply		CG_AV_{DD}	0.9 -27mV	0.9	0.9 +45mV	V	
Clock Gen transceiver supply		CG_OV_{DD}	1.8 -90mV	1.8	1.8 +90mV	V	
High-Speed ADC/ DAC analog supply	AC Supply spec	HS_DCS_AV_{DD}	1.2 -36 mV	1.2	1.2 +36 mV	V	
	DC Supply spec		1.2-18mV	1.2	1.2+18mV	V	
Low-Speed ADC/DAC analog supply		LS_DCS_AV_{DD}	0.8 -24mV	0.8	0.8 +24mV	V	
High-Speed ADC/DAC high analog supply		HS_DCS_AV_{DD}_H	1.8 -54mV	1.8	1.8 +54mV	V	
Low-Speed ADC/DAC high analog supply		LS_DCS_AV_{DD}_H	1.8 -54mV	1.8	1.8 +54mV	V	
Low-Speed ADC/DAC analog supply		LS_DCS_CV_{DD}	0.8 -24mV	0.8	0.8 +24mV	V	
General I/O supply (System Control, FlexSPI, I2C1, I2C2,I2C3, SPI1, SPI2, SPI3,SPI4, SPI5, SPI6, I2C4, I2C5, I2C6, GPIO_1[0:6], GPIO_2[0:31], GPIO_3[0:31], GPIO_4[0:2], IRQ, USIM, UART1, UART2, JTAG, LLCP1, LLCP2, MODEM1 & MODEM2)		OV_{DD}	1.8 -90mV	1.8	1.8 +90mV	V	
Input voltage for General I/O supply (System Control, FlexSPI, I2C1, I2C2,I2C3, SPI1, SPI2, SPI3,SPI4, SPI5, SPI6, I2C4, I2C5, I2C6, GPIO_1[0:6], GPIO_2[0:31], GPIO_3[0:31], GPIO_4[0:2], IRQ, USIM, UART1, UART2, JTAG, LLCP1, LLCP2, MODEM1 & MODEM2)		OV_{IN}	–	GND to OV_{DD}	–	V	
Operating temperature range		T_A , T_J	T_A= 0 (Standard) T_A= -40 (Extended)	–	T_J= 105 T_J= 105	°C	2

Notes:

1. Refer to core and platform supply voltage filtering for additional information.

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit	Note
2. SINAD is measured at completion of calibration procedure. Refer to AN13922 for IP calibration procedures and support for calibration across operating temperature range.						

Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in the Recommended operating conditions table. The input voltage threshold scales with respect to the associated I/O supply voltage. OVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

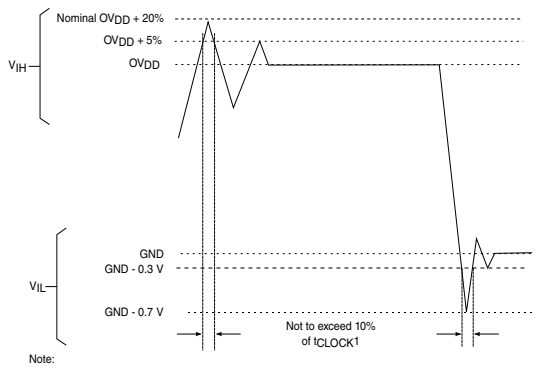


Figure 2. Overshoot/undershoot voltage for OV_{DD}

NOTE

All digital input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.1.3 Output drive capabilities

This chip provides information on the characteristics of the output driver strengths.

Table 4. Digtal Output drive capability

Driver Type	Output impedance (Ω)			Supply_ Voltage
	Minimum	Typ	Maximum	
OV_{DD} I/O signals	30	45	60	OV_{DD} = 1.8V
1. Minimum values reflect estimated numbers based on best-case processed device.				
2. Maximum values reflect estimated numbers based on worst-case processed device.				

3.2 Power sequencing

The following table provides the power-up sequence.

Table 5. Power-up sequence

Power-up sequence		
Step	Procedure	Notes
1	V_{DD}, OV_{DD}, SD_SV_{DD}, SD_OV_{DD}, CG_SV_{DD}, CG_AV_{DD}, CG_OV_{DD}, AV_{DD}_SD_PLLF, AV_{DD}_SD_PLLS, and AV_{DD}_PLAT	1, 2, 3
2	$LS_DCS_AV_{DD}$, $LS_DCS_CV_{DD}$, $LS_DCS_AV_{DD}$_H, $HS_DCS_AV_{DD}$ and $HS_DCS_AV_{DD}$_H	1, 2, 3

Notes:

1. PORESET_B should be driven, asserted, and held during this step
2. All supplies must be at their stable values within 400 ms.
3. Negate the PORESET_B input after a hold time of 32 SYSCLK cycles and after the POR configuration is valid for a minimum of 4 SYSCLK cycles.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

3.4 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 6. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/SD_SV_{DD}/SD_OV_{DD}/ V_{DD}, CG_SV_{DD}/ CG_AV_{DD}/CG_OV_{DD} and AV_{DD}_PLAT supplies.)		25	V/ms	1,2
Required ramp rate for all voltage supplies (including $LS_DCS_AV_{DD}$/$LS_DCS_CV_{DD}$/$LS_DCS_AV_{DD}$_H/$HS_DCS_AV_{DD}$ and $HS_DCS_AV_{DD}$_H supplies.)		18	V/ms	1,2

Notes:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Recommended Operating Conditions).

3.5 Power characteristics

This table provides the thermal VDD power at 85° C.

Table 7. Thermal VDD power at 85° C

e200 frequency (MHz)	Platform frequency (MHz)	VSPA frequency (MHz)	VDD (V)	Power (W)[1] LA1216, LA1218	Power (W)[2] LA1236, LA1238
614.4	614.4	614.4	0.8	7.0	7.3

Notes:

1. Thermal power assumes activity factor of 60% on all e200 cores and FFT running activity factor of 60% on all VSPA cores.

2. Thermal power assumes activity factor of 60% on all e200 cores and FFT running activity factor of 60% on all VSPA cores and and LDPC encoder/decoder running activity factor of 60% on FECA.

3.6 Input clock

3.6.1 Differential system clock (SYSCLK_P/SYSCLK_N) timing specifications

The differential system requires an on-board oscillator to provide reference clock input to SYSCLK_P/SYSCLK_N.

The SYSCLK_P/SYSCLK_N input pair requires an input clock frequency of 122.88 MHz or 125 MHz.

This section provides the differential system clock DC and AC timing specifications.

3.6.1.1 Differential system clock DC electrical characteristics

For DC electrical characteristics, see table below.

Table 8. Differential SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single ended input voltage swing	VIN_CLK_SINGLE	150	-	800	mV	
Input differential peak to peak	VIN_CLK_DIFF	300	-	1600	mV	
Common Mode Voltage Range (external DC-Coupled connection)	V_{CM}	100	-	400	mV	2
Minimum Input Voltage (external DC-Coupled connection)	V_{MIN}	0	-	-	mV	3
Maximum Input Voltage (external DC-Coupled connection)	V_{MAX}	-	-	800	mV	

Table continues on the next page...

Table 8. Differential SYSCLK DC electrical characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input differential termination	RDIFF	80		120	Ω	
Single-ended termination impedance	ZTERM	40	-	60	Ω	

Note:

1. The input differential termination is internal to the device see Figure 3.
2. In AC coupled connection scheme the Vcm will be 0 V.
3. In AC coupled connection scheme the Vmin should not go below -0.3 V.

This figure shows a receiver reference diagram of the differential system clock.

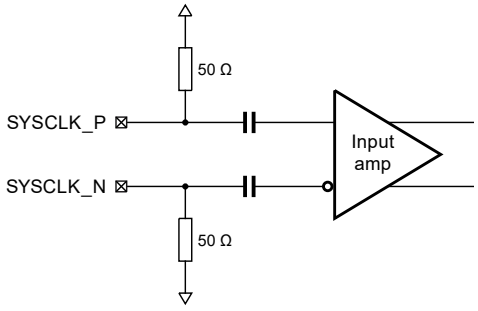


Figure 3. SYSCLK_P/SYSCLK_N receiver

For external DC-coupled connection, the maximum average current requirement sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV.

The figure below shows the reference clock input requirement for DC-coupled connection scheme.

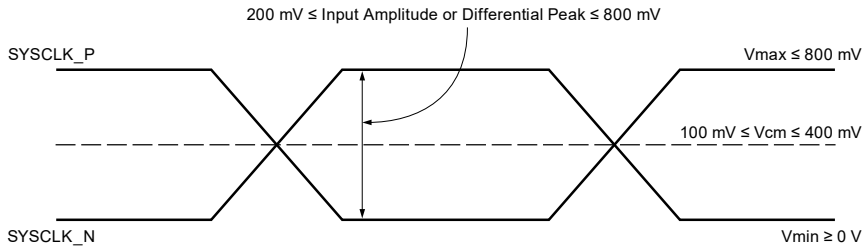


Figure 4. Differential reference clock input DC requirements (external DC-coupled)

For external AC-coupled connection, there is no common mode voltage requirement for SYSCLK_P and SYSCLK_N.

The figure below shows the reference clock input requirement for AC-coupled connection scheme.

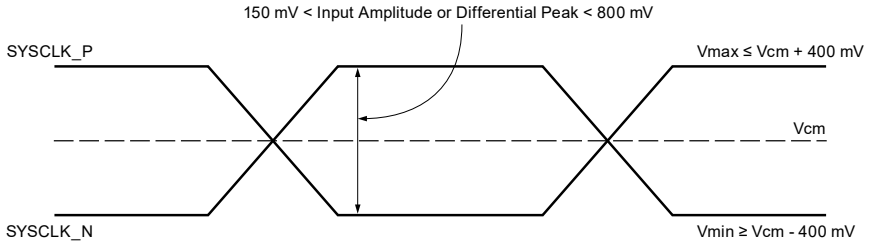


Figure 5. Differential reference clock input DC requirements (external AC-coupled)

3.6.1.2 Differential system clock AC timing specifications

For AC timing specifications, see below.

Table 9. Input Differential SYSCLK AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency	f_{SYSCLK}	-	122.88	-	MHz	
Reference clock frequency offset	F_{REF_OFFSET}	-50	-	50	ppm	
Reference clock RMS jitter						
Slew rate	T_{slew}	0.5	-	4	V/ns	2
Duty Cycle	DC	45	-	55	%	

Note:

1. At recommended operating conditions, see Recommended Operating Conditions.
2. Slew rate measured at 0.35 x V swing to 0.65 x V swing.
3. The integration range from 12 K - 20 MHz

3.7 Reset initialization timing specifications

This table provides the RESET initialization timing specifications.

Table 10. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1.0	-	ms	1
Required assertion time of PORESET_B after stable SYSCLK	1.0	-	µs	2
Required input assertion time of HRESET_B	32.0	-	SYSCLKs	2, 3

Table continues on the next page...

Table 10. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum rise/fall time of HRESET_B	-	10.0	SYSCLK	5
Maximum rise/fall time of PORESET_B	-	1	SYSCLK	4, 6
Input setup time for POR configs with respect to negation of PORESET_B	4.0	-	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2.0	-	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5.0	SYSCLKs	2

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

2. The differential SYSCLK is the primary clock input for the chip.

3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.

4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

5. For HRESET_B the rise/fall time should not exceed 10 SYSCLKs. Rise time refers to signal transitions from 20% to 70% of OV_{DD}. Fall time refers to transitions from 70% to 20% of OV_{DD}.

6. For PORESET_B the rise/fall time should not exceed 1 SYSCLK. Rise time refers to signal transitions from 20% to 70% of OV_{DD}. Fall time refers to transitions from 70% to 20% of OV_{DD}.

This table provides the phase-locked loop (PLL) lock times.

Table 11. PLL lock time

Parameter	Min	Max	Unit
PLL lock times (platform)	-	60.0	µs

3.8 General purpose input/output (GPIO)

3.8.1 GPIO DC electrical characteristics

Table 12. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2

Table continues on the next page...

Table 12. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD}= min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD},= min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.8.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 13. GPIO AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	

The figure below provides the AC test load for the GPIO.

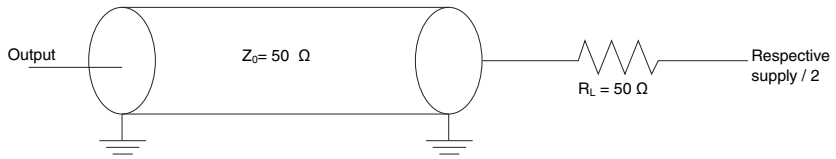


Figure 6. GPIO AC test load

3.9 Universal asynchronous receiver/transmitter (UART)

3.9.1 UART DC electrical characteristics

This table provides the DC electrical characteristics for the UART interface.

Table 14. UART DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2

Table continues on the next page...

Table 14. UART DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.9.2 UART AC timing specifications

This table provides the AC timing specifications for the UART interface.

Table 15. UART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Baud rate	baud	f_{PLAT}/(4 x 1,048,576)	f_{PLAT}/(4 x 16)	baud	1, 2, 3

1. f_{PLAT} refers to the internal platform clock.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3. The actual attainable transfer rate is limited by the latency of interrupt processing.

3.10 Data converter subsystem (DCS) specifications

3.10.1 High-Speed DCS electrical characteristics

The High Speed DCS subsystem consists of two IQ ADC blocks. For correct operation of IQ ADC and IQ DAC blocks application must use HS-DCS firmware version 2.21.2 (included with BSP 2.4 released in Jun-2023) or the later revisions of FW when available. HS-DCS IQ ADC and IQ DAC blocks might not fully meet electrical specifications if used with earlier version of HS-DCS FW. All blocks support sampling rate of 1966.08Msps or 983.04Msps. For electrical specification of IQ_ADC, refer Table 16

This table provides the electrical characteristics for the High-Speed ADC interface.

Table 16. IQ_ADC Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Resolution		ADC_{NOB}	-	10	-	Bits	
Conversion rate		F_S	-	1966.08 or 983.04	-	Msps	

Table continues on the next page...

Table 16. IQ_ADC Characteristics (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Differential Full-Scale Input range		-	-	0.7	-	V_{PP_diff}	1
Input impedance		-	-	100	-	Ω	1
Input common mode voltage		V_{CMIN}	0.4	0.45	0.55	V	1
Signal-to-niose and distortion ratio-SINAD	F_S=1966.08Msps, F_{IN}=700MHz, A_{IN}=-1dBFS	SINAD	-	44.5	-	dB_{FS}	2,4
	F_S=983.04Msps, F_{IN}=400MHz, A_{IN}=-1dBFS	SINAD	-	44.5	-	dB_{FS}	3,4
Signal-to-niose and distortion ratio-SINAD	F_S=1966.08Msps, F_{IN}=700MHz, A_{IN}=-9dBFS	SINAD	44	46	-	dB_{FS}	2,4
	F_S=983.04Msps, F_{IN}=400MHz, A_{IN}=-9dBFS	SINAD	44	46	-	dB_{FS}	3,4

Note:

1. Specs are guaranteed by design through simulation, characterization and/or functional testing.
2. Noise and distortion integrated range is 10KHz to 700MHz.
3. Noise and distortion integrated range is 10KHz to 400MHz.
4. SINAD specification is measured at completion of calibration procedure. Refer to AN13922 for HS-ADC calibration procedure and support for calibration across operating temperature range.

3.10.2 Low-Speed DCS electrical characteristics

The DCS block is comprised of two Low Speed DCS subsystems. Each Low Speed DCS Subsystem consists of four IQ ADC and four IQ DAC blocks. DACs support Sampling clock upto 491.52 Msps and ADCs support sampling clock upto 245.76 Msps. For electrical specification of IQ_ADC and IQ_DAC, refer Table 17 and Table 18

Table 17. IQ_ADC Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Resolution	-	ADC_{NOB}	-	12	-	Bits	
Differential input signal range	1.2*(vrefp-vrefn)/0.8	VFSR	-	1.2	-	$V_{pp\text{-}diff}$	

Table continues on the next page...

Table 17. IQ_ADC Characteristics (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Input Common Mode Voltage	(vrefp+vrefn)/2±0.05	V_{CMIN}	0.35	0.4	0.45	V	1
Signal-to-noise and distortion ratio-SINAD	F_S=245.76Msps, F_{IN}=100MHz, A_{IN}=-1dBFS	SINAD	55	-	-	dB	2
	F_S=122.88Msps, F_{IN}=50MHz, A_{IN}=-1dBFS	SINAD	55	-	-	dB	3
	F_S=61.44Msps, F_{IN}=15MHz, A_{IN}=-1dBFS	SINAD	55	-	-	dB	4
Gain mismatch between IQ channels	-			+/-0.1	+/-0.2	dBc	1
Phase mismatch between IQ channels	-			+/-0.2	+/-0.5	deg	1

Note:

1. Specs are guaranteed by design through simulation, characterization and/or functional testing.
2. Noise and distortion integrated range is 10KHz to 100MHz.
3. Noise and distortion integrated range is 10KHz to 50MHz.
4. Noise and distortion integrated range is 10KHz to 15MHz.

Table 18. IQ_DAC characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Resolution		DAC_{NOB}	-	12	-	Bits	
Phase mismatch			-	±0.3	-	Degrees	1
Signal-to-noise and distortion ratio-SINAD	F_s=491.52Msps, F_{OUT}=100MHz, A_{OUT}=-1dBFS, Gain=15 (0x0F)	SINAD	55	-	-	dB	2
Absolute Gain Error			-	±1	-	dB	1
Channel to Channel gain Mismatch			-	±0.2	-	dB	1
Output Full Scale Current		Ifs	0.5	2.5	5	mA	1

Table continues on the next page...

Table 18. IQ_DAC characteristics (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Output compliance range			-	-	0.85	Volts	1

Note:

1. Specs are guaranteed by design through simulation, characterization and/or functional testing.
2. Noise and distortion integrated range is 10KHz to 100MHz.

3.11 Universal subscriber identity module (USIM)

The USIM module interface consist of a total of five pins. Only “Internal One Wire” interface mode is supported. In this mode, the Rx input of the USIM IP is connected to the TX output of the USIM, which is internal to the device. Only one bidirectional signal (Rx/Tx) is routed to the device pin, which is connected to the external SIM card.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a output clock (SIM_CLK) for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the Rx/Tx pins; however, the SIM module can work with CLK equal to 16 times the data rate on Rx/Tx pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card will be used by the SIM card to recover the clock from the data much like a standard UART. All five pins of SIM module are asynchronous to each other.

There are no required timing relationships between the pads in normal mode, The SIM card is initiated by the interface device, whereupon the SIM card will send a response with an Answer to Reset. Although the SIM interface has no specific requirement, the ISO-7816 specifies reset and power down sequences. For detailed information, see ISO-7816.

3.11.1 USIM DC electrical characteristics

This table provides the DC electrical characteristics for the USIM interface.

Table 19. USIM DC electrical characteristics (OV_{DD} = 1.8V) [1]

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 x OV_{DD}	—	V	2
Input low voltage	V_{IL}	—	—	0.25 x OV_{DD}	V	2
Output high voltage	V_{OH}	I_{OH} = –100 uA at OV_{DD}min	0.75 x OV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 uA at OV_{DD}min	—	0.125 x OV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	OV_{DD} - 0.2	—	V	4
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	4
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	3

1. For recommended operating conditions, see Recommended Operating Conditions.

Table continues on the next page...

Table 19. USIM DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Note
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.						
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.						
4. Open drain mode for SIM cards only.						

3.11.2 USIM AC Timing Requirements

Following table provides the timing requirements for the USIM interface.

Table 20. USIM AC timing specification, high drive strength

Parameter	ID	Symbol	Min	Max	Unit	Note
USIM clock frequency (SIM_CLK)	S11	S_{freq}	1	5	MHz	1
USIM clock rise time (SIM_CLK)	S12	S_{rise}	—	0.09X(1/S_{freq})	ns	2
USIM clock fall time (SIM_CLK)	S13	S_{fall}	—	0.09*X(1/S_{freq})	ns	2
USIM input transition time (SIM_TRXD, SIM_PD)	—	S_{trans}	10	25	ns	-
USIM I/O rise time / fall time (SIM_TRXD)	—	Tr/Tf	—	1	µs	3
USIM RST rise time / fall time (SIM_RST_B)	—	Tr/Tf	—	1	µs	4

Note:

1. 50% duty cycle clock
2. With C = 50 pF
3. With CIN = 30 pF, COUT = 30 pF
4. With CIN = 30 pF

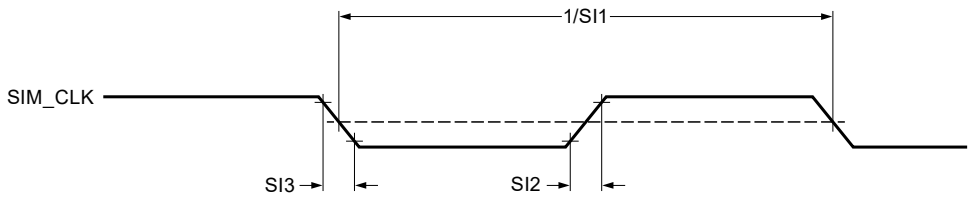


Figure 7. USIM clock timing diagram

3.11.3 USIM reset sequence

3.11.3.1 SIM cards with internal reset

The sequence of reset for this kind of SIM cards is as follows. See figure Figure 8 Internal-reset card sequence.

- After power up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, Rx must be high
- The card must send a response on Rx acknowledging the reset between 400 and 40000 clock cycles after T0

Table 21. Parameters of reset sequence for card with internal reset

Parameter	ID	Symbol	Min	Max	Unit	Note
SIM clock to SIM TX data H	SI7	$S_{clk2dat}$	—	200	SIM_CLK clock cycle	
SIM clock to SIM get ATR dat	SI8	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle	
Note:						

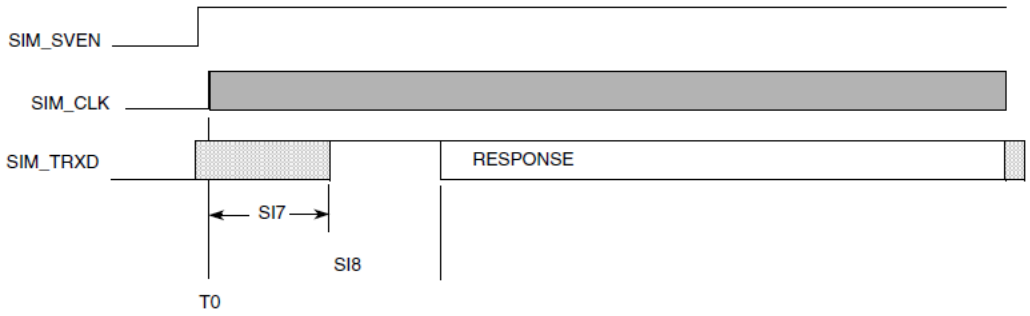


Figure 8. Internal-reset card reset sequence

3.11.3.2 SIM cards with active-low reset

The sequence of reset for this kind of card is as follows see Figure 9

- After powering up, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, SIM_TRXD must be high
- SIM_RST must remain Low for at least 400 clock cycles after T0 (no response is to be received on Rx during those 400 clock cycles)
- SIM_RST is set High (time T1)
- SIM_RST must remain High for at least 40000 clock cycles after T1 and a response must be received on SIM_TRXD between 400 and 40000 clock cycles after T1

Table 22. Parameters of reset sequence for active-low reset card

Parameter	ID	Symbol	Min	Max	Unit	Note
SIM clock to SIM TX data H	SI9	$S_{clk2dat}$	—	200	SIM_CLK clock cycle	

Table continues on the next page...

Table 22. Parameters of reset sequence for active-low reset card (continued)

Parameter	ID	Symbol	Min	Max	Unit	Note
SIM reset rising to SIM TX data low	SI10	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle	
SIM clock to SIM reset signals	SI11	$S_{clk2rst}$	400	—	SIM_CLK clock cycle	
Note:						

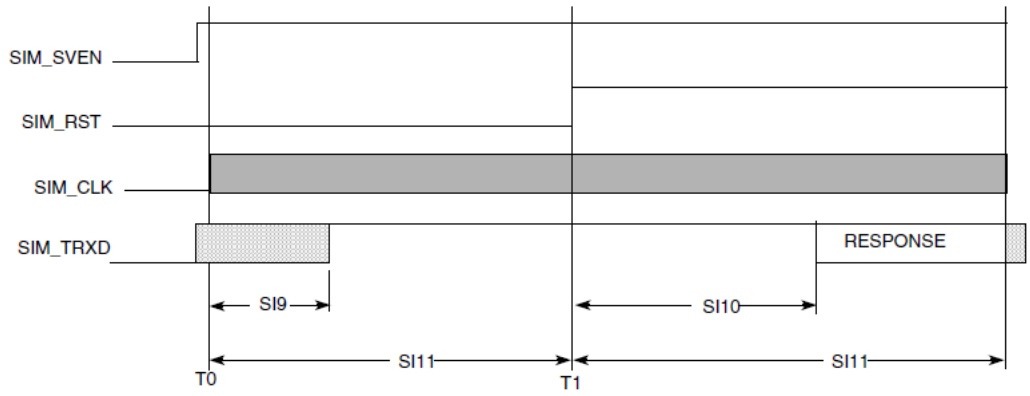


Figure 9. Active-low reset card reset sequence

3.11.3.3 USIM power down sequence

Power down sequence for SIM interface is as follows:

- SIM_PD port detects the removal of the SIM card
- SIM_RST goes low
- SIM_CLK goes low
- SIM_TRXD goes low
- SIM_SVEN goes low

Each of these steps is done in one CKIL period (typically 32 KHz). Power down is initiated by detection of a SIM card removal or is launched by the processor. See Figure 10 and Table 23 with FCKIL = CKIL frequency value.

Table 23. Timing requirements for power down sequence

Parameter	ID	Symbol	Min	Max	Unit	Note
USIM reset to USIM clock stop	SI12	$S_{rst2clk}$	0.9 X 1/Fckil	1.1 X $1/F_{CKIL}$	ns	
USIM reset to USIM Tx data low	SI13	$S_{rst2dat}$	1.8 X 1/Fckil	2.2 X $1/F_{CKIL}$	ns	

Table continues on the next page...

Table 23. Timing requirements for power down sequence (continued)

Parameter	ID	Symbol	Min	Max	Unit	Note
USIM reset to USIM voltage enable low	SI14	$S_{rst2ven}$	2.7 X 1/Fckil	3.3 X $1/F_{CKIL}$	ns	
USIM presence detect to USIM reset low	SI15	S_{pd2rst}	0.9 X 1/Fckil	1.1 X $1/F_{CKIL}$	ns	
Note						

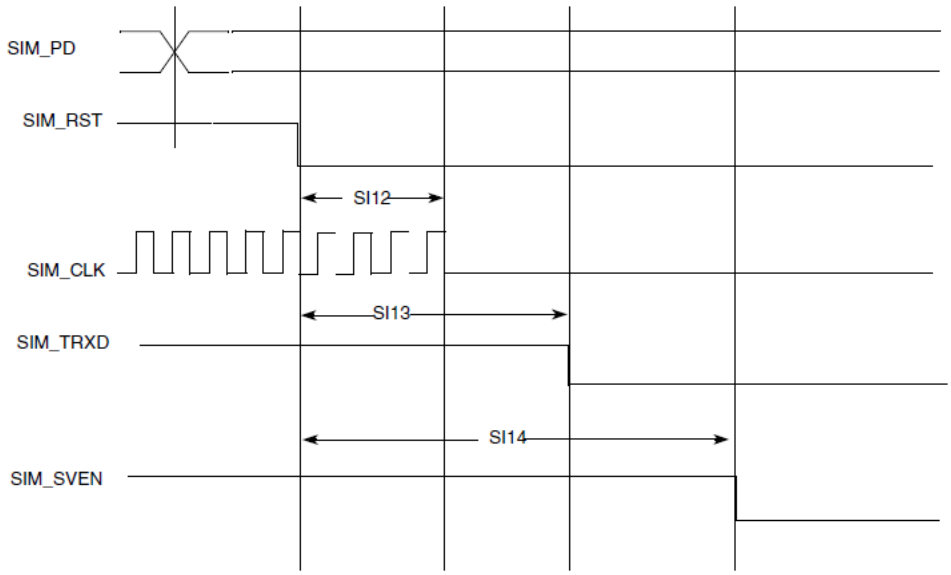


Figure 10. SmartCard interface power down AC timing

3.12 Lightweight LVDS communication protocol interface (LLCP)

This section describes the DC and AC electrical specifications for the LLCP interface.

3.12.1 LLCP DC/AC electrical characteristics

This table provides the DC and AC electrical characteristics for the LLCP interface.

Table 24. LLCP DC/AC electrical characteristics (OV_{DD}= 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Output differential voltage	V_{OD}	200	600	mV	2, 3
Output common mode voltage	V_{OCM}	OV_{DD}/2-20	OV_{DD}/2+20	mV	2, 3
Input differential voltage	V_{ID}	200	600	mV	4
Input common mode voltage	V_{ICM}	0.2	OV_{DD}min -0.2	V	

Table continues on the next page...

Table 24. LLCP DC/AC electrical characteristics (OV_{DD}= 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Receive rate			307.2	Mbps	
Transmit rate			614.4	Mbps	

1. For recommended operating conditions, see Recommended Operating Conditions.

2. |Vpadp-Vpadn|

3. Test condition: Rload=100 Ohm between padp and padn

4. Internal Termination is enabled.

3.13 I2C

3.13.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 25. I^2C DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Output low voltage (OV_{DD} = min, IOL = 2 mA, OV_{DD} ≤ 2V)	V_{OL}	0.0	0.36	V	-
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	3
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} (min) and 0.9 x OV_{DD} (max))	I_I	-	±50	μA	4
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} or $OV1_{IN}$ values found in Recommended Operating Conditions.

3. See the chip reference manual for information about the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if the supply is switched off.

3.13.2 I2C AC timing specifications

This table provides the AC timing specifications for the I^2C interface.

Table 26. I²C AC timing specifications [3, 4, 5]

Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Max. Frequency	f_{I2C}		100	-	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	4.7		1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	4		0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	4.7		0.6	-	µs	-
Hold time (repeated) START condition	t_{I2SXKL}	4		0.6	-	µs	-
Setup time	t_{I2DVKH}	250		100.0	-	ns	1
Input hold time	t_{I2DXKL}	0.0		0.0	-	µs	2
Master output delay time	t_{I2OVKL}		3.45		0.9	µs	3
Input setup time for STOP condition	t_{I2PVKH}	4	-	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	4.7		1.3	-	µs	-
Capacitive load for each bus line	Cb		400.0	-	400.0	pF	4

1. A Fast-mode I²C-bus device can be used in a Standard-modeI²C-bus system, but the requirement of Setup time of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line max rise time + data Setup Time = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

2. A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

3. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. Cb = Total capacitance of one bus line in pF

5. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

6. See Figure 11.

7. See Figure 12.

This figure shows the AC test load for the I²C.

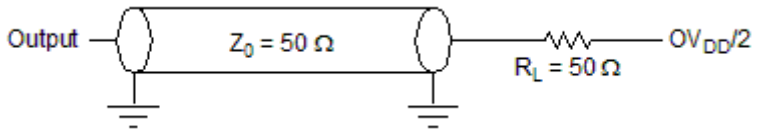


Figure 11. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

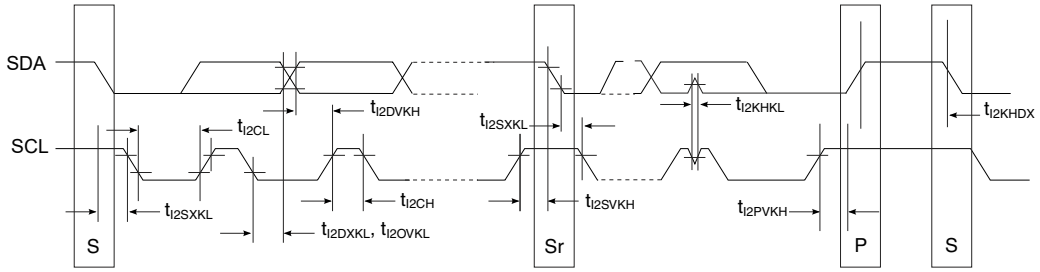


Figure 12. I²C bus AC timing diagram

3.14 JTAG

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.14.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG (IEEE 1149.1) interface.

Table 27. JTAG DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	0.2 x OV_{DD}		V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.14.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 13, Figure 14, Figure 15, and Figure 16.

Table 28. JTAG AC timing specifications [3, 4, 5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0.0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30.0	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15.0	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	1
Input setup times	t_{JTDVKH}	4.0	-	ns	-
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	15.0	ns	2
Output valid times: TDO	t_{JTKLDV}	-	10.0	ns	2
Output hold times	t_{JTKLDX}	0.0	-	ns	2

1. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

2. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

3. The symbols used for timing specifications follow these patterns: t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, tJTDXKH symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

4. See Figure 13.

5. See Figure 14.

6. See Figure 15.

7. See Figure 16.

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

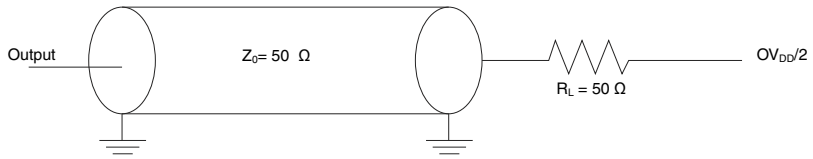


Figure 13. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

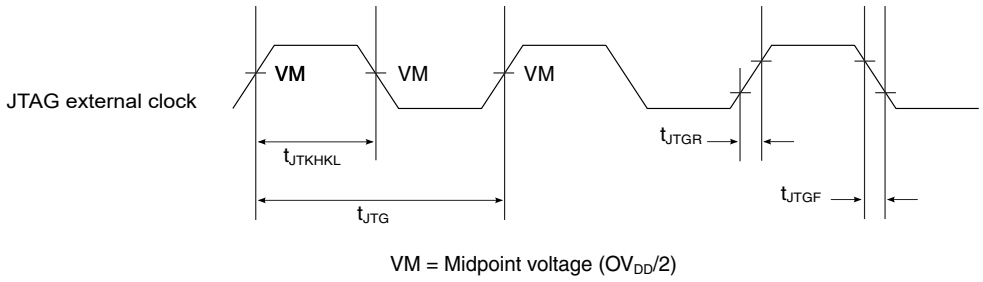


Figure 14. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

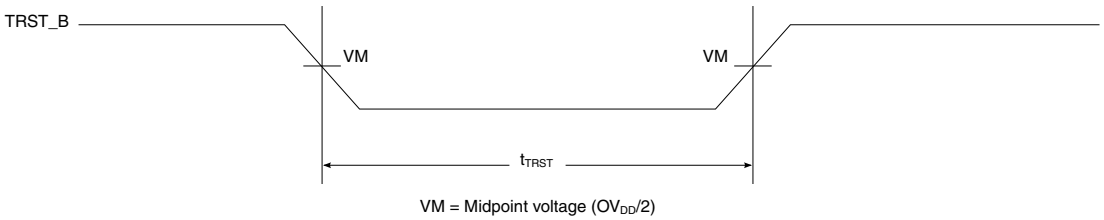


Figure 15. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

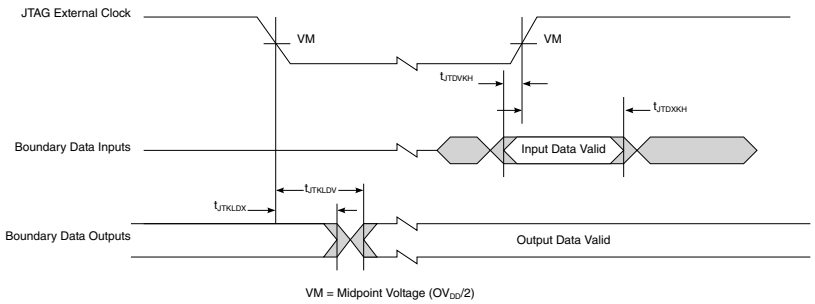


Figure 16. Boundary-scan timing diagram

3.15 Flex serial peripheral interface (FlexSPI)

3.15.1 FlexSPI DC electrical characteristics

This table provides the DC electrical characteristics for the FlexSPI interface.

Table 29. FlexSPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (0V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OH} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.15.2 FlexSPI AC timing specifications

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0 or 0x1 or 0x2

Table 30. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0 or 0x1 or 0x2 [5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	76.8 MHz	MHz	-
Clock low/high time	T_{LOW}/T_{HIGH}	46	54	%	-
CS output hold time	$t_{FSKHOX2}$	(FLSHxCR1[TCSH] * T)+6.35	-	ns	1, 8
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5) * T)+0.41	-	ns	1, 8
Setup time for incoming data	t_{FSIVKH}	5.43	-	ns	-
Hold time for incoming data	t_{FSIXKH}	1.0	-	ns	-
Output data delay	t_{FSKHOV}		3.85	ns	-
Output data hold	t_{FSKHOX}	-2.84	-	ns	-

1. Refer the FLSHxyCR1 LA1238RM for more details, y: 1 or 2

5. See Figure 17.

6. See Figure 18.

7. See Figure 19.

8. T represents the clock period.

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2

Table 31. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1, or 0x2 [4, 5, 9, 11]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	76.8 MHz	MHz	6
Clock low/high time	T_{LOW}/T_{HIGH}	46	54	%	-
CS output hold time	$t_{FSKHOX2}$	((FLSHxCR1[TCSH]+0.5)*T/2) + 6.33	-	ns	1, 10
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5)*T/2) + 0.32	-	ns	1, 10
Data Valid Window	t_{FSIDVW}	0.3	-	UI	7, 8
Output data delay	t_{FSKHOV}/ tFSKLOV	-	3.89	ns	-
Output data hold	t_{FSKHOX}/ tFSKLOX	2.92	-	ns	-

1. Refer the FLSHxyCR1 LA1238RM for more details, y: 1 or 2

4. See Figure 17.

5. See Figure 18.

7. For DDR, Unit Interval (UI) is half of period. For example, 5 ns for 100 MHz

8. See "Data Learning Feature" section in LA1238RM for details

9. See Figure 20.

10. T represents the clock period.

11. The minimum route length on the board is 0.5 inch and maximum length is 3 inches.

This figure shows the AC test load for the FlexSPI interface.

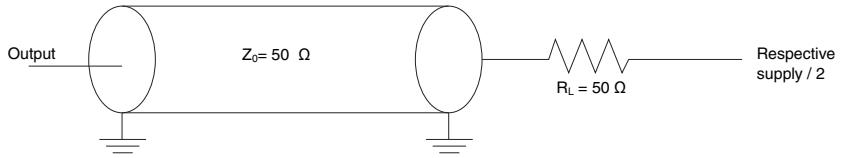


Figure 17. AC test load for FlexSPI

This figure shows the FlexSPI clock input timing diagram.

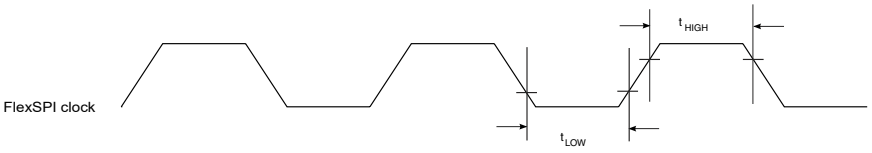


Figure 18. FlexSPI clock input timing diagram

This figure shows the FlexSPI AC timing diagram for SDR mode.

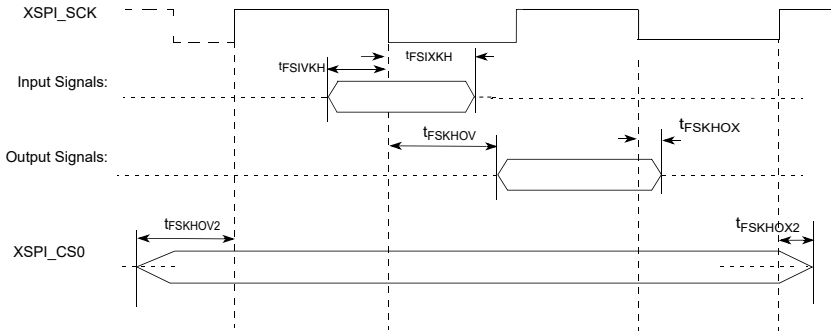


Figure 19. FlexSPI SDR mode AC timing diagram

This figure shows the FlexSPI AC timing diagram for DDR mode 1 and 2.

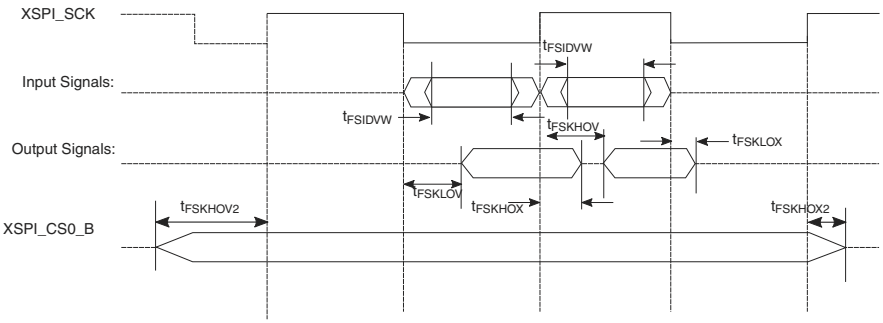


Figure 20. FlexSPI DDR mode 1 and 2 AC timing diagram

3.16 Serial peripheral interface (SPI)

3.16.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface when operating with a single master device.

Table 32. SPI DC electrical characteristics (OV_{DD}= 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85 x OV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 μA)	V_{OL}	-	0.15 x OV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.16.2 SPI AC timing specifications

This table provides the SPI timing specifications when operating with a single master device.

Table 33. SPI AC timing specifications [8, 9]

Parameter	Symbol	Min	Max	Unit	Notes
SCK cycle time	t_{SCK}	20	-	ns	
SCK clock pulse width	t_{SDC}	40.0	60.0	%	-
CS to SCK delay	t_{CSC}	tp*2 - 0.54	-	ns	2, 4, 5
After SCK delay	t_{ASC}	tp*2 - 1.15	-	ns	2, 7, 5
Data setup time for inputs	t_{NIIVKH}	9.0	-	ns	2
Data hold time for inputs	t_{NIIXKH}	0.0	-	ns	2
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	5.0	ns	2
Data hold time for outputs	t_{NIKHOX}	0.0	-	ns	2

2. Master mode

4. Refer the CTARx register in Layerscape Access LA1238RM for more details. The tCSC = tp*(Delay Scaler Value)*CTARx[PCSSCK] + n1, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tCSC = tp*4*3+n1 when CTARx[PCSSCK] = 0b01, CTARx[CSSCK]=0b0001, n1 = 0.54

5. tp is the input clock period for the SPI controller.

7. Refer the CTARx register in Layerscape Access LA1238RM for more details. The tASC = tp*(Delay Scaler Value)*CTARx[PASC] + n2, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tASC = tp*8*3+n2 when CTARx[PASC] = 0b01, CTARx[ASC]=0b0010, n2 = 1.15

Table continues on the next page...

Table 33. SPI AC timing specifications [8, 9] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
8. See Figure 21.					
9. See Figure 22.					

This figure shows the SPI timing master when CPHA = 0.

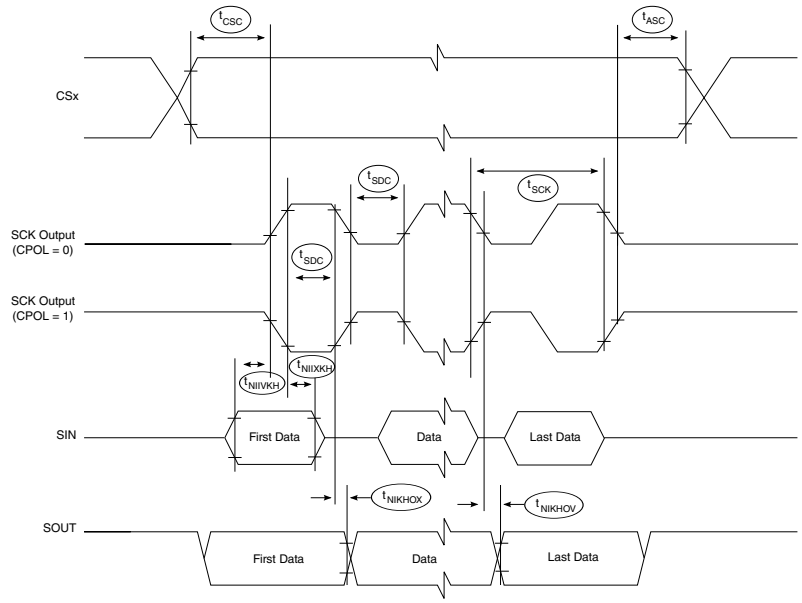


Figure 21. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

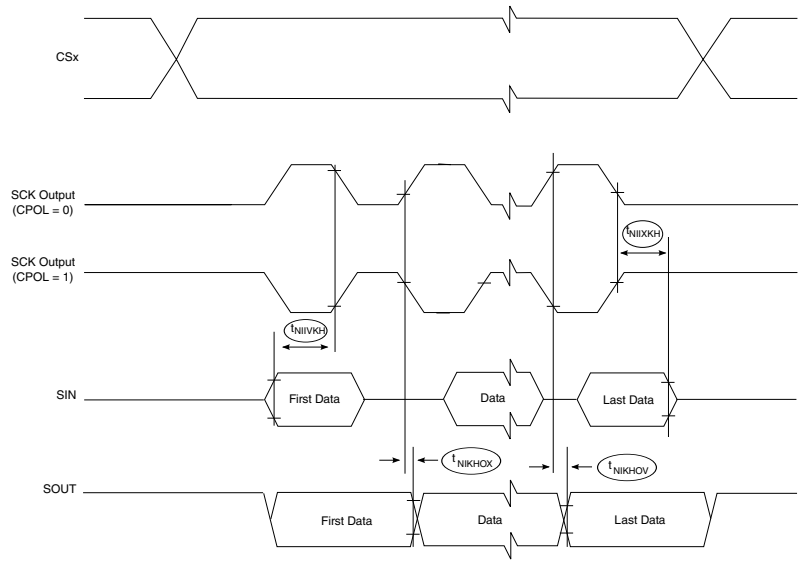


Figure 22. SPI timing master, CPHA = 1

3.17 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCIe in LA1238.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.17.1 Signal terms definitions

The SerDes uses differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. This figure shows the waveform for either a transmitter output (SD_TX_P and SD_TX_N) or a receiver input (SD_RX_P and SD_RX_N). Each signal swings between A volts and B volts where A > B.

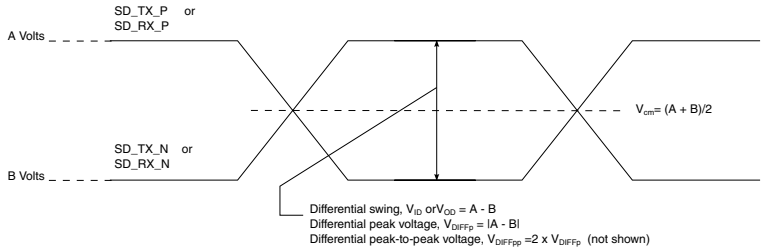


Figure 23. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing — The transmitter output signals and the receiver input signals SD_TX_P, SD_TX_N, SD_RX_P and SD_RX_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing) — The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TX_}$P - $V_{SD_TX_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing) — The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD_RX_P}$- $V_{SD_RX_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp} — The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$ — Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |V_{OD}|.

Differential Waveform — The differential waveform is constructed by subtracting the inverting signal (SD_TX_N, for example) from the non-inverting signal (SD_TX_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 27 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = ($V_{SD_TX_P}$ + $V_{SD_TX_N}$) ÷ 2 = (A + B) ÷ 2, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.17.2 SerDes reference clock

The SerDes reference clock input is applied to an internal PLL whose output creates the clock used by the SerDes lane.

The following sections describe the SerDes reference clock requirements and provide application information.

3.17.3 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clock.

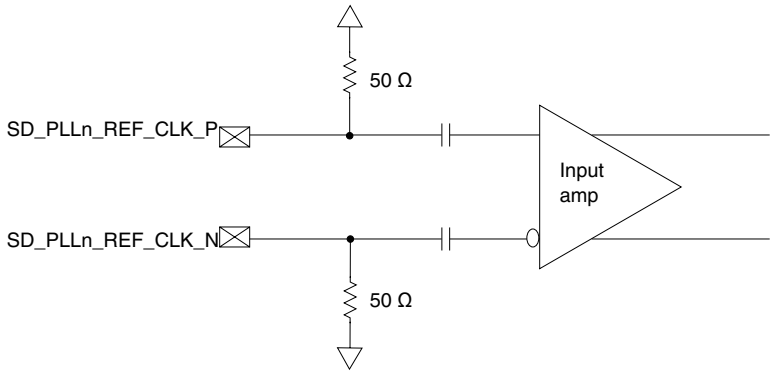


Figure 24. Receiver of SerDes reference clock

3.17.4 DC-level requirement for SerDes reference clock

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 25 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

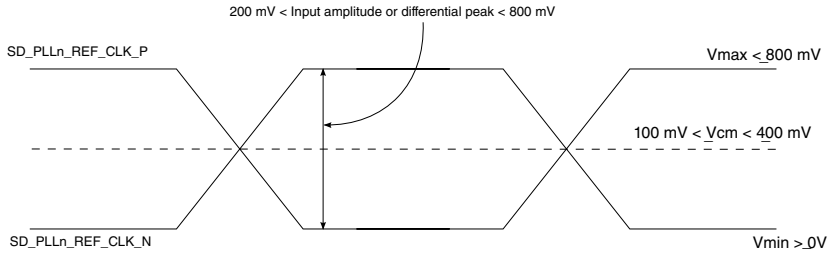


Figure 25. Differential reference clock input DC requirements (external DC-coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD_GND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SD_GND). Figure 26 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

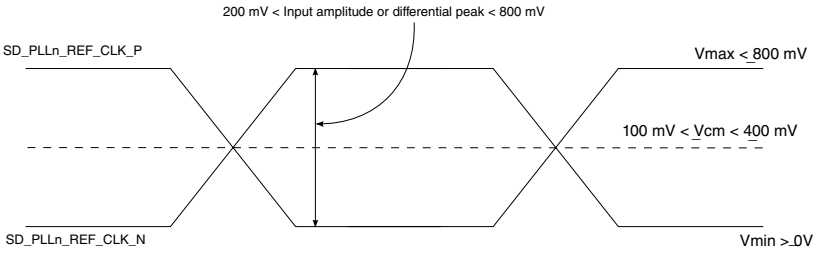


Figure 26. Differential reference clock input DC requirements (external AC-coupled)

3.17.5 SerDes reference clocks AC timing specifications

This table defines the AC requirements for SerDes reference clocks. SerDes reference clocks need to be verified by the customer's application design.

Table 34. SD_PLLn_REF_CLK_P and SD_PLLn_REF_CLK_N input clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	-
SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N clock frequency tolerance	t_{CLK_TOL}	-300	-	300	ppm	1
SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	2
2.5G SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42.0	ps P-P	3, 4

Table continues on the next page...

Table 34. SD_PLLn_REF_CLK_P and SD_PLLn_REF_CLK_N input clock requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
2.5G SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N total reference clock jitter at 10^{-6} BER	t_{CLK_TJ}	-	-	86.0	ps P-P	3, 4
PCIe 5G SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N 10 kHz to 1.5 MHz RMS jitter max	$t_{REFCLK-LF-RMS}$	-	-	3.0	ps RMS	5
PCIe 5G SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK-HF-RMS}$	-	-	3.1	ps RMS	5
PCIe 8G SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N RMS reference clock jitter	$t_{REFCLK-RMS-DC}$	-	-	1.0	ps RMS	6
SD_PLLn_REF_CLK_P/ SD_PLLn_REF_CLK_N rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	-	4.0	V/ns	8, 9
Differential input high voltage	V_{IH}	150.0	-	-	mV	2
Differential input low voltage	V_{IL}	-	-	-150.0	mV	2
Rising edge rate (SD_PLLn_REF_CLK_P) to falling edge rate (SD_PLLn_REF_CLK_N) matching	Rise-Fall matching	-	-	20.0	%	10, 11, 12

1. For PCI Express (2.5, 5, and 8 GT/s).

2. Measurement taken from differential waveform.

3. Limits from PCI Express CEM Rev 2.0.

4. For PCI Express 2.5 GT/s

5. For PCI Express 5 GT/s

6. For PCI Express 8 GT/s

8. Measured from -150 mV to +150 mV on the differential waveform (derived from SD_PLLn_REF_CLK_P minus SD_PLLn_REF_CLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.

9. See Figure 27.

10. Measurement taken from single-ended waveform.

11. Matching applies to rising edge for SD_PLLn_REF_CLK_P and falling edge rate for SD_PLLn_REF_CLK_N. It is measured using a +/- 75 mV window centered on the median cross point where SD_PLLn_REF_CLK_P rising meets SD_PLLn_REF_CLK_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_PLLn_REF_CLK_P must be compared to the fall edge rate of SD_PLLn_REF_CLK_N, the maximum allowed difference should not exceed 20% of the slowest edge rate.

12. See Figure 28.

This figure shows the differential measurement points for rise and fall time.

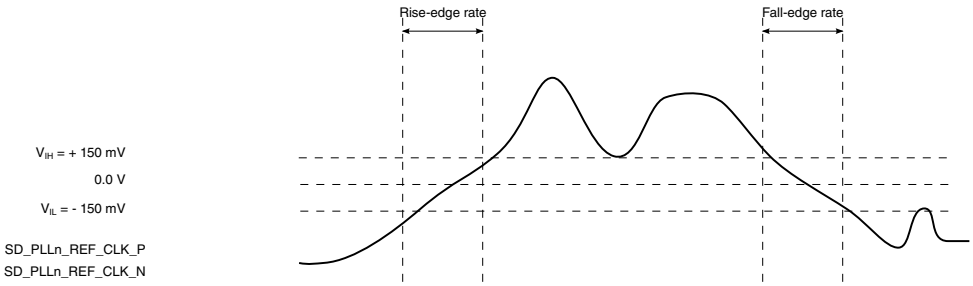


Figure 27. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

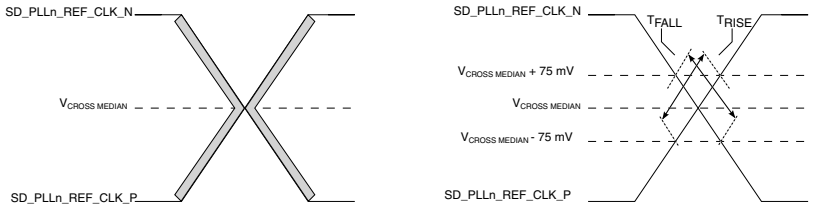


Figure 28. Single-ended measurement points for rise and fall time matching

3.18 PCI Express

3.18.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.18.2 PCI Express clocking requirements for SD_PLLF_REF_CLK and SD_PLLS_REF_CLK

SerDes SD_PLLF_REF_CLK/SD_PLLF_REF_CLK_B and SD_PLLS_REF_CLK/SD_PLLS_REF_CLK_B may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is supported on SerDes.

For more information on these specifications, see SerDes reference clock.

3.18.3 PCI Express DC electrical characteristics

This section describes the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s. This table defines the PCI Express 2.0 (2.5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 35. PCI Express 1.0 (2.5 GT/s) differential transmitter output DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFP-P}$	800.0	1000.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	3

Table continues on the next page...

Table 35. PCI Express 1.0 (2.5 GT/s) differential transmitter output DC electrical characteristics (SD_OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	5

1. For recommended operating conditions, see Recommended Operating Conditions.

2. $V_{TX_DIFFp-p} = 2 \times | V_{TX-D+} - V_{TX-D-} |$

3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

4. Transmitter DC differential mode low impedance

5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 36. PCI Express 1.0 (2.5 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	175.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. $V_{RX_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

3. Measured at the package pins with a test load of 50Ω to GND on each pin.

4. Receiver DC differential mode impedance.

5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

Table continues on the next page...

Table 36. PCI Express 1.0 (2.5 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
9. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$						

This table defines the PCI Express 2.0 (5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 37. PCI Express 2.0 (5 GT/s) differential transmitter output DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFP-P}$	800.0	1000.0	1200.0	mV	2
Low power differential peak-peak output voltage	$V_{TX-DIFFP-P-LOW}$	400.0	500.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	3
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	5

1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{TX_DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
4. Transmitter DC differential mode low impedance
5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 38. PCI Express 2.0 (5 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	120.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5

Table continues on the next page...

Table 38. PCI Express 2.0 (5 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. $V_{RX_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

3. Measured at the package pins with a test load of 50Ω to GND on each pin.

4. Receiver DC differential mode impedance.

5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

9. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

This table defines the PCI Express 3.0 (8 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 39. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics (SD_OV$_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800.0	-	1300.0	mVp-p	2
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400.0	-	1300.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	3
Minimum swing during EIEOS for full swing	$Z_{TX-EIEOS-FS}$	250.0	-	-	mVp-p	4

Table continues on the next page...

Table 39. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics (SD_OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Minimum swing during EIEOS for reduced swing	$Z_{TX-EIEOS-RS}$	232.0	-	-	mVp-p	4
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	5
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	6

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

4. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

5. Transmitter DC differential mode low impedance

6. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 40. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	2, 3
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	4, 5, 3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	6, 7
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	8, 5
Generator launch voltage	$V_{RX-LAUNCH-8G}$	-	800.0	-	mV	9
Eye height (-20dB channel)	$V_{RX-SV-8G}$	25.0	-	-	mV	10
Eye height (-12dB channel)	$V_{RX-SV-8G}$	50.0	-	-	mV	10

Table continues on the next page...

Table 40. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Eye height (-3dB channel)	$V_{RX-SV-8G}$	200.0	-	-	mV	10

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Receiver DC differential mode impedance.

3. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

4. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

5. Measured at the package pins with a test load of 50Ω to GND on each pin.

6. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

7. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

8. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

9. Measured at TP1 per PCI Express base specification Rev 3.0.

10. Measured at TP2 per PCI Express base specification Rev 3.0. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. In the parameter names, "SV" refers to stressed voltage. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2.

3.18.4 PCI Express AC timing specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.This table defines the PCI Express 1.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 41. PCI Express 1.0 (2.5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	6, 3, 4, 5
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.

3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.

Table continues on the next page...

Table 41. PCI Express 1.0 (2.5 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 5. See Figure 30. 6. Jiiter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. 7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. 8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.						

This table defines the AC timing specifications for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timingspecifications do not include RefClk jitter.

Table 42. PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	3, 4, 5
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. 2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE} = 0.6 UI. 3. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. 4. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram. 5. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 43. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	6
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 -T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.

3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.

4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

5. See Figure 30.

6. Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps.

7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the AC timing specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 44. PCI Express 2.0 (5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	-
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.3	UI	-

1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 45. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1
AC coupling capacitor	C_{TX}	176.0	-	265.0	nF	2, 3
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12.0	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24.0	ps p-p	4, 5
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10.0	ps p-p	4, 5
Data-dependent jitter	T_{TX-DDJ}	-	-	18.0	ps p-p	4

1. Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. Measured with optimized preset value after de-embedding to transmitter pin.

5. PWJ parameters shall be measured after data-dependent jitter (DDJ) separation.

This table defines the AC timing specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timingspecifications do not include RefClk jitter.

Table 46. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications [5]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1, 2
Eye width at TP2P	$T_{RX-SV-8G}$	0.3	-	0.35	UI	2
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14.0	-	-	mV	3
Sinusoidal jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	-	-	0.1	UI p-p	4, 5

Table continues on the next page...

Table 46. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications [5] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Random jitter	$T_{RX-SV-RJ-8G}$	-	-	2.0	ps RMS	6, 5

1. Each UI is 125 ps ± 300 ppm. UI does not account for spreadspectrum clock dictated variations.

2. $T_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

3. Frequency = 2.1GHz. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.

4. Fixed at 100 MHz. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency.

5. See Figure 29.

6. Random jitter spectrally flat before filtering. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.

This figure shows the swept sinusoidal jitter mask.

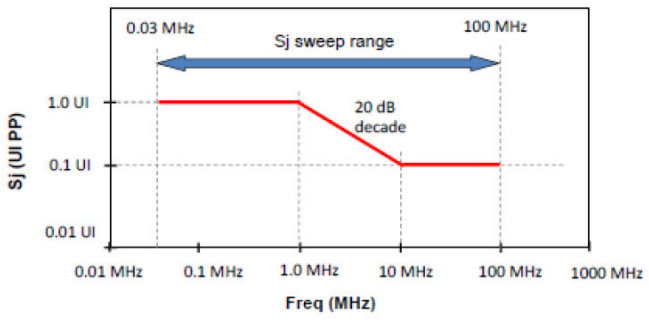


Figure 29. Swept sinusoidal jitter mask

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure. Note that the allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and Dpackage pins.

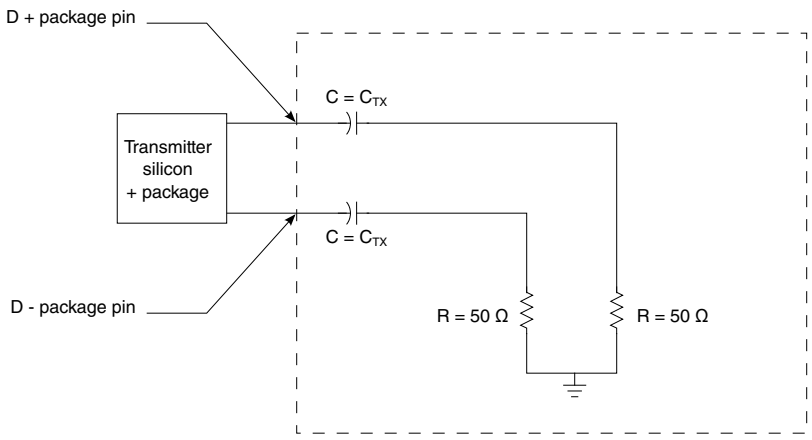


Figure 30. Test and measurement load

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, VSPA, SerDes, FlexSPI, SPI and I2c.

Table 47. Processor, platform, clocking ranges

Characteristics	Minimum Frequency	Maximum Frequency	Unit	Note
e200z7 Core	-	614.4	MHz	1
Platform		614.4	MHz	
VSPA Core	491.52	614.4	MHz	1
SerDes	-	100/125	MHz	
FlexSPI	-	76.8	MHz	1, 2
SPI	-	50	MHz	1
USIM (SIM_CLK)	1	5	MHz	
DUART	Max Baudrate = (1/16) x (Platform_clk/4)		KHz	1
I2C	-Up to 100 Kbps in standard mode -Up to 400 kbps in fast mode		Kbps	

Notes:

1. Clock source is SYSCLK_P/SYSCLK_N is 122.88MHz. The Min/Max frequency depend on PLL parameter setup.
2. FlexSPI DDR & SDR mode.

4.2 ADC Input and DAC Output Signals

The data converter analog input and output signals should be routed as differential lines on the PCB. Attention should be paid to good symmetry and length matching. Sharp turns should be avoided but if that is not possible the turns should be rounded or beveled. To avoid coupling with other high speed signals or clocks proper separation or grounded shields should be used. Solid ground plane should be maintained underneath the traces. If filtering is included on the PCB between the data converter and the RX or TX device, symmetrical PCB layout should be used for the filter components.

The external DAC load resistors can act as termination for the PCB trace and should be placed close to the device. The transmission line impedance should be designed based on the chosen DAC load resistor value.

4.3 Power supply design

For additional details on the power supply design, see the applicable chip design checklist.

4.3.1 Core and platform supply voltage filtering

The VDD supply is normally derived from a linear regulator or switching power supply that can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure a quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than + 24 mV (negative transient undershoot should comply with specification of -24 mV) and slew rate of 7 A/us for current steps up to 50% to 100% rise and 100% to50% fall of defined maximum current.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Refer to Design Check List Application Note AN13410 for further decoupling recommendations.

5 Thermal

This table shows the thermal rating for the chip.

Table 48. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to case thermal resistance	JED51-9, 1s	$R_{\Theta JC}$	0.46	°C/W	1,2

Notes:

1. Junction-to-Case thermal resistance is determined using an isothermal cold plate heat extraction through the top side of the package. Case temperature is the surface temperature at the package lid’s geometric centre.
2. Thermal test board meets JEDEC specification for this package (JESD51-9).

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature Monitoring

The chip has two options for temperature monitoring capability. One is Thermal Monitoring Unit (TMU) and the second option is thermal diode. The TMU module is implemented on the chip and does not require external temperature monitoring device.

The TMU Temperature reading accuracy is within ±5°C. For detail on TMU implementations refer to device reference manual. The thermal diode option can be used to monitor its temperature by using an external temperature monitoring device (such as NXP SA56004x).

The following are the specifications of the chip's on-board temperature diodes:

Operating range: 14 - 240 µA

The ideality factor over temperature range 85ºC to 105ºC, n = 1.022 ± 0.003, with approximate error +/- 1.5 ºC and approximate error under +/- 3 ºC for temperature range 0 ºC to 85ºC.

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 31. The heat sink should be attached to the printed-circuit board with the spring force centered over the lid. This spring force should not exceed 10 pounds force (45 Newton).

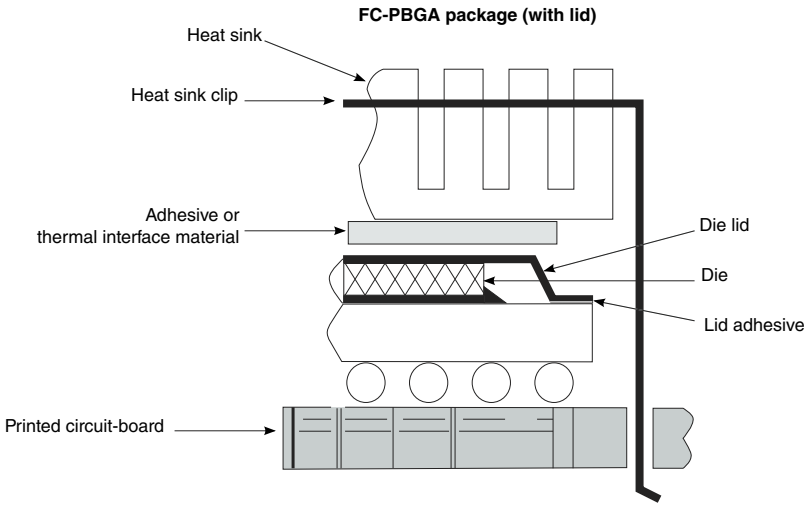


Figure 31. Package exploded, cross-sectional view-FC-PBGA (w/ Lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 31).

The system board designer can choose among several types of commercially available thermal interface materials.

6 Package information

6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list.

- Package outline: 21 mm x 21 mm, lidded FCBGA
- Interconnects: 621 I/O
- Ball Pitch: 0.8 mm
- Ball Diameter (typical): 0.4 mm
- Solder Balls Composition: 96.5% Sn, 3.5% Ag
- Module height: 2.52 mm (maximum)
- Case outline number: 98ASA01492D The Package Outline Drawing document SOT2037-1 is available on NXP.com

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

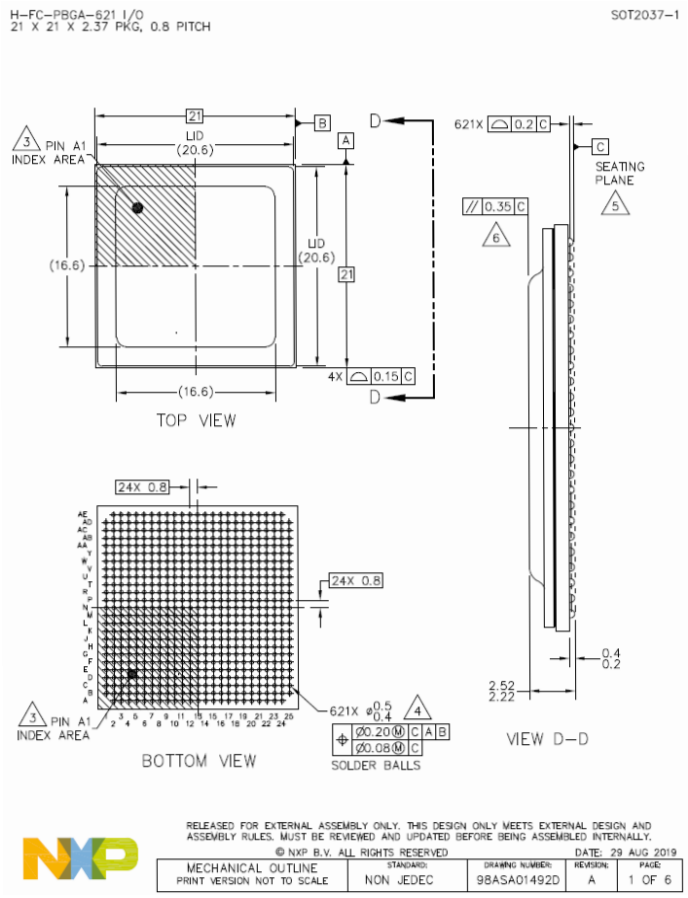


Figure 32. Mechanical dimensions of the FC-PBGA

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
7. LID OVERHANG ON SUBSTRATE NOT ALLOWED.

7 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

7.1 Part numbering nomenclature

This figure provides the NXP Layerscape platform part numbering nomenclature.

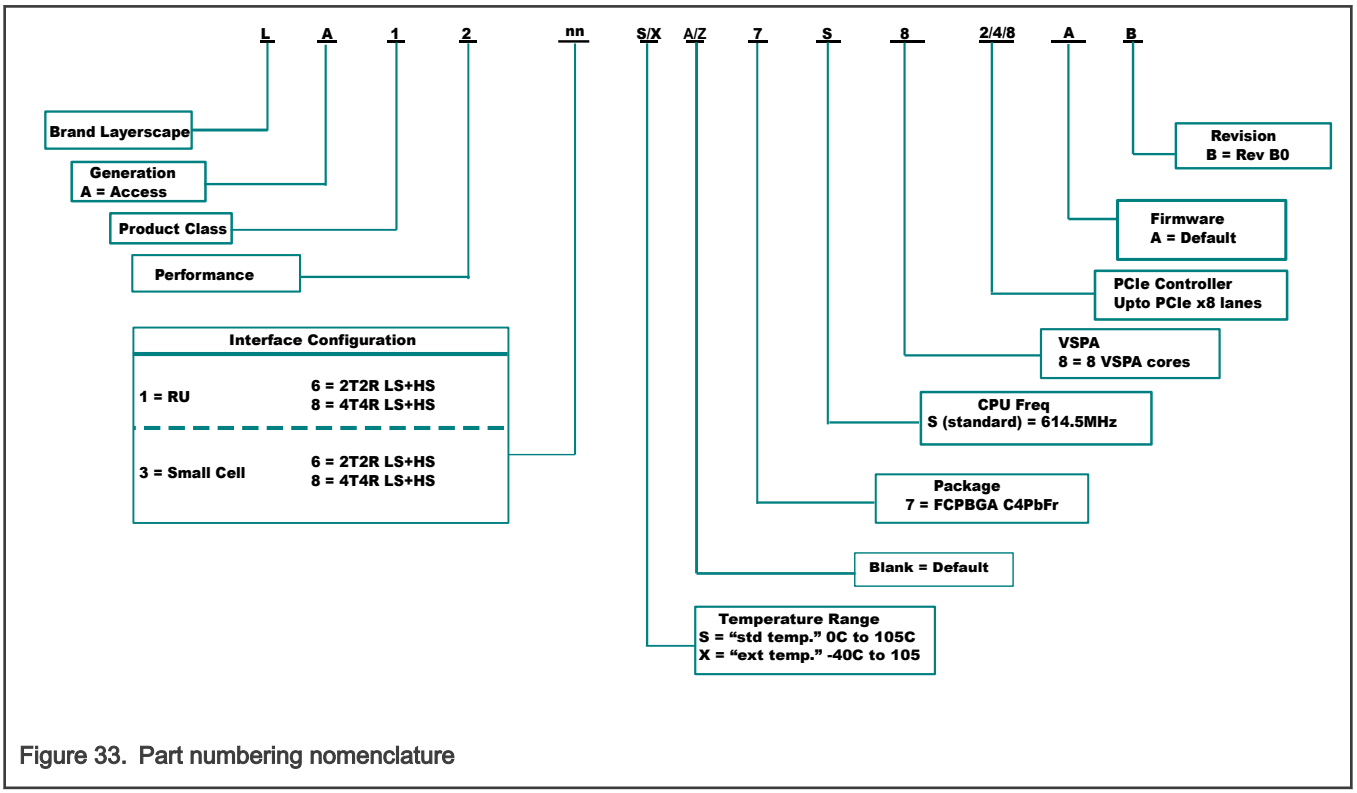
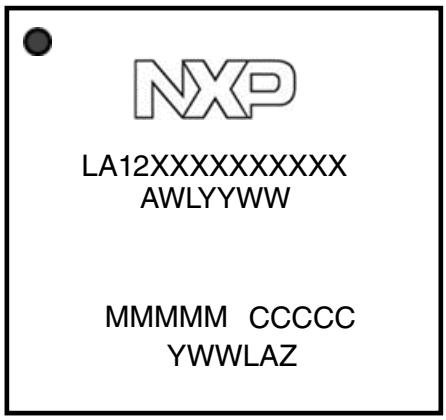


Figure 33. Part numbering nomenclature

7.2 Part marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Legend:
Marking format place holder for -
LA12XXXXXXXXXX - Product ID
AWLYYWW -Test Traceability
MMMMM - Die Build Series
CCCCC - Country of Origin
YWWLAZ - Assembly Traceability

Figure 34. Preliminary part marking for FC-PBGA chip

8 Revision history

This table summarizes revisions to this document.

Table 49. Revision history

Revision	Date	Description
2	04/2024	• In Pinout list by bus, updated signal spec from "HS_DCS_AVNN" to "RSVD_M8 " and updated its signal description to "Reserved" and its related note. • In Absolute maximum ratings, Recommended_operating_conditions, Power-on ramp rate and Power sequencing removed "HS_DCS_AV_{NN}" instance • In High-Speed DCS electrical characteristics, added information "For correct operation of IQ ADC and IQ DAC blocks application must use HS-DCS firmware …."
1	06/2023	• Updated Features • Updated Block Diagram • Updated Introduction • Updated Low-Speed DCS electrical characteristicsand High-Speed DCS electrical characteristics • Added footnote in Table 3 • Removed topic "DCS VREF Pins for LS_DCS"

Table continues on the next page...

Table 49. Revision history (continued)

Revision	Date	Description
		• Added Package outline drawing document number in Package parameters for the FC-PBGA • Removed topic "DCS Analog Power and Ground" • Added sentence "The TMU Temperature reading accuracy is within ±5°C" in Temperature Monitoring • Updated ADC Input and DAC Output Signals
0	12/2022	• Initial release.

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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