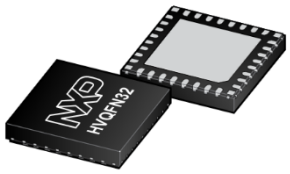
FS2400

Fail-safe system basis chip with SMPS and LDO, CAN FD transceiver

Rev. 5.0 — 16 July 2025 **Product data sheet**



Document information

Information	Content
Keywords	Fail-safe system basis chip, SMPS, LDO, CAN FD transceiver, ultra-wide band (UWB), Near Field Communication (NFC), Bluetooth Low Energy (BLE) devices, small applications, low power
Abstract	The FS2400 is a family of automotive safety system basis chip devices with multiple power supplies designed to support secure car-access application while maintaining flexibility to fit other small applications requiring low power and CAN FD communication.

1 General description

FS2400 is a family of automotive safety system basis chip (SBC) devices with multiple power supplies designed to support secure car access application using ultra-wide band (UWB), near-field communication (NFC) and Bluetooth Low Energy (BLE) devices. The FS2400 can also fit other small applications requiring low power and CAN FD communication.

This family of devices supports a wide range of applications, offering choice of output voltage settings, physical interface, integrated system-level features to address low-power and noise-sensitive applications with automotive safety integrity levels (ASIL) up to ASIL B.

The FS2400 integrates a battery-connected switched-mode regulator (V1) and a battery-connected linear regulator (V3) to supply microcontroller, communication devices and others. V1 offers a high-performance switching regulator capable of operating in Pulse Frequency Modulation (PFM) mode and Force Pulse Width Modulation (FPWM) mode. The mode of operation can be changed using wake pins to optimize noise management.

The FS2400 is developed in compliance with the ISO 26262:2018 standard. It includes enhanced safety features, with fail-safe output, becoming part of a full safety-oriented system, covering ASIL B safety integrity level.

The FS2400 is offered in a 5 mm x 5 mm, 32-Ld HVQFN package with wettable flanks.

2 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Low-power off mode with very low sleep current and multiple wake-up sources
- Low-power on mode with HVBUCK (V1) active, HVLDO (V3) selectable by OTP and multiple wake-up sources

Power supplies

- V1: High-voltage synchronous buck converter with integrated FETs. Configurable output voltage (2.0 V to 5 V) and switching frequency, output DC current capability up to 400 mA and PFM mode for Low-power on mode operation
- V3: High-voltage LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V or 5 V and up to 150 mA current capability

System support

- One CAN FD supporting up to 5 Mbps communication following ISO 11898-2:2016 and SAE J2284 standards
- Four wake-up inputs (40 V capable): WAKEx pins, HVIO1 pin, CAN FD or SPI command
- Hardware ID detection capability
- One high-voltage I/O with wake-up capability (40 V capable): HVIO1
- Device control via 32 bits SPI interface, with CRC
- Integrated long duration timer (LDT) for system shutdown and wake-up control, programmable up to 194 days
- 12-channel analog multiplexer (AMUX) for system monitoring (temperature, battery voltage, internal voltages)

Functional safety

- Developed following ISO 26262:2018 standard to fit for ASIL B applications
- Internal monitoring circuitry with its own reference.
- Additional input for external voltage monitoring
- Window or timeout watchdog function to monitor the MCU software failure
- Analog built-in self-test (ABIST) on demand
- Safety outputs (RSTB, LIMP0)
- Safety input to monitor external IC state (ERRMON)

Configuration and enablement

- HVQFN32: HVQFN, 32 pins with exposed pad for optimized thermal management, wettable flanks, 5 mm x 5 mm x 0.85 mm, 0.5 mm pitch
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP emulation mode for system development and evaluation

3 Applications

- UWB anchors
- NFC anchors
- BLE anchors
- Combo anchors (UWB + BLE)
- UWB radar
- All small applications requiring low power and CAN FD

4 Ordering information

This section describes the part numbers available to be purchased along with their main differences. It also describes how the part number reference is built.

4.1 Part numbers definition

Figure 1 describes how the FS24 part numbers are built.

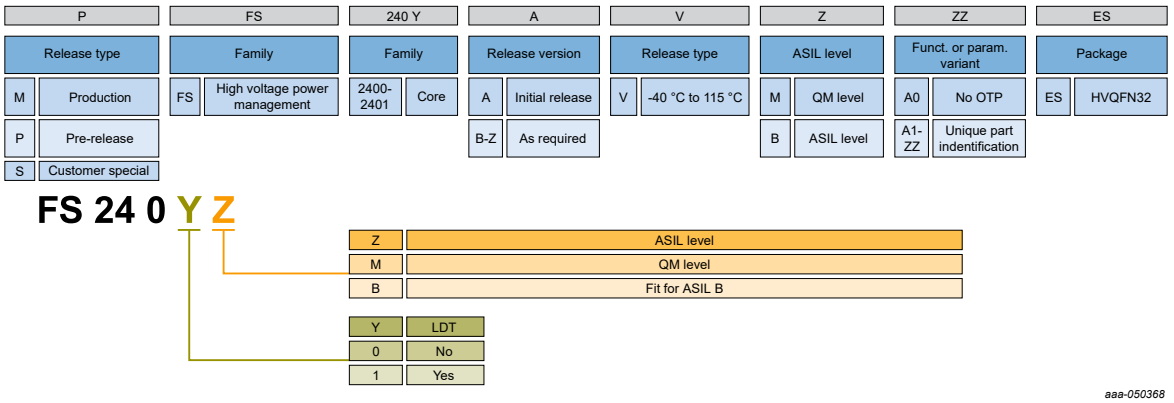


Figure 1. FS24 product numbering scheme

4.2 Part numbers list

Table 1. Device segmentation

Generic part number	Description	Fit for ASIL	LDT	RSTB	LIMP0	VMON (1, 3)	VMON_EXT (VMON0)	Watchdog	Cyclic INIT CRC check	RSTB 8 sec timer	ABIST	Package
FS2400M[1]	QM without LDT	QM	No	Yes	Option	Yes	No	Option	No	No	No	HVQFN32
FS2401M[1]	QM with LDT	QM	Yes	Yes	Option	Yes	No	Option	No	No	No	HVQFN32
FS2400B[1]	ASIL B without LDT	B	No	Yes	Option	Yes	Option	Yes	Yes	Yes	Yes	HVQFN32
FS2401B[1]	ASIL B with LDT	B	Yes	Yes	Option	Yes	Option	Yes	Yes	Yes	Yes	HVQFN32

[1] Exact orderable part numbers are defined in Table 2.

Table 2. Orderable part numbers

Part number[1]	Description	Package
MFS2400AVMA0ES[2]	Superset covering FS2400M devices.	HVQFN32
MFS2401AVMA0ES[2]	Superset covering FS24001M devices.	
MFS2400AVBA0ES[2]	Superset covering FS2400B devices.	
MFS2401AVBA0ES[2]	Superset covering FS2401B devices.	
MFS2400AVMA1ES	Configuration given as an example for Ranger 5 attach, V1 at 3.3 V and V3 at 5 V. QM, LDT disabled.	
MFS2401AVBA1ES	Configuration given as an example for Ranger 5 attach, V1 at 3.3 V and V3 at 5 V. ASIL B, LDT enabled.	
MFS2401AVMAFES	Configuration given as an example for S32K1xx + NCF3321 attach, V1 at 5 V and V3 at 3.3 V. QM, LDT enabled.	
MFS2400AVBAAES	Configuration given as an example for S32K31x, V1 at 5V and V3 at 5V, ASIL B	

[1] To order parts in tape and reel, add the R2 suffix to the full part number reference.
[2] A0 parts are non-programmed OTP configurations. Preprogrammed OTP configurations are managed through part number extension. For a custom OTP configuration, please contact a local NXP sales representative.

5 Block diagram

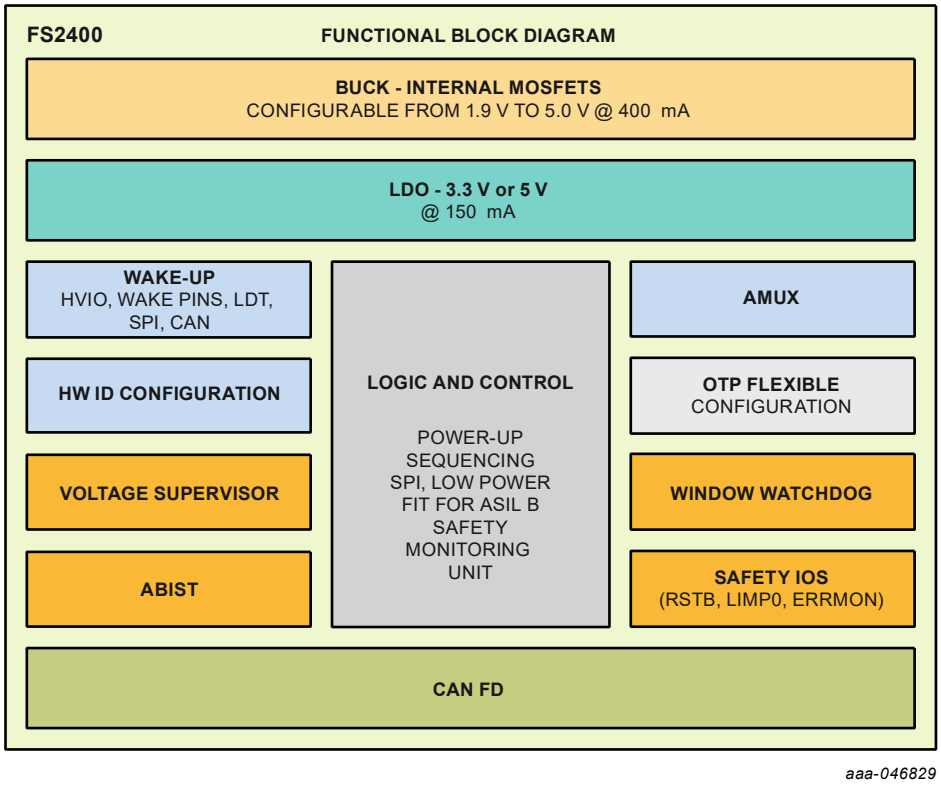


Figure 2. Functional block diagram

5.1 Internal block diagram

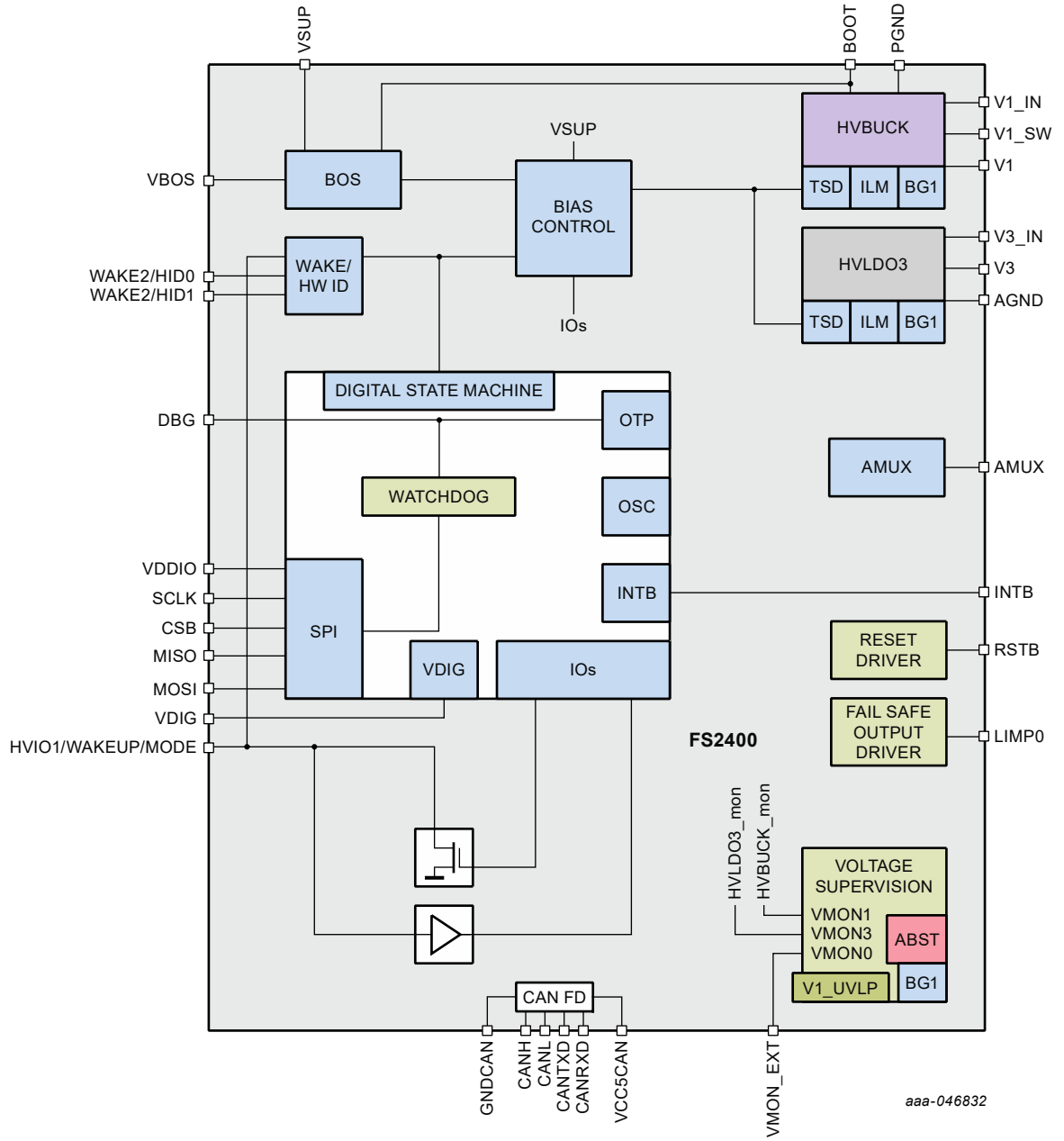


Figure 3. FS2400 block diagram

5.2 Simplified application diagram

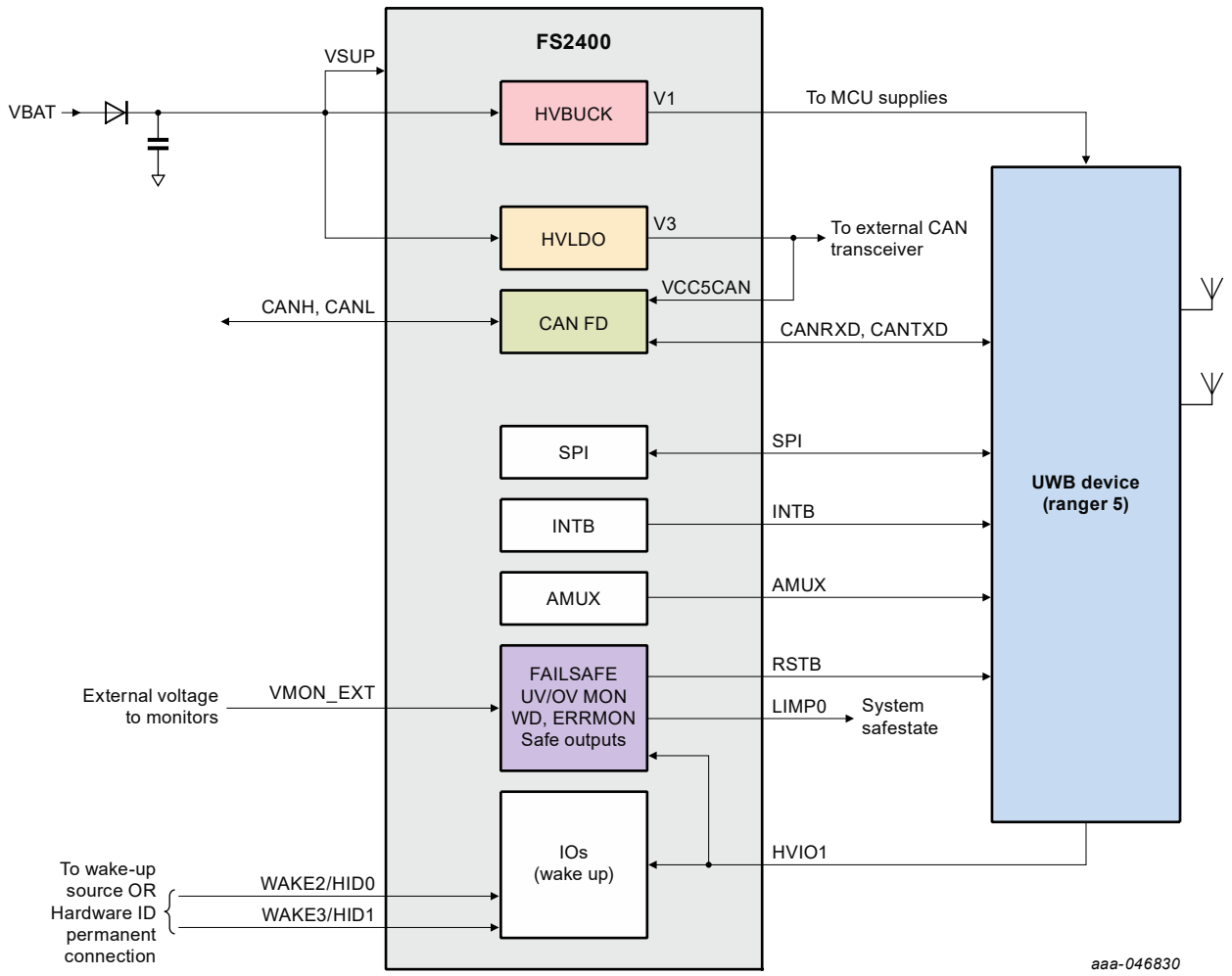


Figure 4. FS24 for UWB Simplified application diagram

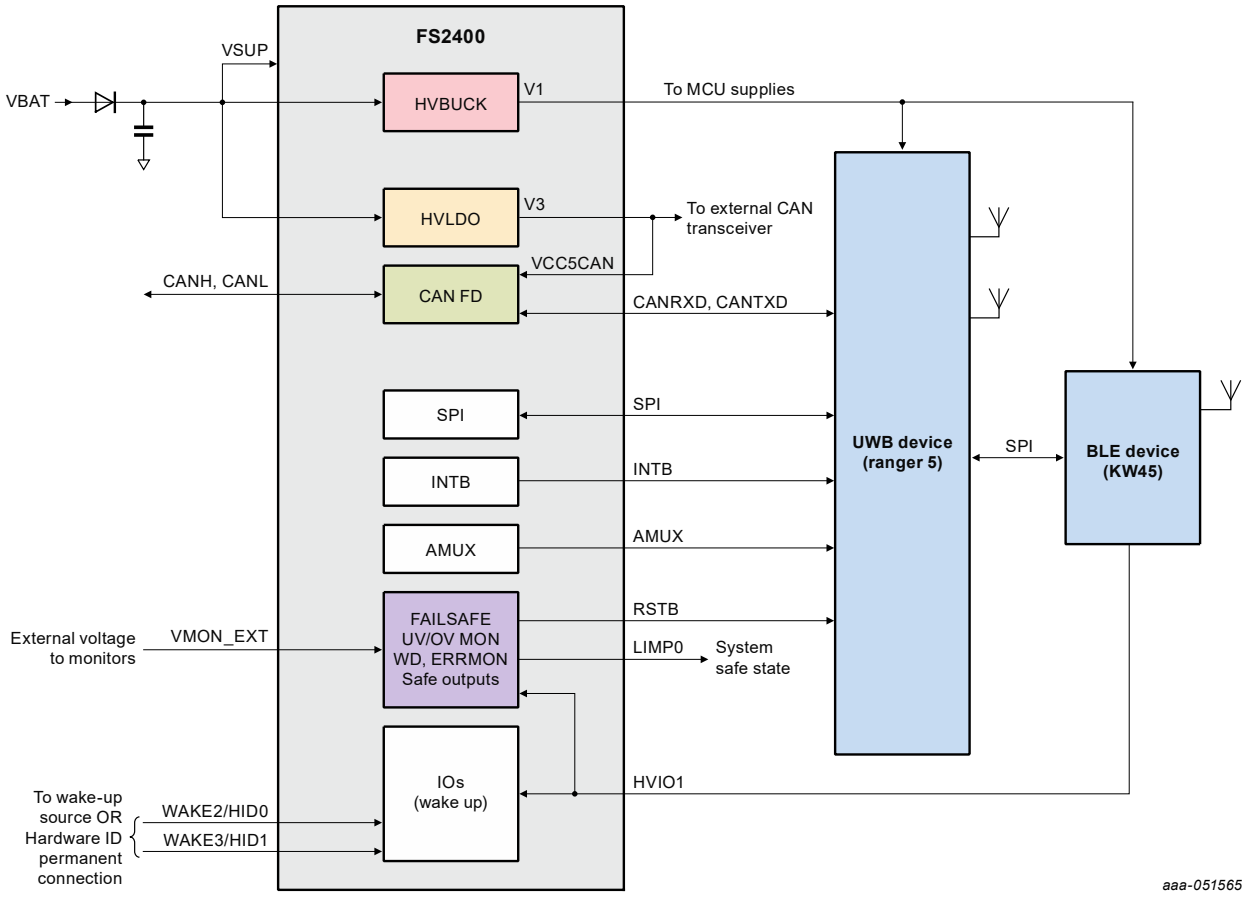


Figure 5. FS24 for UWB and BLE Simplified application diagram

6 Pinning information

6.1 Pinning

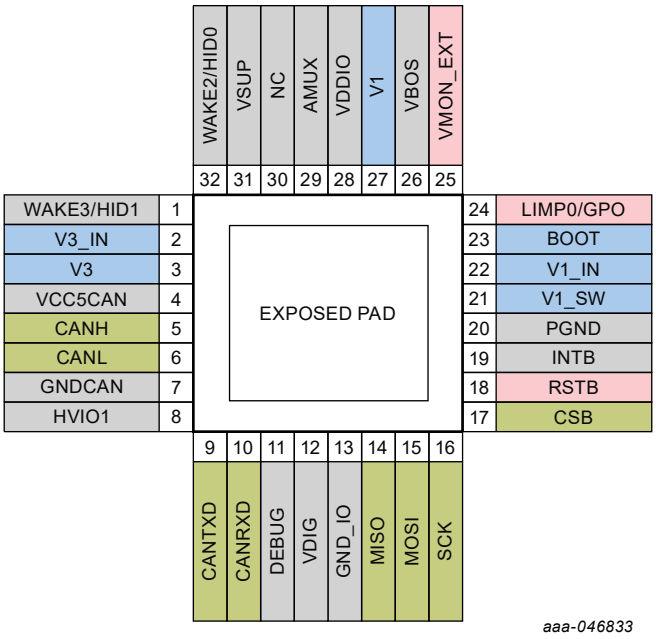


Figure 6. FS2400 pin configuration

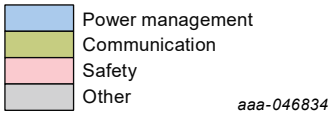


Figure 7. FS2400 pin configuration legend

6.2 Pin description

Table 3. Pin description

Pin	Pin name	Type	Description
1	WAKE3/HID1	Analog input	Wake-up input 3 / Hardware ID 1
2	V3_IN	Analog input	V3 regulator input voltage
3	V3	Analog output	V3 regulator output voltage
4	VCC5CAN	Analog input	CAN input supply pin
5	CANH	Analog input/output	CAN bus. CAN High
6	CANL	Analog input/output	CAN bus. CAN Low
7	GNDCAN	Ground	CAN bus ground
8	HVIO1	Digital input/output	High-voltage IO 1, with wake-up capability
9	CANTXD	Digital input	Transceiver input from the MCU, which controls the state of the CAN bus.
10	CANRXD	Digital output	Receiver output, which reports the state of the CAN bus to the MCU.
11	DEBUG	Analog input	Debug mode entry and OTP input supply
12	VDIG	Analog output	Internal digital supply
13	GND_IO	Ground	IOs ground connection

Table 3. Pin description...*continued*

Pin	Pin name	Type	Description
14	MISO	Digital output	SPI bus. Controller Input Device Output[1]
15	MOSI	Digital input	SPI bus. Controller Output Device Input[1]
16	SCK	Digital input/output	SPI bus. Clock input
17	CSB	Digital input/output	SPI bus. Chip select (active low)
18	RSTB	Digital input/output	Reset input/output. Active low. The main function is to reset the MCU. Reset input voltage is monitored in order to detect external reset and fault condition.
19	INTB	Digital output	Interrupt output
20	PGND	Ground	Power ground connection (V1 HVBUCK)
21	V1_SW	Analog input/output	Switching node (V1 HVBUCK)
22	V1_IN	Analog input	V1 regulator input voltage
23	BOOT	Analog input/output	V1 bootstrap capacitor (V1 HVBUCK)
24	LIMP0/GPO	Digital output	LIMP home-mode output 0. Active low (high by default) / general-purpose output
25	VMON_EXT	Analog input	External voltage monitoring input
26	VBOS	Analog output	Best of supply output voltage
27	V1	Analog output	V1 regulator output voltage
28	VDDIO	Analog input	Input voltage for SPI and AMUX
29	AMUX	Analog output	Multiplexed output to be connected to an MCU ADC with selection of the analog parameter though SPI.
30	NC	Not connected	Not connected
31	VSUP	Analog input	Power supply of the device
32	WAKE2/HID0	Analog input	Wake-up input 2 / Hardware ID 0

[1] Changed description to remove non-inclusive language. See v. 5.0 revision history.

6.2.1 Connection of unused pins

Table 4. Connection of unused pins

Pin	Pin name	Type	Description
1	WAKE3/HID1	Analog input	Open (WAKE3PUPD_OTP = 01)
2	V3_IN	Analog input	Grounded
3	V3	Analog output	Grounded or open
4	VCC5CAN	Analog input	Grounded
5	CANH	Analog input/output	Open
6	CANL	Analog input/output	Open
7	GNDCAN	Ground	Connection mandatory
8	HVIO1	Digital input/output	Open (HVIO1PUPD_OTP = 01)
9	CANTXD	Digital input	Open (200 kΩ internal pull up to VDDIO)
10	CANRXD	Digital output	Open (push-pull structure)
11	DEBUG	Analog input	Connection mandatory to GND in application mode
12	VDIG	Analog output	Connection mandatory
13	GND_IO	Ground	Connection mandatory
14	MISO	Digital output	Open

Table 4. Connection of unused pins*...continued*

Pin	Pin name	Type	Description
15	MOSI	Digital input	Open (200 kΩ internal pull up to VDDIO)
16	SCK	Digital input/output	Connection mandatory
17	CSB	Digital input/output	Connection mandatory
18	RSTB	Digital input/output	Connection mandatory
19	INTB	Digital output	Open
20	PGND	Ground	Connection mandatory
21	V1_SW	Analog input/output	Connection mandatory
22	V1_IN	Analog input	Connection mandatory
23	BOOT	Analog input/output	Connection mandatory
24	LIMP0/GPO	Digital output	Open
25	VMON_EXT	Analog input	GND
26	VBOS	Analog output	Connection mandatory
27	V1	Analog output	Connection mandatory
28	VDDIO	Analog input	Connection mandatory
29	AMUX	Analog output	Open
30	NC	Not connected	Open
31	VSUP	Analog input	Connection mandatory
32	WAKE2/HID0	Analog input	Open (WAKE2PUPD_OTP = 01)
33	EP	Ground	Exposed pad (to be connected to ground)

7 Functional description

The FS24 device has one main state machine. The main state machine manages the power management, the Low-power modes, and the wake-up sources. It also manages the monitoring of the power management, the monitoring of the MCU and the monitoring of an external IC.

In parallel, an INIT state machine is implemented to manage the INIT state of the device. This state is used for the configuration of the device per SPI.

The safety pins RSTB and LIMP0 are managed independently of on another, in parallel of the main state machine.

7.1 Main state machine description

Power-on reset and power-up sequence

The FS24 starts when VBOS > V_{BOS_POR} and V_{DIG_OV} > VDIG > V_{DIG_POR}. VBOS is the first supply to start. The internal 1.6 V supply of the digital circuitry, VDIG, is generated from VBOS. When VBOS > V_{BOS_UV}, the high power (HP) analog circuitry is enabled and the OTP registers content is loaded into mirror registers. When VSUP > V_{SUP_UVH}, the power-up sequence starts in Slot 0, with V1 (HVBUCK) at least, and power-up sequencing follows the OTP programming for V3 (HVLDO) and HVIO1 if used as an output.

Transition to fail-safe during the power up

During the power-up sequence, if VBOS < V_{BOS_UV}, the device goes to Fail-safe mode and all regulators are disabled. If an overvoltage or an overtemperature is detected, the device goes to Fail-safe mode, depending on the OTP configuration.

Normal mode

When the power up is finished, the main state machine is in Normal mode. Normal mode is the application running mode and V_{SUP_UVH} has no effect even if VSUP < V_{SUP_UVH}, except generating an interruption. If VBOS < V_{BOS_UV}, the device goes to Fail-safe mode. See Figure 10 for the minimum operating voltage.

Transitions to Low-power modes

The device can go to Low-power modes via an SPI command from the MCU or via the mode selection feature of the HVIO1 pin. A GO2LPOFF command starts the power-down sequence to go in LPOFF mode. A GO2LPON command will start the power-down sequence to go in LPON mode. The device goes in Low-power mode after the power-down sequence. During power-down sequence, the device stops all the regulators in the reverse order of the power-up sequence. In case the device goes in LPON, V1 regulator is kept ON but switches from FPWM to PFM mode.

Transition to Fail-safe from Normal mode

In case of loss of VBOS (VBOS < V_{BOS_UV}), the device goes directly to Fail-safe mode without power-down sequence.

In case of overvoltage detection, or thermal shutdown detection (TSD) on a regulator, depending on OTP configuration, or when the fault error counter reaches its maximum value, the device stops and goes directly to Fail-safe mode without power-down sequence.

Fail-safe state exit

Two behaviors are configurable by OTP to exit the Fail-safe state:

- Automatic restart after TFS_DUR (autoretry feature, configurable by OTP at 100 ms or 4 s)
- Semi-automatic restart after TFS_DUR: The device exits Fail-safe state and enters LPOFF state, then waits for a wake-up source to transition to M2 and restarts (FS_LPOFF_OTP = 1).

7.2 Detailed functional state diagram

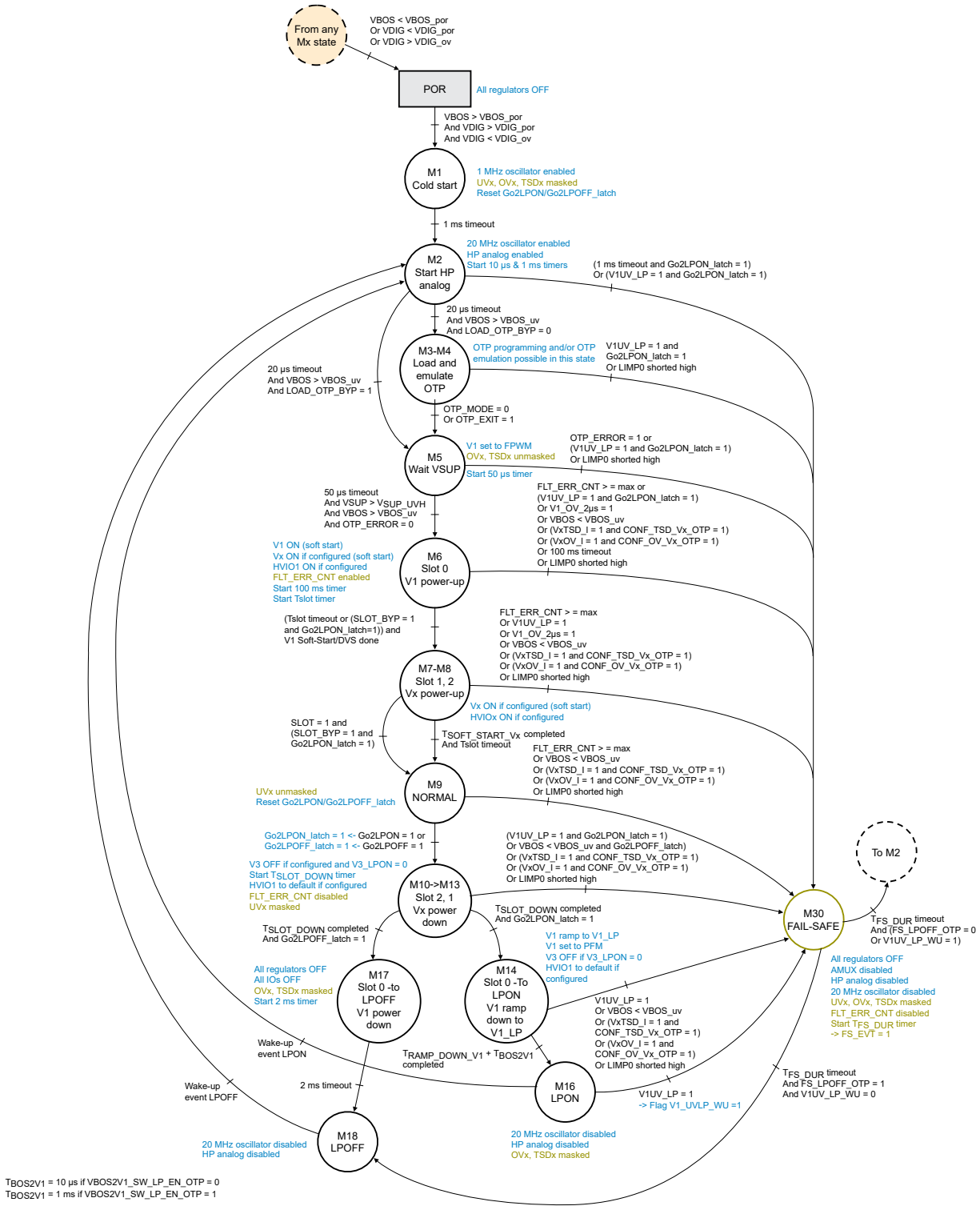


Figure 8. Detailed functional state diagram

7.3 INIT state machine

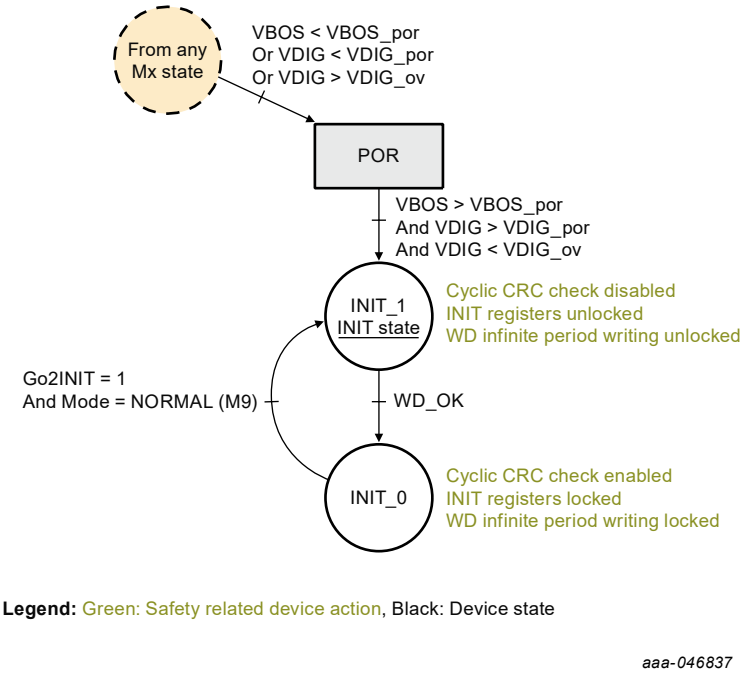


Figure 9. Simplified INIT state diagram

At power-on reset (POR), the device is automatically in INIT state. In this state, the INIT registers (FS_I_xxxxx) are available for writing and configuring the device safety features and reactions. The cyclic CRC check that protects these registers is disabled. Also in this mode, the watchdog period can be configured as infinite, which is equivalent to disabling the watchdog, for MCU programming for example. See Section 7.6.

Initialization should be done within 256 ms after RSTB release to avoid watchdog errors. Initialization phase is closed by first correct watchdog refresh. The INIT registers, as well as the infinite watchdog period configuration, are then protected against write access. The cyclic CRC check on the INIT registers is activated, and occurs every 5 ms.

The INIT state can be accessed again from Normal mode by sending a GO2INIT request by SPI.

The device will not enter the INIT state again when waking up from LPON or LPOFF states, or when restarting from Fail-safe state.

Note: *If the device goes in LPON or LPOFF or Fail-safe mode while in INIT state, the device stays in INIT state, which can lead to misconfiguration of the device. It is recommended to read the INIT_S status bit in M_STATUS register before going to LPON or LPOFF mode, and to go only if the device is no longer in INIT state.*

7.4 Power sequencing

V1 is the first regulator to start automatically in SLOT_0, then V3 regulator and HVIO1 (if configured) start following the OTP power sequencing configuration. Three slots are available, from SLOT_0 to SLOT_2, to program the startup sequence of V3 regulator, as well as HVIO1 release or assertion. A power-up slot (Tslot) lasts at least 500 µs. If V1 configured soft-start is longer than 500 µs, SLOT_0 will end once V1 soft-start is done.

The power-up sequence starts at SLOT_0 toward SLOT_2. The power-down sequence is executed in reverse order, starting at SLOT_2 toward SLOT_0.

All regulators not assigned in any slot are not started during the power-up sequence. These regulators can be started later when the main state machine is in Normal mode with an SPI command to write in M_REG_CTRL register if they were enabled by OTP.

When waking from LPON mode, the TSLOT timer can be skipped from SLOT_0 to SLOT_1 and from SLOT_2 to Normal mode by setting the SLOT_BYP bit to 1. During the power-down sequence, when the SLOT_BYP bit is set to 1, the TSLOT timer between SLOT_2 and SLOT_1 will be bypassed, as well.

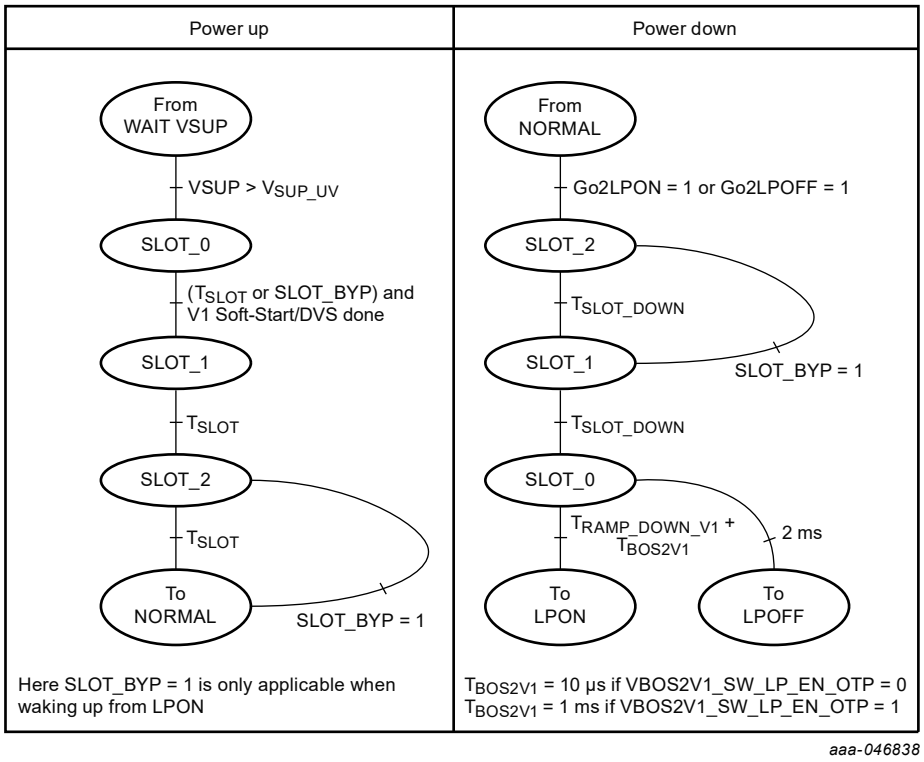


Figure 10. Power sequencing

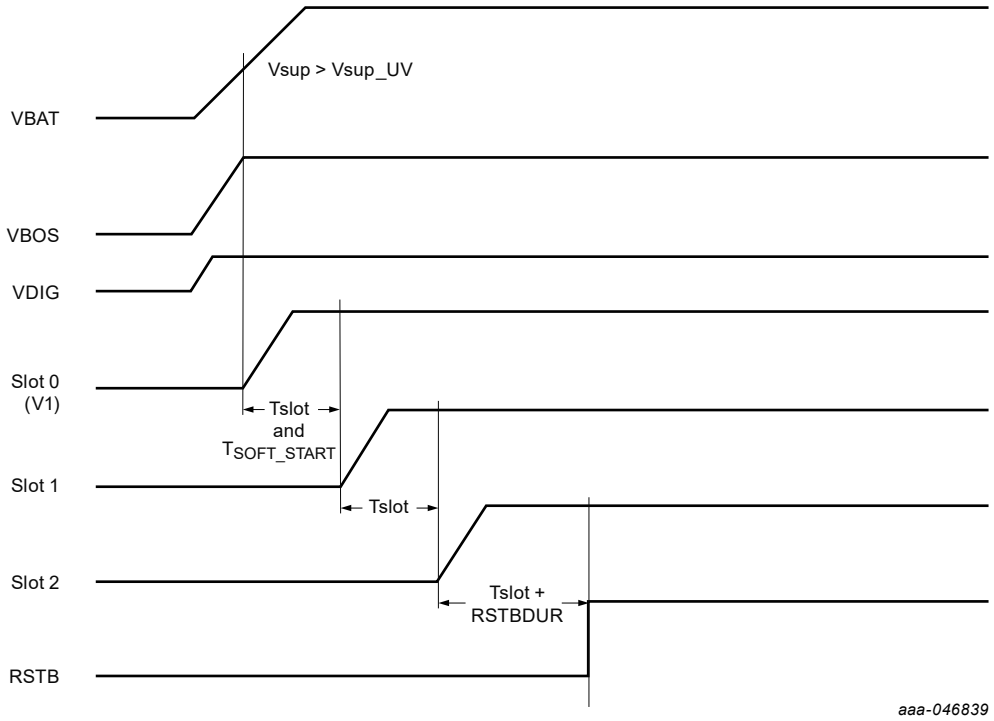


Figure 11. Power-up sequence example

7.5 Debug and OTP modes

OTP emulation and programming performed by the customer is allowed during engineering development using NXP's latest GUI and socketed evaluation board. The customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

The FS24 enters Fail-safe Debug mode when DBG pin voltage $V_{DBG} > V_{DBG\_MODE}$ before M4 state. It is recommended to connect the DBG pin to the VBOS pin through a diode ($V_{DBG} = V_{BOS} – Vd \approx 4.3$ V). The Debug mode disables the watchdog (period configured as infinite), the RSTB 8 s timer and Fail-safe mode entry via the fault error counter. In Debug mode, CAN transceiver is set to active mode by default. The Debug mode status is reported by the DBG_MODE bit in M_SYS1_CFG. To exit Debug mode, write 1 in the DBG_EXIT bit in the M_SYS1_CFG register.

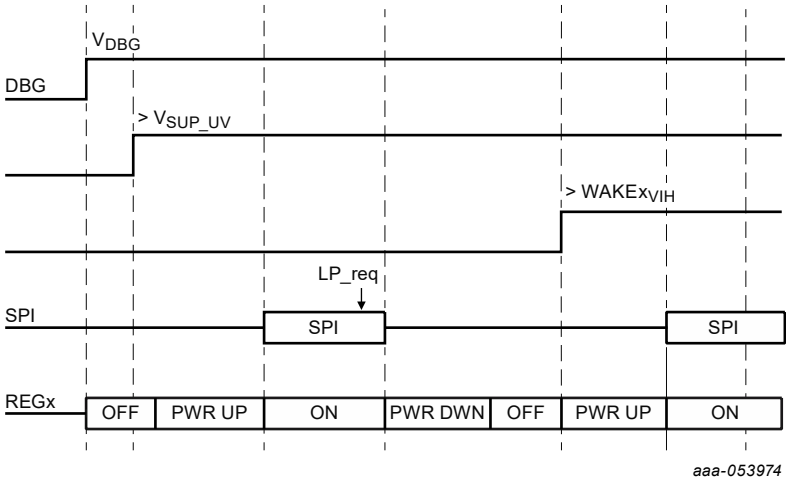


Figure 12. Debug mode

The FS24 enters OTP mode when V_{DBG} > V_{OTP_MODE} before M4 state . NXP recommends applying V_{OTP_MODE} with an external power supply at the DBG pin before applying V_{SUP}. In this case, the diode protects VBOS. V_{OTP_MODE} shall be equal to 7.95 V for OTP programming process.

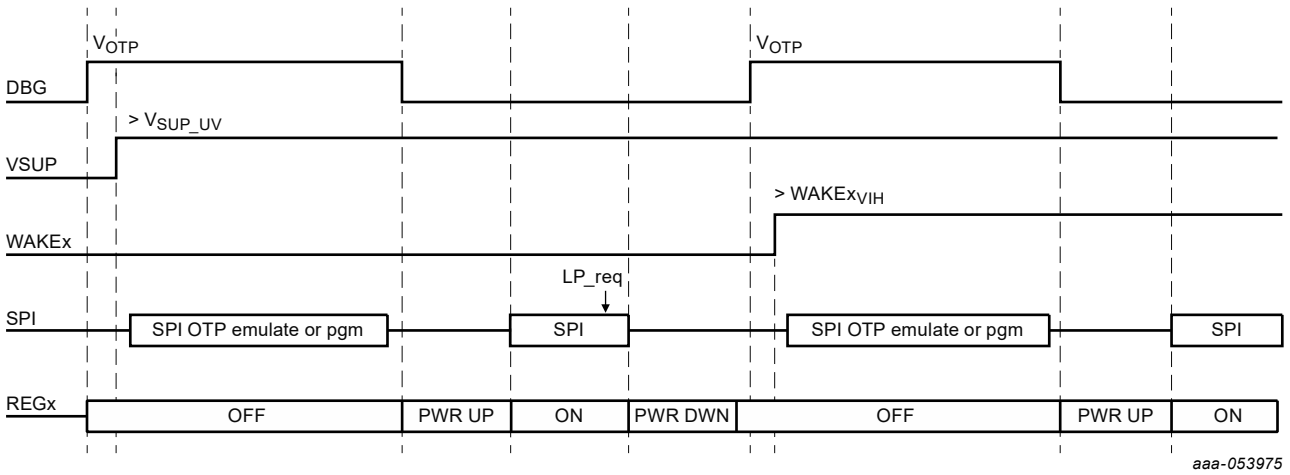


Figure 13. OTP mode time chart

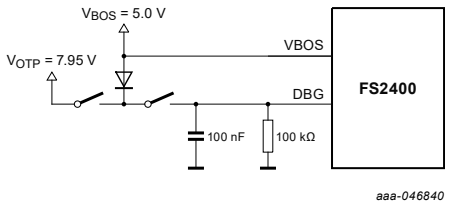


Figure 14. Debug pin circuitry

7.5.1 Electrical characteristics

Table 5. Electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Debug mode					
V_{DBG_MODE}	Voltage to apply at DBG pin to enter Debug mode	3.5	4.5	5.5	V
T_{DBG_MODE}	Debug mode entry filtering time	4	5.5	7	us
V_{OTP_MODE}	Voltage to apply at DBG pin to program the OTP	7.75	7.95	8.15	V
T_{OTP_MODE}	OTP mode entry filtering time	4	5.5	7	us
I_{DBG}	DBG pin input current consumption	-	-	30	µA

7.6 MCU programming

MCU programming can be done at any time. To prevent any watchdog error detection and RSTB pin assertion while programming, the watchdog period should be extended (up to 16384 ms) or set as infinite (window is fully opened). If the watchdog is not disabled, the user must refresh it during the MCU programming.

To disable the watchdog, NXP advises the user to start the device in Debug mode by applying the correct voltage to the DEBUG pin before M4 state.

7.7 Best of supply (BOS)

7.7.1 Functional description

The VBOS regulator manages the best of supply from VSUP or V1 to efficiently generate the internal biasing of the device, in all device modes. VBOS is also the supply of V1 High-Side and Low-Side gate drivers.

VBOS undervoltage may not guarantee the full functionality of the device. Consequently, V_{BOS_UV} detection powers down the device by going into fail-safe state.

VBOS is composed of two regulators implemented in parallel: VBOS_HP used to supply the HP analog internal biasing, and VBOS_LP used to supply the internal biasing in Low-power modes.

At power up, VBOS_LP is automatically enabled. VBOS_HP is enabled when the HP analog circuitry is enabled (State #M2). Both VBOS_LP and VBOS_HP are generated from VSUP.

In LPON mode, VBOS can be connected to V1 (VBOS2V1 switch closed) to optimize the efficiency. This way, the current consumption beneficiate from the VBAT to V1 ratio and is reduced. This function is enabled or disabled by OTP using VBOS2V1_SW_LP_EN_OTP bit.

When waking up from LPON mode, VBOS transition to VBOS_LP than immediately to VBOS_HP.

In LPOFF mode, only VBOS_LP is enabled.

The behavior of the VBOS regulator is summarized in Figure 15.

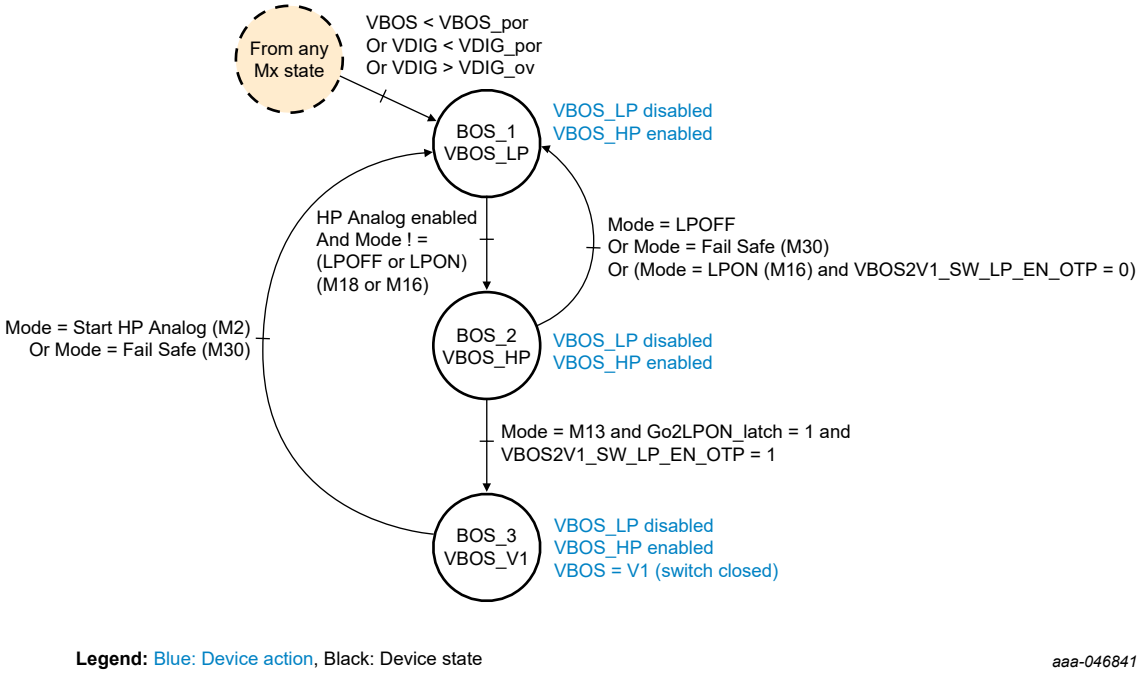


Figure 15. Simplified VBOS state diagram

7.7.2 Best of supply (BOS) electrical characteristics

Table 6. Best of supply electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 40 V, unless otherwise specified. All voltages referenced to ground."

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BOS}	Best of supply high-power output voltage	-	5	-	V
	Best of supply low-power output voltage (when not connected to V1 HVBUCK regulator)	-	4.7	-	V
V_{BOS_UV}	V_{BOS} undervoltage threshold in Normal mode	3.2	3.3	3.4	V
$V_{BOS\_POR\_UVL}$	V_{BOS} power-on reset threshold on falling edge	2.5	2.65	2.8	V
$V_{BOS\_POR\_UVH}$	V_{BOS} power-on reset threshold on rising edge	2.9	3.05	3.2	V
$V_{BOS\_HP\_DROP}$	Maximum V_{BOS_HP} dropout voltage (VSUP = 4 V, I_{BOS} = 5 mA, VBOS = 3.4 V)	-	-	600	mV
$V_{BOS\_SW\_V1}$	V_{BOS} to V1 switch dropout voltage (V1 = 3.3 V, I_{BOS} = 5 mA)	-	-	200	mV
Dynamic electrical characteristics					
T_{BOS_UV}	V_{BOS_UV} filtering time	0.13	1	3.1	µs
T_{BOS_POR}	V_{BOS_POR} filtering time	0.13	1	3.1	µs

Table 6. Best of supply electrical characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 40 V, unless otherwise specified. All voltages referenced to ground."

Symbol	Parameter	Min	Typ	Max	Unit
T_{BOS_START}	V_{BOS} low power starting time (VSUP = 5.2V, C_{OUT_BOS} = 1 µF, VBOS = 2.6 V)	-	-	500	µs
External components					
C_{OUT_BOS}	Effective output capacitor	-	1	-	µF

8 Limiting values

Minimum and maximum ratings

Table 7. Limiting values

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 1.8 V to 5 V, unless otherwise specified. All voltages referenced to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
WAKE2/HID0, WAKE3/HID1, LIMP0, HVIO1	Global pins	-0.3	40	V
V1_IN, VSUP, V3_IN	Global supply input pins	-1	40	V
CANH, CANL	Global communication pins	-33	40	V
BOOT	High-voltage pin/local pin	-0.3	45	V
V1_SW, VMON_EXT	High-voltage pins/local pins	-0.3	40	V
DEBUG	Debug pin to enter in Debug mode; should be grounded in the application	-0.3	10	V
V1,V3, VCC5CAN	Local pins	-0.3	5.6	V
VDDIO, VBOS, AMUX	Local pins	-0.3	5.5	V
CANRXD, CANTXD, MISO, MOSI, SCK, CSB, RSTB, INTB	Local pins	-0.3	VDDIO + 0.3	V
VDIG	Local pin	-0.3	2	V
GND_IO, PGND, GNDCAN	Ground pins	-0.3	0.3	V

9 Static characteristics

Table 8. Static characteristics

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q100 Rev H.				
V_{ESD_HBM}	All pins	-2	2	kV
$V_{ESD\_GLOBAL\_HBM}$	Global pins (VSUP, Vx_IN, LIMP0, WAKEx, HVIO1)	-4	4	kV
$V_{ESD\_CAN\_HBM}$	CAN bus interface pins (CANH, CANL)	-8	8	kV
Charged device model				
V_{ESD_CDM}	All pins, per AEC-Q100 rev H	-500	500	V
$V_{ESD\_CDM\_c}$	Pins 1, 8, 9, 16, 17, 24, 25, 32	-750	750	V
Gun discharged contact test				
V_{ESD_GUN1}	330 Ω/150 pF unpowered according to IEC 61000-4-2 Global pins and bus interface pins	-8	8	kV
V_{ESD_GUN2}	2 kΩ/150 pF unpowered according to ISO 10605:2008 Global pins and bus interface pins	-8	8	kV
V_{ESD_GUN3}	2 kΩ/330 pF powered, GND connected, according to ISO 10605:2008 Global pins and bus interface pins	-8	8	kV
V_{ESD_GUN4}	330 Ω/150 pF unpowered, GND connected, according to ISO 10605:2008 Global pins and bus interface pins	-8	8	kV

10 Thermal characteristics

Table 9. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
Thermal ratings				
T_A	Ambient temperature	-40	115	°C
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C
Thermal resistance (per JEDEC JESD51-9)				
$R_{\theta JA}$	Thermal resistance junction to ambient[1]	-	28.6	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom [2][3]	-	3.1	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top [4]	-	0.3	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed-circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

11 Application information

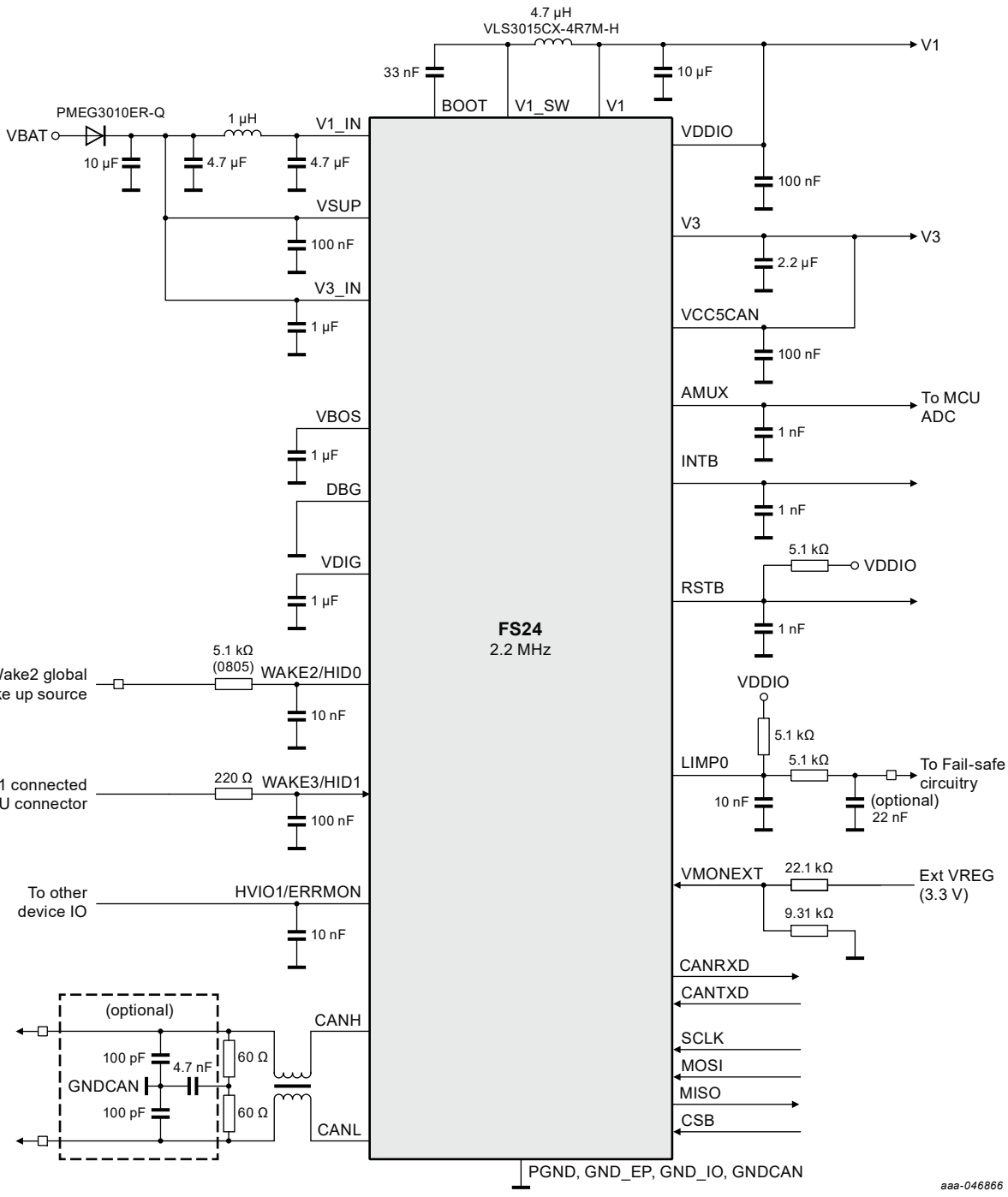


Figure 16. Application schematic, 2.2 MHz HVBUCK, SPI interface

Optional components depend on the application EMC and battery voltage ISO 7637-2 pulses requirements.

12 EMC compliancy

The FS24 EMC performance is verified against BISS generic IC EMC Test Specification version 2.0 from 07.2012 and FMC1278 Rev3 Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems from 2018.

In addition, EMC performance is verified against SAE J2962-2 (2019) and IEC 62228-3 (2019) for CAN performances.

13 Operating range and current consumption

13.1 Supply voltage

Electrical characteristics

Table 10. Supply voltage

TA = –40 °C to 115 °C, unless otherwise specified. VSUP from 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Device power supply					
V_{SUP}	Device input supply voltage	V_{SUP_UVH}	-	40	V
V_{SUP_OV}	VSUP overvoltage threshold	20	-	22	V
V_{SUP_UVHL}	VSUP undervoltage rising threshold, low configuration VSUP_UVTH_OTP = 0. Can be used when V1 ≤ 3.3 V	4.5	4.7	4.9	V
V_{SUP_UVHH}	VSUP undervoltage rising threshold, high configuration VSUP_UVTH_OTP = 1. Must be used when V1 = 5 V.	5.5	5.7	5.9	V
V_{SUP_UVLL}	VSUP undervoltage falling threshold (VSUP_4P7_I flag)	4.5	4.7	4.9	V
V_{SUP_UVLH}	VSUP undervoltage falling threshold (VSUP_5P7_I flag)	5.5	5.7	5.9	V
T_{SUP_OV}	V_{SUP_OV} filtering time	6	10	15	us
T_{SUP_UV}	V_{SUP_UVL} filtering time	6	10	15	us
Internal digital supply					
V_{DIG}	Device digital supply voltage	1.55	1.6	1.65	V
V_{DIG_OV}	VDIG overvoltage threshold	1.85	2	2.15	V
T_{DIG_OV}	V_{DIG_OV} filtering time	0.13	1	3.1	us
V_{DIG_POR}	VDIG power-on reset threshold on falling edge	1.35	1.41	1.47	V
T_{DIG_POR}	V_{DIG_POR} filtering time	0.13	1	3.1	us
Interface supply pins					
V_{DDIO}	VDDIO supply voltage range	1.8	-	5.5	V

The V_{SUP_OV} comparator triggers a flag in the SPI mapping for MCU diagnostic to indicate a load dump happened but has no direct action to the safety pins (RSTB, LIMP0).

13.2 Operating range

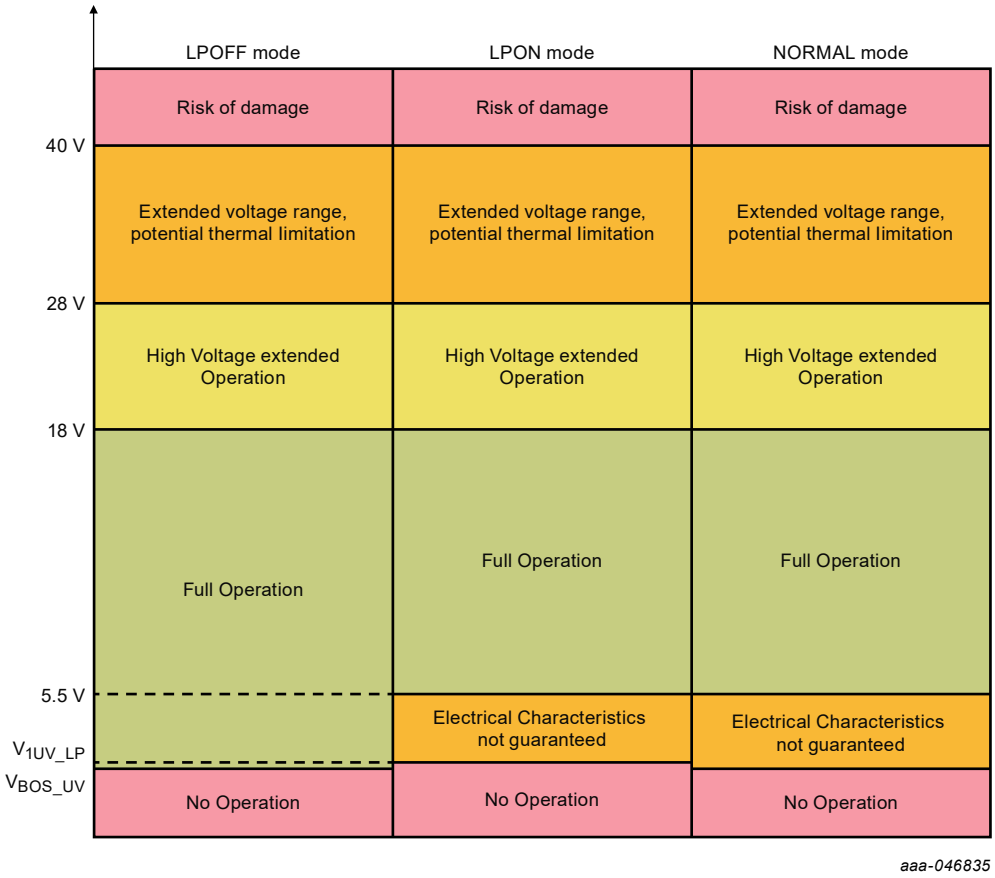


Figure 17. Input voltage range in LPOFF, LPON, and NORMAL mode

- VSUP > 28 V: potential thermal limitation (risk of TSD detection)
- VSUP > 18 V: extended high-voltage transient operation (Load dump)
- VSUP < 5.5 V: linear regulator needs a minimum of 5.5 V input when configured to deliver 5 V output. AMUX, CAN and IO specified for VSUP > 5.5 V
- VSUP < VBOS_UV in LPOFF mode: wake-up capability of the device is not guaranteed anymore, risk of POR
- VSUP < V1UV_LP in LPON mode: undervoltage detected on V1 in LPON mode leads the device to Fail-safe mode, with all regulators OFF
- VSUP < VBOS_UV in NORMAL mode: the device goes to Fail-safe mode, with all regulators OFF

13.3 Current consumption

Electrical characteristics

Table 11. Current consumption

TA = –40 °C to 115 °C, unless otherwise specified. VSUP from V_{SUP_UVH} to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Quiescent current					
I_{NORMAL}	Current in Normal mode • V1 in Force PWM mode • V3 enabled • CAN in Wake-up mode • V1 output current = 0 mA • V3 output current = 0 mA • Wake pins ignored	-	5	10	mA
I_{Q_LPON}	Current in Low-power on (LPON) mode Typical value at Tj=25 °C. Maximum value at Tj = 85 °C • VSUP = 12 V • V1 output voltage set ≥ 3.3 V[1] • V1 in Pulse Frequency Modulation (PFM) mode • HVIO1 wake-up only	-	40	50	µA
	Current in Low-power on (LPON) mode Typical value at Tj = 25 °C. Maximum value at Tj = 85 °C • VSUP = 12 V • V1 output voltage set < 3.3 V • V1 in Pulse Frequency Modulation (PFM) mode • HVIO1 wake-up only	-	65	80	µA
$I_{Q\_LPOFF\_CWK}$	Current in Low-power off (LPOFF) mode Typical value at Tj = 25 °C. Maximum value at Tj = 85 °C • VSUP = 12 V • V1 off • V3 off • HVIO1 wake-up only	-	35	55	µA

[1] In LPON mode, when V1 is equal or superior to 3.3 V, the quiescent current can be reduced by supplying VBOS from V1 (closing VBOS2V1 switch, if configured by OTP). This way, the current consumption beneficiates from the ratio between VBAT and V1 output.

14 Power management

Table 12. FS24 regulators list

Regulator	Type	Input supply	Output range	Max DC current
V1	HV buck regulator	V1_IN (V1+ 1 V to 40 V)	1.9 V to 5.5 V	400 mA
V3	HV Linear regulator	V3_IN (V3+500 mV to 40 V)	3.3 V or 5 V	150 mA

The FS24 includes two regulators, all supplied in parallel from the battery line.

The FS24 starts when VSUP > V_{SUP_UVH}, with VBOS first, followed by V1 (HVBUCK), and the power-up sequencing from the OTP programming for the remaining regulator V3 (HVLDO).

14.1 V1 HVBUCK: High-voltage buck regulator

14.1.1 Functional description

HVBUCK block is a high-voltage, integrated synchronous buck. It can be used to supply the ECU MCU and other local loads inside the ECU.

General operation

HVBUCK operates in force PWM or PFM modes and uses internal N-type FETs. The output voltage (1.9 V to 5 V) and the switching frequency (450 kHz or 2.25 MHz) are configurable by OTP. Compensation is ensured by internal circuitry.

The current in the inductor is sensed via the internal FETs, through the High-Side switch when it's turned on and through the Low-Side switch when it's turned on. This information is used to compute an average that is reflecting the output DC current.

Mode-specific operation

HVBUCK operates in PWM when the FS24 is in Normal mode and in PFM when the FS24 is in Low-power on mode (LPON). HVBUCK output voltage can be different in Normal mode and in LPON mode. The voltage rampup/down between the normal and the LPON voltages is done in PWM mode.

Current limitation

HVBUCK has current limitation protection features. In PWM mode, HVBUCK has both peak and average current limitations, configurable by OTP. In PFM mode, HVBUCK has a peak current limitation, also configurable by OTP. An overcurrent detection is also implemented on the Low-Side MOSFET, to detect high-negative current in case of output short to the battery.

When HVBUCK current reaches one of its current limitations, V1OC_I flag is set. The regulator stays enabled but it induces a duty-cycle reduction and therefore an output voltage drop, which could lead to an undervoltage detection (V1UV_I flag generated).

Input voltage range

When I_{BUCK} current load is higher than 400 mA, V1_IN shall be above (V_{BUCK} + ((Max(RLS_BUCK) + Max(RDCR_L_{BUCK})) x I_{BUCK}))/0.905 to guarantee HVBUCK output-voltage regulation (4.06 V at I_{BUCK} = 400 mA with RDCR_L_{BUCK} = 200 mΩ and V_{BUCK} = 3.3 V).

Thermal shutdown

When a thermal shutdown is detected, the regulator is disabled and V1TSD_I flag is generated. The device can also transition to the Fail-safe state if configured by OTP.

Dynamic output voltage scaling

The HVBUCK output voltage can be modified while running by using the dynamic voltage scaling (DVS) function to adapt to the supplied device needs. This is done by setting the bits of the M_REG2_CTRL SPI register.

14.1.2 HVBUCK clock management

14.1.2.1 Description

The HVBUCK oscillator 20 MHz frequency can be modulated with a triangular or pseudo-random carrier frequency of 19 kHz, with a ±10 % deviation range around the oscillator frequency. The spread-spectrum feature can be selected by SPI. The MOD_EN bit enables the spread-spectrum feature and the MOD_CONF bit selects the triangular or pseudo-random modulation. These two bits are in the M_SYS_CFG SPI register. By default, the spread-spectrum feature is configured following the OTP configuration.

The main purpose of the spread-spectrum feature is to improve EMC performance by spreading out the energy of the HVBUCK switching frequency.

14.1.2.2 Spread spectrum

Triangular spread spectrum

The triangular spread spectrum is activated in the M_SYS_CFG SPI register by setting the MOD_EN bit high and the MOD_CONF bit low. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with a ±10 % deviation range of the nominal oscillator frequency.

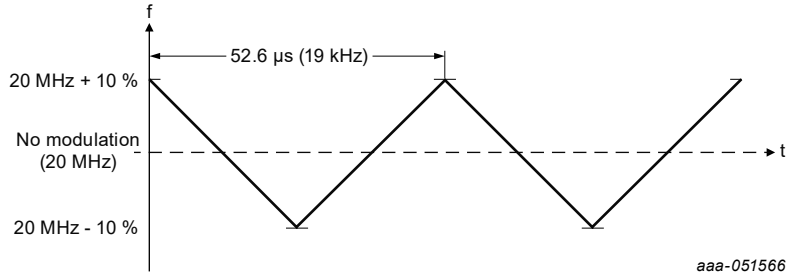


Figure 18. Triangular modulation

Pseudo-random spread spectrum

The pseudo-random triangular spread spectrum is activated in the M_SYS_CFG SPI register by setting the MOD_EN bit high and the MOD_CONF bit high. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with ±10 % deviation range of the nominal oscillator frequency, but two random commutations on the carrier slope are added in each half period to increase the spectrum content.

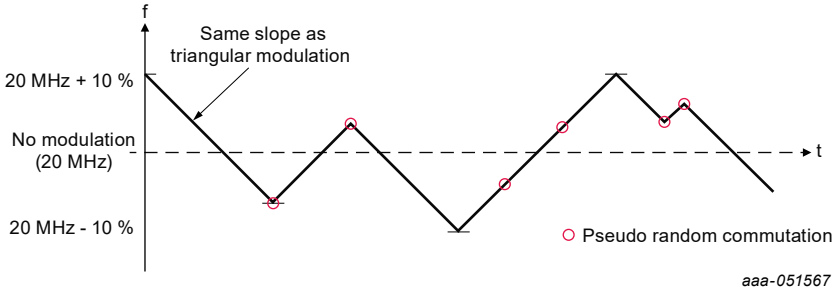


Figure 19. Pseudo-random modulation

14.1.3 Application schematic

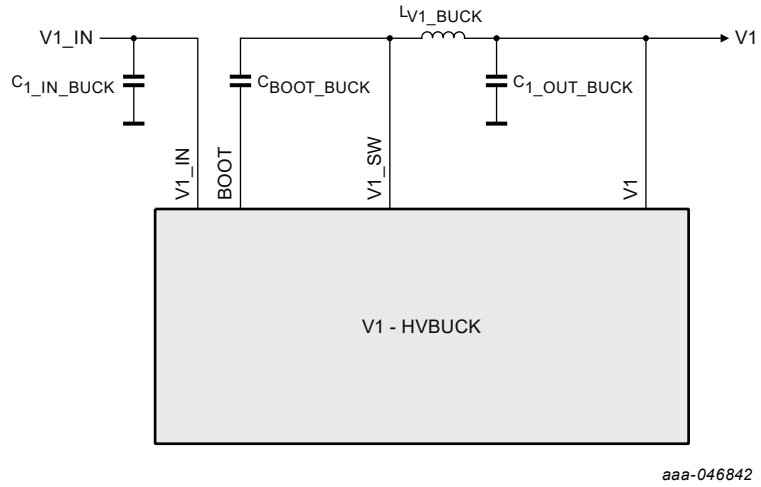


Figure 20. HVBUCK schematic with connection to V_{1_IN}

14.1.4 Electrical characteristics

Table 13. Electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. $V_{BUCK\_IN(min)}$ < V1_IN pin voltage < 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{BUCK\_IN\_STUP}$	Input voltage range during startup	4.6	-	36	V
V_{BUCK_IN}	Input voltage range (after startup) With VBOS = 5 V	(Vout+(Max(RLS_BUCK)+Max(RDCR_LBUCK))*IBUCK)/0.905	-	36	V
V_{BUCK}	Output voltage in : • Normal mode using VV1_BUCK_OTP and VV1_BUCK_RANGE_OTP OTP registers) • Low-power on mode using VV1_LP_BUCK_OTP and VV1_BUCK_RANGE_OTP OTP registers)	1.9	-	5	V
V_{BUCK_ACCPWM}	Output voltage accuracy in PWM mode	-2	-	2	%
V_{BUCK_ACCPFM}	Output voltage accuracy in PFM mode	-4	-	4	%
I_{BUCK_PWM}	Output current capability in PWM mode	-	-	400	mA
I_{BUCK_PFM}	Output current capability in PFM mode (LPON mode only)	-	-	100	mA
R_{HS_BUCK}	High-Side MOSFET RDSON (VBOS = 5 V, including bonding) Typical value at Tj = 25 °C. Maximum value at Tj = 150 °C	-	350	735	mΩ
R_{LS_BUCK}	Low-Side MOSFET RDSON (VBOS = 5 V, including bonding) Typical value at Tj = 25 °C. Maximum value at Tj = 150 °C	-	350	735	mΩ
R_{BUCK_DIS}	Feedback discharge resistor (when HVBUCK is disabled – LPOFF)	-	15	30	Ω
$TWARN_{V1}$	Temperature pre-warning	133	145	156	°C
TSD_{V1}	Thermal shutdown threshold	175	185	200	°C
TSD_{V1_HYST}	Thermal shutdown threshold hysteresis	5	9	12	°C

Table 13. Electrical characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. $V_{BUCK\_IN(min)}$ < V1_IN pin voltage < 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$I_{OC\_AVG\_PWM}$	Average overcurrent threshold in PWM mode				mA
	BUCK_AVG_OC_PWM_OTP[2:0] = 000	130	200	290	
	BUCK_AVG_OC_PWM_OTP[2:0] = 001	210	300	400	
	BUCK_AVG_OC_PWM_OTP[2:0] = 010	300	400	505	
	BUCK_AVG_OC_PWM_OTP[2:0] = 011	390	500	630	
	BUCK_AVG_OC_PWM_OTP[2:0] = 100	468	600	735	
	BUCK_AVG_OC_PWM_OTP[2:0] = 101	546	700	854	
$I_{OC\_PK\_PWM}$	Peak overcurrent threshold in PWM mode for F_{SW_BUCK} = 450 kHz				mA
	BUCK_PK_OC_PWM_OTP[2:0] = 010	300	400	500	
	BUCK_PK_OC_PWM_OTP[2:0] = 011	375	500	635	
	BUCK_PK_OC_PWM_OTP[2:0] = 100	468	600	732	
	BUCK_PK_OC_PWM_OTP[2:0] = 101	546	700	854	
	BUCK_PK_OC_PWM_OTP[2:0] = 110	624	800	976	
	BUCK_PK_OC_PWM_OTP[2:0] = 111	702	900	1150	
	Peak overcurrent threshold in PWM mode for F_{SW_BUCK} = 2.2 MHz				
	BUCK_PK_OC_PWM_OTP[2:0] = 010	292	450	639	
	BUCK_PK_OC_PWM_OTP[2:0] = 011	357	550	781	
	BUCK_PK_OC_PWM_OTP[2:0] = 100	422	650	910	
	BUCK_PK_OC_PWM_OTP[2:0] = 101	540	750	1050	
	BUCK_PK_OC_PWM_OTP[2:0] = 110	630	850	1190	
	BUCK_PK_OC_PWM_OTP[2:0] = 111	712	950	1235	
$I_{OC\_PK\_PFM}$	Peak overcurrent threshold in PFM mode				mA
	BUCK_PK_OC_PFM_OTP[2:0] = 101	546	700	854	
	BUCK_PK_OC_PFM_OTP[2:0] = 110	624	800	976	
	BUCK_PK_OC_PFM_OTP[2:0] = 111	702	900	1150	
I_{OC_LS}	Low-Side FET overcurrent threshold	0.3	0.8	1.18	A
Dynamic electrical characteristics					
DCmax_drop	Maximum duty cycle in Dropout mode	-	90.5	-	%
$t_{V1OV\_DGLT\_STUP}$	Overvoltage deglitch time at startup	1	2	3	µs
t_{V1OC_DGLT}	Overcurrent deglitch time				µs
	BUCK_OC_DGLT_OTP[1:0] = 00	212.5	250	287.5	
	BUCK_OC_DGLT_OTP[1:0] = 01	425	500	575	
	BUCK_OC_DGLT_OTP[1:0] = 10	850	1000	1150	
	BUCK_OC_DGLT_OTP[1:0] = 11	1700	2000	2300	
t_{BUCK_SS}	Soft-start from 10 % to 90 %				µs
	BUCK_SS_OTP[1:0] = 00	200	269	410	
	BUCK_SS_OTP[1:0] = 01	431	538	645	
	BUCK_SS_OTP[1:0] = 10	873	1077	1281	
	BUCK_SS_OTP[1:0] = 11	1753	2150	2547	
t_{BUCK_DVS}	DVS slope from 10 % to 90 % of the difference between initial and final voltage, at VV1_BUCK_RANGE_OTP = 1 (values are multiplied by 2 for VV1_BUCK_RANGE_OTP = 0)				mV/µs
	BUCK_LP_DVS_OTP[1:0] = 00	9	11.25	13.5	
	BUCK_ LP_DVS _OTP[1:0] = 01	4.5	5.6	6.8	
	BUCK_ LP_DVS _OTP[1:0] = 10	2.2	2.8	3.4	
	BUCK_ LP_DVS _OTP[1:0] = 11	1.1	1.4	1.7	
$V_{BUCK\_LINE\_REG\_PWM}$	Transient line in PWM mode VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{BUCK} = 1 mA and 400 mA dv/dt= 100 mV/µs F_{SW_BUCK} = 450 kHz: L_{V1_BUCK} = 22 µH, C_{OUT_BUCK} = 40 µF F_{SW_BUCK} = 2.2 MHz : L_{V1_BUCK} = 4.7 µH, C_{OUT_BUCK} = 10 µF	-3	-	3	%

Table 13. Electrical characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. $V_{BUCK\_IN(min)}$ < V1_IN pin voltage < 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{BUCK\_LINE\_REG\_DO}$	Transient line after dropout exit VSUP = VBUCK - 0.4 V to 14 V I_{BUCK} = 1 mA and 400 mA dv/dt= 200 mV/µs, F_{SW_BUCK} = 450 kHz : L_{V1_BUCK} = 22 µH, C_{OUT_BUCK} = 40 µF F_{SW_BUCK} = 2.2 MHz : L_{V1_BUCK} = 4.7 µH, C_{OUT_BUCK} = 10 µF	-3	-	3	%
$V_{BUCK\_LOTR\_PWM}$	Transient load response in PWM mode 1mA to 200 mA step di/dt = 300 mA/µs F_{SW_BUCK} = 450 kHz : L_{V1_BUCK} = 22 µH, C_{OUT_BUCK} = 40 µF F_{SW_BUCK} = 2.2 MHz : L_{V1_BUCK} = 4.7 µH, C_{OUT_BUCK} = 10 µF	-3	-	3	%
$V_{BUCK\_LOTR\_PFM}$	Transient load response in PFM mode 0.1mA to 100 mA step di/dt = 100 mA/µs, F_{SW_BUCK} = 450 kHz : L_{V1_BUCK} = 22 µH, C_{OUT_BUCK} = 40 µF F_{SW_BUCK} = 2.2 MHz : L_{V1_BUCK} = 4.7 µH, C_{OUT_BUCK} = 10 µF	-3	-	3	%
F_{SW_BUCK}	Operating frequency in PWM mode BUCK_CLK_OTP = 0 BUCK_CLK_OTP = 1	 405 2.025	 450 2.25	 495 2.475	 kHz MHz
t_{BUCKHS_SLR}	High-Side FET rising slew rate BUCK_SRHSON_OTP[2:0] = 000 (for 450 kHz only) BUCK_SRHSON_OTP[2:0] = 001 (for 450 kHz only) BUCK_SRHSON_OTP[2:0] = 010 (for 450 kHz only) BUCK_SRHSON_OTP[2:0] = 011 BUCK_SRHSON_OTP[2:0] = 100 BUCK_SRHSON_OTP[2:0] = 101 BUCK_SRHSON_OTP[2:0] = 110 BUCK_SRHSON_OTP[2:0] = 111	 10 10 7 4.1 3 2.5 1.5 0.5	 20 20 15 10 6.3 5 3 2	 32 32 23.7 15 12 10 6 4	 ns
t_{BUCKHS_SLF}	High-Side FET falling slew rate BUCK_SRHSOFF_OTP[1:0] = 00 (for 450 kHz only) BUCK_SRHSOFF_OTP[1:0] = 01 (for 450 kHz only) BUCK_SRHSOFF_OTP[1:0] = 10 BUCK_SRHSOFF_OTP[1:0] = 11	 13 10 6.4 2.5	 20 15 10 5	 29 21.5 14 9	 ns
$t_{BUCKHS\_ON\_2M2\_3V3}$	High-Side FET ON time in PFM mode, VBUCK = 3.3 V, VBUCK_IN = 12 V, FSW_BUCK = 2.25 MHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	 129 165 204 243	 162 209 257 305	 196 253 310 367	 ns
$t_{BUCKHS\_ON\_450k\_3V3}$	High-Side FET ON time in PFM mode, VBUCK = 3.3 V, VBUCK_IN = 12 V, FSW_BUCK = 450 kHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	 687 858 1026 1195	 820 1023 1221 1422.5	 953 1188 1426 1650	 ns
$t_{BUCKHS\_ON\_2M2\_5V}$	High-Side FET ON time in PFM mode, VBUCK = 5 V, VBUCK_IN = 12 V, FSW_BUCK = 2.25 MHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	 160 205 254 303	 205 263 324 386	 250 322 395 469	 na

Table 13. Electrical characteristics...*continued*

T_A = –40 °C to 115 °C, unless otherwise specified. $V_{BUCK\_IN(min)}$ < V1_IN pin voltage < 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$t_{BUCKHS\_ON\_450k\_5V}$	High-Side FET ON time in PFM mode, VBUCK = 5 V, VBUCK_IN = 12 V, FSW_BUCK = 450 kHz BUCK_PFM_TON_OTP[1:0] = 00 BUCK_PFM_TON_OTP[1:0] = 01 BUCK_PFM_TON_OTP[1:0] = 10 BUCK_PFM_TON_OTP[1:0] = 11	 842 1050 1255 1465	 1021 1272.5 1632.5 1772.5	 1200 1495 2010 2080	ns
t_{BUCKHS_OFF}	High-Side FET OFF time in PFM mode F_{SW_BUCK} = 2.25 MHz BUCK_PFM_TOFF_OTP[1:0] = 00 BUCK_PFM_TOFF_OTP[1:0] = 01 BUCK_PFM_TOFF_OTP[1:0] = 10 BUCK_PFM_TOFF_OTP[1:0] = 11 F_{SW_BUCK} = 450 kHz BUCK_PFM_TOFF_OTP[1:0] = 00 BUCK_PFM_TOFF_OTP[1:0] = 01 BUCK_PFM_TOFF_OTP[1:0] = 10 BUCK_PFM_TOFF_OTP[1:0] = 11	 85 160 230 300 380 730 1070 1420	 130 250 360 475 605 1170 1725 2285	 195 360 525 695 890 1700 2520 3340	ns
External components					
$L_{\_BUCK}$	Nominal inductor for F_{SW_BUCK} = 450 kHz (± 30 % tolerance)	15	22	33	µH
	Nominal inductor for F_{SW_BUCK} = 2.25 MHz (± 30 % tolerance)	3.3	4.7	5.5	µH
C_{IN_BUCK}	Nominal input capacitor	4.7	10	-	µF
C_{BOOT_BUCK}	Nominal[1] bootstrap capacitor	-	22	-	nF
$C_{OUT\_BUCK\_450k\_3V3}$	Effective[2] output capacitor for F_{SW_BUCK} = 450 kHz, V_{BUCK} = 3.3 V	25	50	100	µF
$C_{OUT\_BUCK\_450k\_5V}$	Effective[2] output capacitor for F_{SW_BUCK} = 450 kHz, V_{BUCK} = 5 V	25	40	100	µF
$C_{OUT\_BUCK\_2M2\_3V3}$	Effective[2] output capacitor for FSW_BUCK = 2.2 MHz, VBUCK = 2 - 3.3 V	6.5	10	30	µF
$C_{OUT\_BUCK\_2M2\_5V}$	Effective[2] output capacitor for FSW_BUCK = 2.2 MHz, VBUCK = 5 V	13	20	40	µF
Oscillator and spread spectrum					
F_{20MHz}	HVBUCK oscillator nominal frequency	19	20	21	Mhz
F_{SSMOD}	Spread-spectrum frequency modulation	-	19	-	kHz
$F_{SSRANGE}$	Spread-spectrum range	-10	-	10	%

[1] For all regulators, the nominal capacitor value is the capacitor value normalized
[2] For all regulators, the effective capacitor value is the capacitor value after Tolerance, DC bias and Aging removal.

14.1.5 HVBUCK efficiency

The HVBUCK efficiency was measured at 2.25 MHz in PWM and PFM mode using the exact hardware and OTP configurations listed in Table 14.

Table 14. Hardware and configurations

		3.3 V		2.5 V		2 V	
	Inductor reference	**TFM**	**VLS**	**TFM**	**VLS**	**TFM**	**VLS**
	Vin	14	14	14	14	14	14
Hardware	Cin (eff.)	3.4 uF	3.4 uF	3.4 uF	3.4 uF	3.4 uF	3.4 uF
	Cin_esr	3.4 mΩ	3.4 mΩ	3.4 mΩ	3.4 mΩ	3.4 mΩ	3.4 mΩ
	Cout (eff.)	8.9 uF	8.9 uF	9.3 uF	9.3 uF	9.6 uF	9.6 uF
	Cout_esr	3.1 mΩ	3.1 mΩ	3.1 mΩ	3.1 mΩ	3.1 mΩ	3.1 mΩ
	L (eff.)	4.7 µH	3.8 µH	4.7 µH	3.8 µH	4.7 µH	3.8 µH
	L_dcr	200 mΩ	120 mΩ	200 mΩ	120 mΩ	200 mΩ	120 mΩ
	C_boot	33 nF	33 nF	33 nF	33 nF	33 nF	33 nF

Table 14. Hardware and configurations*...continued*

		3.3 V		2.5 V		2 V	
	Inductor reference	TFM	VLS	TFM	VLS	TFM	VLS
OTP	BUCK_SRHSOFF	10 ns	10 ns	10 ns	10 ns	10 ns	10 ns
	BUCK_SRHSON	10 ns	10 ns	10 ns	10 ns	10 ns	10 ns
	BUCK_CLK	2.25 MHz	2.25 MHz	2.25 MHz	2.25 MHz	2.25 MHz	2.25 MHz
	BUCK_AVG_OC_PWM	600 mA	600 mA	600 mA	600 mA	600 mA	600 mA
	BUCK_PK_OC_PWM	800 mA	800 mA	800 mA	800 mA	800 mA	800 mA
	BUCK_PFM_TON	305 ns	305 ns	-	-	-	-
	BUCK_PFM_TOFF	250 ns	250 ns	-	-	-	-
	VV1_BUCK	3.3 V	3.3 V	2.5 V	2.5 V	2.0 V	2.0 V
	VV1_LP_BUCK	3.3 V	3.3 V	-	-	-	-
	BUCK_SEL_PFM_TON	0b'0	0b'0	-	-	-	-
	BUCK_RRV_LV	12 ns	12 ns	12 ns	12 ns	12 ns	12 ns
	VBOS2V1_SW_LP_EN	0b'0	0b'0	0b'0	0b'0	0b'0	0b'0

Figure 21 and Figure 22 are the HVBUCK efficiency measured in PWM at 2.2 MHz, using the TFM252012ALMA4R7MTAA reference inductor and the VLS3015CX-4R7M-H reference inductor, respectively.

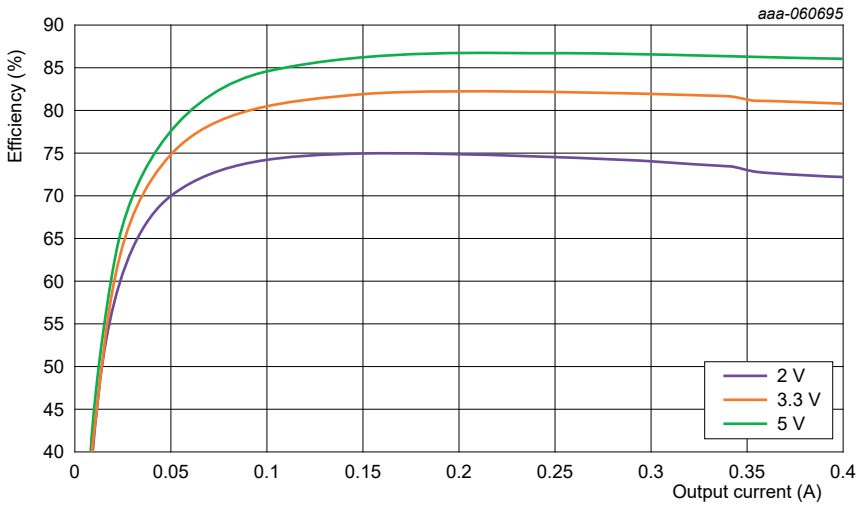


Figure 21. HVBUCK efficiency using 2.25 MHz using TFM252012ALMA4R7MTAA

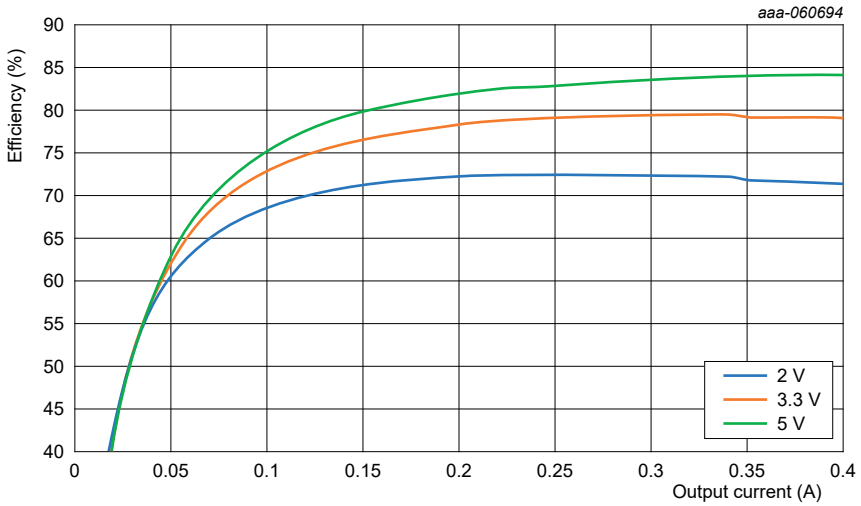


Figure 22. HVBUCK efficiency at 2.25 MHz using VLS3015CX-4R7M-H

Figure 23 is the HVBUCK efficiency measured in PFM, using the TFM252012ALMA4R7MTAA reference inductor and the VLS3015CX-4R7M-H reference inductor.

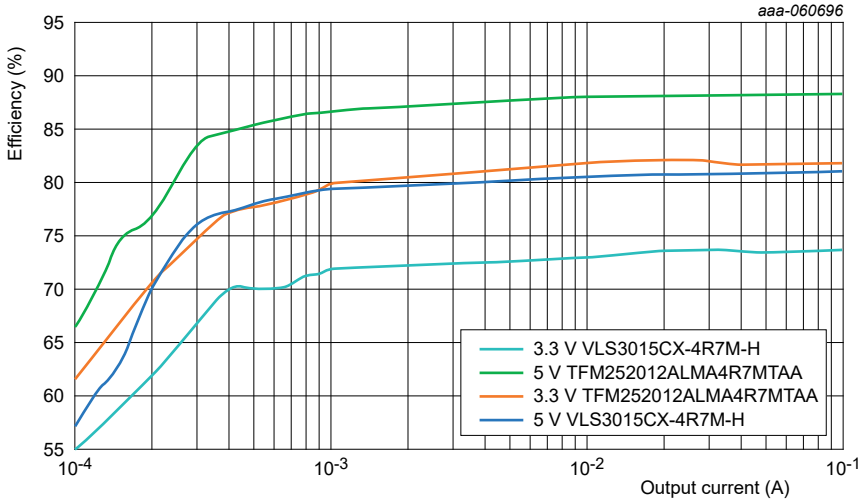


Figure 23. HVBUCK PFM efficiency

14.2 V3 HVLDO: High-voltage linear regulator

14.2.1 Functional description

HVLDO3 is a high-voltage, linear-voltage regulator. It can be supplied from the battery, or from V1 if its regulated output voltage is greater than the V3 regulated output voltage. The output voltage is configurable by OTP at 3.3 V or 5 V. A minimum voltage drop of 500 mV is required.

HVLDO3 is low-power capable and can stay enabled in LPON mode by setting V3ON_LPON bit by SPI. However, if disabled in LPON mode, it cannot be enabled again by SPI in this mode.

This regulator is meant to supply the integrated CAN transceiver. The connection is made externally. HVLDO3 can also supply an additional external transceiver on the module. If V3 is used to supply the voltage for integrated CAN, V3 should be set to 5 V in OTP.

An overcurrent detection and a thermal shutdown are implemented on HVLDO3 to protect the internal pass device. When an overcurrent is detected, V3OC_I flag is generated and the regulator remains enabled. It is the MCU's responsibility to disable the regulator by SPI using V3DIS bit, and to decide when to enable it using V3EN bit. When a thermal shutdown is detected, the regulator is disabled and V3TSD_I flag is generated.

The device can also transition to the Fail-safe state if configured by OTP.

14.2.2 Application schematic

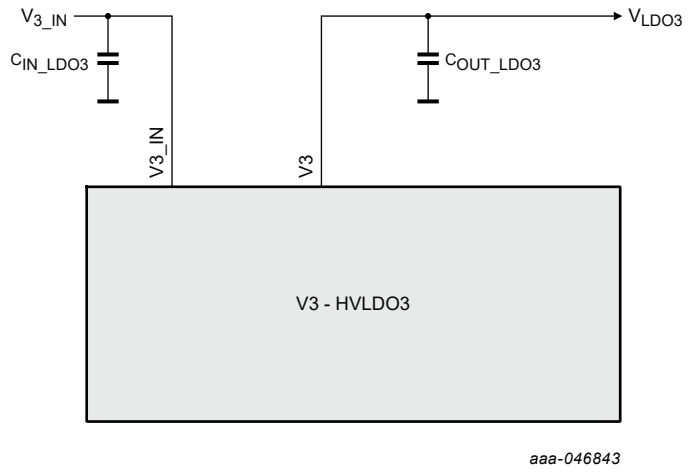


Figure 24. HVLDO3 application schematic

14.2.3 Electrical characteristics

HVLDO3 electrical characteristics

Table 15. Electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. V3_IN = VSUP = 5.5 V to 40 V if V3 = 5 V, or V3_IN = VSUP = 4 V to 40 V if V3 = 3.3 V, unless otherwise specified. I_{LDO3} = 0 mA to 150 mA unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDO3_IN}	Input voltage range	4	-	40	V
V_{LDO3}	Output voltage (OTP configurable) VV3_OTP = 0 VV3_OTP = 1	3.234 4.9	3.3 5	3.366 5.1	V
V_{LDO3_ACC}	Output voltage accuracy	-2	-	2	%
V_{LDO3_DROP}	Maximum voltage drop	500	-	-	mV
I_{LDO3}	DC current capability	-	-	150	mA
I_{LDO3_ILIM}	Internal PMOS current limitation	160	-	260	mA
I_{QLDO3}	Quiescent current on V3_IN, no load (typ @25 °C, max @85 °C)	-	25	30	µA
	Quiescent current on V3_IN, I_{LDO3} = 50 µA (typ @25 °C, max @85 °C)	-	30	35	µA
Dynamic electrical characteristics					
$t_{LDO3\_SOFT\_START}$	Soft start (from 10 % to 90 %)	150	300	500	µs
t_{LDO3_PDWN}	Discharge time when disabled	-	-	2	ms

Table 15. Electrical characteristics...*continued*

T_A = –40 °C to 115 °C, unless otherwise specified. V3_IN = VSUP = 5.5 V to 40 V if V3 = 5 V, or V3_IN = VSUP = 4 V to 40 V if V3 = 3.3 V, unless otherwise specified. I_{LDO3} = 0 mA to 150 mA unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
t_{LDO3_ILIM}	Current limit filtering time	16	20	24	µs
$V_{LDO3\_LINE\_REG\_NORMAL}$	Transient Line Response in Normal mode VSUP = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{LDO3} = 0.1 mA and 35 mA V_{LDO3} = 3.3 V and 5 V dv/dt = 100 mV/µs, C_{OUT_LDO3} = 2.2 µF	-3	-	3	%
$V_{LDO3\_LTR\_NORMAL}$	Transient Load Regulation in Normal mode I_{LDO3} = 10 mA to 50 mA in 10 µs, and from 50 mA to 10 mA in 10 µs, V_{LDO3} = 5 V, C_{OUT_LDO3} = 2.2 µF	-2	-	2	%
V_{LDO3_PSRR}	DC PSRR I_{LDO3} = 0.1 mA to 100 mA, LDO3 = 3.3 V or 5 V, VDROP = 500 mV (min), 20 Hz to 500 kHz	-	-40	-20	dB
External Components					
C_{IN_LDO3}	Input capacitor (close to V3_IN pin)	-	1.0	-	µF
C_{OUT_LDO3}	Effective output capacitor	1.3	-	10	µF

15 AMUX: Analog multiplexer

15.1 Functional description

The AMUX pin delivers internal analog voltage channels to the MCU ADC input. The voltage channels delivered to AMUX pin can be selected by SPI. The maximum AMUX output voltage range is VDDIO. An external output capacitor C_{AMUX_OUT} is required for the buffer stability.

15.2 AMUX schematic diagram

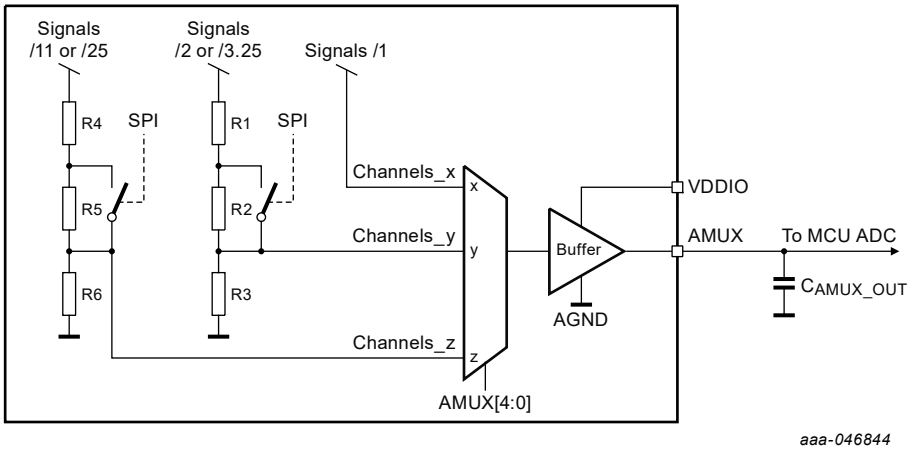


Figure 25. AMUX block diagram

15.3 Channel selection

Table 16. AMUX output selection

Channel	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
0	00000	AGND	N/A	N/A
1	00001	VDIG : internal voltage supply (1.6 V)	1	1
2	00010	V1 voltage	2	3.25
3	00011	Reserved	N/A	N/A
4	00100	V3 voltage	3.25	3.25
5	00101	VBOS internal voltage	3.5	3.5
6	00110	VSUP voltage (divider ratio configurable by SPI)	11	25
7	00111	Reserved	N/A	N/A
8	01000	Reserved	N/A	N/A
9	01001	Reserved	N/A	N/A
10	01010	Reserved	N/A	N/A
11	01011	Reserved	N/A	N/A
12	01100	V1 TWARN temperature sensor (Die temperature sensor)	1	1
13	01101	V1 temperature sensor	1	1
14	01110	Reserved	N/A	N/A
15	01111	V3 temperature sensor	1	1
16	10000	VDDIO voltage	2	3.25

Table 16. AMUX output selection*...continued*

Channel	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
17	10001	CAN temperature sensor	1	1
18	10010	VMON_EXT	1	1
19	11011	Reserved	N/A	N/A
20	11100	Reserved	N/A	N/A
21	10101	VCC5CAN	3.25	3.25
> 21	1xxxx	Reserved	N/A	N/A

It is possible to set the AMUX pin to high-impedance output by disabling the AMUX and the pulldown resistor using the AMUX_EN and AMUX_PD_DIS bits, respectively, from M_AMUX_CTRL register.

15.4 Electrical characteristics

AMUX electrical characteristics

Table 17. Electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO =1.8 V to 5.5 V, unless otherwise specified. I_{AMUX} = -1 mA to 1 mA, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
AMUX					
V_{AMUX_IN}	Input voltage range for VSUP, WAKE2, WAKE3, HVIO1 • AMUX_DIV = 0 • AMUX_DIV = 1	4.5 18	- -	20 40	V
V_{AMUX_OUT}	AMUX output voltage range	0.3	-	VDDIO – 0.2	V
R_{PD_AMUX}	Output pulldown resistance	200	400	800	kΩ
V_{AMUX_OFF}	Offset voltage	-8	-	8	mV
V_{AMUX_RATIO}	Ratio accuracy • Ratio 1 • Other ratio	-0.5 -1.5	- -	0.5 1.5	%
V_{TEMP25}	Temperature sensor voltage at 25 °C	1.36	1.38	1.4	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-3.95	-3.88	-3.8	mV/°C
T_{AMUX_SET}	Settling time	-	-	10	us
C_{AMUX_OUT}	Output capacitor	-	-	1	nF

16 I/O interface pins

16.1 WAKE2/HID0, WAKE3/HID1

WAKEx/HIDx pin has two different roles. It can be used either as a wake-up pin or as hardware ID detection pin.

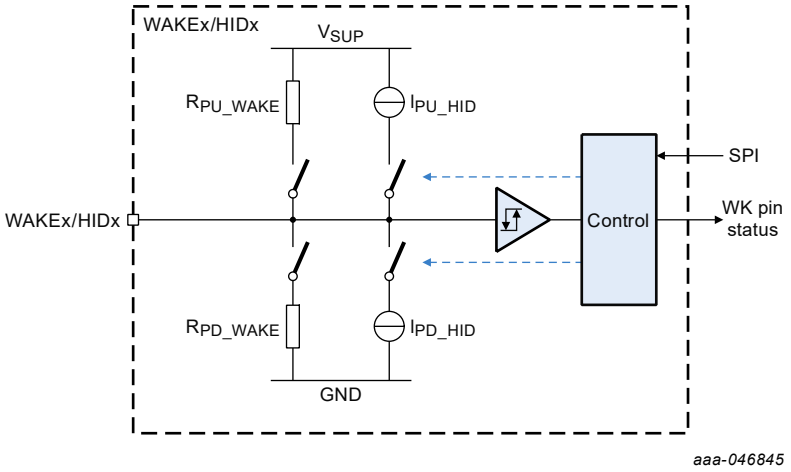


Figure 26. WAKEx/HIDx diagram

16.1.1 WAKE feature

WAKEx/HIDx pins are high-voltage inputs used as wake-up sources for the device.

WAKE2 and WAKE3 are wake-up input signals with analog measurement capability through AMUX. WAKE2 can be, for example, connected to a switched VBAT and WAKE3 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, an R - C protection is required.

In Normal mode, any event on the WAKE2 or WAKE3 pins generates a flag (WKx_I), when not masked (WKx_M). In Low-power modes, a wake-up event can be generated on high or low level depending on WKx_WUCFG[1:0] bits.

Wake-up filtering time is configurable by SPI using WKx_DGLT bits. Internal pulldown and pullup resistors can be enabled, disabled, or configured as cell repeater, as per WKxPUPD_OTP[1:0] bits.

Note: *Cell repeater configuration is used to reduce the current consumption. In this configuration, the pullup or pulldown selection follows the state of the internal buffer output after filtering. If the buffer output is low, pulldown resistor is selected. If the buffer output is high, the pullup resistor is selected.*

16.1.2 Hardware ID feature

Hardware ID feature comes on top of WAKE 2 pin and WAKE 3 pin to allow electronic control unit (ECU) location in the car based on WAKEx/HIDx pins hardware connection.

The WAKEx/HIDx pin state can be:

- Connected to VBAT
- Connected to GND
- Open

Using the two WAKEx/HIDx pins allows up to nine different hardware ID combinations.

This feature is only available in Normal mode and is activated by writing HIDWx_ENABLE = 1 in the M_HW_ID SPI register.

ECU identification is done by controlling the HID pullup and pulldown current sources (HIDWxPU/PD_EN or HIDWxPU/PD_DIS) and reading the associated WAKEx pin status using the WKx_S bits of the M_STATUS SPI register.

The pin threshold (HIDWx_TH_SEL), and pullup/pulldown current values (HIDWx_10MA_EN) are programmable via the M_HW_ID SPI register to allow integration into different systems.

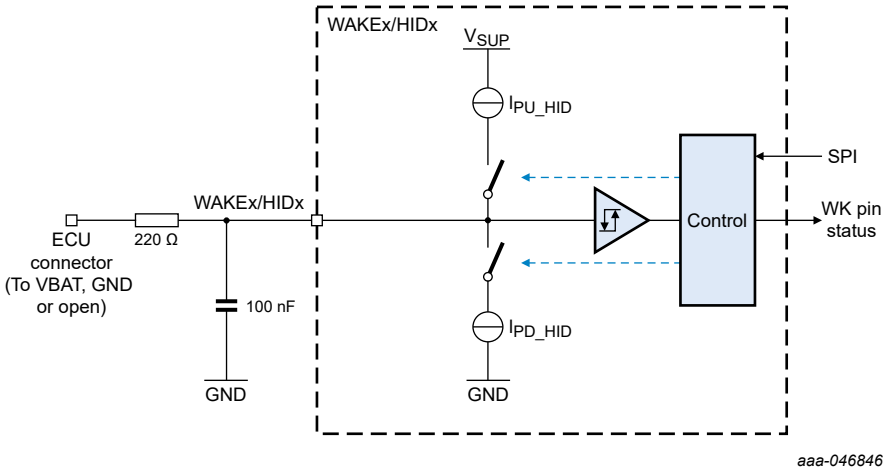


Figure 27. Example of application for hardware ID function (either using solution 1 OR 2)

In addition, the input buffer on the LIMP0 may be used as an additional HW ID pin if needed. In this case, an external bias current may be applied using a resistor as shown in Figure 28. To do so, the FS2400 must be programmed with LIMP0_EN_OTP = 0 and the MCU must configure LIMP0_GPO = 1 during INIT phase. The pin state is controlled using LIMP0_REQ and LIMP0_REL control bits. Its state can be read using LIMP0_SNS bit from FS_SAFETY_OUTPUTS SPI register.

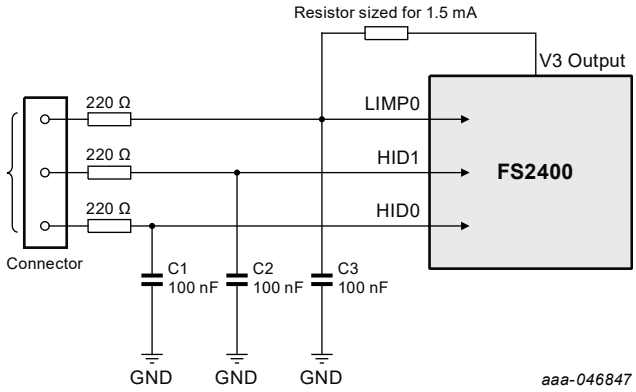


Figure 28. Using LIMP0 as a third HW ID pin

16.1.3 Electrical characteristics

Table 18. WAKE23/HID01 electrical characteristics

T_A = −40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
WAKE2, WAKE3					
V_{WAKE_IN}	Input voltage range	0	-	40	V
$WAKE23_{VILL}$	Digital low-input voltage threshold (falling) HIDW2/3_TH_SEL = 0	-	-	2.0	V
$WAKE23_{VILH}$	Digital high-input voltage threshold (falling) HIDW2/3_TH_SEL = 1	-	-	3.0	V
$WAKE23_{VIHL}$	Digital low-input voltage threshold (rising) HIDW2/3_TH_SEL = 0	2.97	-	-	V
$WAKE23_{VIHH}$	Digital high-input voltage threshold (rising) HIDW2/3_TH_SEL = 1	4	-	-	V
$WAKE23_{HYST}$	Hysteresis	100	-	400	mV
R_{PD_WAKE23}	Pulldown resistance	100	200	400	kΩ
R_{PU_WAKE23}	Pullup resistance	100	200	400	kΩ
I_{PD_HID01}	Low pulldown current for the hardware ID function (HIDW2_10MA_EN = 0)	3.5	4.25	5	mA
	High pulldown current for the hardware ID function (HIDW2_10MA_EN = 1)	8	10	12	mA
I_{PU_HID01}	Low pullup current for the hardware ID function (HIDW2_10MA_EN = 0)	1	1.5	2	mA
	High pullup current for the hardware ID function (HIDW2_10MA_EN = 1)	8	10	12	mA
I_{IN_WAKE}	Input current on WAKEx pins (No pull down or pull up)	-5	-	5	µA
T_{WAKE23_FLT}	Wake-up filtering time • WKx_DGLT = 0 • WKx_DGLT = 1	12 50	15 65	20 80	µs

16.2 HVIO1

HVIO1 pin is a high-voltage input/output. It can be used as input (as a wake-up source, a mode selection pin or an external device monitoring pin) or as open-drain output.

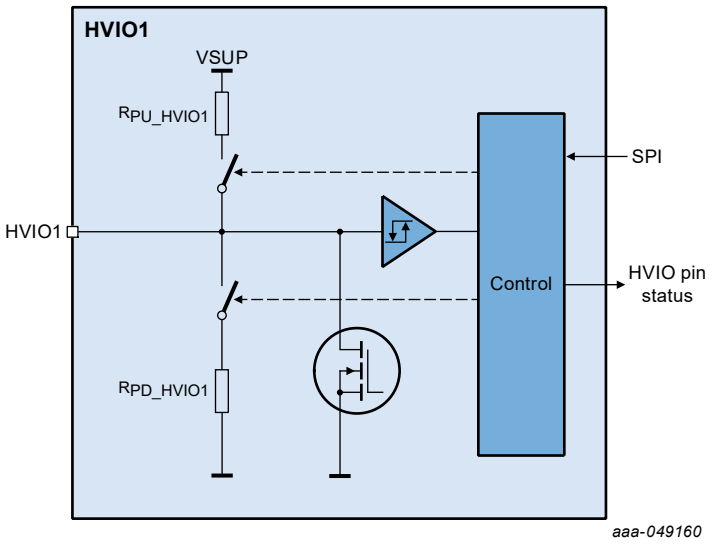


Figure 29. HVIO1 pin

16.2.1 HVIO1 used as input

The HVIO1 pin can be used as a simple wake-capable input. In this case, when the device is in Normal mode, any event on HVIO1 pin generates a flag (HVIO1_I), when not masked (HVIO1_M). In Low-power modes, wake-up event can be generated on level (high or low) depending on HVIO1_WUCFG[1:0] bits.

Using the same bits, the MCU can configure HVIO1 as "mode selection". When configured as mode selection, HVIO1 pin voltage level commands the transition between Normal mode and LPON (Low-power on). A logical low level makes FS2400 switch from Normal to LPON mode, a logical high level makes FS2400 switch from LPON to Normal mode.

When used as a wake-up source, wake-up filtering time is configurable by SPI using HVIO1_DGLY bit. Internal pulldown and pullup resistors can be enabled, disabled or configured as cell repeater as per HVIO1PUPD_OTP[1:0] bits.

Note: *Cell-repeater configuration is used to reduce the current consumption. In this configuration, the pullup or pulldown selection follows the state of the internal buffer output after filtering. If the buffer output is low, pulldown resistor is selected. If the buffer output is high, the pullup resistor is selected.*

When an HVIO pin is used as a global input pin, an R - C protection is required. See Section 11.

HVIO1 can also be configured as ERRMON input, to provide MCU or external device error detection. See Section 19.4.

16.2.2 HVIO1 used as output

HVIO1 can be configured as open-drain output by OTP via HVIO1_OUT_EN_OTP bits. In this case, the output state can be controlled by SPI using HVIO1HI and HVIO1LO control bits.

The default output state can be configured by OTP using HVIO1_OUT_DFLT_OTP. HVIO1 can also be assigned to one of the slots (SLOT0/1/2) by OTP using HVIO1_SLOT_POL_OTP. In this case, during power up, the pin follows the default state as soon as the OTP configuration is loaded in the mirror registers, and the pin

state is inverted when the configured slot starts. At power down, the pin goes back to its default value when the configured slot starts. See Figure 30 as an example of HVIO pins configuration, with HVIO1 default state low and assigned to SLOT1.

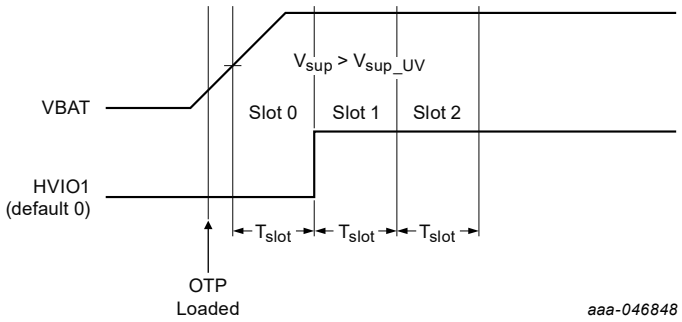


Figure 30. Example of HVIO1 pin configuration in the slots, at power up

16.2.3 Electrical characteristics

Table 19. HVIO1 electrical characteristics

T_A = −40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
HVIO1					
$HVIO1_{VIL}$	Digital low-input voltage threshold (falling)	-	-	2	V
$HVIO1_{VIH}$	Digital high-input voltage threshold (rising)	2.97	-	-	V
$HVIO1_{VIL}$	Digital low-input voltage threshold (falling) for mode selection	-	-	0.3 * VDDIO	V
$HVIO1_{VIH}$	Digital high-input voltage threshold (rising) for mode selection	0.7 * VDDIO	-	-	V
$HVIO1_{HYST}$	Hysteresis	100	-	400	mV
$HVIO1_{VOL}$	Low-output level (I_{OUT} = 2 mA)	-	-	0.4	V
$HVIO1_{ILIM}$	Current limitation	4	-	22	mA
I_{IN_HVIO1}	Input current on HVIO1 pin (No pull down or pull up)	-5	-	5	µA
R_{PD_HVIO1}	Pulldown resistance	100	200	400	kΩ
R_{PU_HVIO1}	Pullup resistance	100	200	400	kΩ
T_{HVIO1_FLT}	Wake-up filtering time • HVIO1_DGLT = 0 • HVIO1_DGLT = 1	 12 50	 15 65	 20 80	µs
T_{HVIO1_FALL}	Fall time using open drain (external pullup at VUP = 14 V, C_{OUT_HVIO1} = 10 nF)	-	-	30	µs
T_{HVIO1_WU}	Time between HVIO1 rising and V1 switching from PFM to PWM mode when HVIO1 configured as “mode selection” • LOAD_OTP_BYP = 0 • LOAD_OTP_BYP = 1	 - -	 150 50	 - -	µs

16.3 INTB

INTB is an open-drain output pin with internal pullup to VDDIO. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt.

An INTB pulse can be required for diagnosis by the MCU setting the SPI INTB_REQ bit in M_SYS_CFG SPI register.

16.3.1 Interrupts and wake-up events management

Two types of interruptions must be dissociated:

- "Classic" interrupts used to diagnose the device state and to report events
- Wake-up interrupts used to manage the wake-up from the Low-power modes

See Table 21 for a list of all interrupts.

The classic interrupts are maskable. If these interrupts are not masked, they will generate a pulse on INTB pin. Out of Normal mode, most of these interrupt flags will not be generated because the monitoring functions associated will be disabled. In addition, the WKx_I, HVIO1_I flags are not generated out of Normal mode.

WAKEx/HIDx pins, HVIO1 pin, CAN and LDT can be configured as wake-up sources using xxxx_WUEN[1:0] SPI configuration bits. Each wake-up source can be configured to generate an interrupt, a transition to Normal mode or both. In this last case, a wake-up event on these functions will generate a non-maskable wake-up flag (xxxx_WU_I) and an interrupt pulse on INTB.

In LPON mode, if a wake-up event occurs and the wake-up source is enabled, an interrupt is generated and/or the device transitions to Normal mode. If only the interrupt generation is enabled, it is the MCU decision to request a transition to Normal mode or not, via GO2NORMAL SPI bit.

In LPOFF mode, if a wake-up event occurs and the wake-up source is enabled, the device transitions to Normal mode.

16.3.2 Electrical characteristics

Table 20. INTB electrical characteristics

T_A = −40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Interrupt pin					
$INTB_{PULLUP}$	Internal pullup resistor to VDDIO	5	10	20	kΩ
$INTB_{VOL}$	Low-output level (I_{OUT} = 2 mA)	-	-	0.4	V
$INTB_{VOH}$	High-output level	VDDIO – 0.5	-	-	V
$INTB_{ILIM}$	INTB current limitation	4	-	22	mA
T_{INTB_PULSE}	Pulse duration (without output capacitor) • INTB_DUR = 0 (short) • INTB_DUR = 1 (long)	 17.5 70	 25 100	 32.5 130	µs
T_{INTB_TO}	INTB timeout for wake-up event	8	10	12	ms
T_{INTB_DLY}	Delay between INTB_REQ command reception and INTB pulse start	36	40	44	µs

Table 21. List of interrupts from main logic

Interrupt	Description	Mask/Enable
Event interrupt		
VSUPUV_4P7_I	VSUP 4.7 V threshold undervoltage	VSUPUV_4P7_M
VSUPUV_5P7_I	VSUP 5.7 V threshold undervoltage	VSUPUV_5P7_M
VSUPOV_I	VSUP overvoltage	VSUPOV_M

Table 21. List of interrupts from main logic*...continued*

Interrupt	Description	Mask/Enable
V1TWARN_I	V1 high temperature warning	V1TWARN_M
VxTSD_I	Vx overtemperature (x = 1, 3)	VxTSD_M
VxOC_I	Vx overcurrent (x = 1, 3)	VxOC_M
VxOV_I	Vx overvoltage (x = 0, 1, 3)	VxOV_M
VxUV_I	Vx undervoltage (x = 0, 1, 3)	VxUV_M
WKx_I	WAKEx state change in Normal mode (x = 2, 3)	WKx_M
HVIO1_I	HVIO1 state change in Normal mode	HVIO1_M
LDT_I	Long duration timer event	LDT_M
CAN_TSD_I	CAN overtemperature	CAN_TSD_M
CAN_TXD_TO_I	CAN dominant timeout	CAN_TXD_TO_M
WD_NOK_I	Watchdog refresh error	WD_NOK_M
INIT_CRC_NOK_I	INIT registers CRC error	INIT_CRC_NOK_M
Configurable wake-up event interrupt		
WKx_WU_I	WAKEx wake-up event (x = 2, 3)	WKx_WUEN[1:0]
HVIO1_WU_I	HVIO1 wake-up event	HVIO1_WUEN[1:0]
CAN_WU_I	CAN wake-up event	CAN_WUEN[1:0]
Non-configurable wake-up event interrupt		
GO2NORMAL_WU	SPI GO2NORMAL wake-up event	None
INT_TO_WU	Interrupt timeout generating a wake-up event	None
V1_UVLP_WU	V1 undervoltage wake-up event in LPON	None
WD_OFL_WU	WD error counter overflow wake-up event	None
EXT_RSTB_WU	External reset wake-up event	EXT_RSTB_DIS

17 Long duration timer (LDT)

FS24 features a long duration timer (LDT) with an integrated oscillator. The timer is configurable by SPI and can operate in normal and in Low-power modes. It provides several functions and offers a wide range of configurable counting periods, as well as a calibration mechanism for oscillator compensation.

The timer can be activated in Normal mode and all prescaler options can be selected to allow timer circuitry verification.

The timer is based on a 24-bits counter, with a 1 MHz oscillator, allowing a 1 second time base.

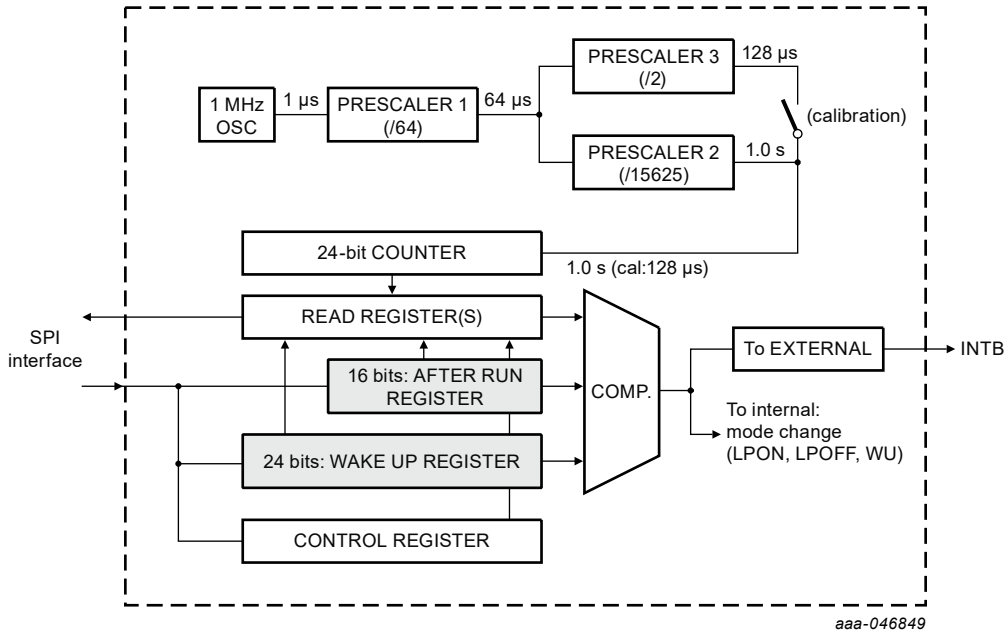


Figure 31. Long duration timer block diagram

In Normal mode operation, the timer can count up to 194 days, with 1 second resolution. In calibration mode, the prescaler 2 is bypassed and the timer can count up to 36 minutes, with 128 µs resolution.

Table 22. Long duration timer characteristics

Mode	Input clock frequency	Input clock period	Prescaler	Counter resolution	Max count	
Operation	1 MHz	1 µs	64 x 15625	1 s	4660 hrs	194 days
Calibration	1 MHz	1 µs	64 x 2	128 µs	2160 s	36 min

The LDT has two modes of operation based on the prescaler used during the count:

- When LDT_MODE = 0, the LDT is set in Long-count mode.
- When LDT_MODE = 1, the LDT is set in Short-count mode.

The LDT_AFTER_RUN[15:0] bits can set and read the after run value in Normal mode. When the run value corresponds to the timer value, that triggers either a transition to LP mode or an interrupt.

The LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits allows the MCU to set and read the wake-up value. The wake-up value corresponds to the timer value that triggers a wake-up event:

- The LDT_WUP_H[7:0] contains the eight most significant bits of the wake-up value.
- The LDT_WUP_L[15:0] contains the 16 least significant bits of the wake-up value.

The LDT_SEL bit allows the MCU to read the value of the 24-bits LDT counter in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.

- When LDT_SEL = 0, the MCU reads or writes the wake-up value in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.
- When LDT_SEL = 1, the MCU reads the counter current value.

The LDT_EN bit shall be provided to start the LDT timer operation:

- When LDT_EN = 0, the LDT is disabled.
- When LDT_EN = 1, the LDT starts counting as defined in the M_LDT_CTRL and L_LDT_CFGx registers.

The LDT2LP bit selects which Low-power mode (LPON or LPOFF) it needs to go once the after-run timer is expired, when timer function 2 or 3 is selected.

- When LDT2LP = 0, the device goes into LPON mode when the after-run timer expires.
- When LDT2LP = 1, the device goes into LPOFF mode when the after-run timer expires.
- When timer function 4 or 5 is selected and the LDT_EN = 1, the LDT does not start any count until the device enters the corresponding Low-power mode.

17.1 Calibration procedure

The calibration procedure consists of the MCU activating the counter for a specific duration. Once the timer expires, the MCU reads back the timer final value, compares it with its own accurate time of activation to calculate a time offset. It is recommended to perform the calibration between -20 °C and +85 °C.

Calibration example:

- Set the Timer mode to short count and select the timer function 1. Set the after-run value at max value 0xFFFF (~8.39 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 6 s.
- If the oscillator period is at the exact typical value (absolutely no deviation error), expected reading is 46875.
- The exact reading calculates the error correction factor ECF = exact_reading / expected_reading
- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.
- After calibration, the new after-run or wake-up values to set the counter are “after run x ECF” and “wake-up x ECF”.

17.2 Timer functions

Table 23. LDT functions

LDT_FNCT[2:0]	LDT Function
000	**Function 1:** In Normal mode, count and generate a flag or an interrupt when the counter reaches the after-run value.
001	**Function 2:** In Normal mode, count until the counter reaches the after-run value and enters Low-power mode.
010	**Function 3:** In Normal mode, count until the counter reaches the after-run value and enters Low-power mode. Once in Low-power mode, count until the counter reaches the wake-up value and wakes up.
011	**Function 4:** In Low-power mode, count until the counter reaches the wake-up value and wakes up.
100	**Function 5:** In Low-power mode, count and do not wake up unless the counter overflow occurs or if the device wakes up by wake-up input source.

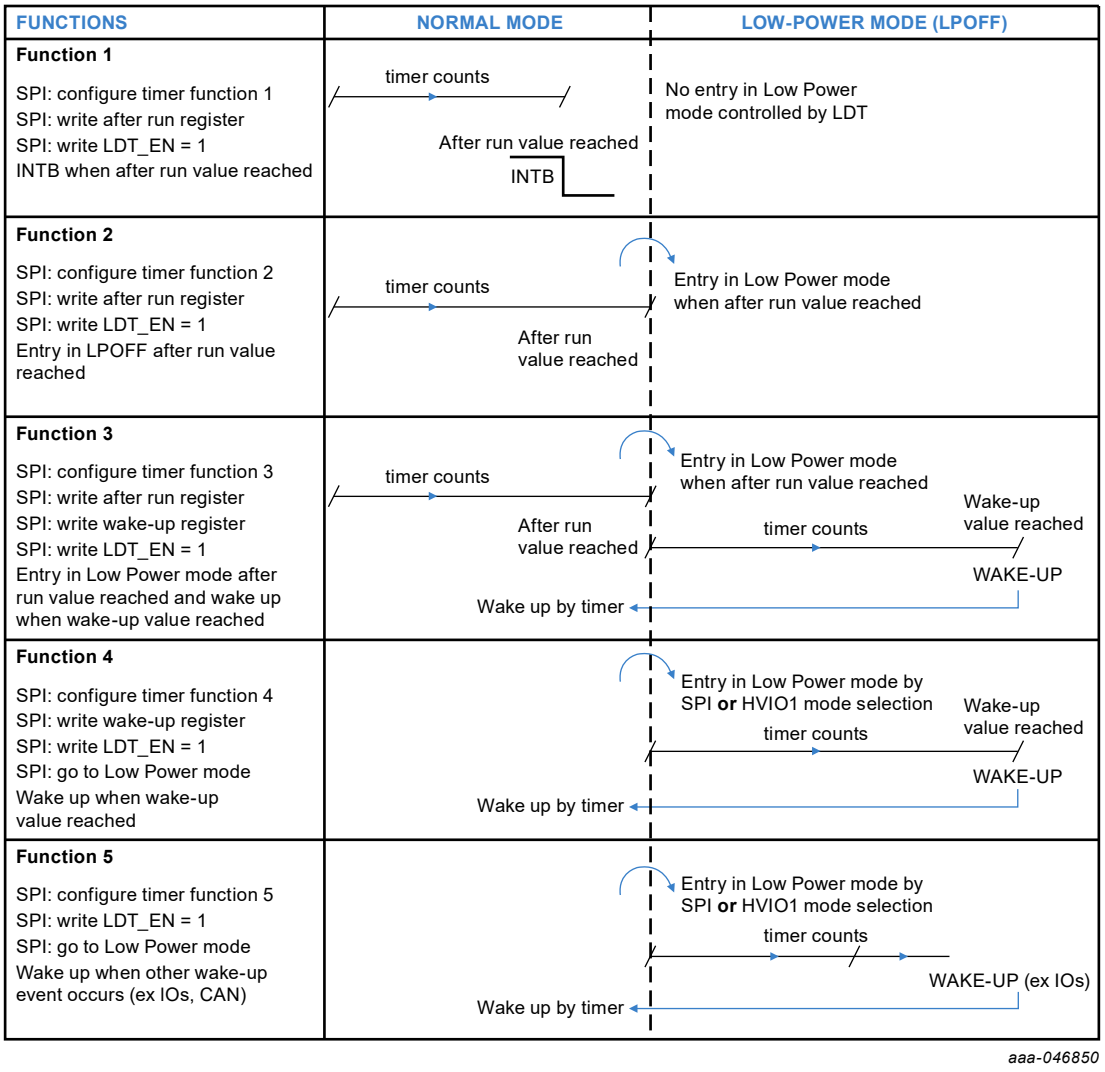


Figure 32. Long duration timer functions

17.3 Electrical characteristics

Table 24. Long duration timer electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 18 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
$F_{IN\_CLK\_LDT}$	Long duration timer source clock (1 MHz / 64)	-	15.625	-	kHz
	T_{BASE_LDT}	- -	1 128	- -	s µs
$I_{Q\_LDT\_85}$	Long duration timer quiescent current consumption (Tj = 85 °C)	-	2	5	µA
$I_{Q\_LDT\_125}$	Long duration timer quiescent current consumption (Ta = 125 °C)	-	5	10	µA
LDT_{ACC1}	Long duration timer accuracy without calibration	-10	-	10	%
LDT_{ACC2}	Long duration timer accuracy with calibration In LPOFF or LPON states Including month aging drift (max) Including temperature drift 0 °C < Tj < 85 °C	-5	-	5	%
LDT_{DRIFT}	Long duration timer maximum drift per hour after calibration In LPOFF or LPON states Within 20 °C temperature variation.	-1	-	1	%

18 Physical layer

18.1 CAN FD transceiver

FS24 device includes an integrated CAN FD transceiver, 5 Mbps capable, developed in compliance with the ISO 11898-2:2016 and SAE J2284 standards. The CAN FD transceiver is compliant with SAE J2962-2 (2019) and IEC 62228-3 (2019) for EMC performances. It provides the physical interface between the CAN protocol controller of an MCU and the physical CAN bus.

The CAN FD transceiver bus driver is meant to be supplied through the VCC5CAN pin. The CAN can be supplied by V1 or by V3. No matter which channel is used, the pin should be supplied by 5 V.

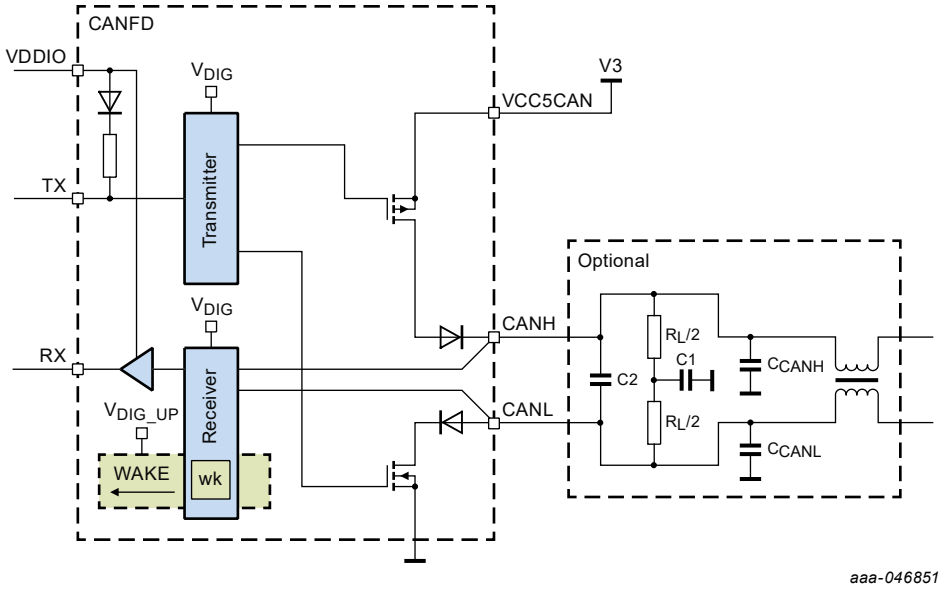


Figure 33. CAN FD transceiver internal diagram, with external components

18.1.1 CAN operating modes

The CAN transceiver has four modes:

- Off
- Wake-capable
- Listen-only
- Active

The Listen-only and Active modes are only available when the device is in Normal mode. In Low-power modes, the transceiver can be kept in Wake-capable mode in order to be used as a wake-up source for the device and the module.

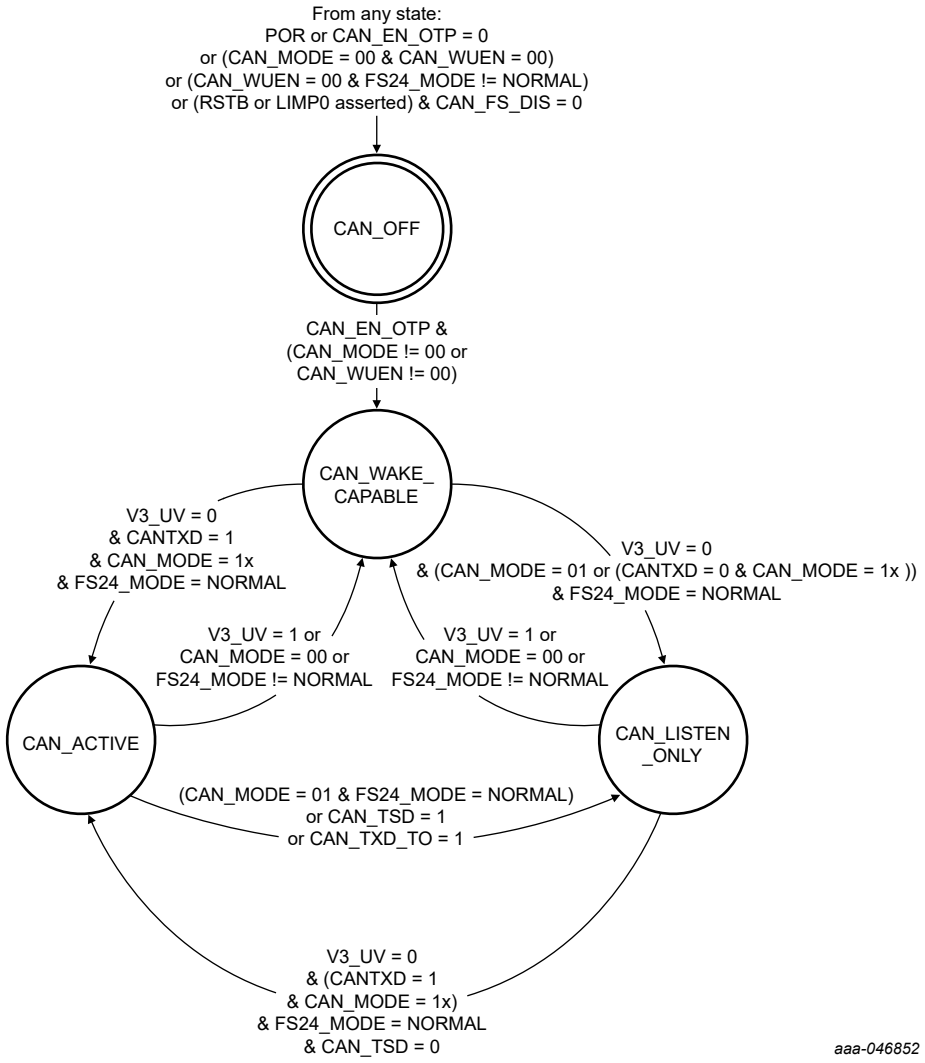


Figure 34. CAN transceiver state machine

18.1.1.1 CAN off mode

When the CAN mode is set to 2b'00 and the CAN wake-up capability is disabled, or if the device is not in Normal mode, for example in LPON or LPOFF modes, and the wake-up capability is disabled, the CAN transceiver is in OFF mode. The CAN transceiver can also transition to OFF mode if RSTB or LIMP0 is asserted and the MCU has set the CAN_FS_DIS bit to 0.

In this mode, the normal and low-power receivers and the transmitter of the CAN transceiver are disabled, the CANH and CANL pins are set high ohmic, and the CANRXD pin is driven high.

18.1.1.2 CAN Wake-capable mode

The CAN transceiver is in Wake-capable mode as soon as the CAN mode is different from 2b'00 or as soon as the wake-up capability of the CAN is enabled, regardless of the device state once powered up.

In this mode, the CAN transmitter and the CAN normal receiver are disabled. Only the low-power wake-capable receiver is enabled to allow wake-up pattern detection and device wake-up, when the device is in Low-power

mode. The CANH and CANL pins are biased to ground via the common-mode input resistor $R_{CAN\_IN\_CM}$ and the CANRXD pin is driven high.

18.1.1.3 CAN wake-up

When the CAN transceiver is in Wake-capable mode, a valid CAN wake-up is detected when a dominant – recessive – dominant pattern is observed on the CAN bus, where the dominant and recessive phases are longer than $T_{CAN\_WU\_FILT}$. The total pattern is valid only if it is shorter than the wake-up timeout time $T_{CAN\_WU\_TO}$.

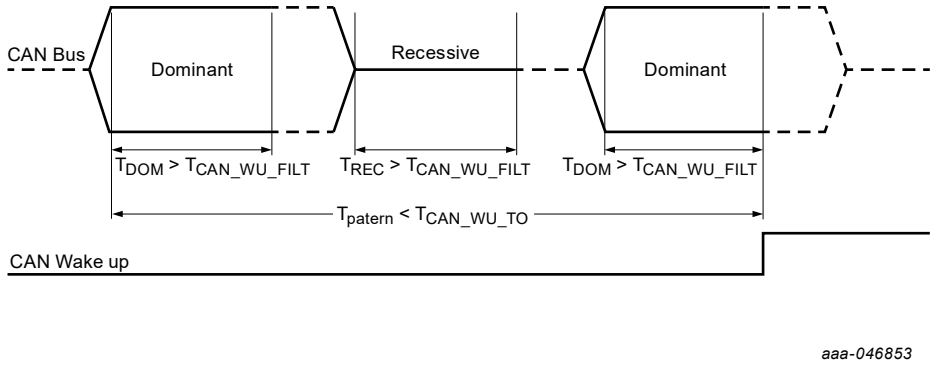


Figure 35. CAN Wake-up timing diagram

After a CAN wake-up event if CAN_WU_TMR_BYP = 0, once the FS2400 state machine reaches Normal mode, CANRXD pin will be asserted low for 1.5 ms.

CAN_WU_I flag indicates that the FS2400 woke up from Low-power mode after a CAN wake-up pattern. The flag must be cleared after each wake-up event in order for the CAN communication to work properly.

18.1.1.4 CAN Listen-only mode

The CAN transceiver Listen-only mode is entered from Wake-capable mode when CAN mode is set to 2b’01 or when CAN mode is set to 2b’10 or 2b’11 and CANTXD is low (bus dominant) for more than $T_{CAN\_DOM\_TO}$. The device must be in Normal mode and no undervoltage on V3 must be detected.

In this mode, CANH and CANL pins are biased to 0.5 x V3 and CANTXD is maintained high by an internal pullup resistor R_{CANTXD_PU} connected to VDDIO.

The low-power wake-up receiver and the transmitter are disabled. Only the normal receiver is enabled. The device is only able of reporting the bus level to the CANRXD pin. The device is not able to transmit information from TXD to the bus.

18.1.1.5 CAN Active mode

The CAN transceiver Active mode is entered from Wake-capable or Listen-only mode when CAN mode is set to 2b’10 or 2b’11 and CANTXD is high (bus recessive). The device must be in Normal mode and no undervoltage on V3 should be detected. When a TSD- or a CAN-dominant timeout is detected, the transceiver goes back to Listen-only mode and the transmitter is disabled.

In this mode, the normal receiver and the transmitter are enabled, and the low-power receiver is disabled. The device can transmit information from CANTXD to the CAN bus and report the bus level to the CANRXD pin.

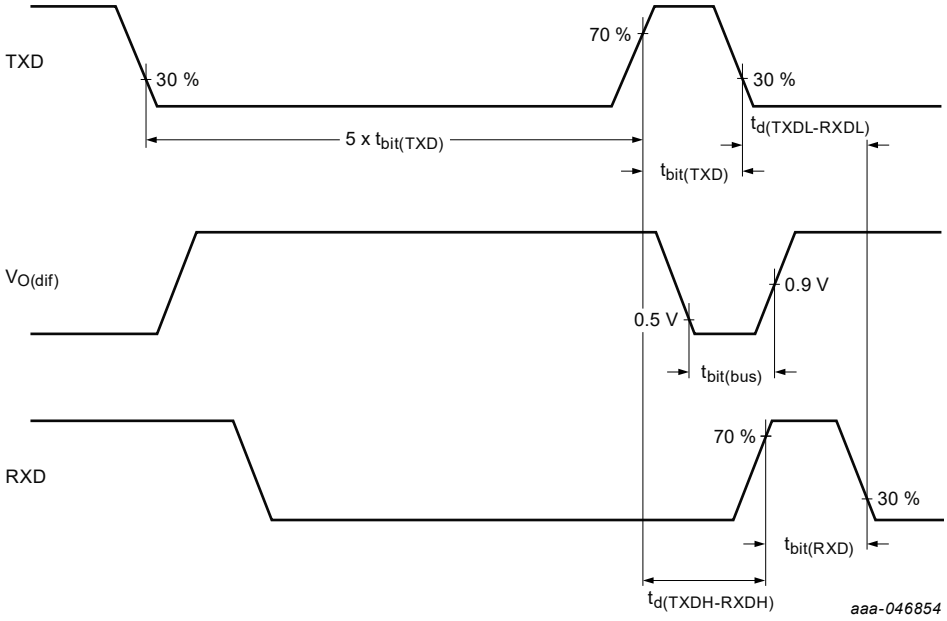


Figure 36. CAN timing definition according to ISO 11898-2:2016

18.1.2 Electrical characteristics

Table 25. CAN FD transceiver characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. $V_{VCC5CAN}$ = 4.5 to 5.5 V, unless otherwise specified. VDDIO = 1.8 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static characteristics					
CANTXD					
V_{CANTXD_IH}	CANTXD input threshold high	0.7 x VDDIO	-	-	V
V_{CANTXD_IL}	CANTXD input threshold low	-	-	0.3 x VDDIO	V
R_{CANTXD_PU}	CANTXD pullup resistance	90	200	400	kΩ
CANRXD					
V_{CANRXD_OH}	CANRXD output high level, I_{OUT} = -2 mA	VDDIO – 0.4 V	-	-	V
V_{CANRXD_OL}	CANRXD output low level, I_{OUT} = 2 mA	-	-	0.4	V
CAN Bus					
$V_{CAN\_DIFF\_MAX}$	CAN maximum rating for VDIFF	-5	-	10	V
$V_{CANH\_OUT\_DOM}$	CAN dominant output voltage on pin CANH, Active mode R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
$V_{CANL\_OUT\_DOM}$	CAN dominant output voltage on pin CANL, Active mode R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{CAN\_OUT\_SYM}$	CAN output voltage symmetry (V_{CANH} + V_{CANL}), Active mode F_{CANTXD} = 1 MHz (2 Mbps), RL = 60 Ω, C1 = 4.7 nF	0.9 x V3	1 x V3	1.1 x V3	V
$V_{CAN\_OUT\_CM\_PK}$	CAN common mode peak-to-peak voltage, Active mode	-	-	300	mV

Table 25. CAN FD transceiver characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. $V_{VCC5CAN}$ = 4.5 to 5.5 V, unless otherwise specified. VDDIO = 1.8 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{CAN\_OUT\_DIFF\_DOM}$	CAN bus differential output voltage, Active mode, dominant state, $V_{VCC5CAN}$ = 4.75 V to 5.5 V, R_L = 50 Ω to 65 Ω	1.5	2	3	V
	CAN bus differential output voltage, Active mode, dominant state, $V_{VCC5CAN}$ = 4.75 V to 5.5 V, R_L = 45 Ω to 75 Ω	1.4	2	3.3	V
	CAN bus differential output voltage, Active mode, dominant state, $V_{VCC5CAN}$ = 4.75 V to 5.5 V, R_L = 2240 Ω	1.5	-	5	V
$V_{CAN\_OUT\_DIFF\_REC}$	CAN bus differential output voltage, ACTIVE mode and recessive state, or Listen-only mode, or Wake capable mode, bus biasing active $V_{VCC5CAN}$ = 4.75 V to 5.5 V, no load, C1 = C2 = C_{CANRXD} = 0 pF	-50	-	50	mV
$V_{CAN\_OUT\_DIFF\_REC}$	CAN bus differential output voltage, Wake-capable mode, recessive state, no load	-0.2	0	0.2	V
$V_{CAN\_OUT\_REC\_ACT}$	CAN recessive output voltage, Active mode, no load	2	-	3	V
$V_{CAN\_OUT\_REC\_WC}$	CAN recessive output voltage, Wake-capable mode, no load	-0.1	0	0.1	V
$V_{CAN\_OUT\_REC\_LO}$	CAN recessive output voltage, Listen-only mode, no load, $V_{VCC5CAN}$ = 0 V	2	2.5	3	V
$V_{CAN\_IN\_DIFF}$	CAN differential receiver threshold voltage, Active or Listen-only mode	0.5	0.8	0.9	V
$V_{CAN\_IN\_DIFF\_LP}$	CAN differential low power receiver threshold voltage, Wake-capable mode	0.4	0.7	1.15	V
$V_{CAN\_IN\_DIFF\_HYST}$	CAN differential receiver hysteresis voltage, Active or Listen-only mode	50	200	400	mV
$V_{CAN\_IN\_DIFF\_REC}$	CAN recessive state differential input voltage range, Active or Listen-only mode, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	-4	-	0.5	V
	CAN recessive state differential input voltage range, no biasing, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	-4	-	0.4	V
$V_{CAN\_IN\_DIFF\_DOM}$	CAN dominant state differential input voltage range, Active or Listen-only mode, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	0.9	-	9	V
	CAN dominant state differential input voltage range, no biasing, V_{CANH} = -12 V to 12 V, V_{CANL} = -12 V to 12 V	1.1	-	9	V
$R_{CAN\_IN\_CM}$	CAN common mode input resistance, Active mode V_{CANH} = -2 V to 7 V, V_{CANL} = -2 V to 7 V	6	-	50	kΩ
$R_{CAN\_IN\_DIFF}$	CAN differential input resistance V_{CANH} = -2 V to 7 V, V_{CANL} = -2 V to 7 V	12		100	kΩ
ΔR_{CAN_IN}	CAN input resistance deviation V_{CANH} = V_{CANL} = 5 V	-3	-	3	%
$C_{CAN\_IN\_CM}$	CAN Common mode input capacitance	-	-	20	pF
$C_{CAN\_IN\_DIFF}$	CAN differential input capacitance	-	-	10	pF
$I_{CANH\_OUT\_SC}$	CANH short circuit output current, Active mode, dominant state, $V_{VCC5CAN}$ =5 V, V_{CANH} = -15 V to 40 V	-115	-	-	mA
$I_{CANL\_OUT\_SC}$	CANL short circuit output current, Active mode, dominant state, $V_{VCC5CAN}$ = 5 V, V_{CANL} = -15 V to 40 V	-	-	115	mA
$I_{CAN\_OUT\_REC}$	CAN recessive output current, recessive state, V_{CANH} = V_{CANL} = -27 V to 32 V	-3	-	3	mA

Table 25. CAN FD transceiver characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. $V_{VCC5CAN}$ = 4.5 to 5.5 V, unless otherwise specified. VDDIO = 1.8 V to 5.5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$I_{CAN\_ACT\_DOM}$	CAN current consumption, Active mode, dominant state, Tj = 150 °C, $V_{VCC5CAN}$ = 5 V	-	-	60	mA
$I_{CAN\_ACT\_REC}$	CAN current consumption, Active mode, recessive state, Tj = 150 °C, $V_{VCC5CAN}$ = 5 V	1	4	7	mA
I_{CAN_WU}	CAN current consumption, wake-up capability, Tj = 85 °C, VBOS = 5 V	1	3	10	µA
I_{QCANH}	CANH input leakage current V_{CANH} = 5 V, all supply inputs connected to GND	-10	-	10	µA
I_{QCANL}	CANL input leakage current, V_{CANL} = 5 V, all supply inputs connected to GND	-10	-	10	µA
Dynamic characteristics					
T_{CAN_EN}	Setup time needed when going to Active mode of the transceiver before sending data.	15	17	19	µs
$T_{CAN\_DOM\_TO}$	CAN CANTXD dominant timeout time	0.8	-	9	ms
T_{CAN_LOOP}	CAN loop delay time from CANTXD to CANRXD, C_{CANRXD} = 15 pF, R_L = 45 Ω to 70 Ω, C_{CAN} = 100 pF, F_{CANTXD} < 2.5 MHz	-	-	255	ns
$T_{CAN\_TX2BUS\_DOM}$	CAN delay time from CANTXD to bus dominant	-	-	127.5	ns
$T_{CAN\_TX2BUS\_REC}$	CAN delay time from CANTXD to bus recessive	-	-	127.5	ns
$T_{CAN\_BUS2RX\_DOM}$	CAN delay time from bus dominant to CANRXD	-	-	127.5	ns
$T_{CAN\_BUS2RX\_REC}$	CAN delay time from bus recessive to CANRXD	-	-	127.5	ns
$T_{CAN\_BIT\_RX\_2M}$	CAN received recessive bit width @ 2 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	400	500	550	ns
$T_{CAN\_BIT\_RX\_5M}$	CAN received recessive bit width @ 5 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	120	200	220	ns
$T_{CAN\_BIT\_BUS\_2M}$	CAN transmitted recessive bit width @ 2 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	435	500	530	ns
$T_{CAN\_BIT\_BUS\_5M}$	CAN transmitted recessive bit width @ 5 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	155	200	210	ns
$\Delta T_{CAN\_BIT\_RXBUS\_2M}$	CAN receiver timing symmetry @ 2 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	-65	-	40	ns
$\Delta T_{CAN\_BIT\_RXBUS\_5M}$	CAN receiver timing symmetry @ 5 Mbps R_L = 60 Ω, C_{CANRXD} = 15 pF, C1 = 0 nF , C2 = 100 pF	-45	-	15	ns
$T_{CAN\_WU\_FILT}$	CAN recessive/dominant filter time for wake-up	0.5	1.4	1.8	us
$T_{CAN\_WU\_TO}$	CAN wake-up timeout time	0.8	-	10	ms

19 Safety

19.1 Functional description

The FS24 includes multiple safety mechanisms to guarantee the functional safety of the system and reach up to ASIL B level. Safety features are configurable, either by OTP or by SPI, allowing scalability depending on the application needs. FS24 also provides an on-demand ABIST to cover latent faults.

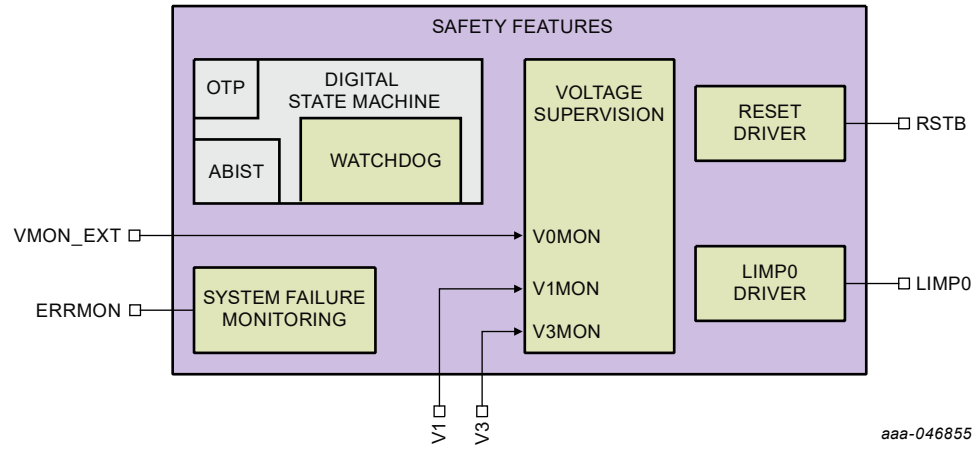


Figure 37. Fail-safe features block diagram

19.2 Watchdog

A watchdog is implemented through the SPI bus to continuously check the microcontroller software activity and its ability to perform basic computing. FS24 checks by awaiting a specific answer from the microcontroller during a predefined period called the watchdog window. The first half of the watchdog window is said *closed* and the second half is said *open*.

A good watchdog refresh is a good watchdog answer during the open window. A bad watchdog refresh is a bad watchdog answer during the open window, no watchdog refresh during the open window or a good watchdog answer during the closed window. After a good or a bad watchdog refresh, a new window period starts immediately for the microcontroller to keep the synchronization with the windowed watchdog. The first good watchdog refresh closes the initialization phase of the FS24. Then the watchdog window is running and the microcontroller must refresh the watchdog in the open window of the watchdog window period.

The watchdog functionality can be enabled or disabled by OTP with WD_INF_OTP bit. The duration of the watchdog window is configurable from 1 ms to 16384 ms with the WDW_PERIOD[3:0] SPI bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window can be disabled only during the initialization phase of the FS24. The watchdog disable is effective when the initialization phase is closed. The watchdog configuration requires the MCU to write in FS_WDW_CFG registers.

In LPON mode, the watchdog stays enabled or is disabled depending on WD_DIS_LPON bit (configurable during INIT phase). When enabled in LPON, the watchdog operates in Timeout mode.

The watchdog uses two keys, 0x5AB2 (default value after POR) and 0xD564 to validate the answer. The key is stored in the WD_TOKEN register, and is changed alternatively after each good WD refresh.

The MCU reads the WD_TOKEN register and writes the correct answer (WD_TOKEN register value) through the SPI in WD_ANSWER register, in the right timing. The WD error counter is incremented when the answer is wrong or not given at the right moment, or not given at all at the end of the watchdog period.

When the watchdog is disabled (for example, RSTb event or transition to LPON with WD_DIS_LPON = 1), the watchdog configuration is reset as it would be after a POR. The watchdog token is set to 0x5AB2,the window period is set to 256 ms, and the watchdog type is set to timeout watchdog.

Table 26. Watchdog window period configuration

WDW_PERIOD[3:0]	Watchdog window period
0000	DISABLE (infinite open window)
0001	1 ms
0010	2 ms
0011	4 ms
0100	8 ms
0101	16 ms
0110	32 ms
0111	64 ms
1000	128 ms
1001 (default)	**256 ms**
1010	512 ms
0011	1024 ms
1100	2048 ms
1101	4096 ms
1110	8192 ms
1111	16384 ms

19.2.1 Watchdog selection

Two types of watchdog monitoring, timeout and window watchdog, are implemented and can be selected and changed during operation by SPI using WDW_EN bit.

Table 27. Watchdog type configuration

WDW_EN	Watchdog type selection
0	**Timeout watchdog (default)**
1	Window watchdog

19.2.1.1 Timeout watchdog

The timeout watchdog is the default configuration at start up. In this mode, the watchdog period is considered fully open, and the MCU writes the correct value in WD_ANSWER register before the period ends. If the answer is wrong, or if the answer is not sent before the watchdog timer overflows, the WD error counter is incremented and WD_NOK_I flag is set to 1.

19.2.1.2 Window watchdog

The window watchdog can be enabled by SPI by setting WDW_EN bit at 1. In this mode, the watchdog period is divided in two. The first half is said *closed* and the second is said *open*. The MCU writes the correct value in WD_ANSWER register during the open window. If the answer is wrong, or if the answer is sent during the closed window, or if the answer is not sent before the watchdog timer overflows, the WD error counter is incremented and WD_NOK_I flag is set to 1.

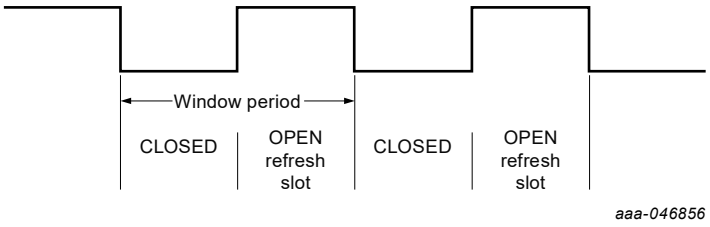


Figure 38. Window watchdog time diagram

Table 28. Watchdog answer and refresh validation

SPI	Window WD		Timeout WD
	CLOSED	OPEN	(always open)
BAD key	WD_NOK	WD_NOK	WD_NOK
GOOD key	WD_NOK	WD_OK	WD_OK
None (timeout)	N/A	WD_NOK	WD_NOK

19.2.2 Watchdog error counter

A watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The watchdog error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures a cyclic OK/NOK behavior converges to a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable with the WD_ERR_LIMIT[1:0] bits during the INIT phase.

Table 29. Watchdog error counter limit configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter value
00	8
01 (default)	**6**
10	4
11	2
Reset condition	POR

The watchdog error counter value can be read by the MCU for diagnostic with the WD_ERR_CNT[3:0] bits.

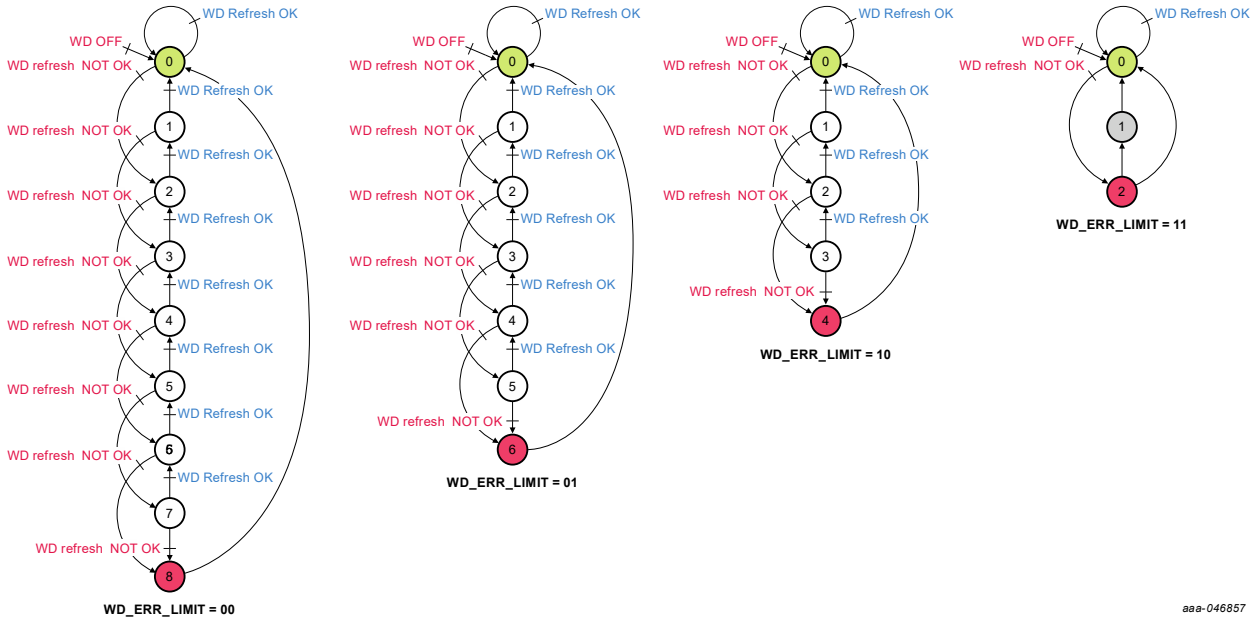


Figure 39. Watchdog error counter configurations

19.2.3 Watchdog refresh counter

The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by 1. Each time the watchdog refresh counter reaches its maximum value (6 by default) and if next WD refresh is also good, the fault error counter is decremented by 1. Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to 0.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable with the WD_RFR_LIMIT[1:0] bits during the INIT_FS phase.

Table 30. Watchdog refresh counter limit configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (default)	**6**
01	4
10	2
11	1
Reset condition	POR

The watchdog refresh counter value can be read by the MCU for diagnostic with the WD_RFR_CNT[2:0] bits.

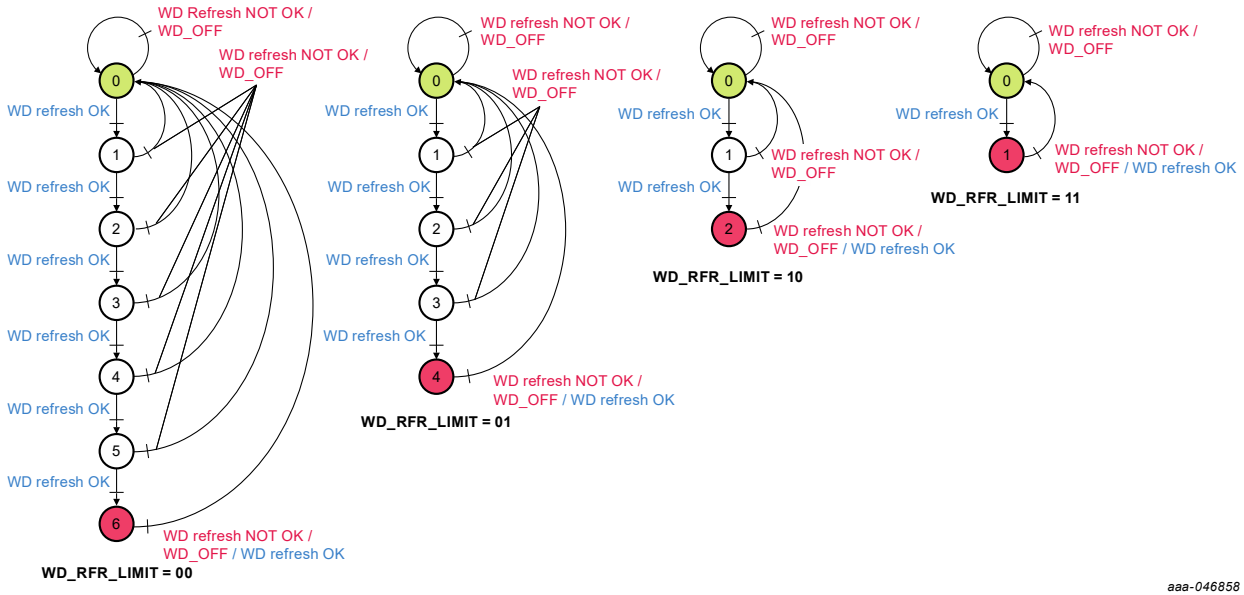


Figure 40. Watchdog refresh counter configurations

19.2.4 Watchdog error impact

When the watchdog error counter reaches its maximum value, in Normal mode or in LPON mode, the fail-safe reaction on RSTB or LIMP0 is configurable with the WD_RSTB/LIMP0_IMPACT bits during the INIT phase. If it happens in LPON mode, the device also wakes up.

Table 31. Watchdog error impact configuration

WD_RSTB/LIMP0_IMPACT	WD impact on RSTB/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/LIMP0 is asserted**
Reset condition	POR

19.2.5 Watchdog electrical characteristics

Table 32. Watchdog electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Watchdog					
WD_{PER_ACC}	Watchdog period accuracy	-10	-	10	%
WD_{DUTY_CYCLE}	Window watchdog duty cycle	47.5	50	52.5	%

19.3 Voltage supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of all the supply generated by the FS24, Vx (x = 1, 3), and of VMON_EXT input pin. The overvoltage monitoring is activated before the power-up slots start. The undervoltage monitoring is activated once the device is in Normal mode. UV/OV flags are then reported accordingly. VMON0 monitoring on VMON_EXT pin is enabled by OTP (V0MON_EN_OTP).

19.3.1 V0MON (VMON_EXT) monitoring

VMON_EXT input pin can be connected to an external regulator. The regulator connected to VMON_EXT must be at least 1 V to be compatible with overvoltage and undervoltage monitoring thresholds. An external resistor bridge must be used to divide the regulator voltage if higher than 1 V. The resistor bridge middle point voltage must be set to 1 V. The external resistors accuracy must be at least ±1 %, to ensure a total accuracy of ±2.5 % with the internal thresholds accuracy (±1.5 %).

The MCU can monitor VMON_EXT pin voltage using the AMUX by selecting channel 18, see Section 15.3.

19.3.2 VxMON monitoring (x = 1, 3)

V1 and V3 regulators are monitored via the corresponding V1 and V3 pins, which also serve as feedback pins. The expected voltage for each regulator is automatically selected based on the OTP output voltage configuration.

Each voltage monitoring channel is connected to a pulldown resistor to detect an undervoltage in case of disconnection.

The VxMON UV/OV threshold have ±1 % accuracy (trimmed at 5 V setting, 5 % VMON threshold).

19.3.3 VxMON UV/OV threshold

The OV and UV thresholds are configured independently for each VxMON (x = 0, 1, 3) by OTP at VxMON_UVTH_OTP[3:0] and VxMON_OVTH_OTP[3:0]. UV thresholds are configurable from 96.5 % to 91.5 % and OV thresholds are configurable from 102.5 % to 110 %. When a regulator is configured at 5 V, five additional UV thresholds are available at 62 %, 63.5 %, 64 %, 64.5 %, and 65 %.

Table 33. VMON UV/OV threshold configuration

VMONx_UVTH_OTP[3:0] VMONx_OVTH_OTP[3:0]	VMONx undervoltage threshold configuration	VMONx overvoltage threshold configuration
0000	65 %	102.5 %
0001	64.5 %	103.0 %
0010	96.5 %	103.5 %
0011	96.0 %	104.0 %
0100	95.5 %	104.5 %
0101	95.0 %	105.0 %
0110	94.5 %	105.5 %
0111	94.0 %	106.0 %
1000	93.5 %	106.5 %
1001	93.0 %	107.0 %
1010	92.5 %	107.5 %
1011	92.0 %	108.0 %
1100	91.5 %	108.5 %
1101	64 %	109.0 %
1110	63.5 %	109.5 %
1111	62 %	110.0 %

19.3.4 VxMON deglitch time

The OV and UV deglitch times are configured independently by OTP at VxMON_UVDGLT_OTP[1:0] and VxMON_OVDGLT_OTP.

Table 34. VMON deglitch time configuration

VxMON_UVDGLT_OTP[1:0]	UV detection time	VxMON_OVDGLT_OTP	OV detection time
00	5 µs	0	25 µs
01	15 µs	1	45 µs
10	25 µs		
11	40 µs		

19.3.5 VxMON safety reaction (impact)

When an overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB and LIMP0 is configurable with VxMON_OV/UV_RSTB/LIMP0_IMPACT bits during the INIT phase, for each monitoring input. The reactions of RSTB pin can be preconfigured by OTP. Also, if an OV fault occurs for Vx, the OV power rail will turn itself off or enter Fail-safe mode using the CONF_Vx_OV_OTP setting in OTP.

19.3.6 V1UVLP monitoring

In LPON mode, all the VxMON monitoring is disabled. Only V1 is monitored for undervoltages at V1_UVLP, which is configurable using the V1UVLP_TH_OTP OTP bit. In case the V1 voltage goes lower than this threshold, the device goes into fail-safe state (not configurable), and V1_UVLP_WU bit is set to 1.

V1 is also monitored for V1UVLP when the device powers up after a wake-up from LPON, and during a cold start after $T_{SOFT\_START\_V1}$. If at the end of the softstart V1 is still under V1UVLP threshold, then the device goes into fail-safe state.

19.3.7 Electrical characteristics

Table 35. VxMON electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VxMON (x from 0 to 3)					
VxMON_OVTH	VxMON overvoltage threshold	-	102.5+0.5*code_ov	-	%
VxMON_UVTH	VxMON undervoltage thresholds (code_uv = 0010 to 1100)	-	96.5-0.5*code_uv	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 0000)	-	65	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 0001)	-	64.5	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1101)	-	64	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1110)	-	63.5	-	%
	VxMON undervoltage threshold at 5 V output voltage (code_uv = 1111)	-	62	-	%
$VxMON_{OV\_ACC}$	V0MON OV threshold maximum accuracy	-1	-	1	%
$VxMON_{UV\_ACC}$	V0MON UV threshold maximum accuracy	-1	-	1	%

Table 35. VxMON electrical characteristics*...continued*

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
T_{OV_DGLT}	VxMON overvoltage deglitch time (VxMON_OVDGLT_OTP = 0)	20	25	30	µs
	VxMON overvoltage deglitch time (VxMON_OVDGLT_OTP = 1)	40	45	50	µs
T_{UV_DGLT}	VxMON undervoltage deglitch time (VxMON_UVDGLT_OTP[1:0] = 00)	2.5	5	7.5	µs
	VxMON undervoltage deglitch time (VxMON_UVDGLT_OTP[1:0] = 01)	10	15	20	µs
	VxMON undervoltage deglitch time (VxMON_UVDGLT_OTP[1:0] = 10)	20	25	30	µs
	VxMON undervoltage deglitch time (VxMON_UVDGLT_OTP[1:0] = 11)	35	40	45	µs
VxMON (x = 1, 3)					
$VxMON_{RPD}$	VxMON internal passive pulldown	100	250	400	kΩ
$T_{OV\_DGLT\_START\_UP}$	V1MON OV deglitcher time when V1MON_OVTH_OTP[3:0] is forced to 110 % at startup	1	2	3	µs
V0MON					
$V0MON_{RPD}$	V0MON internal passive pulldown	1	2	5	MΩ
V1UVLP					
V1UVLP	V1_UVLP detection threshold (V1UVLP_TH_OTP=1)	3.0	3.065	3.13	V
	V1_UVLP detection threshold (V1UVLP_TH_OTP=0)	1.77	1.8	1.83	V
T_{V1UVLP_FILT}	V1_UVLP filtering time	0.26	2	6	us

19.4 External IC monitoring

To monitor another device (on top of the microcontroller) in the application, the HVIO1 pin can be configured as a digital input. This external IC monitoring feature is enabled by OTP. As soon as this feature is activated, the HVIO1 pin is used to monitor an external IC.

This monitoring is active in Normal mode. A transition detected at HVIO1 pin indicates an error from the external IC.

During the initialization phase of the FS24, various parameters can be configured if an external IC must be monitored in the application:

- Polarity of the fault signal, configurable with ERRMON_FLT_POLARITY bit during the initialization phase
- Desired reaction on RSTB and LIMP0
- Time allowed to the microcontroller for receiving error acknowledgment

When an error is detected, the microcontroller should acknowledge the FS24 device. If the acknowledgment is not received by the FS24 within the predefined time, the FS24 asserts LIMP0 and/or RSTB pin as defined during the initialization phase.

The following tables, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, depict the different SPI bits used by this external IC monitoring function:

Table 36. Signal polarity to detect an error on HVIO1 pin

ERRMON_FLT_POLARITY	Condition to detect a fault
0 (default)	**High to low level**
1	Low to high level

Table 37. Reaction when an error is detected HVIO1 pin

ERRMON_FS_REACTION	Reaction
0	Error on HVIO1 pin asserts LIMP0 only
1 (default)	Error on HVIO1 pin asserts LIMP0 and RSTB

Table 38. Allowed time before receiving microcontroller acknowledge when an external IC error is detected

ERRMON_ACK_TIME[1:0]	Time allowed for acknowledgment
00	0 ms
01 (default)	2 ms
10	4 ms
11	8 ms

Table 39. Error flag for external IC monitoring

ERRMON	Error flag on HVIO1
0	No error detected by FS24
1	Error detected. FS24 is waiting for an acknowledgment within the allowed time.

Table 40. Acknowledgment from MCU register

ERRMON_ACK	Error flag on HVIO1
0	No error reported by MCU
1	Error detected and reported to FS24 by MCU

The acknowledgment by the MCU is done through SPI communication according to Figure 41:

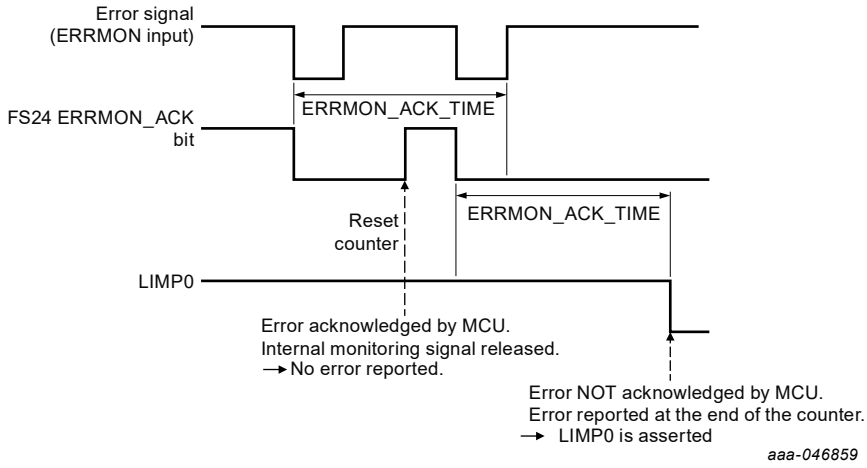


Figure 41. External IC monitoring timing diagram

Table 41. External IC monitoring electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. V_{SUP} = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IH_ERRMON}	High-level input voltage threshold	0.7 x VDDIO	—	—	V
V_{IL_ERRMON}	Low-level input voltage threshold	—	—	0.3 x VDDIO	V
$V_{IN\_HYS\_ERRMON}$	Threshold hysteresis	100	—	—	mV
t_{ERRMON_ERR}	Filtering time	4	6	8	µs
$t_{ERRMON\_ACK\_ACC}$	Acknowledgment counter accuracy	-10	—	10	%
R_{PD_ERRMON}	ERRMON pulldown resistor value	200	400	800	kΩ

19.5 Fault management

19.5.1 Fault error counter

The FS24 integrates a configurable fault error counter, which is counting the number of faults related to the device and also caused by external events. The fault error counter starts at 1 after a POR or resuming from LPON or LPOFF. The final value of the fault error counter is used to transition in fail-safe state (all safety pins asserted). The maximum value of this counter is configurable with the FLT_ERR_LIMIT[1:0] bits during the INIT phase.

Table 42. Fault error counter configuration

FLT_ERR_LIMIT[1:0]	Fault error counter max value configuration	Fault error counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6
Reset condition	POR	

The fault error counter has two output values: intermediate and final. The intermediate value can be used to force LIMP0 activation or generate a RSTB pulse according to the FLT_MID_RSTB/LIMP0_IMPACT bits configuration (INIT phase).

Table 43. Fault error counter fail-safe impact

FLT_MID_RSTB/LIMP0_IMPACT	Intermediate value impact on RSTB/LIMP0
0	No effect on the pin
1 (default)	**The pin RSTB/LIMP0 is asserted**
Reset condition	POR

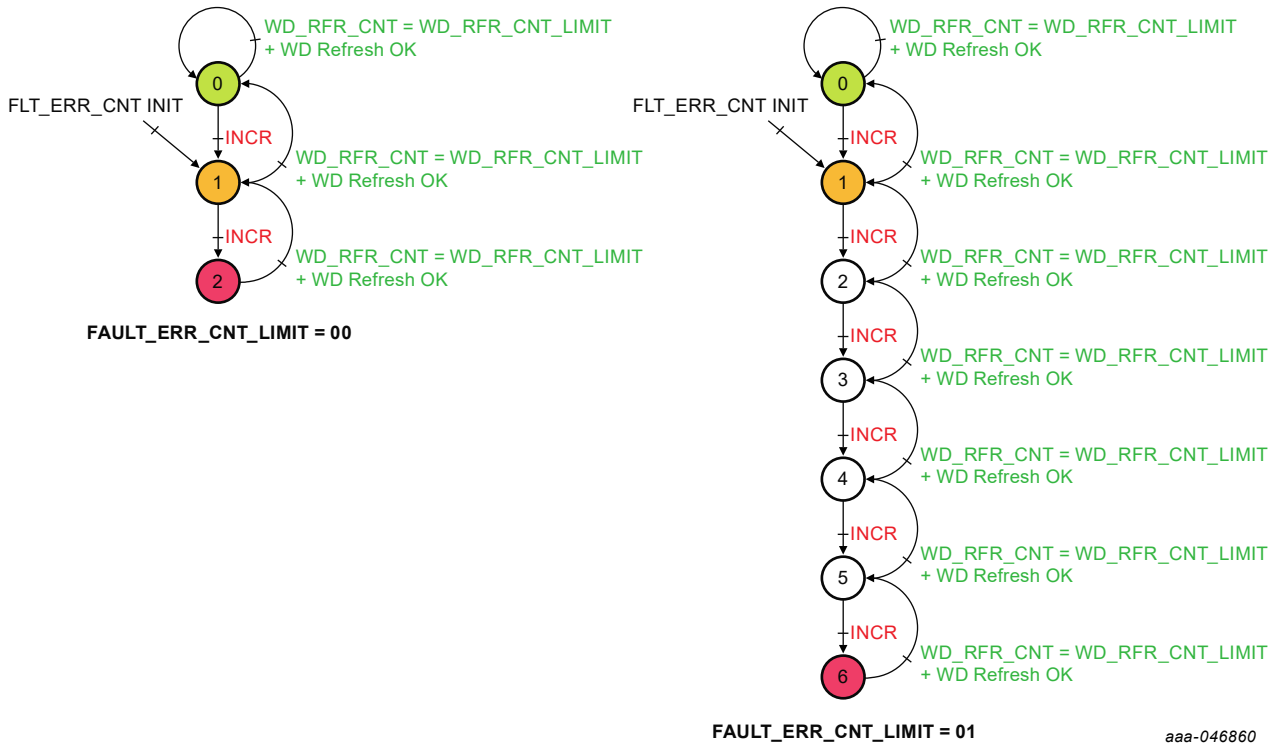


Figure 42. Fault error counter diagram with maximum value = 2 or 6

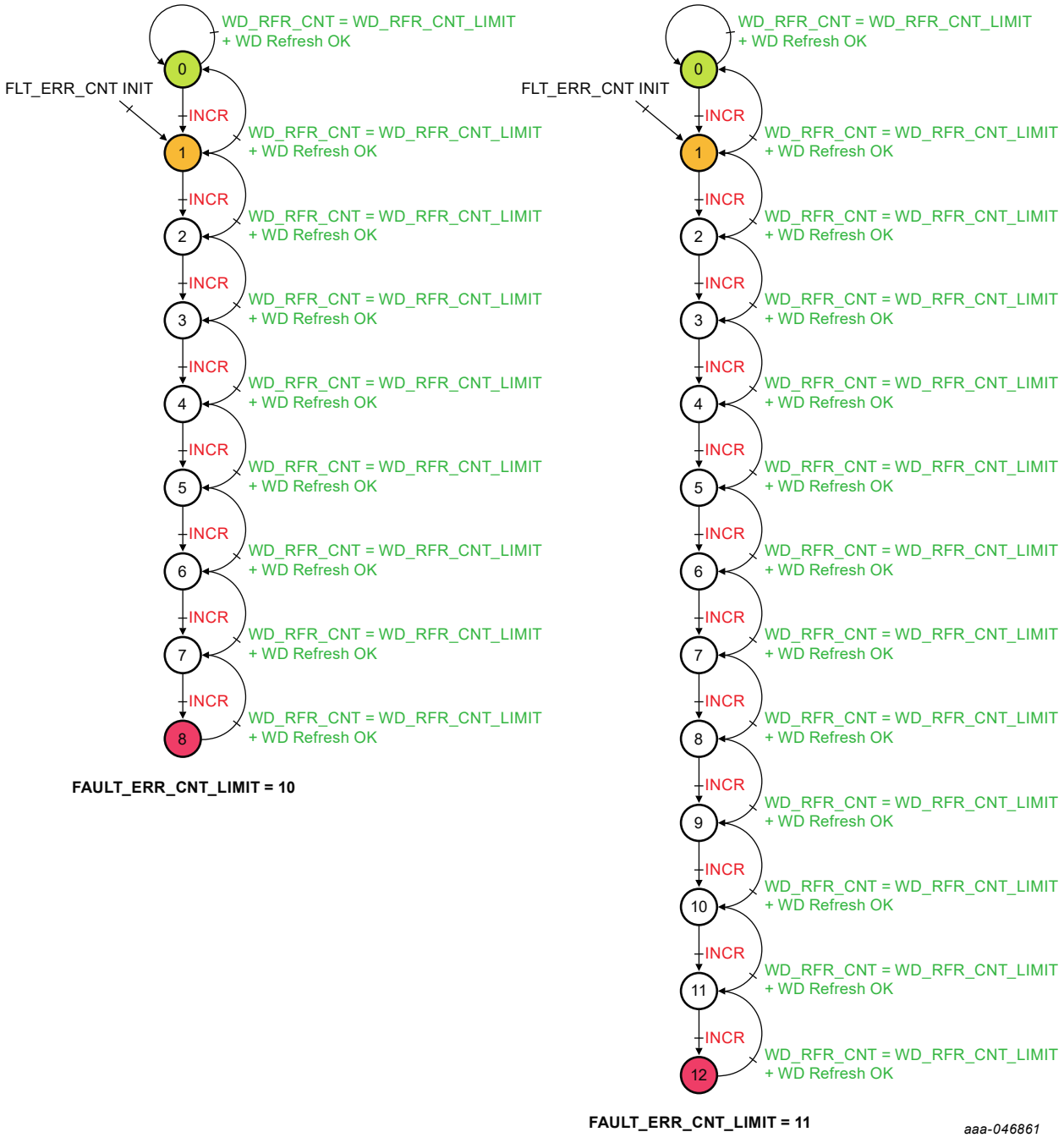


Figure 43. Fault error counter diagram with maximum value = 8 or 12

19.5.2 Fault source and reaction

In normal operation when LIMP0 and RSTB are released, the fault-error counter is incremented when a fault is detected by the FS24 state machine. Table 44 lists all the faults and their impact on RSTB and LIMP0 pins according to the device configuration. The faults that are configured to not assert RSTB and LIMP0 will not increment the fault-error counter. In that case, only the flags are available for MCU diagnostic. The fault-error counter is incremented by 1, each time the RSTB and/or LIMP0 pin is asserted.

In Orange, the reaction is not configurable.

In Green, the reaction is configurable by OTP and SPI for RSTB and by SPI for LIMP0 in INIT mode.

Table 44. Application related fail-safe fault list and reaction

Mode	Fault Source	Fault error counter	RSTB assertion	LIMP0 assertion
Slot 0 to Normal state	VxTSD & CONF_TSD_Vx_OTP	Max	Yes [1]	Yes[1]
	VxMON_OV & CONF_OV_Vx_OTP	Max	Yes[1]	Yes[1]
	VxMON OV & !CONF_OV_Vx_OTP	+1	VxMON_OV_ RSTB_IMPACT	VxMON_OV_ LIMP0_IMPACT
	VxMON UV	+1	VxMON_UV_ RSTB_IMPACT	VxMON_UV_ LIMP0_IMPACT
	First fault & FIRST_FAULT_EN_OTP	Max	Yes[1]	Yes[1]
	FLT_ERR_CNT = MID VALUE	No change	FLT_MID_RSTB_IMPACT	FLT_MID_LIMP0_IMPACT
	WD_ERR_CNT = WD_ERR_LIMIT	+1	WD_RSTB_IMPACT	WD_LIMP0_IMPACT
	ERRMON	+1	ERRMON_FS_REACTION	ERRMON_FS_REACTION
	RSTB request by MCU	No change	Yes	No
	WD reset by MCU (WD_RSTB_REQ)	No change	No	No
	LIMP0 request by MCU	No change	No	Yes
	External reset (out of extended RSTB)	+1	No	No
	RSTB short to high	No change	No	Yes
	LIMP0 short to high	Max	Yes[1]	Yes[1]
	RSTB short 8 s	Max	Yes[1]	Yes[1]
	INIT_CRC_NOK	+1	No	INIT_CRC_LIMP0_ IMPACT
	1MHz_STUCK_AT	N/A	Yes	Yes
LPON state	V1_UVLP	Clear at 1	Yes[1]	Yes[1]
	WD_ERR_CNT = WD_ERR_LIMIT	Clear at 1	WD_RSTB_IMPACT	WD_LIMP0_IMPACT
	No Fault (default)	Clear at 1	No	No
LPOFF state	No Fault (default)	Clear at 1	Yes by default[2]	No
Fail-safe state	State Machine in fail-safe (default)	Clear at 1	Yes by default[2]	Yes by default [2]

[1] By cascading effect, the fault error counter reaches its maximum value, which leads to the assertion low of RSTB and LIMP0, because the FS2400 is transitioning to Fail-safe state.

[2] By default (when no fault), RSTB is asserted in LPOFF mode. In the Fail-safe state, RSTB and LIMP0 are asserted.

19.5.3 Fail-safe mode

FS24 enters in Fail-safe (FS) mode when:

- The fault error counter reaches its maximum value (not configurable)
- VBOS UV is detected
- RSTB is asserted low for 8 s (if enabled by OTP)
- VxOV is detected (if configured by OTP)
- VxTSD is detected (if configured by OTP)
- V1UVLP is detected in LPON mode or during transition from LPON mode to Normal mode
- When the first fault is detected (if configured by OTP)

In Fail-safe mode, all the regulators are turned OFF, the high-power analog circuitry is disabled, the 20 MHz oscillator is disabled, the OV/UV monitoring are masked and FS_EVT bit is set to 1.

The fault error counter is reset to 1 and disabled.

The device exits the fail-safe state after T_{FS_DUR} time. If FS_LPOFF_OTP bit is set to 1, the device exits FS state and goes to LPOFF. Otherwise it goes back to power-up sequence.

Table 45. Fail-safe state electrical characteristics

T_A = -40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Fail-safe					
T_{FS_DUR}	Fail-safe state duration • FS_DUR_CFG_OTP = 0 • FS_DUR_CFG_OTP = 1	90 3.6	100 4	110 4.4	ms s

19.6 RSTB, LIMP0

Two safety output pins, RSTB and LIMP0, are implemented in order to guarantee the safe state of the system. All of those safety outputs are active low.

RSTB is activated during power up and can only be released when the device is in Normal mode. LIMP0 is released at startup and is only asserted when a fault occurs.

The two pins are managed independently in parallel of the main-state machine.

19.6.1 RSTB

RSTB is an open-drain output that can be connected in the application to the reset of the MCU. RSTB requires an external pullup resistor to VDDIO. An internal pulldown $RSTB_{RPD}$ ensures RSTB low level in case of POR. Redundant supplies of RSTB driver ensures that the pin will be driven low when VSUP is lost. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transitions in Fail-safe mode. RSTB assertion depends on the device configuration during INIT phase. The configurations can be preselected by OTP. RSTB can also be asserted at MCU request by SPI, to check the correct HW connection.

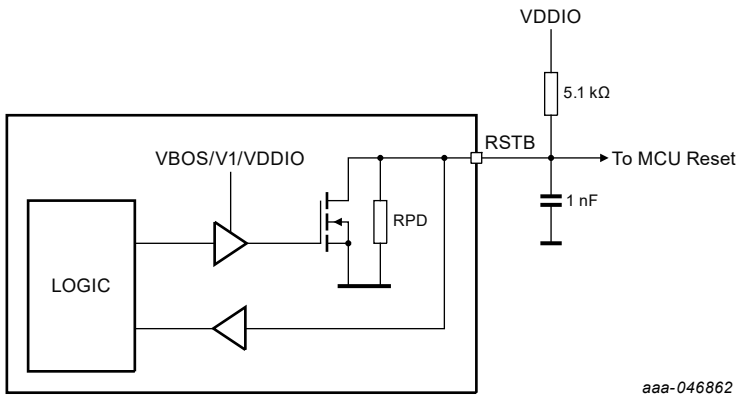


Figure 44. RSTB pin implementation

A 1 ms or 10 ms delay is added before RSTB is released, depending on RSTB_DUR bit (preselectable by OTP) to accommodate specific MCU requirement asking for voltage supply stabilization before RSTB is released.

Table 46. RSTB electrical characteristics

T_A = -40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
$RSTB_{VIL}$	Low-level Input voltage	-	-	0.7	V
$RSTB_{VIH}$	High-level Input voltage	1.5	-	-	V
$RSTB_{VOL}$	Low-level output voltage (I = 2.0 mA)	-	-	0.4	V
$RSTB_{RPD}$	Internal pulldown resistor	0.9	2	4	MΩ

Table 46. RSTB electrical characteristics...*continued*

T_A = -40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$RSTB_{ILIM}$	Current limitation	4	-	22	mA
Dynamic electrical characteristics					
$RSTB_{TFB}$	Feedback filtering time	8	10	15	us
$RSTB_{TSC}$	Short- to high-detection timer	500	650	800	us
$RSTB_{TLG}$	Long pulse (configurable with RSTB_DUR bit)	9	-	11	ms
$RSTB_{TST}$	Short pulse (configurable with RSTB_DUR bit)	0.9	-	1.1	ms
$RSTB_{T8S}$	8 second timer	7	8	9	s
$RSTB_{TFALL}$	Fall time (pullup to VDDIO = 5 V, 1 nF output capacitor)	-	-	8	us
$RSTB_{TRELEASE}$	Time to release RSTB from POR or LPOFF - with all slots used - with RSTB_DUR = 1 (1 ms)	-	4	6	ms
External components					
$RSTB_{RPU}$	External pullup resistor to VDDIO (nominal)	-	5.1	-	kΩ
$RSTB_{COUT}$	External filtering capacitor (optional depending on the EMC requirements)	-	1	-	nF

19.6.2 LIMP0 as a safety output

LIMP0 is an open-drain output that can be used to transition the system in safe state. It is released high by default. It is asserted low in case of fault and depending on the fault impact configuration. In Low-power modes (LPON and LPOFF), LIMP0 works as it does in Normal mode.

LIMP0 requires an external pullup resistor to VSUP or VDDIO, a 10 nF filtering capacitor to GND for immunity when LIMP0 is a local pin, and an additional RC network when LIMP0 is a global pin to be robust against ESD GUN and ISO 7637 transient pulses. A weak internal pulldown RPD ensures LIMP0 low level in case of pin lift. An internal pulldown RPD_STUP ensures LIMP0 is released at startup

LIMP0 assertion depends on the device configuration during INIT phase. LIMP0 can also be asserted at MCU request by SPI, to check the correct HW connection.

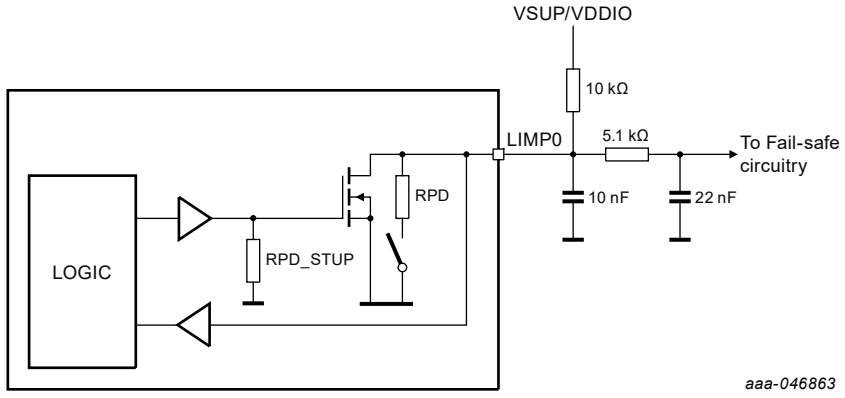


Figure 45. LIMP0 pin implementation

Table 47. LIMP0 electrical characteristics

T_A = -40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static electrical characteristics					
$LIMP0_{VIL}$	Low-level Input voltage LIMP0_TH_SEL = 0 LIMP0_TH_SEL = 1	 - -	 - -	 0.7 2	V
$LIMP0_{VIH}$	High-level Input voltage LIMP0_TH_SEL = 0 LIMP0_TH_SEL = 1	 1.5 3	 - -	 - -	V
$LIMP0_{VOL}$	Low-level output voltage (I = 2.0 mA)	-	-	0.4	V
$LIMP0_{RPD}$	Internal pulldown resistor	1	2	4	MΩ
$LIMP0_{ILIM}$	Current limitation	4	-	22	mA
Dynamic electrical characteristics					
$LIMP0_{TFB}$	Feedback filtering time	8	10	15	µs
$LIMP0_{TSC}$	Short- to high-detection timer	500	650	800	µs
$LIMP0_{TFALL}$	Fall time (pullup to VSUP = 14 V, 10 nF output capacitor)	-	-	25	µs
External components					
$LIMP0_{RPU}$	External pullup resistor to VDDIO (nominal)	-	5.1	-	kΩ
	External pullup resistor to VSUP (nominal)	-	10	-	kΩ
$LIMP0_{RSER}$	External serial resistor (optional, 0805 package size)	-	5.1	-	kΩ
$LIMP0_{COUT1}$	External output capacitor (close to the pin)	-	10	-	nF
$LIMP0_{COUT2}$	External output capacitor (optional, after the serial resistor)	-	22	-	nF

19.6.3 LIMP0 as a safety output release

When the fail-safe output LIMP0 is asserted low by the device because a fault, some conditions must be validated before allowing the LIMP0 pin to be released by the device. These conditions are:

- No fault affecting LIMP0 reported
- Fault error counter = 0
- Device in Normal mode
- Device not in INIT mode
- FS_LIMP0_REL register filled with the correct value, depending on current WD_TOKEN[15:0], (WD_TOKEN[15:8] with LSB and MSB inverted, then complemented)

19.6.4 LIMP0 as a GPO

When LIMP0 is not used as a safety output, it can be used as a general purpose output (GPO). To use LIMP0 as a GPO, LIMP0_EN_OTP bit must be set to 0 and the MCU must configure LIMP0_GPO = 1 during INIT phase. The pin is set to low level by setting the LIMP0_REQ bit and set to high level (biased by the external pull up) by setting the LIMP0_REL bit.

19.7 Analog built-in self-test (ABIST)

The FS24 provides an analog built-in self-test (ABIST) to verify the correct functionality of the voltage monitoring functions. The ABIST is executed on demand, after an SPI request from the MCU. ABIST can only be launched from Normal mode.

ABIST can be launched for all the voltage monitoring channels at the same time (via LAUNCH_ABIST bit), or individually (via ABIST_Vxxxx individual bits). An individual diagnostic bit is available for each channel once the ABIST is done (ABIST_DONE = 1). A CLEAR_ABIST bit is available to clear the diagnostic flags before launching the next ABIST. The flags have no impact on the safety pins.

If one of the concerned monitored voltage is out of range (OV or UV), the ABIST on demand command is ignored. While the ABIST is running, the other monitoring functions are kept available.

Table 48. ABIST electrical characteristics

T_A = −40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ABIST					
T_{ABIST}	ABIST duration for one monitoring channel	-	-	20	µs

19.8 Cyclic CRC check

The FS24 provides an 8-bit cyclic CRC check to verify the integrity of the INIT registers (FS_I_xxxx) containing the safety configuration information (configurable in INIT mode only). This mechanism allows for the detection of a misconfiguration from the MCU or a bit flip in the INIT registers.

The 8-bit CRC is computed on the result of the concatenation of the following register bits:

- FS_I_OVUV_CFG1[15:0]
- FS_I_OVUV_CFG2[15:0]
- FS_I_ERRMON_LIMP0_CFG[15:0]
- FS_I_FSSM_CFG[15:4]
- FS_I_WD_CFG[15:7]

The calculation to apply on the result of the concatenation is the same as the SPI CRC, using x^8+x^4+x^3+x^2+1 polynomial. The MCU must write the obtained CRC in the FS_CRC register before closing the INIT phase, after the modification of the INIT registers.

Once the INIT phase is closed and the device is in Normal mode, the cyclic CRC check is launched automatically each 5 ms (T_{CRC}) (<FTTI).

Each 5 ms, the device logic recalculates the CRC and compares it to the value stored in FS_CRC register. If a mismatch is reported, the INIT_CRC_NOK_I bit is set and LIMP0 is asserted depending on its impact configuration (INIT_CRC_LIMP0_IMPACT).

Table 49. Cyclic CRC check characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Cyclic CRC check					
T_{CRC}	CRC check timing interval	4.75	5	5.25	ms

19.9 Clock monitoring

The 1 MHz clock is monitored for stuck-at faults in Normal mode. In case a stuck-at is detected, the two safety pins RSTB and LIMP0 are asserted.

20 MCU communication

The FS24 provides SPI interface for device configuration, control and diagnostic, in Normal and LPON modes.

20.1 SPI communication

The FS24 provides a 32-bit SPI interface with the following arrangement:

Primary output secondary in bits (MOSI):

- Bits 31 to 25: register address
- Bit 24: read/write (For reading Bit 24 = ‘0’; For writing Bit 24 = ‘1’)
- Bits 23 to 8: control bits
- Bits 7 to 0: cyclic redundant check (CRC)

Primary input secondary out bits (MISO):

- Bits 31 to 24: general device status
- Bits 23 to 8: device internal control register content
- Bits 7 to 0: cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is driving MOSI. FS24 is driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge. MSB is sent first. In write command, MISO [31:24] bits are the general status flags, [23:8] bits are all 0 and MISO [7:0] is the CRC of the message sent by the FS24. In read command, MOSI [23:8] bits are all 0 and MOSI [7:0] is the CRC of the message sent by the MCU. Table 50 and Table 51 describe SPI communication protocol for writing data into the FS24 or reading data from the FS24.

Table 50. SPI write command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**Write data [15:8]**							
MISO	0	WD_G	PHYG	WUG	IOG	COMG	VSUPG	VXG	**Read data [15:8]**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
MOSI	**Write data [7:0]**								**CRC [7:0]**							
MISO	**Read data [7:0]**								**CRC [7:0] - response**							

Table 51. SPI read command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**0x00**							
MISO	0	WD_G	PHYG	WUG	IOG	COMG	VSUPG	VXG	**Read data [15:8]**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
MOSI	**0x00**								**CRC [7:0]**							
MISO	**Read data [7:0]**								**CRC [7:0] - response**							

Table 52. MISO general device status bits descriptions

Bit	Symbol	Description
31	/	0
30	WD_G	**Report a safety related error WD_G = WD_NOK_I**
		0 No error
		1 Watchdog refresh error reported
		Reset on POR, cleared when all individual bits are cleared
29	PHYG	**Flags reported: CAN_TSD_I or CAN_TXD_TO_I**
		0 No error
		1 CAN error reported
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: CAN_TSD_I or CAN_TXD_TO_I
28	WUG	**Interrupt notification from M_IOWU_FLG or M_WU1_FLG registers**
		0 No event reported in M_IOWU_FLG or M_WU1_FLG registers
		1 An interrupt or flag is present in M_IOWU_FLG or M_WU1_FLG registers
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: WK2_WU_I, WK3_WU_I, HVIO1_WU_I CAN_WU_I, LDT_WU_I, INT_TO_WU, WD_OFL_WU, V1_UVLP_WU, GO2NORMAL_WU, EXT_RSTB_WU
27	IOG	**Interrupt notification from M_IO_TIMER_G register**
		0 No event reported in M_IO_TIMER_G register
		1 An interrupt or flag is present in M_IO_TIMER_G register
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: WK3_I, WK2_I, HVIO1_I, LDT_I
26	COMG	**Interrupt notification from M_VSUP_COM_FLG register**
		0 No event reported into M_VSUP_COM_FLG register
		1 An interrupt or flag is present in the M_VSUP_COM_FLG register
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: SPI_REQ_I, SPI_CLK_I, SPI_CRC_I
25	VSUPG	**Interrupt notification from M_VSUP_COM_FLG register**
		0 No event reported into M_VSUP_COM_FLG register
		1 An interrupt or flag is present in the M_VSUP_COM_FLG register
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: VSUPUV_4P7_I, VSUPUV_5P7_I, VSUPOV_I
24	VxG	**Interrupt notification from M_REG_FLG register**
		0 No event reported into M_REG_FLG register
		1 An interrupt or flag is present in the M_REG_FLG register
		Reset on POR, cleared when all individual bits are cleared
		Flags reported: V0UV_I, V0OV_I, V1OC_I, V1UV_I, V1OV_I, V1TSD_I, V1TWARN_I, V3OC_I, V3UV_I, V3OV_I, V3TSD_I

20.1.1 Cyclic redundancy check

An 8-bit CRC is required for each write and read SPI command. Computation of a cyclic-redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a seed value of hexadecimal '0xFF'.

Figure 46 is an example of CRC encoding HW implementation:

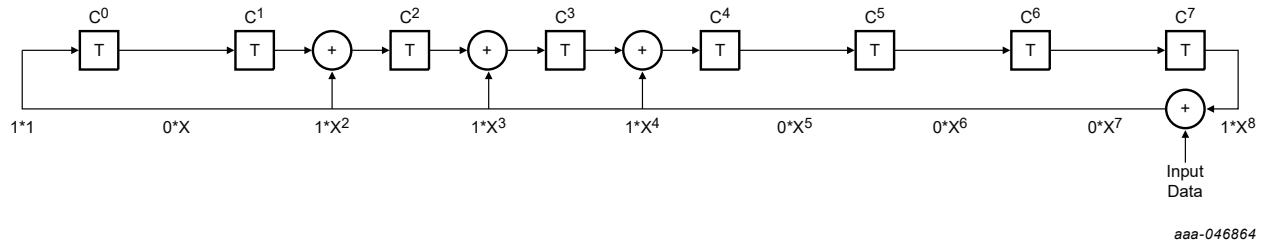


Figure 46. CRC encoder example

The effect of CRC encoding procedure is shown in Table 53. The seed value is appended into the most significant bits of the shift register.

Table 53. Data preparation for CRC encoding

Seed	Register address	Read/Write	Data_MSB	Data_LSB
0xFF	Bits[31:25]	Bit[24]	Bits[23:16]	Bits[15:8]

Table 54. Data preparation for CRC encoding

Seed …	… padded with the message to encode	… padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted.
   Note: *The 32-bits message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).*
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.
   Use the following steps for CRC decoding:

Procedure for CRC decoding

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

- If the shift register contains all zeros, the CRC is correct.
- If the shift register contains a value other than zero, the CRC is incorrect.

20.1.2 Electrical characteristics

Table 55. SPI electrical characteristics

T_A = –40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 1.8 V to 5 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Interface I/O input supply					
V_{DDIO}	VDDIO supply voltage range	1.8	-	5.5	V
Static electrical characteristics					
SPI_{VIL}	CSB, SCLK, MOSI Low-level input voltage	-	-	0.3 x VDDIO	V
SPI_{VIH}	CSB, SCLK, MOSI High-level input voltage	0.7 x VDDIO	-	-	V
SPI_{HYST}	CSB, SCLK, MOSI input voltage hysteresis	0.1	-	0.6	V
$SCLK_{PULL-Down}$	SCLK internal pulldown	90	200	400	kΩ
$MISO_{VOH}$	MISO High-output voltage (I = 2.0 mA)	VDDIO - 0.4	-	-	V
$MISO_{VOL}$	MISO Low-output voltage (I = 2.0 mA)	-	-	0.4	V
I_{MISO}	3-state leakage current (VDDIO = 5 V)	-5.0	-	5.0	µA
$SPI_{PULL-up}$	CSB, MOSI internal pullup (pullup to VDDIO)	90	200	400	kΩ
Dynamic electrical characteristics					
F_{SPI}	SPI operation frequency (50 % DC)	0.5	-	4	MHz
t_{CLH}	Minimum time SCLK = HIGH	125	-	-	ns
t_{CLL}	Minimum time SCLK = LOW	125	-	-	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge), Cout = 100 pF max	-	-	50	ns
t_{CSDV}	CSB = low to data at MISO active	-	-	100	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	125	-	-	ns
t_{HCLCL}	SCLK change L/H after CSB = low	125	-	-	ns
t_{SCLD}	MOSI input setup time (SCLK change H/L after MOSI data valid)	100	-	-	ns
t_{HCLD}	MOSI input hold time (MOSI data hold after SCLK change H/L)	50	-	-	ns
t_{SCLCL}	SCLK low before CSB high	125	-	-	ns
t_{HCLCH}	SCLK high after CSB high	125	-	-	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	-	-	100	ns
t_{ONCSB}	CSB min. high time between two frames	5	-	-	µs

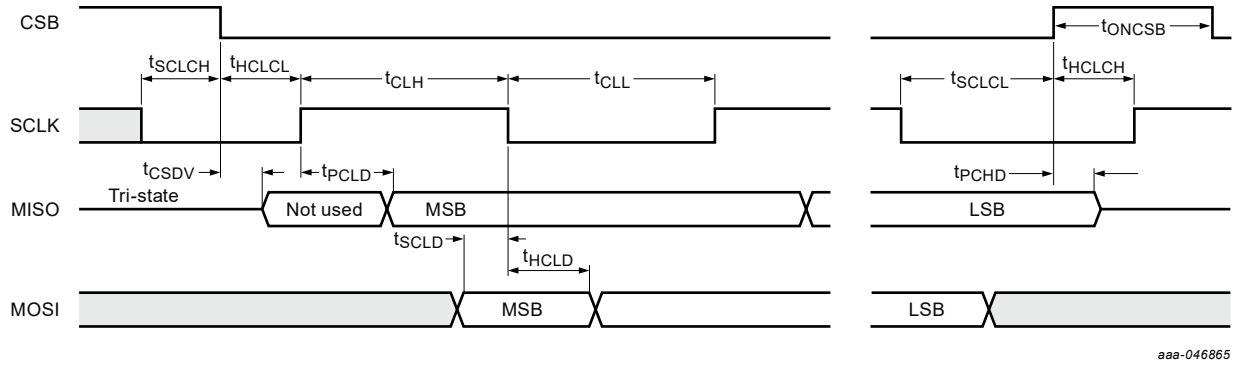


Figure 47. SPI timing diagram

21 Register mapping

Table 56. Main register mapping

Register	# (Hex)	Address							R/W SPI	Read/Write	Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0			
M_DEV_CFG	00	0	0	0	0	0	0	0	0	Read only	Section 22.1
M_DEV_PROG_ID	01	0	0	0	0	0	0	1	0	Read only	Section 22.2
M_GEN_FLAG	02	0	0	0	0	0	1	0	0	Read only	Section 22.3
M_STATUS	03	0	0	0	0	0	1	1	0	Read only	Section 22.4
Reserved	04	0	0	0	0	1	0	0	-	Reserved	
M_SYS_CFG	05	0	0	0	0	1	0	1	0/1	Read/write	Section 22.5
M_SYS1_CFG	06	0	0	0	0	1	1	0	0/1	Read/write	Section 22.6
M_REG_CTRL	07	0	0	0	0	1	1	1	0/1	Read/write	Section 22.7
Reserved	08	0	0	0	1	0	0	0	-	Reserved	
M_REG2_CTRL	09	0	0	0	1	0	0	1	0/1	Read/write	Section 22.8
M_REG_FLG	0A	0	0	0	1	0	1	0	0/1	Read/write	Section 22.9
M_REG_MSK	0B	0	0	0	1	0	1	1	0/1	Read/write	Section 22.10
M_REG1_FLG	0C	0	0	0	1	1	0	0	0/1	Read/write	Section 22.11
M_REG1_MSK	0D	0	0	0	1	1	0	1	0/1	Read/write	Section 22.12
M_IO_CTRL	0E	0	0	0	1	1	1	0	0/1	Read/write	Section 22.13
M_IO_TIMER_FLG	0F	0	0	0	1	1	1	1	0/1	Read/write	Section 22.14
M_IO_TIMER_MSK	10	0	0	1	0	0	0	0	0/1	Read/write	Section 22.15
M_VSUP_COM_FLG	11	0	0	1	0	0	0	1	0/1	Read/write	Section 22.16
M_VSUP_COM_MSK	12	0	0	1	0	0	1	0	0/1	Read/write	Section 22.17
M_IOWU_CFG	13	0	0	1	0	0	1	1	0/1	Read/write	Section 22.18
M_IOWU_EN	14	0	0	1	0	1	0	0	0/1	Read/write	Section 22.19
M_IOWU_FLG	15	0	0	1	0	1	0	1	0/1	Read/write	Section 22.20
M_WU1_EN	16	0	0	1	0	1	1	0	0/1	Read/write	Section 22.21
M_WU1_FLG	17	0	0	1	0	1	1	1	0/1	Read/write	Section 22.22
Reserved	18	0	0	1	1	0	0	0	-	Reserved	
Reserved	19	0	0	1	1	0	0	1	-	Reserved	
Reserved	1A	0	0	1	1	0	1	0	-	Reserved	
Reserved	1B	0	0	1	1	0	1	1	-	Reserved	
Reserved	1C	0	0	1	1	1	0	0	-	Reserved	
Reserved	1D	0	0	1	1	1	0	1	-	Reserved	
Reserved	1E	0	0	1	1	1	1	0	-	Reserved	
Reserved	1F	0	0	1	1	1	1	1	-	Reserved	
Reserved	20	0	1	0	0	0	0	0	-	Reserved	
Reserved	21	0	1	0	0	0	0	1	-	Reserved	
Reserved	22	0	1	0	0	0	1	0	-	Reserved	
Reserved	23	0	1	0	0	0	1	1	-	Reserved	
Reserved	24	0	1	0	0	1	0	0	-	Reserved	
M_AMUX_CTRL	25	0	1	0	0	1	0	1	0/1	Read/write	Section 22.23
M_LDT_CFG1	26	0	1	0	0	1	1	0	0/1	Read/write	Section 22.24
M_LDT_CFG2	27	0	1	0	0	1	1	1	0/1	Read/write	Section 22.25
M_LDT_CFG3	28	0	1	0	1	0	0	0	0/1	Read/write	Section 22.26
M_LDT_CTRL	29	0	1	0	1	0	0	1	0/1	Read/write	Section 22.27
M_CAN	2A	0	1	0	1	0	1	0	0/1	Read/write	Section 22.28
Reserved	2B	0	1	0	1	0	1	1	-	Reserved	
M_CAN_MSK	2C	0	1	0	1	1	0	0	0/1	Read/write	Section 22.29
M_MEMORY0	2D	0	1	0	1	1	0	1	0/1	Read/write	Section 22.30
M_MEMORY1	2E	0	1	0	1	1	1	0	0/1	Read/Write	Section 22.31
M_HW_ID	2F	0	1	0	1	1	1	1	0/1	Read/write	Section 22.32

Table 57. Safety-related register mapping

Register	# (Hex)	Address							R/W SPI	Read/write	Reference
		Adr_6	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0			
FS_I_OVUV_CFG1	32	0	1	1	0	0	1	0	0/1	Write during INIT then read only	Section 23.1
FS_I_OVUV_CFG2	33	0	1	1	0	0	1	1	0/1	Write during INIT then read only	Section 23.2
Reserved	34	0	1	1	0	1	0	0	—	Reserved	
FS_I_ERRMON_LIMP0_CFG	35	0	1	1	0	1	0	1	0/1	Write during INIT then read only	Section 23.3
FS_I_FSSM_CFG	36	0	1	1	0	1	1	0	0/1	Write during INIT then read only	Section 23.4
FS_I_WD_CFG	37	0	1	1	0	1	1	1	0/1	Write during INIT then read only	Section 23.5
FS_WDW_CFG	38	0	1	1	1	0	0	0	0/1	Read/write	Section 23.6
FS_WD_TOKEN	39	0	1	1	1	0	0	1	0	Read only	Section 23.7
FS_WD_ANSWER	3A	0	1	1	1	0	1	0	0/1	Read/write	Section 23.8
Reserved	3B	0	1	1	1	0	1	1	—	Reserved	
FS_LIMP0_REL	3C	0	1	1	1	1	0	0	0/1	Read/write	Section 23.9
FS_ABIST	3D	0	1	1	1	1	0	1	0/1	Read/write	Section 23.10
Reserved	3E	0	1	1	1	1	1	0	6	Reserved	
FS_SAFETY_OUTPUTS	3F	0	1	1	1	1	1	1	0/1	Read/write	Section 23.11
FS_SAFETY_FLG	40	1	0	0	0	0	0	0	0/1	Read/write	Section 23.12
FS_CRC	41	1	0	0	0	0	0	1	0/1	Read/write	Section 23.13

22 Main register mapping

22.1 M_DEV_CFG

Table 58. M_DEV_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	CAN_EN	0	LDTIM_EN	0	0	0
Reset	0	0	OTP fuse	0	OTP fuse	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	0	0	—	—	—	—	—	—
Read	0	ABIST_EN	0	0	LIMP0_EN	V0MON_EN	0	0
Reset	0	OTP fuse	0	0	OTP fuse	OTP fuse	0	0

Go to main register map

Table 59. M_DEV_CFG register bit description

Bit	Symbol	Description
2	V0MON_EN	**Report the enable of VMON_EXT**
		0 VMON_EXT is disabled
		1 VMON_EXT is enabled
		OTP Fuse load
3	LIMP0_EN	**Report the enable of LIMP0**
		0 LIMP0 is disabled
		1 LIMP0 is enabled
6	ABIST_EN	**Report the enable of ABIST on demand**
		0 ABIST on demand is disabled
		1 ABIST on demand is enabled
		OTP Fuse load
11	LDTIM_EN	**Report the enable of LDT**
		0 LDT is disabled
		1 LDT is enabled
		OTP Fuse load
13	CAN_EN	**Report the enable of the CAN**
		0 The CAN is disabled
		1 The CAN is enabled
		OTP fuse load

22.2 M_DEV_PROG_ID

Table 60. M_DEV_PROG_ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	FULL_LAYER_REV			METAL_LAYER_REV			0	0
Reset	0	1	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	PROG_IDH				PROG_IDL			

Table 60. M_DEV_PROG_ID register bit allocation*...continued*

Reset	OTP fuse	OTP fuse

Go to main register map

Table 61. M_DEV_PROG_ID register bit description

Bit	Symbol	Description
0 to 3	PROG_IDL	**Report the second digit of the OTP code (0-F)**
		Program ID dependent
		OTP fuse load
4 to 7	PROG_IDH	**Report the first digit of the OTP code (A-R)**
		Program ID dependent
		OTP fuse load
10 to 12	METAL_ LAYER_REV	**Report the Metal Mask revision**
		0000 Rev X.0 (default full layer revision)
		N/A
13 to 15	FULL_LAYER_REV	**Report the Full Layer Mask revision (X)**
		0000 unused
		0001 Pass A silicon
		0010 Pass B silicon
		N/A

22.3 M_GEN_FLAG

Table 62. M_GEN_FLAG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	0	WD_G	PHYG	WUG	IOG	COMG	VSUPG	VxG
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 63. M_GEN_FLAG register bit description

Bit	Symbol	Description
0	VxG	**Report an event on a regulator VxG = V3OC_I or V3OV_I or V3UV_I or V3TSD_I or V1OC_I or V1OV_I or V1UV_I or V1TSD_I or V1TWARN_I or V0UV_I or V0OV_I**
		0 no event
		1 Vx event occurred
		POR, cleared when all Vx flags are cleared
1	VSUPG	**Report a VSUP error VSUPG = VSUPUV_4P7_I or VSUPUV_5P7_Ior VSUPOV_I**
		0 no error
		1 VSUP error reported
		POR, cleared when all VSUP flags are cleared

Table 63. M_GEN_FLAG register bit description*...continued*

Bit	Symbol	Description
2	COMG	**Report an error on the communication (SPI) COMG = SPI_REQ_I or SPI_CLK_I**
		0 no error
		1 Communication error reported
		POR, cleared when all COM flags are cleared
3	IOG	**Report an IO or LDT event IOTIMG = WK2_I or WK3_I or HVIO1_I or LDT_I**
		0 no event
		1 event occurred
		POR, cleared when all IO and LDT flags are cleared
4	WUG	**Report a wake-up event WUG = HVIO1_WU_I or WK2_WU_I or WK3_WU_I or CAN_WU_I or LDT_WU_I or INT_TO_WU or WD_OFL_WU or V1_UVLP_WU or GO2NORMAL_WU or EXT_RSTB_WU**
		0 no event
		1 wake-up event occurred
		POR, cleared when all WU flags are cleared
5	PHYG	**Report a Physical Layer error PHYG = CAN_TSD_I or CAN_TXD_TO_I**
		0 no error
		1 CAN error reported
		POR, cleared when all CAN flags are cleared
6	WD_G	**Report a safety related error WD_G = WD_NOK_I**
		0 no error
		1 watchdog refresh error reported
		POR, cleared when all WD flags are cleared

22.4 M_STATUS

Table 64. M_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	V1TWARN_S	LPON_S	NORMAL_S	INIT_S	WK3_S	WK2_S	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	HVIO1_S	0	0	0	V1_MODE	V1_S	0	V3_S
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 65. M_STATUS register bit description

Bit	Symbol	Description
0	V3_S	**Real-time status of V3 regulator**
		0 V3 is disabled
		1 V3 is enabled
		Real-time information

Table 65. M_STATUS register bit description*...continued*

Bit	Symbol	Description
2	V1_S	**Real-time status of V1 regulator**
		0 V1 is disabled
		1 V1 is enabled
		Real-time information
3	V1_MODE	**Real-time status of the HVBUCK mode**
		0 BUCK is in PWM mode
		1 BUCK is in PFM mode
		Real-time information
7	HVIO1_S	**Real-time status of HVIO1 input**
		0 HVIO1 is low
		1 HVIO1 is high
		Real-time information
10	WK2_S	**Real-time status of WAKE2 input**
		0 WAKE2 is low
		1 WAKE2 is high
		Real-time information
11	WK3_S	**Real-time status of WAKE3 input**
		0 WAKE3 is low
		1 WAKE3 is high
		Real-time information
12	INIT_S	**Real-time status of INIT mode**
		0 Device is not in INIT mode
		1 Device is in INIT mode
		Real-time information
13	NORMAL_S	**Real-time status of Normal mode**
		0 Device is not in Normal mode
		1 Device is in Normal mode
		Real-time information
14	LPON_S	**Real-time status of LPON mode**
		0 Device is not in LPON mode
		1 Device is in LPON mode
		Real-time information
15	V1TWARN_S	**Real-time status of V1 temperature**
		0 V1 temperature is < $TWARN_{V1}$
		1 V1 temperature is > $TWARN_{V1}$
		Real-time information

22.5 M_SYS_CFG

Table 66. M_SYS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	BAT_FAIL	0	POR	0	0	GO2INIT	GO2NORMAL
Read	0	BAT_FAIL	0	POR	0	0	0	0
Reset	0	1	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	GO2LPON	GO2LPOFF	INT_TO_WUEN	INTB_REQ	INTB_DUR	0	MOD_CONF	MOD_EN
Read	0	0	INT_TO_WUEN	0	INTB_DUR	0	MOD_CONF	MOD_EN
Reset	0	0	0	0	0	0	OTP fuse	OTP fuse

Go to main register map

Table 67. M_SYS_CFG register bit description

Bit	Symbol	Description
0	MOD_EN	**Enable the frequency spread spectrum**
		0 Spread spectrum is disabled (regardless of OTP configuration)
		1 Spread spectrum is enabled (regardless of OTP configuration)
		OTP fuse load
1	MOD_CONF	**Select the spread spectrum modulation type**
		0 Triangular modulation is selected
		1 Pseudo random modulation is selected
		OTP fuse load
3	INTB_DUR	**Select INTB pulse duration**
		0 INTB pulse = 25 us
		1 INTB pulse = 100 us
		POR
4	INTB_REQ	**Request INTB pulse**
		0 No effect
		1 INTB pulse is requested
		POR, or self-clear
5	INT_TO_WUEN	**Enable interrupt time-out wake-up capability**
		0 Interrupt timeout will not generate a wake-up event
		1 Interrupt time out will generate a wake-up event
		POR
6	GO2LPOFF	**Request to go in LPOFF mode from Normal mode**
		0 No action
		1 Go to LPOFF mode
		POR, self-clear
7	GO2LPON	**Request to go in LPON mode from Normal mode**
		0 No action
		1 Go to LPON mode
		POR, Self-clear

Table 67. M_SYS_CFG register bit description*...continued*

Bit	Symbol	Description
8	GO2NORMAL	**Request to go in Normal mode from LPON mode**
		0 No action
		1 Go to Normal mode
		POR, Self-clear
9	GO2INIT	**Request to go in INIT phase**
		0 No action
		1 Go to INIT phase
		POR, self-clear
12	POR	**Report a POR of the digital POR = VBOS_POR or VDIG_UV_POR or VDIG_OV_POR or SOFTPOR_REQ**
		0 No POR event
		1 Digital POR event occurred
		POR
14	BAT_FAIL	**Report battery failure event (not reset by SOFTPOR_REQ) BAT_FAIL = VBOS_POR or VDIG_UV_POR or VDIG_OV_POR**
		0 No battery failure event
		1 Battery failure event occurred
		HARD_POR

22.6 M_SYS1_CFG

Table 68. M_SYS1_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	LOAD_ OTP_BYP	SLOT_BYP	TSLOT_ DOWN_CFG
Read	M_FSM_STATE					LOAD_ OTP_BYP	SLOT_BYP	TSLOT_ DOWN_CFG
Reset	0	0	0	0	0	0	OTP fuse	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	SOFTPOR_REQ	0	DBG_EXIT	0	0	OTP_EXIT	0
Read	0	0	0	0	DBG_MODE	0	0	OTP_MODE
Reset	0	0	0	0	0	0	OTP fuse	0

Go to main register map

Table 69. M_SYS1_CFG register bit description

Bit	Symbol	Description
0	OTP_MODE	**Real-time status of OTP mode**
		0 Device is not in OTP mode
		1 Device is in OTP mode
		Real-time information

Table 69. M_SYS1_CFG register bit description*...continued*

Bit	Symbol	Description
1	OTP_EXIT	**Leave OTP mode**
		0 No action
		1 Leave OTP mode
		POR, self-clear
3	DBG_MODE	**Real-time status of debug mode**
		0 Device is not in Debug mode
		1 Device is in Debug mode
		Real-time information
4	DBG_EXIT	**Leave Debug mode**
		0 No action
		1 Leave Debug mode
		POR, Self-clear
6	SOFTPOR_REQ	**Request a software POR of FS24 (reset the digital and restart from POR)**
		0 No action
		1 Software POR is requested
		POR, Self-clear
8	TSLOT_DOWN_CFG	**Select the power down time slot**
		0 TSLOT = 2 ms
		1 TSLOT = 0 ms
		POR
9	SLOT_BYP	**Bypass unnecessary slots**
		0 Slots are not bypassed
		1 Bypass unnecessary slots during power down or wake-up from LPON
		OTP fuse load
10	LOAD_OTP_BYP	**Bypass the OTP loading during power up**
		0 OTP loading is not bypassed
		1 OTP loading is bypassed
		POR or in main FSM M4 state

Table 69. M_SYS1_CFG register bit description*...continued*

Bit	Symbol	Description
11 to 15	M_FSM_STATE	**VBOS to V1 switch always enabled**
		00000 -
		00001 M1
		00010 M2
		00011 M3
		00100 M4
		00101 M5
		00110 M6
		00111 M7
		01000 M8
		01001 M9
		01010 M10
		01011 M11
		01100 M12
		01101 M13
		01110 M14
		01111 M15
		10000 M16
		10001 M17
		10010 M18
		10011 -
		10100 -
		10101 -
		10110 -
		10111 -
		11000 -
		11001 -
		11010 -
		11011 -
		11100 -
		11101 -
		11110 M30
		11111 -
		POR

22.7 M_REG_CTRL

Table 70. M_REG_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	BUCK_SRHSOFF		BUCK_SRHSON		
Read	0	0	0	BUCK_SRHSOFF		BUCK_SRHSON		
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	0
Write	V1EN	V1DIS	0	0	0	V3ON_LPON	V3EN	V3DIS
Read	0	0	0	0	0	V3ON_LPON	0	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 71. M_REG_CTRL register bit description

Bit	Symbol	Description
0	V3DIS	**Request to disable V3**
		0 No effect (Regulator remain in its current state)
		1 Request to disable V3
		POR, Self-clear
1	V3EN	**Request to enable V3**
		0 No effect (Regulator remain in its current state)
		1 Request to enable V3
		POR, Self-clear
2	V3ON_LPON	**Configure V3 state in LPON mode**
		0 Follow the power down slot configuration
		1 Keep V3 ON in LPON if V3 was already ON in NORMAL mode
		POR
6	V1DIS	**Request to disable V1**
		0 No effect (Regulator remain in its current state)
		1 Request to disable V1
		POR, Self-clear
7	V1EN	**Request to enable V1**
		0 No effect (Regulator remain in its current state)
		1 Request to enable V1
		POR, Self-clear

Table 71. M_REG_CTRL register bit description*...continued*

Bit	Symbol	Description
8 to 10	BUCK_SRHSON	**Select BUCK slew rate when the High Side turns ON**
		000 HS rising slew rate is 20 ns (for 450 kHz only)
		001 HS rising slew rate is 20 ns (for 450 kHz only)
		010 HS rising slew rate is 15 ns (for 450 kHz only)
		011 HS rising slew rate is 10 ns
		100 HS rising slew rate is 6.3 ns
		101 HS rising slew rate is 5 ns
		110 HS rising slew rate is 3 ns
		111 HS rising slew rate is 2 ns
		POR or OTP Fuse load
11 to 12	BUCK_SRHSOFF	**Select BUCK slew rate when the High Side turns OFF**
		00 HS falling slew rate is 20 ns (for 450 kHz only)
		01 HS falling slew rate is 15 ns (for 450 kHz only)
		10 HS falling slew rate is 10 ns
		11 HS falling slew rate is 5 ns
		POR or OTP Fuse load

22.8 M_REG2_CTRL

Table 72. M_REG2_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	GO2DFLT	GO2DVS
Read	0	0	0	0	0	VV1_BUCK_S	0	0
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	VV1_BUCK_DVS_SR		VV1_BUCK_DVS					
Read	VV1_BUCK_DVS_SR		VV1_BUCK_DVS					
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 73. M_REG2_CTRL register bit description

Bit	Symbol	Description
0 to 5	VV1_BUCK_DVS	**Select V1 output voltage**
		Range 1: 1.8 V + VV1_BUCK_DVS[5:0]*25 mV[1] Range 2: 3 V + VV1_BUCK_DVS[5:0]*50 mV[1]
		POR

Table 73. M_REG2_CTRL register bit description*...continued*

Bit	Symbol	Description
6 to 7	VV1_BUCK_DVS_SR	**Select rate to operate voltage change on V1**
		00 22 mV/µs
		01 11.25 mV/µs
		10 5.63 mV/µs
		11 2.81 mV/µs
		POR
8	GO2DVS	**Set V1 output voltage to DVS value**
		0 No effect
		1 V1 is set to DVS Value
		POR
9	GOTODFLT[2]	**Set V1 output voltage to default value**
		0 No effect
		1 V1 is set to default Value
		POR
10	VV1_BUCK_S	**Report the ongoing V1 voltage setting**
		0 Buck is set to default value
		1 Buck is set to DVS value
		POR

[1] The range is set using the VV1_BUCK_RANGE_OTP bit
[2] After setting the GO2DVS bit, ensure that the software waits for the DVS completion before setting the GOTODFLT bit. The DVS completion time is determined by the voltage settings and the VV1_BUCK_DVS_SR[1:0] setting.

22.9 M_REG_FLG

Table 74. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	V1LSOC_I	V1UVW_I	V1TWARN_I	V1TSD_I	0	V3TSD_I	V1UVLP_I	V1UV_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	0	V3UV_I	V1OV_I	0	V3OV_I	V1OC_I	0	V3OC_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 75. M_REG_FLG register bit description

Bit	Symbol	Description
0	V3OC_I	**Report V3 overcurrent event**
		0 No event detected
		1 V3 OC occurred
		POR, or clear on write (write '1')

Table 75. M_REG_FLG register bit description...*continued*

Bit	Symbol	Description
2	V1OC_I	**Report V1 overcurrent event**
		0 No event detected
		1 V1 OC occurred
		POR, or clear on write (write '1')
3	V3OV_I	**Report V3 overvoltage event**
		0 No event detected
		1 V3 OV occurred
		POR, or clear on write (write '1')
5	V1OV_I	**Report V1 overvoltage event**
		0 No event detected
		1 V1 OV occurred
		POR, or clear on write (write '1')
6	V3UV_I	**Report V3 undervoltage event**
		0 No event detected
		1 V3 UV occurred
		POR, or clear on write (write '1')
8	V1UV_I	**Report V1 undervoltage event**
		0 No event detected
		1 V1 UV occurred
		POR, or clear on write (write '1')
9	V1UVLP_I	**Report V1 undervoltage event in LPON**
		0 No event detected
		1 V1 undervoltage event occurred in LPON
		POR, or clear on write (write '1')
10	V3TSD_I	**Report V3 thermal shutdown event**
		0 No event detected
		1 V3 TSD occurred
		POR, or clear on write (write '1')
12	V1TSD_I	**Report V1 thermal shutdown event**
		0 No event detected
		1 V1 TSD occurred
		POR, or clear on write (write '1')
13	V1TWARN_I	**Report V1 temperature warning event**
		0 No event detected
		1 die V1 TWARN occurred
		POR, or clear on write (write '1')
14	V1UVW_I	**Report V1 undervoltage pre-warning event**
		0 No event detected
		1 V1 undervoltage pre-warning event occurred
		POR, or clear on write (write '1')

Table 75. M_REG_FLG register bit description...*continued*

Bit	Symbol	Description
15	V1LSOC_I	**Report V1 low side overcurrent event**
		0 No event detected
		1 V1 LS OC occurred
		POR, or clear on write (write '1')

22.10 M_REG_MSK

Table 76. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	V1LSOC_M	V1UVW_M	V1TWARN_M	V1TSD_M	0	V3TSD_M	V1UVLP_M	V1UV_M
Read	V1LSOC_M	V1UVW_M	V1TWARN_M	V1TSD_M	0	V3TSD_M	V1UVLP_M	V1UV_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	V3UV_M	V1OV_M	0	V3OV_M	V1OC_M	0	V3OC_M
Read	0	V3UV_M	V1OV_M	0	V3OV_M	V1OC_M	0	V3OC_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 77. M_REG_MSK register bit description

Bit	Symbol	Description
0	V3OC_M	**Inhibit V3 overcurrent interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
2	V1OC_M	**Inhibit V1 overcurrent interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
3	V3OV_M	**Inhibit V3 overvoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
5	V1OV_M	**Inhibit V1 overvoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
6	V3UV_M	**Inhibit V3 undervoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
8	V1UV_M	**Inhibit V1 undervoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

Table 77. M_REG_MSK register bit description*...continued*

Bit	Symbol	Description
9	V1UVLP_M	**Inhibit V1 undervoltage in LPON interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is Inhibited
		POR
10	V3TSD_M	**Inhibit V3 thermal shutdown interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
12	V1TSD_M	**Inhibit V1 thermal shutdown interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
13	V1TWARN_M	**Inhibit V1 thermal warning interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
14	V1UVW_M	**Inhibit V1 undervoltage pre-warning interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
15	V1LSOC_M	**Inhibit V1 low side overcurrent interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

22.11 M_REG1_FLG

Table 78. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	V0UV_I	V0OV_I	0	0	0	0	0	0
Read	V0UV_I	V0OV_I	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 79. M_REG_FLG register bit description

Bit	Symbol	Description
14	V0OV_I	**Report VMON_EXT overvoltage event**
		0 No event detected
		1 VMON_EXT UV occurred
		POR, or Clear on Write (write '1')

Table 79. M_REG_FLG register bit description*...continued*

Bit	Symbol	Description
15	V0UV_I	**Report VMON_EXT undervoltage event**
		0 No event detected
		1 VMON_EXT OV occurred
		POR, or Clear on Write (write '1')

22.12 M_REG1_MSK

Table 80. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	V0UV_M	V0OV_M	0	0	0	0	0	0
Read	V0UV_M	V0OV_M	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 81. M_REG_MSK register bit description

Bit	Symbol	Description
14	V0OV_M	**Inhibit VMON_EXT overvoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
15	V0UV_M	**Inhibit VMON_EXT undervoltage interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

22.13 M_IO_CTRL

Table 82. M_IO_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WK2PUPD		WK3PUPD		HVIO1PUPUD		HVIO1HI	HVIO1LO
Read	WK2PUPD		WK3PUPD		HVIO1PUPUD		0	0
Reset	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse	OTP fuse	0	0
Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 83. M_IO_CTRL register bit description

Bit	Symbol	Description
8	HVIO1LO	**Request to assert HVIO1 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to assert HVIO1 low
		POR, self-clear
9	HVIO1HI	**Request to release HVIO1 when configured as an output**
		0 No effect (IO remain in its current state)
		1 Request to release HVIO1 high
		POR, self-clear
10 to 11	HVIO1PUPUD	**Select the internal pulldown/up on HVIO1 pin**
		00 HVIO1 internal pulldown and pullup are disabled
		01 HVIO1 internal pulldown is enabled and pullup is disabled
		10 HVIO1 internal pulldown is disabled and pullup is enabled
		11 HVIO1 internal pulldown and pullup are configured as cell repeater
		OTP fuse load
12 to 13	WK3PUPD	**Select the internal pulldown/up on WAKE3 pin**
		00 WAKE3 internal pulldown and pullup are disabled
		01 WAKE3 internal pulldown is enabled and pullup is disabled
		10 WAKE3 internal pulldown is disabled and pullup is enabled
		11 WAKE3 internal pulldown and pullup are configured as cell repeater
		OTP fuse load
14 to 15	WK2PUPD	**Select the internal pulldown/up on WAKE2 pin**
		00 WAKE2 internal pulldown and pullup are disabled
		01 WAKE2 internal pulldown is enabled and pullup is disabled
		10 WAKE2 internal pulldown is disabled and pullup is enabled
		11 WAKE2 internal pulldown and pullup are configured as cell repeater
		OTP fuse load

22.14 M_IO_TIMER_FLG

Table 84. M_IO_TIMER_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	LDT_I
Read	0	0	0	0	0	0	0	LDT_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	HVIO1_I	WK3_I	WK2_I	0
Read	0	0	0	0	HVIO1_I	WK3_I	WK2_I	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 85. M_IO_TIMER_FLG register bit description

Bit	Symbol	Description
1	WK2_I	**Report WAKE2 input state change event if not masked**
		0 No event on WAKE2
		1 Event on WAKE2 occurred
		POR, or clear on write (write '1')
2	WK3_I	**ReportWAKE3 input state change event if not masked**
		0 No event on WAKE3
		1 Event on WAKE3 occurred
		POR, or clear on write (write '1')
3	HVIO1_I	**Report HVIO1 input state change event if not masked**
		0 No event on HVIO1
		1 Event on HVIO1 occurred
		POR, or clear on write (write '1')
8	LDT_I	**Report LDT event**
		0 No event on LDT
		1 Event on LDT occurred
		POR, or clear on write (write '1')

22.15 M_IO_TIMER_MSK

Table 86. M_IO_TIMER_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	LDT_M
Read	0	0	0	0	0	0	0	LDT_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	HVIO1_M	WK3_M	WK2_M	0
Read	0	0	0	0	HVIO1_M	WK3_M	WK2_M	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 87. M_IO_TIMER_MSK register bit description

Bit	Symbol	Description
1	WK2_M	**Inhibit WAKE2 input state change interrupt**
		0 Interrupt is not inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
2	WK3_M	**Inhibit WAKE3 input state change interrupt**
		0 Interrupt is not inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR
3	HVIO1_M	**Inhibit HVIO1 input state change interrupt**
		0 Interrupt is not inhibited in Normal mode
		1 Interrupt is always Inhibited
		POR

Table 87. M_IO_TIMER_MSK register bit description...*continued*

Bit	Symbol	Description
8	LDT_M	**Inhibit LDT event interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is always Inhibited
		POR

22.16 M_VSUP_COM_FLG

Table 88. M_VSUP_COM_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	VBOS_UV_I	0	0	0
Read	0	0	0	VBOS2V1SW_S	VBOS_UV_I	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	SPI_CRC_I	SPI_CLK_I	SPI_ REQ_I	0	0	VSUPUV_5P7_I	VSUPOV_I	VSUPUV_ _4P7_I
Read	SPI_CRC_I	SPI_CLK_I	SPI_REQ_I	0	0	VSUPUV_5P7_I	VSUPOV_I	VSUPUV_ _4P7_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 89. M_VSUP_COM_FLG register bit description

Bit	Symbol	Description
0	VSUPUV_4P7_I	**Report VSUP UV event** at 4.7 V
		0 No VSUP UV event at 4.7 V
		1 VSUP UV event occurred at 4.7 V
		POR, or clear on write(write '1')
1	VSUPOV_I	**Report VSUP OV event**
		0 No VSUP OV event
		1 VSUP OV event occurred
		POR, or clear on write (write '1')
2	VSUPUV_5P7_I	**ReportVSUP UV event at 5.7 V**
		0 No VSUP UV event at 5.7 V
		1 VSUP UV event occurred at 5.7 V
		POR, or clear on write (write '1')
5	SPI_REQ_I	**Report SPI request error due to writing or reading in an invalid register**
		0 No error
		1 SPI request error reported
		POR, or clear on write(write'1)
6	SPI_CLK_I	**Report SPI clock error due to wrong number of clock pulses**
		0 No error
		1 SPI clock error reported
		POR, or clear on write (write'1)
7	SPI_CRC_I	**Report SPI CRC error due to incorrect CRC calculation**
		0 No error
		1 SPI CRC error reported
		POR, or clear on write (write'1)

Table 89. M_VSUP_COM_FLG register bit description...*continued*

Bit	Symbol	Description
11	VBOS_UV_I	**Report VBOS undervoltage event**
		0 No event detected
		1 VBOS UV occurred
		POR, or clear on write (write'1)
12	VBOS2V1SW_S	**Real-time status of the switch between VBOS and V1**
		0 The switch is opened
		1 The switch is closed
		Real-time information

22.17 M_VSUP_COM_MSK

Table 90. M_VSUP_COM_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	0	0	VSUPUV_4P7_M	VSUPOV_M	VSUPUV_4P7_M
Read	SPI_CRC_M	SPI_CLK_M	SPI_REQ_M	0	0	VSUPUV_4P7_M	VSUPOV_M	VSUPUV_4P7_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 91. M_VSUP_COM_MSK register bit description

Bit	Symbol	Description
0	VSUPUV_4P7_M	**Inhibit VSUPUV interrupt at 4.7 V**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
1	VSUPOV_M	**Inhibit VSUPOV interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
2	VSUPUV_5P7_M	**Inhibit VSUPUV interrupt at 5.7 V**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
5	SPI_REQ_M	**Inhibit SPI request error interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
6	SPI_CLK_M	**Inhibit SPI clock error interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

Table 91. M_VSUP_COM_MSK register bit description...*continued*

Bit	Symbol	Description
7	SPI_CRC_M	**Inhibit SPI CRC error interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

22.18 M_IOWU_CFG

Table 92. M_IOWU_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	HVIO1_DGLT	WK3_DGLT	WK2_DGLT	0
Read	0	0	0	0	HVIO1_DGLT	WK3_DGLT	WK2_DGLT	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO1_WUCFG		WK3_WUCFG		WK2_WUCFG		0	0
Read	HVIO1_WUCFG		WK3_WUCFG		WK2_WUCFG		0	0
Reset	0	0	0	0	0	1	0	1

Go to main register map

Table 93. M_IOWU_CFG register bit description

Bit	Symbol	Description
2 to 3	WK2_WUCFG	**Configure WAKE2 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High-level wake-up is configured
		10 Low-level wake-up is configured
		11 Reserved
		POR
4 to 5	WK3_WUCFG	**Configure WAKE3 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High-level wake-up is configured
		10 Low-level wake-up is configured
		11 Reserved
		POR
6 to 7	HVIO1_WUCFG	**Configure HVIO1 wake-up polarity**
		00 Input comparator disabled in LP modes only (no consumption)
		01 High-level wake-up is configured
		10 Low-level wake-up is configured
		11 Wake-up via mode selection is configured
		POR
9	WK2_DGLT	**Configure WAKE2 deglitcher time**
		0 WAKE2 deglitcher = 15 us
		1 WAKE2 deglitcher = 65 us
		POR, Write

Table 93. M_IOWU_CFG register bit description*...continued*

Bit	Symbol	Description
10	WK3_DGLT	**Configure WAKE3 deglitcher time**
		0 WAKE3 deglitcher = 15 us
		1 WAKE3 deglitcher = 65 us
		POR, write
11	HVIO1_DGLT	**Configure HVIO1 deglitcher time**
		0 HVIO1 deglitcher = 15 us
		1 HVIO1 deglitcher = 65 us
		POR, write

22.19 M_IOWU_EN

Table 94. M_IOWU_EN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HVIO1_WUEN		WK3_WUEN		WK2_WUEN		0	0
Read	HVIO1_WUEN		WK3_WUEN		WK2_WUEN		0	0
Reset	0	1	0	1	0	1	0	0

Go to main register map

Table 95. M_IOWU_EN register bit description

Bit	Symbol	Description
2 to 3	WK2_WUEN	**Configure WAKE2 wake-up and interrupt capability**
		00 No wake-up and no interrupt
		01 Wake-up only
		10 Interrupt only
		11 Wake-up and interrupt
		POR or Fail-safe state
4 to 5	WK3_WUEN	**Configure WAKE3 wake-up and interrupt capability**
		00 No wake-up and no interrupt
		01 Wake-up only
		10 Interrupt only
		11 Wake-up and interrupt
		POR or Fail-safe state
6 to 7	HVIO1_WUEN	**Configure HVIO1 wake-up and interrupt capability**
		00 No wake-up and no interrupt
		01 Wake=up only
		10 Interrupt only
		11 Wake-up and interrupt
		POR or Fail-safe state

22.20 M_IOWU_FLG

Table 96. M_IOWU_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	HVIO1_WU_I	0	0	WK3_WU_I	WK2_WU_I	0
Read	0	0	HVIO1_WU_I	0	0	WK3_WU_I	WK2_WU_I	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 97. M_IOWU_FLG register bit description

Bit	Symbol	Description
1	WK2_WU_I	**Report WAKE2 wake-up event**
		0 No wake-up by WAKE2 (level)
		1 Wake-up by WAKE2 occurred (level)
		POR, Go to LP modes (clear_all_wu_flg)
2	WK3_WU_I	**Report WAKE3 wake-up event**
		0 No wake-up by WAKE3 (level)
		1 Wake-up by WAKE3 occurred (level)
		POR, Go to LP modes (clear_all_wu_flg)
5	HVIO1_WU_I	**Report HVIO1 wake-up event**
		0 No wake-up by HVIO1 (level)
		1 Wake-up by HVIO1 occurred (level)
		POR, Go to LP modes (clear_all_wu_flg)

22.21 M_WU1_EN

Table 98. M_WU1_EN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	LDT_WUEN		0	0	CAN_WUEN	
Read	0	0	LDT_WUEN		0	0	CAN_WUEN	
Reset	0	0	0	0	0	0	0	1

Go to main register map

Table 99. M_WU1_EN register bit description

Bit	Symbol	Description
0 to 1	CAN_WUEN	**Configure CAN wake-up and interrupt capability**
		00 No wake-up and no interrupt
		01 Wake-up only
		10 Interrupt only
		11 Wake-up and interrupt
		POR or Fail-safe state
4 to 5	LDT_WUEN	**Configure LDT wake-up and interrupt capability**
		00 No wake-up and no interrupt
		01 Wake-up only
		10 Interrupt only
		11 Wake-up and interrupt
		POR or Fail-safe state

22.22 M_WU1_FLG

Table 100. M_WU1_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	FS_EVT	EXT_RSTB_WU
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	WD_OFL_WU	V1_UVLP_WU	INT_TO_WU	GO2NORMAL_WU	0	LDT_WU_I	0	CAN_WU_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 101. M_WU1_FLG register bit description

Bit	Symbol	Description
0	CAN_WU_I	**Report CAN wake-up event**
		0 No wake-up by CAN
		1 Wake-up by CAN occurred
		POR, Go to LP modes (clear_all_wu_flg)
2	LDT_WU_I	**Report LDT wake-up event**
		0 No wake-up by LDT
		1 Wake-up by LDT occurred
		POR, Go to LP modes (clear_all_wu_flg)
4	GO2NORMAL_WU	**Report GO2NORMAL request from MCU wake-up event**
		0 No wake-up by MCU GO2NORMAL request
		1 Wake-up by MCU GO2NORMAL request occurred
		POR, Go to LP modes (clear_all_wu_flg)
5	INT_TO_WU	**Report a wake-up event generated by an interrupt time out**
		0 No wake-up generated by Interrupt time out
		1 Wake-up by Interrupt Time Out occurred
		POR, Go to LP modes (clear_all_wu_flg)

Table 101. M_WU1_FLG register bit description*...continued*

Bit	Symbol	Description
6	V1_UVLP_WU	**Report V1 LPON undervoltage wake-up event**
		0 No wake-up by V1 LPON undervoltage
		1 Wake-up by V1 LPON undervoltage occurred
		POR, Go to LP modes (clear_all_wu_flg)
7	WD_OFL_WU	**Report watchdog max error failure wake-up event**
		0 No wake-up by max error failure
		1 Wake-up by watchdog max error failure occurred
		POR, Go to LP modes (clear_all_wu_flg)
8	EXT_RSTB_WU	**Report RSTB assertion wake-up event**
		0 No wake-up by to RSTB assertion
		1 Wake-up by to RSTB assertion occurred
		POR, Go to LP modes (clear_all_wu_flg)
9	FS_EVT	**Report a fail-safe event**
		0 No fail-safe event
		1 Fail-safe event occurred (FSM went to Fail-safe state)
		POR, or clear on write (write '1')

22.23 M_AMUX_CTRL

Table 102. M_AMUX_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	AMUX_PD_DIS	0	AMUX_EN	AMUX_DIV
Read	0	0	0	0	0	0	AMUX_EN	AMUX_DIV
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	AMUX				
Read	0	0	0	AMUX				
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 103. M_AMUX_CTRL register bit description

Bit	Symbol	Description
0 to 4	AMUX	**Select AMUX input channel**
		00000 AGND is selected
		00001 V1p6 internal voltage (VDIG) is selected
		00010 V1 voltage is selected
		00011 Reserved
		00100 V3 voltage is selected
		00101 VBOS internal voltage is selected
		00110 VSUP voltage is selected (divider ratio configurable by SPI)
		00111
		01000
		01001
		01010
		01011
		01100 V1 TWARN temperature sensor (die temperature sensor) is selected temperature sensor (0.4 V-1.65 V)
		01101 V1 TSD temperature sensor is selected (0.4 V-1.65 V)
		01110 Reserved
		01111 V3 temperature sensor is selected
		10000 VDDIO not divided is selected
		10001 CAN temperature sensor is selected (0.4 V-1.65 V)
		10010 VMON_EXT pin voltage is selected
		10011 low-power main band gap is selected (0.995 V-1.005 V)
		10100 VANA (main analog voltage supply) is selected (1.3 V-1.65 V)
		10101 VCC5CAN pin voltage is selected (3.3 V-5.5 V)
		POR
8	AMUX_DIV	**Select AMUX divider ratio for high-voltage channels**
		0 Low divider ratio is selected (div by 7.5)
		1 High divider ratio is selected (div by 14)
		POR
9	AMUX_EN	**Enable AMUX block**
		0 AMUX is disabled (HIZ, int pulldown)
		1 AMUX is enabled in Normal mode only
		POR
11	AMUX_PD_DIS	**Disable AMUX pulldown**
		0 AMUX pin pulldown is enabled
		1 AMUX pin pulldown is disabled
		POR

22.24 M_LDT_CFG1

Table 104. M_LDT_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_AFTER_RUN							
Read	LDT_AFTER_RUN							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LDT_AFTER_RUN							
Read	LDT_AFTER_RUN							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 105. M_LDT_CFG1 register bit description

Bit	Symbol	Description
0 to 15	LDT_AFTER_RUN	**Configure and read the after-run LDT timer**
		LDT timer value in Normal mode
		POR, LDT count started

22.25 M_LDT_CFG2

Table 106. M_LDT_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_WUP_L							
Read	LDT_WUP_L							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LDT_WUP_L							
Read	LDT_WUP_L							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 107. M_LDT_CFG2 register bit description

Bit	Symbol	Description
0 to 15	LDT_WUP_L	**Configure and read the 16 less significant bits of wake-up LDT timer**
		LDT timer value in LP mode (LSB)
		POR, LDT count started

22.26 M_LDT_CFG3

Table 108. M_LDT_CFG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LDT_WUP_H							
Read	LDT_WUP_H							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 109. M_LDT_CFG3 register bit description

Bit	Symbol	Description
0 to 7	LDT_WUP_H	**Configure and read the 8 more significant bits of LDT wake-up timer**
		LDT timer value in LP mode (MSB)
		POR, LDT count started

22.27 M_LDT_CTRL

Table 110. M_LDT_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	-
Read	LDT2LP	LDT_FNCT			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 111. M_LDT_CTRL register bit description

Bit	Symbol	Description
0	LDT_RUN	**LDT status**
		0 LDT is idle
		1 LDT is busy
		POR, LDT stopped
1	LDT_EN	**Start LDT timer operation**
		0 LDT is disabled
		1 LDT starts counting
		POR

Table 111. M_LDT_CTRL register bit description*...continued*

Bit	Symbol	Description
2	LDT_MODE	**Set LDT operation mode**
		0 LDT is set to long count (1 s)
		1 LDT is set to short count (128 us)
		POR
3	LDT_SEL	**Configure and read LDT timer selection**
		0 Target value of wake-up LDT timer can be read or write
		1 Real-time value of 24-bits timer is reported (once LDT stopped)
		POR
4 to 6	LDT_FNCT[2:0]	**Select LDT function**
		000 Function1 is selected
		001 Function2 is selected
		010 Function3 is selected
		011 Function4 is selected
		100 Function5 is selected
		101 Not used
		110 Not used
		111 Not used
		POR
7	LDT2LP	**Select LP mode transition from LDT F2 and F3**
		0 Go to LPOFF
		1 Go to LPON
		POR

22.28 M_CAN

Table 112. M_CAN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	CAN_WU_TMR_BYP	CAN_MODE	
Read	0	0	0	0	0	CAN_WU_TMR_BYP	CAN_MODE	
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	CAN_FS_DIS	0	0	0	CAN_TXD_TO_I	CAN_TSD_I
Read	CAN_ACTIVE_MODE_S	0	CAN_FS_DIS	0	CAN_TXD_TO_S	CAN_TSD_S	CAN_TXD_TO_I	CAN_TSD_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 113. M_CAN register bit description

Bit	Symbol	Description
0	CAN_TSD_I	**Report CAN overtemperature event**
		0 No event detected
		1 CAN thermal shutdown occurred
		POR, or clear on write (write '1')
1	CAN_TXD_TO_I	**Report CAN TXD dominant timeout event**
		0 No event detected
		1 Dominant timeout occurred
		POR, or clear on write (write '1')
2	CAN_TSD_S	**Real-time status of CAN thermal shutdown**
		0 Tj < thermal shutdown limit
		1 Tj > thermal shutdown limit
		Real-time information
3	CAN_TXD_TO_S	**Real-time status of CAN transceiver TXD dominant timeout**
		0 Normal operation
		1 TXD dominant timeout condition is present
		Real-time information
5	CAN_FS_DIS	**Disable the CAN when RSTB or LIMP0 is activated**
		0 CAN transceiver is set offline
		1 CAN transceiver keeps the current state
		POR
7	CAN_ACTIVE_MODE_S	**Real-time status of CAN mode**
		0 CAN is neither in listen-only mode nor in Normal mode
		1 CAN is either in listen-only mode or in Normal mode
		Real-time information
8 to 9	CAN_MODE	**Select the CAN mode control**
		00 Transceiver offline (TX and RX disabled)
		01 Transceiver receive-only mode (TX disabled and RX enabled)
		10 Transceiver active mode (TX and RX enabled) reacting on V3UV
		11 Transceiver active mode (TX and RX enabled) reacting on V3UV
		POR
10	CAN_WU_TMR_BYP	**Bypass CANRXD assert low after CAN WU**
		0 Trxd_wu_timeout not bypassed
		1 Trxd_wu_timeout bypassed
		POR

22.29 M_CAN_MSK

Table 114. M_CAN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0			CAN_TXD_TO_M	CAN_TSD_M
Read	0	0	0	CAN_FSM_STATE_S			CAN_TXD_TO_M	CAN_TSD_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 115. M_CAN_MSK register bit description

Bit	Symbol	Description
0	CAN_TSD_M	**Inhibit CAN temperature shutdown interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR, or clear on write (write '1')
1	CAN_TXD_TO_M	**Inhibit CAN TXD Dominant timeout interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR, or clear on write (write '1')
2 to 4	CAN_FSM_STATE_S	**Report the CAN state machine state**
		000 CAN OFF
		001 CAN_WAKE_CAPABLE
		010 Invalid state
		011 CAN_OFF
		100 Invalid state
		101 CAN_LISTEN_ONLY
		110 Invalid state
		111 CAN_ACTIVE
		Real-time information

22.30 M_MEMORY0

Table 116. M_MEMORY0 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEMORY0							
Read	MEMORY0							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	MEMORY0							
Read	MEMORY0							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 117. M_MEMORY0 register bit description

Bit	Symbol	Description
0 to 15	MEMORY0	**Provide 16 memory bits**
		Read or write MEMORY0 memory bits
		Reset on power-on reset (POR)

22.31 M_MEMORY1

Table 118. M_MEMORY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEMORY1							
Read	MEMORY1							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	MEMORY1							
Read	MEMORY1							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 119. M_MEMORY1 register bit description

Bit	Symbol	Description
0 to 15	MEMORY1	**Provide 16 memory bits**
		Read or write MEMORY1 memory bits
		Reset on power-on reset (POR)

22.32 M_HW_ID

Table 120. M_HW_ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	LIMP0_ TH_SEL	HIDW2_ TH_SEL	HIDW3_ TH_SEL	HIDW2_ 10MA_EN	HIDW3_ 10MA_EN	HIDW2_ ENABLE	HIDW3_ ENABLE
Read	0	LIMP0_ TH_SEL	HIDW2_ TH_SEL	HIDW3_ TH_SEL	HIDW2_ 10MA_EN	HIDW3_ 10MA_EN	HIDW2_ ENABLE	HIDW3_ ENABLE
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	HIDW2PU_EN	HIDW2PU_DIS	HIDW2PD_EN	HIDW2PD_DIS	HIDW3PU_EN	HIDW3PU_DIS	HIDW3PD_EN	HIDW3PD_DIS
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 121. M_HW_ID register bit description

Bit	Symbol	Description
0	HIDW3PD_DIS	**Request to disable HWID pulldown for WAKE 3**
		0 No effect (pulldown remains in its current state)
		1 Request to disable pulldown
		POR

Table 121. M_HW_ID register bit description*...continued*

Bit	Symbol	Description
1	HIDW3PD_EN	**Request to enable HWID pulldown for WAKE 3**
		0 No effect (pulldown remains in its current state)
		1 Request to enable pulldown
		POR
2	HIDW3PU_DIS	**Request to disable HWID pullup for WAKE 3**
		0 No effect (pullup remains in its current state)
		1 Request to disable pullup
		POR
3	HIDW3PU_EN	**Request to enable HWID pullup for WAKE 3**
		0 No effect (pullup remains in its current state)
		1 Request to enable pullup
		POR
4	HIDW2PD_DIS	**Request to disable HWID pulldown for WAKE 2**
		0 No effect (pulldown remains in its current state)
		1 Request to disable pulldown
		POR
5	HIDW2PD_EN	**Request to enable HWID pulldown for WAKE 3**
		0 No effect (pulldown remains in its current state)
		1 Request to enable pulldown
		POR
6	HIDW2PU_DIS	**Request to disable HWID pullup for WAKE 2**
		0 No effect (pullup remain in its current state)
		1 Request to disable pullup
		POR
7	HIDW2PU_EN	**Request to enable HWID pullup for WAKE 2**
		0 No effect (pullup remains in its current state)
		1 Request to enable pullup
		POR
8	HIDW3_ENABLE	**Request to use WAKE3 pin as HID**
		0 WAKE3 not used as HID
		1 WAKE3 used as HID (set by user when configuring PU/PD)
		POR
9	HIDW2_ENABLE	**Request to use WAKE2 pin as HID**
		0 WAKE2 not used as HID
		1 WAKE2 used as HID (set by user when configuring PU/PD)
		POR
10	HIDW3_10MA_EN	**HID1 (WAKE3 pin) current source selection**
		0 Lower-current setting for PU/PD
		1 Higher-current setting for PU/PD (10 mA)
		POR
11	HIDW2_10MA_EN	**HID0 (WAKE2 pin) current source selection**
		0 Lower-current setting for PU/PD
		1 Higher-current setting for PU/PD (10 mA)
		POR

Table 121. M_HW_ID register bit description*...continued*

Bit	Symbol	Description
12	HIDW3_TH_SEL	**HID1 (WAKE3 pin) input threshold selection**
		0 Lower threshold
		1 Higher threshold
		POR
13	HIDW2_TH_SEL	**HID0 (WAKE2 pin) input threshold selection**
		0 Lower threshold
		1 Higher threshold
		POR
14	LIMP0_TH_SEL	**LIMP0 input threshold selection**
		0 Lower threshold
		1 Higher threshold
		POR

23 Fail-safe register mapping

23.1 FS_I_OVUV_CFG1

Table 122. FS_I_OVUV_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	V1MON_OV_ RSTB_IMPACT	0	V1MON_OV_ LIMP0_IMPACT	V1MON_UV_ RSTB_IMPACT	0
Read	0	0	0	V1MON_OV_ RSTB_IMPACT	0	V1MON_OV_ LIMP0_IMPACT	V1MON_UV_ RSTB_IMPACT	0
Reset	0	0	0	OTP fuse	0	1	OTP fuse	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	V1MON_UV_ LIMP0_IMPACT	0	0	0	0	0	0	0
Read	V1MON_UV_ LIMP0_IMPACT	0	0	0	0	0	0	0
Reset	1	0	0	0	0	0	0	0

Go to safety-related register map

Table 123. FS_I_OVUV_CFG1 register bit description

Bit	Symbol	Description
7	V1MON_UV_LIMP0_IMPACT	**Configure V1MON UV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
9	V1MON_UV_RSTB_IMPACT	**Configure V1MON UV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load
10	V1MON_OV_LIMP0_IMPACT	**Configure V1MON OV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
12	V1MON_OV_RSTB_IMPACT	**Configure V1MON OV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load

23.2 FS_I_OVUV_CFG2

Table 124. FS_I_OVUV_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	V3MON_OV_RSTB_IMPACT	0	V3MON_OV_LIMP0_IMPACT	V3MON_UV_RSTB_IMPACT	0
Read	0	0	0	V3MON_OV_RSTB_IMPACT	0	V3MON_OV_LIMP0_IMPACT	V3MON_UV_RSTB_IMPACT	0
Reset	0	0	0	OTP fuse	0	1	OTP fuse	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	V3MON_UV_LIMP0_IMPACT	0	V0MON_OV_RSTB_IMPACT	0	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	0	V0MON_UV_LIMP0_IMPACT
Read	V3MON_UV_LIMP0_IMPACT	0	V0MON_OV_RSTB_IMPACT	0	V0MON_OV_LIMP0_IMPACT	V0MON_UV_RSTB_IMPACT	0	V0MON_UV_LIMP0_IMPACT
Reset	1	0	OTP fuse	0	1	OTP fuse	0	1

Go to safety-related register map

Table 125. FS_I_OVUV_CFG2 register bit description

Bit	Symbol	Description
0	V0MON_UV_LIMP0_IMPACT	**Configure VMON_EXT UV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
2	V0MON_UV_RSTB_IMPACT	**Configure VMON_EXT UV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load
3	V0MON_OV_LIMP0_IMPACT	**Configure VMON_EXT OV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
5	V0MON_OV_RSTB_IMPACT	**Configure VMON_EXT OV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load
7	V3MON_UV_LIMP0_IMPACT	**Configure V3MON UV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
9	V3MON_UV_RSTB_IMPACT	**Configure V3MON UV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load

Table 125. FS_I_OVUV_CFG2 register bit description*...continued*

Bit	Symbol	Description
10	V3MON_OV_LIMP0_IMPACT	**Configure V3MON OV impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
12	V3MON_OV_RSTB_IMPACT	**Configure V3MON OV impact on RSTB**
		0 No effect
		1 RSTB assertion
		OTP fuse load

23.3 FS_I_ERRMON_LIMP0_CFG

Table 126. FS_I_ERRMON_LIMP0_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LIMP0_GPO	0	0	0	0	0	0	0
Read	LIMP0_GPO	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	ERRMON_M	ERRMON_FLT_POLARITY	ERRMON_ACK_TIME		ERRMON_FS_REACTION
Read	0	0	0	ERRMON_M	ERRMON_FLT_POLARITY	ERRMON_ACK_TIME		ERRMON_FS_REACTION
Reset	0	0	0	0	0	0	0	1

Go to safety-related register map

Table 127. FS_I_ERRMON_LIMP0_CFG register bit description

Bit	Symbol	Description
0	ERRMON_FS_REACTION	**Configure reaction on RSTb or fail-safe output when a fault is detected on ERRMON**
		0 LIMP0 only is asserted low in case of fault detection on ERRMON
		1 RSTb and LIMP0 only is asserted low in case of fault detected on ERRMON
		POR
1 to 2	ERRMON_ACK_TIME	**Configure acknowledge timing following a fault detection on ERRMON**
		00 0 ms
		01 2 ms
		10 4 ms
		11 8 ms
		POR
3	ERRMON_FLT_POLARITY	**Configure ERRMON fault polarity**
		0 Low-level is a fault after a negative-edge transition
		1 High-level is a fault after a positive-edge transition
		POR
4	ERRMON_M	**Interruption mask on ERRMON**
		0 Interruption not masked
		1 Interruption masked
		POR

Table 127. FS_I_ERRMON_LIMP0_CFG register bit description*...continued*

Bit	Symbol	Description
15	LIMP0_GPO	**Configure LIMP0 pin behavior**
		0 LIMP0 is a safety pin
		1 LIMP0 is a GPO
		POR

23.4 FS_I_FSSM_CFG

Table 128. FS_I_FSSM_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	RSTB_ REQ_EN	EXT_ RSTB_DIS	RSTB8S_DIS	RSTB_DUR	0	0	0	FLT_ERR_ LIMIT
Read	RSTB_ REQ_EN	EXT_ RSTB_DIS	RSTB8S_DIS	RSTB_DUR	0	0	0	FLT_ERR_ LIMIT
Reset	0	0	OTP fuse	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FLT_ERR_ LIMIT	FLT_MID_ RSTB_IMPACT	0	FLT_MID_ LIMP0_IMPACT	FLT_ERR_CNT			
Read	FLT_ERR_ LIMIT	FLT_MID_ RSTB_IMPACT	0	FLT_MID_ LIMP0_IMPACT	FLT_ERR_CNT			
Reset	1	1	0	1	0	0	0	1

Go to safety-related register map

Table 129. FS_I_FSSM_CFG register bit description

Bit	Symbol	Description
0 to 3	FLT_ERR_CNT	**Reflect the value of the fault-error counter**
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12
		1101 12
		1110 12
		1111 12
		POR
4	FLT_MID_LIMP0_IMPACT	**Configure LIMP0 reaction when external reset is detected fault-error counter ≥ intermediate value**
		0 No action
		1 LIMP0 assertion
		POR

Table 129. FS_I_FSSM_CFG register bit description*...continued*

Bit	Symbol	Description
6	FLT_MID_RSTB_IMPACT	**Configure RSTB reaction when external reset is detected fault-error counter ≥ intermediate value**
		0 No action
		1 RSTB assertion
		POR
7 to 8	FLT_ERR_LIMIT	**Configure the fault-error counter max value**
		00 Max Value = 2
		01 Max Value = 6
		10 Max Value = 8
		11 Max Value = 12
		POR
12	RSTB_DUR	**Configure RSTB pulse duration**
		0 10 ms
		1 1 ms
		POR
13	RSTB8S_DIS	**Disable the RSTB low 8 s timer**
		0 RSTB low 8 s timer is enabled
		1 RSTB low 8 s time is disabled
		OTP Fuse load
14	EXT_RSTB_DIS	**Disable the external RSTB monitoring (except RSTB 8 s time out)**
		0 External RSTB monitoring is enabled
		1 External RSTB monitoring is disabled
		POR
15	RSTB_REQ_EN	**Enable the RSTB request by the MCU**
		0 RSTB_REQ disabled
		1 RSTB_REQ enabled
		POR

23.5 FS_I_WD_CFG

Table 130. FS_I_WD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	WD_RSTB_IMPACT	0	WD_LIMP0_IMPACT	WD_DIS_LPON	WD_RFR_LIMIT		WD_ERR_LIMIT
Read	0	WD_RSTB_IMPACT	0	WD_LIMP0_IMPACT	WD_DIS_LPON	WD_RFR_LIMIT		WD_ERR_LIMIT
Reset	0	1	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WD_ERR_LIMIT	0			0			
Read	WD_ERR_LIMIT	WD_RFR_CNT			WD_ERR_CNT			
Reset	1	0	0	0	0	0	0	0

Go to safety-related register map

Table 131. FS_I_WD_CFG register bit description

Bit	Symbol	Description
0 to 3	WD_ERR_CNT	**Reflect the value of the watchdog error counter**
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 8
		1010 9
		1011 10
		1100 11
		1101 12
		1110 12
		1111 12
		POR
4 to 6	WD_RFR_CNT	**Reflect the value of the watchdog refresh counter**
		000 0
		001 1
		010 2
		011 3
		100 4
		101 5
		110 6
		111 7
		POR
7 to 8	WD_ERR_LIMIT	**Configure the watchdog error counter limit**
		00 8
		01 6
		10 4
		11 2
		POR
9 to 10	WD_RFR_LIMIT	**Configure the watchdog refresh counter limit**
		00 6
		01 4
		10 2
		11 1
		POR
11	WD_DIS_LPON	**Automatically disable the watchdog in LPON mode (when GO2LPON)**
		0 WD stays enabled in LPON
		1 WD is disabled in LPON
		POR

Table 131. FS_I_WD_CFG register bit description...*continued*

Bit	Symbol	Description
12	WD_LIMP0_IMPACT	**Configure watchdog error impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
14	WD_RSTB_IMPACT	**Configure watchdog error impact on RSTB**
		0 No effect
		1 RSTB assertion
		POR

23.6 FS_WDW_CFG

Table 132. FS_WDW_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	WDW_EN	0	WDW_PERIOD
Read	0	0	0	0	0	WDW_EN	0	WDW_PERIOD
Reset	0	0	0	0	0	0	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WDW_PERIOD			0	0	0	0	0
Read	WDW_PERIOD			0	0	0	0	0
Reset	0	0	1	0	0	0	0	0

Go to safety-related register map

Table 133. FS_WDW_CFG register bit description

Bit	Symbol	Description
5 to 8	WDW_PERIOD	**Configure the watchdog window period**
		0000 INFINITE Time Out, Window fully opened
		0001 1 ms
		0010 2 ms
		0011 4 ms
		0100 8 ms
		0101 16 ms
		0110 32 ms
		0111 64 ms
		1000 128 ms
		1001 256 ms (default value)
		1010 512 ms
		1011 1024 ms
		1100 2048 ms
		1101 4096 ms
		1110 8192 ms
		1111 16384 ms
		POR, WD_DISABLE

Table 133. FS_WDW_CFG register bit description...*continued*

Bit	Symbol	Description
10	WDW_EN	**Enable the watchdog window**
		0 Watchdog window is disabled (watchdog time out)
		1 Watchdog window is enabled (watchdog window 50 %)
		POR

23.7 FS_WD_TOKEN

Table 134. FS_WD_TOKEN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0							
Read	WD_TOKEN							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0							
Read	WD_TOKEN							
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 135. FS_WD_TOKEN register bit description

Bit	Symbol	Description
0 to 15	WD_TOKEN	**Read watchdog token code**
		0x5AB2 (default value) or 0xD564
		Reset on power-on reset (POR) or WD disabled

23.8 FS_WD_ANSWER

Table 136. FS_WD_ANSWER register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ANSWER							
Read	0							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	WD_ANSWER							
Read	0							
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 137. FS_WD_ANSWER register bit description

Bit	Symbol	Description
0 to 15	WD_ANSWER	**Write the WD answer**
		WD_TOKEN[15:0] should be written
		POR

23.9 FS_LIMP0_REL

Table 138. FS_ LIMP0_REL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	RELEASE_LIMP0							
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write								LIMP0_REL
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 139. FS_LIMP0_REL register bit description

Bit	Symbol	Description
0	LIMP0_REL	**Request the LIMP0 pin release when use a GPO**
		0 No action
		1 LIMP0 release
		POR, Self clear
8 to 15	RELEASE_LIMP0	**Write secured 8 bits word to release LIMP0 when used as a safety pin**
		WD_TOKEN[15:8] with LSB and MSB inverted, then complemented
		POR

23.10 FS_ABIST

Table 140. FS_ABIST register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	LAUNCH_ABIST	CLEAR_ABIST	0	0	0	0	0
Read	0	0	0	ABIST_DONE	0	ABIST_V0 MON_DIAG	ABIST_V1 UVLP_DIAG	ABIST_V1 MON_DIAG
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	ABIST_V0MON	ABIST_ V1UVLP	ABIST_V1MON	0	ABIST_V3MON
Read	0	ABIST_V3 MON_DIAG	0	ABIST_V0MON	ABIST_ V1UVLP	ABIST_V1MON	0	ABIST_V3MON
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 141. FS_ABIST register bit description

Bit	Symbol	Description
0	ABIST_V3MON	**Request ABIST on V3MON**
		0 No ABIST
		1 ABIST on V3MON requested
		POR

Table 141. FS_ABIST register bit description*...continued*

Bit	Symbol	Description
2	ABIST_V1MON	**Request ABIST on V1MON**
		0 No ABIST
		1 ABIST on V1MON requested
		POR
3	ABIST_V1UVLP	**Request ABIST on V1UVLP**
		0 No ABIST
		1 ABIST on V1UVLP requested
		POR
4	ABIST_V0MON	**Request ABIST on VMON_EXT**
		0 No ABIST
		1 ABIST on VMON_EXT requested
		POR
6	ABIST_V3MON_DIAG	**Report ABIST status on V3MON**
		0 ABIST not executed on V3MON or fail on V3MON
		1 V3MON ABIST PASS
		POR / Clear on write / LAUNCH_ABIST
8	ABIST_V1MON_DIAG	**Report ABIST status on V1MON**
		0 ABIST not executed on V1MON or fail on V1MON
		1 V1MON ABIST PASS
		POR / CLEAR_ABIST
9	ABIST_V1UVLP_DIAG	**Report ABIST status on V1UVLP**
		0 ABIST not executed on V1UVLP or fail on V1UVLP
		1 V1UVLP ABIST PASS
		POR / CLEAR_ABIST
10	ABIST_V0MON_DIAG	**Report ABIST status on V0MON**
		0 ABIST not executed on V0MON or fail on V0MON
		1 V0MON ABIST PASS
		POR / CLEAR_ABIST
12	ABIST_DONE	**Diagnostic of ABIST on demand**
		0 ABIST not executed
		1 ABIST executed
		POR / CLEAR_ABIST
13	CLEAR_ABIST	**Clear ABIST flags**
		0 No action
		1 Clear ABIST flags (ABIST_DONE, ABIST_VxMON_DIAG, ABIST_V1UVLP_DIAG)
		POR
14	LAUNCH_ABIST	**Launch ABIST on selected VMON**
		0 No action
		1 Launch ABIST
		POR

23.11 FS_SAFETY_OUTPUTS

Table 142. FS_SAFETY_OUTPUTS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ RSTB_REQ	RSTB_EXT	RSTB_EVT	0	0	RSTB_DIAG	RSTB_REQ	0
Read	0	RSTB_EXT	RSTB_EVT	RSTB_DRV	RSTB_SNS	RSTB_DIAG	0	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	LIMP0_DIAG	LIMP0_REQ
Read	0	0	0	0	LIMP0_DRV	LIMP0_SNS	LIMP0_DIAG	0
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 143. FS_SAFETY_OUTPUTS register bit description

Bit	Symbol	Description
0	LIMP0_REQ	**Request an assertion of LIMP0**
		0 No action
		1 LIMP0 assertion
		POR, Self clear
1	LIMP0_DIAG	**Report a LIMP0 short to HIGH**
		0 No failure
		1 Short to high detected
		POR, or clear on write (write '1')
2	LIMP0_SNS	**Sense LIMP0 pad**
		0 LIMP0 pad is sensed low
		1 LIMP0 pad is sensed high
		Real-time information
3	LIMP0_DRV	**Report the digital command of LIMP0 driver**
		0 LIMP0 Driver command sensed low
		1 LIMP0 Driver command sensed high
		Real-time information
9	RSTB_REQ	**Request an assertion of reset**
		0 No action
		1 RSTB assertion (pulse)
		POR, Self clear
10	RSTB_DIAG	Report a reset short to high
		0 No failure
		1 Short to high detected
		POR, or clear on write (write '1')
11	RSTB_SNS	**Sense RSTB pad**
		0 RSTB pad is sensed low
		1 RSTB pad is sensed high
		Real-time information

Table 143. FS_SAFETY_OUTPUTS register bit description*...continued*

Bit	Symbol	Description
12	RSTB_DRV	**Report the digital command of RSTB driver**
		0 RSTB Driver command sensed low
		1 RSTB Driver command sensed high
		Real-time information
13	RSTB_EVT	**Report a RSTB Event generated by FS24**
		0 No RSTB event
		1 RSTB event occurred
		POR, or clear on Write(write '1')
14	RSTB_EXT	**Report a RSTB pin assertion**
		0 No RSTB pin assertion
		1 RSTB pin assertion Occurred
		POR, or clear on write (write '1')
15	WD_RSTB_REQ	**Request a WD timer Reset without asserting RSTB pin**
		0 No action
		1 WD timer reset requested
		POR, or clear on write (write '1')

23.12 FS_SAFETY_FLG

Table 144. FS_SAFETY_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	ERRMON_ TMR_EXP_I	ERRMON_ACK	ERRMON_I	0	WD_NOK_M	WD_NOK_I
Read	0	0	ERRMON_ TMR_EXP_I	0	ERRMON_I	ERRMON_RT	WD_NOK_M	WD_NOK_I
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 145. FS_SAFETY_FLG register bit description

Bit	Symbol	Description
8	WD_NOK_I	**Report a watchdog refresh error**
		0 WD refresh OK
		1 WD refresh not OK
		POR, or clear on write '1'
9	WD_NOK_M	**Mask watchdog not OK refresh interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR
10	ERRMON_RT	**Report ERRMON real-time pin state**
		0 Low level
		1 High Level
		POR

Table 145. FS_SAFETY_FLG register bit description*...continued*

Bit	Symbol	Description
11	ERRMON_I	**Report an error in the ERRMON input**
		0 No error
		1 Error detected
		POR, or clear on write (write '1')
12	ERRMON_ACK	**Acknowledge ERRMON Failure Timer**
		0 No error
		1 Acknowledge ERRMON timeout
		POR
13	ERRMON_TMR_EXP_I	**Report that the ERRMON timer was not acknowledged by user**
		0 No error/error acknowledged by user on time
		1 ERRMON timer expired with no acknowledgement by user
		POR, or clear on write (write '1')

23.13 FS_CRC

Table 146. FS_CRC register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	INIT_CRC_NOK_M	INIT_CRC_NOK_I	0	0	INIT_CRC_LIMP0_IMPACT	0
Read	0	0	INIT_CRC_NOK_M	INIT_CRC_NOK_I	0	0	INIT_CRC_LIMP0_IMPACT	0
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	CRC_VALUE							
Read	CRC_VALUE							
Reset	0	0	0	0	0	0	0	0

Go to safety-related register map

Table 147. FS_CRC register bit description

Bit	Symbol	Description
0 to 7	CRC_VALUE	**INIT registers CRC value calculated by the MCU (CRC check every 5 ms in Normal mode only)**
		CRC_VALUE[7:0]
		POR
9	INIT_CRC_LIMP0_IMPACT	**Configure CRC impact on LIMP0**
		0 No effect
		1 LIMP0 assertion
		POR
12	INIT_CRC_NOK_I	**Report an INIT register CRC error**
		0 No error detected
		1 INIT registers CRC error detected
		POR
13	INIT_CRC_NOK_M	**Mask CRC not OK interrupt**
		0 Interrupt is not inhibited
		1 Interrupt is inhibited
		POR

24 OTP bits description

24.1 Main OTP overview

Table 148. Main OTP overview

Address	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x1C	**OTP_DEVICE_VER**	—	—	RSTB_DUR_OTP	ABIST_EN_OTP	CAN_EN_OTP	LDTIM_EN_OTP	LIMP0_EN_OTP	V0MON_EN_OTP
0x1D	**OTP_PROG_ID**	PROG_IDH_OTP[3:0]				PROG_IDL_OTP[3:0]			
0x1E	**OTP_V1_CFG1**	VSUP_UVTH_OTP	BUCK_SRHSON_OTP[2:0]			BUCK_SRHSOFF_OTP[1:0]		BUCK_SS_OTP[1:0]	
0x1F	**OTP_V1_CFG2**	BUCK_CLK_OTP	BUCK_RCOMP_OTP[2:0]			BUCK_CCOMP_OTP[1:0]		-	
0x20	**OTP_V1_CFG3**	BUCK_OC_DGLT_OTP[1:0]		BUCK_SC_OTP[5:0]					
0x21	**OTP_V1_CFG4**	—	BUCK_PK_OC_PFM_OTP[2:0]			BUCK_PFM_TOFF_OTP[1:0]		BUCK_PFM_TON_OTP[1:0]	
0x22	**OTP_V1_CFG5**	CONF_OV_V1_OTP	CONF_TSD_V1_OTP	BUCK_PK_OC_PWM_OTP[2:0]			BUCK_AVG_OC_PWM_OTP[2:0]		
0x23	**Reserved**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x24	**OTP_V1_CFG7**	V1UVLP_TH_OTP	VV1_BUCK_RANGE_OTP	VV1_BUCK_OTP[5:0]					
0x25	**OTP_V1_CFG8**	BUCK_LP_DVS_OTP[1:0]		VV1_LP_BUCK_OTP[5:0]					
0x26	**OTP_V3_CFG**	—	—	CONF_OV_V3_OTP	CONF_TSD_V3_OTP	—	VV3_OTP	V3_SLOT_OTP[1:0]	
0x27	**OTP_HVIO_CFG1**	HVIO1PUPD_OTP[1:0]		WK2PUPD_OTP[1:0]		WK3PUPD_OTP[1:0]		HVIO1PUPD_OTP[1:0]	
0x28	**OTP_HVIO_CFG2**	HVIO1_OUT_EN_OTP	HVIO1_OUT_DFLT_OTP	HVIO1_SLOT_POL_OTP	HVIO1_PU_SEL_OTP	—	—	—	—
0x29	**OTP_MAIN_SYS_CFG**	VBOS2 V1_SW _LP_EN_OTP	MOD_CONF_OTP	MOD_EN_OTP	SLOT_BYP_OTP	—	CRC_DIS_OTP	CRC_DBG_DIS_OTP	CRC_INV_OTP

24.2 Main OTP bits description

Table 149. Main OTP bits description

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x1C	OTP_DEVICE_VER	RSTB_DUR_OTP	Configure RSTB pulse duration	**0**	**10 ms**
				1	1 ms
		ABIST_EN_OTP	Enable ABIST checks	**0**	**ABIST checks are disabled**
				1	ABIST checks are enabled
		CAN_EN_OTP	Enable the CAN physical layer	**0**	**CAN is disabled**
				1	CAN is enabled
		LDTIM_EN_OTP	Enable the Long Duration Timer	**0**	**LDT is disabled**
				1	LDT is enabled
		LIMP0_EN_OTP	Enable LIMP0 safety output	**0**	**LIMP0 is disabled**
				1	LIMP0 is enabled
		V0MON_EN_OTP	Enable VMON_EXT pin for V0MON monitoring	**0**	**VMON_EXT pin is disabled**
				1	VMON_EXT pin is enabled

Table 149. Main OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x1D	OTP_PROG_ID	PROG_IDH_OTP[3:0]	Report the OTP code	**0000**	**A**
				0001	B
				0010	C
				0011	D
				0100	E
				0101	F
				0110	G
				0111	H
				1000	J
				1001	K
				1010	L
				1011	M
				1100	N
				1101	P
				1110	Q
				1111	R
		PROG_IDL_OTP[3:0]	Report the OTP code	**0000**	**0**
				0001	1
				0010	2
				0011	3
				0100	4
				0101	5
				0110	6
				0111	7
				1000	8
				1001	9
				1010	A
				1011	B
				1100	C
				1101	D
				1110	E
				1111	F
0x1E	OTP_V1_CFG1	VSUP_UVTH_OTP	Select V_{SUP_UVH} threshold	**0**	**VSUP_UVTH low threshold selected (4.7 V)**
				1	VSUP_UVTH high threshold selected (5.7 V)
	OTP_V1_CFG1	BUCK_SRHSON_OTP[2:0]	Select BUCK slew rate when the High Side turns ON	000	HS raising slew rate is 20 ns (for 450 kHz only)
				001	HS raising slew rate is 20 ns (for 450 kHz only)
				010	HS raising slew rate is 15 ns (for 450 kHz only)
				011	**HS raising slew rate is 10 ns**
				100	HS raising slew rate is 6.3 ns
				101	HS raising slew rate is 5 ns
				110	HS raising slew rate is 3 ns
				111	HS raising slew rate is 2 ns
	OTP_V1_CFG1	BUCK_SRHSOFF_OTP[1:0]	Select BUCK slew rate when the High Side turns OFF	00	HS falling slew rate is 20 ns (for 450 kHz only)
				01	HS falling slew rate is 15 ns (for 450 kHz only)
				10	**HS falling slew rate is 10 ns**
				11	HS falling slew rate is 5 ns
	OTP_V1_CFG1	BUCK_SS_OTP[1:0]	Select V1 soft start ramp	00	Soft start is 269 µs
				01	Soft start is 538 µs
				10	**Soft start is 1077 µs**
				11	Soft start is 2150 µs

Table 149. Main OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x1F	OTP_V1_CFG2	BUCK_CLK_OTP	select BUCK switching frequency	0	Switching frequency is 450 kHz
				1	**Switching frequency is 2.25 MHz**
	OTP_V1_CFG2	BUCK_RCOMP_OTP[2:0]	Select BUCK compensation network resistor	**010**	**975 kohms**
	OTP_V1_CFG2	BUCK_CCOMP_OTP[1:0]	Select BUCK compensation network capacitor	01	23 pf
				10	33.5 pf
				11	44.5 pf
0x20	OTP_V1_CFG3	BUCK_OC_DGLT_OTP[1:0]	Select BUCK overcurrent deglitcher time	00	Overcurrent deglitcher is 250 µs
				01	Overcurrent deglitcher is 500 µs
				10	**Overcurrent deglitcher is 1000 µs**
				11	Overcurrent deglitcher is 2000 µs
		BUCK_SC_OTP[5:0]	Select BUCK slope compensation[2][3]	000111	SC = 918 mV/µs (recommended when Fsw = 450 kHz, LV1_buck = 22 µH and Vbuck = 2 – 2.5 V)
				001010	**SC = 4345 mV/µs (recommended when Fsw = 2.25 MHz, LV1_buck = 4.7 µH and Vbuck = 2 V – 2.5 V)**
				010111	SC = 3275 mV/µs (recommended when Fsw = 2.25 MHz, LV1_buck = 4.7 µH and Vbuck = 3.3 V)
				011100	SC = 2865 mV/µs (recommended when Fsw = 2.25 MHz, LV1_buck = 4.7 µH and Vbuck = 5 V)
				100101	SC = 426 mV/µs (recommended when Fsw = 450 kHz, LV1_buck = 22 µH and Vbuck = 3.3 V)
				101001	SC = 360 mV/µs (recommended when Fsw = 450 kHz, LV1_buck = 22 µH and Vbuck = 5 V
0x21	OTP_V1_CFG4	BUCK_PK_OC_PFM_OTP[2:0]	Select PFM mode high-side peak current detection threshold	010	Overcurrent (peak) detection threshold is 400 mA
				011	Overcurrent (peak) detection threshold is 500 mA
				100	Overcurrent (peak) detection threshold is 600 mA
				101	**Overcurrent (peak) detection threshold is 700 mA**
				110	Overcurrent (peak) detection threshold is 800 mA
				111	Overcurrent (peak) detection threshold is 900 mA
	OTP_V1_CFG4	BUCK_PFM_TOFF_OTP[1:0]	Select BUCK TOFF time in PFM	00	TOFF time in PFM is 130 ns at 2.2 MHz and 605 ns at 450 kHz
				01	**TOFF time in PFM is 250 ns at 2.2 MHz and 1170 ns at 450 kHz**
				10	TOFF time in PFM is 360 ns at 2.2 MHz and 1725 ns at 450 kHz
				11	TOFF time in PFM is 475 ns at 2.2 MHz and 2285 ns at 450 kHz
	OTP_V1_CFG4	BUCK_PFM_TON_OTP[1:0]	Select BUCK TON time in PFM	00	TON time in PFM is 162.5 ns at 2.2 MHz and 820 ns at 450 kHz
				01	TON time in PFM is 209 ns at 2.2 MHz and 1023 ns at 450 kHz
				10	**TON time in PFM is 257 ns at 2.2 MHz and 1221 ns at 450 kHz**
				11	TON time in PFM is 305 ns at 2.2 MHz and 1422.5 ns at 450 kHz

Table 149. Main OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x22	OTP_V1_CFG5	CONF_OV_V1_OTP	Select the device reaction in case of V1 overvoltage detection	**0**	**The V1 is disabled in case of OV**
				1	The device transition to fail-safe state (M30) in case of OV
	OTP_V1_CFG5	CONF_TSD_V1_OTP	Select the device reaction in case of V1 thermal-shutdown detection	**0**	**The V1 is disabled in case of TSD**
				1	the device transition to fail-safe state (M30) in case of TSD
	OTP_V1_CFG5	BUCK_PK_OC_PWM_OTP[2:0]	Select PWM mode High-Side peak current detection threshold	010	Overcurrent (peak) threshold is 400 mA
				011	Overcurrent (peak) threshold is 500 mA
				100	Overcurrent (peak) threshold is 600 mA
				101	Overcurrent (peak) threshold is 700 mA
				110	**Overcurrent (peak) threshold is 800 mA**
				111	Overcurrent (peak) threshold is 900 mA
	OTP_V1_CFG5	BUCK_AVG_OC_PWM_OTP[2:0]	Select PWM mode average current detection threshold	000	Average current detection threshold is 200 mA
				001	Average current detection threshold is 300 mA
				010	Average current detection threshold is 400 mA
				011	Average current detection threshold is 500 mA
				100	**Average current detection threshold is 600 mA**
				101	Average current detection threshold is 700 mA
0x24	OTP_V1_CFG7	V1UVLP_TH_OTP	Select V1UVLP threshold	**0**	**V1UVLP threshold is typical 1.8 V**
				1	V1UVLP threshold is typical 3.07 V
		VV1_BUCK_RANGE_OTP	Select V1 BUCK regulator output voltage range	0	Range = 2 for V1 from 3.3 V to 5 V
				1	**Range = 1 for V1 from 1.9 V to 3.375 V**
		VV1_BUCK_OTP[5:0]	Select V1 BUCK regulator output voltage in Normal mode	001000	V1 = 2 V with Range 1
				011100	**V1 = 2.5 V with Range 1**
				101000	V1 = 5 V with Range 2
				111100	V1 = 3.3 V with Range 1
0x25	OTP_V1_CFG8	BUCK_LP_DVS_OTP[1:0]	Select BUCK DVS ramp rate at FSW_BUCK = 2.2 MHz (values are multiplied by 2 for FSW_BUCK = 450 kHz)	00	11.25 mV/µs
				01	5.6 mV/µs
				10	**2.8 mV/µs**
				11	1.4 mV/µs
	OTP_V1_CFG8	VV1_LP_BUCK_OTP[5:0]	Select V1 BUCK regulator output voltage in LPON mode	001000	V1 = 2 V with Range 1
				011100	V1 = 2.5 V with Range 1
				101000	V1 = 5 V with Range 2
				111100	**V1 = 3.3 V with Range 1**
0x26	OTP_V3_CFG	CONF_OV_V3_OTP	Select the device reaction in case of V3 overvoltage detection	**0**	**The V3 is disabled in case of OV**
				1	the device transition to Fail-safe state (M30) in case of OV
		CONF_TSD_V3_OTP	Select the device reaction in case of V3 thermal-shutdown detection	**0**	**The V3 is disabled in case of TSD**
				1	The device transition to Fail-safe state (M30) in case of TSD
		VV3_OTP	Select V3 LDO regulator output voltage	**0**	**V3 = 3.3 V**
				1	V3 = 5.0 V
		V3_SLOT_OTP[1:0]	Select the power sequence slot for V3	**00**	**V3 starts and stops in slot 0**
				01	V3 starts and stops in slot 1
				10	V3 starts and stops in slot 2
				11	V3 does not start in a slot (enabled by SPI)

Table 149. Main OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x27	OTP_HVIO_CFG1	HVIO1PUPD_OTP[1:0]	Select the pulldown on HVIO1 pin	**00**	**HVIO1 internal pulldown and pullup are disabled**
				01	HVIO1 internal pulldown is enabled and pullup is disabled
				10	HVIO1 internal pulldown is disabled and pullup is enabled
				11	HVIO1 internal pulldown and pullup are configured as cell repeater
		WK2PUPD_OTP[1:0]	Select the pulldown on WAKE2 pin	**00**	**WAKE2 internal pulldown and pullup are disabled**
				01	WAKE2 internal pulldown is enabled and pullup is disabled
				10	WAKE2 internal pulldown is disabled and pullup is enabled
				11	WAKE2 internal pulldown and pullup are configured as cell repeater
		WK3PUPD_OTP[1:0]	Select the pulldown on WAKE3 pin	**00**	**WAKE3 internal pulldown and pullup are disabled**
				01	WAKE3 internal pulldown is enabled and pullup is disabled
				10	WAKE3 internal pulldown is disabled and pullup is enabled
				11	WAKE3 internal pulldown and pullup are configured as cell repeater
		HVIO1_SLOT_OTP[1:0]	Select the power sequence slot for HVIO1	**00**	**HVIO1 polarity is changed in slot 0**
				01	HVIO1 polarity is changed in slot 1
				10	HVIO1 polarity is changed in slot 2
				11	HVIO1 is not released in a slot (enabled by SPI)
0x28	OTP_HVIO_CFG2	HVIO1_OUT_EN_OTP	Configure the HVIO1 pin as an output	**0**	**HVIO1 is configured as an input**
				1	HVIO1 is configured as an output
		HVIO1_OUT_DFLT_OTP	Configure the HVIO1 pin default state when HVIO1 is an output	**0**	**HVIO1 default state is low (asserted)**
				1	HVIO1 default state is high (HIZ)
		HVIO1_SLOT_POL_OTP	Configure the HVIO1 polarity when activated by a slot	**0**	**HVIO1 is turned high (HIZ) on an active slot**
				1	HVIO1 is turned low (asserted) on an active slot
		HVIO1_PU_SEL_OTP	Select pull up source on HVIO1 when used as an output	**0**	**Pullup to VSUP**
				1	Pullup to VDDIO
0x29	OTP_MAIN_SYS_CFG	VBOS2V1_SW_LP_EN_OTP	Control VBOS to V1 switch in LPON mode when V1 = BUCK	**0**	**VBOS to V1 switch is open in LPON mode**
				1	VBOS to V1 switch is closed in LPON mode
		MOD_CONF_OTP	Select default clock modulation configuration (when FS24 boots up)	**0**	**Triangular modulation is selected by default**
				1	Pseudo random modulation is selected by default
		MOD_EN_OTP	Select the default state of the clock modulation on 20 MHz clock (when FS24 boots up)	**0**	**Modulation is disabled by default**
				1	Modulation is enabled by default
		SLOT_BYP_OTP	Bypass unecessary slots	**0**	**Slots are not bypassed**
				1	Bypass unnecessary slots during power-down or wake-up from LPON
		CRC_DIS_OTP	Disable SPI CRC check	**0**	**SPI CRC is enabled, SPI CRC bits on MOSI must be equal to the CRC results and are monitored by the FS24**
				1	SPI CRC is disabled, SPI CRC bits on MOSI can all be set to 0 and are not monitored by the FS24
		CRC_DBG_DIS_OTP	Disable SPI CRC check in Debug mode only	**0**	**SPI CRC is enabled in Debug mode when CRC_DIS_OTP = 1, stay disabled otherwise**
				1	SPI CRC is disabled in Debug mode
		CRC_INV_OTP	Invert the result of the polynomial calculation for SPI CRC	**0**	**SAE J-1850 = (x^8+x^4+x^3+x^2+1) XOR 0x00**
				1	CRC-8-AUTOSAR / SAE J-1850 = (x^8+x^4+x^3+x^2+1) XOR 0xFF

[1] Default values for a blank part are in bold.
[2] These codes are suggested as best fit for the described use cases. In case other values are needed, contact local support.
[3] The slope compensation values are given for a typical V1_IN at 13.5 V.

24.3 Fail-safe OTP overview

Table 150. Fail-safe OTP overview

ADDRESS	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x2A	**OTP_FS_SYS_CFG**	ERRMON_EN_OTP	—	INIT_CRC_DIS_OTP	FS_LPOFF_OTP	FS_DUR_CFG_OTP	WD_INF_OTP	RSTB8S_DIS_OTP	FIRST_FAULT_EN_OTP
0x2B	**OTP_OVUV_CFG1**	V1MON_UVTH_OTP[3:0]				V1MON_OVTH_OTP[3:0]			
0x2C	**OTP_OVUV_CFG2**	V3MON_UVTH_OTP[3:0]				V3MON_OVTH_OTP[3:0]			
0x2D	**OTP_OVUV_CFG3**	V0MON_UVTH_OTP[3:0]				V0MON_OVTH_OTP[3:0]			
0x2E	**OTP_UV_DGLT_CFG**	V0MON_UVDGLT_OTP[1:0]		V1MON_UVDGLT_OTP[1:0]		—	—	V3MON_UVDGLT_OTP[1:0]	
0x2F	**OTP_LIMP_OV_DGLT_CFG**	—	—	—	—	V0MON_OVDGLT_OTP	V1MON_OVDGLT_OTP	V1_UV_PW_EN_OTP	V3MON_OVDGLT_OTP
0x30	**OTP_RSTB_IMPACT_CFG**	V0UV_RSTB_IMPACT_OTP	V0OV_RSTB_IMPACT_OTP	V1UV_RSTB_IMPACT_OTP	V1OV_RSTB_IMPACT_OTP	—	—	V3UV_RSTB_IMPACT_OTP	V3OV_RSTB_IMPACT_OTP

24.4 Fail-safe OTP bits description

Table 151. Fail-safe OTP bits description

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x2A	OTP_FS_SYS_CFG	ERRMON_EN_OTP	Enable ERRMON functionality	**0**	**ERRMON is disabled**
				1	ERRMON is enabled
		INIT_CRC_DIS_OTP	Disable the INIT registers CRC protection	**0**	**CRC is enabled**
				1	CRC is disabled
		FS_LPOFF_OTP	Configure FS state exit	**0**	**Automatic restart after FS state**
				1	GoTo LPOFF after FS state
		FS_DUR_CFG_OTP	Configure FS state duration	**0**	**FS state duration is 100 ms**
				1	FS state duration is 4 s
		WD_INF_OTP	Disable the watchdog	**0**	**Watchdog is enabled**
				1	Watchdog is put into infinite window duration
		RSTB8S_DIS_OTP	Disable the RSTB 8 s timer	**0**	**RSTB 8 s timer is enabled**
				1	RSTB 8 s timer is disabled
		FIRST_FAULT_EN_OTP	Configure the first fault to send the device in Fail-safe mode	**0**	**Do not got to Fail-safe at first fault**
				1	Go to Fail-safe at first fault

Table 151. Fail-safe OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x2B	OTP_OVUV_CFG1	V1MON_UVTH_OTP[3:0]	Select V1MON UV threshold	**0000**	**V1MON UV = 65 %**
				0001	V1MON UV = 64.5 %
				0010	V1MON UV = 96.5 %
				0011	V1MON UV = 96 %
				0100	V1MON UV = 95.5 %
				0101	V1MON UV = 95 %
				0110	V1MON UV = 94.5 %
				0111	V1MON UV = 94 %
				1000	V1MON UV = 93.5 %
				1001	V1MON UV = 93 %
				1010	V1MON UV = 92.5 %
				1011	V1MON UV = 92 %
				1100	V1MON UV = 91.5 %
				1101	V1MON UV = 64 %
				1110	V1MON UV = 63.5 %
				1111	V1MON UV = 62 %
		V1MON_OVTH_OTP[3:0]	Select V1MON OV threshold	**0000**	**V1MON OV = 102.5 %**
				0001	V1MON OV = 103 %
				0010	V1MON OV = 103.5 %
				0011	V1MON OV = 104 %
				0100	V1MON OV = 104.5 %
				0101	V1MON OV = 105 %
				0110	V1MON OV = 105.5 %
				0111	V1MON OV = 106 %
				1000	V1MON OV = 106.5 %
				1001	V1MON OV = 107 %
				1010	V1MON OV = 107.5 %
				1011	V1MON OV = 108 %
				1100	V1MON OV = 108.5 %
				1101	V1MON OV = 109 %
				1101	V1MON OV = 109.5 %
				1111	V1MON OV = 110 %

Table 151. Fail-safe OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x2C	OTP_OVUV_CFG2	V3MON_UVTH_OTP[3:0]	Select V3MON UV threshold	**0000**	**V3MON UV = 65 %**
				0001	V3MON UV = 64.5 %
				0010	V3MON UV = 96.5 %
				0011	V3MON UV = 96 %
				0100	V3MON UV = 95.5 %
				0101	V3MON UV = 95 %
				0110	V3MON UV = 94.5 %
				0111	V3MON UV = 94 %
				1000	V3MON UV = 93.5 %
				1001	V3MON UV = 93 %
				1010	V3MON UV = 92.5 %
				1011	V3MON UV = 92 %
				1100	V3MON UV = 91.5 %
				1101	V3MON UV = 64 %
				1110	V3MON UV = 63.5 %
				1111	V3MON UV = 62 %
		V3MON_OVTH_OTP[3:0]	Select V3MON OV threshold	**0000**	**V3MON OV = 102.5 %**
				0001	V3MON OV = 103 %
				0010	V3MON OV = 103.5 %
				0011	V3MON OV = 104 %
				0100	V3MON OV = 104.5 %
				0101	V3MON OV = 105 %
				0110	V3MON OV = 105.5 %
				0111	V3MON OV = 106 %
				1000	V3MON OV = 106.5 %
				1001	V3MON OV = 107 %
				1010	V3MON OV = 107.5 %
				1011	V3MON OV = 108 %
				1100	V3MON OV = 108.5 %
				1101	V3MON OV = 109 %
				1110	V3MON OV = 109.5 %
				1111	V3MON OV = 110 %

Table 151. Fail-safe OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x2D	OTP_OVUV_CFG3	V0MON_UVTH_OTP[3:0]	Select V0MON UV threshold	**0000**	**V0MON UV = 65 %**
				0001	V0MON UV = 64.5 %
				0010	V0MON UV = 96.5 %
				0011	V0MON UV = 96 %
				0100	V0MON UV = 95.5 %
				0101	V0MON UV = 95 %
				0110	V0MON UV = 94.5 %
				0111	V0MON UV = 94 %
				1000	V0MON UV = 93.5 %
				1001	V0MON UV = 93 %
				1010	V0MON UV = 92.5 %
				1011	V0MON UV = 92 %
				1100	V0MON UV = 91.5 %
				1101	V0MON UV = 64 %
				1110	V0MON UV = 63.5 %
				1111	V0MON UV = 62 %
		V0MON_OVTH_OTP[3:0]	Select V0MON threshold	**0000**	**V0MON = 102.5 %**
				0001	V0MON = 103 %
				0010	V0MON = 103.5 %
				0011	V0MON = 104 %
				0100	V0MON = 104.5 %
				0101	V0MON = 105 %
				0110	V0MON = 105.5 %
				0111	V0MON = 106 %
				1000	V0MON = 106.5 %
				1001	V0MON = 107 %
				1010	V0MON = 107.5 %
				1011	V0MON = 108 %
				1100	V0MON = 108.5 %
				1101	V0MON = 109 %
				1110	V0MON = 109.5 %
				1111	V0MON = 110 %
0x2E	OTP_UV_DGLT_CFG	V0MON_UVDGLT_OTP[1:0]	Select V0MON UV deglitcher time (VMON_EXT)	**00**	**V0MON UV deglitcher = 5 µs**
				01	V0MON UV deglitcher = 15 µs
				10	V0MON UV deglitcher = 25 µs
				11	V0MON UV deglitcher = 40 µs
		V1MON_UVDGLT_OTP[1:0]	Select V1MON UV deglitcher time	**00**	**V1MON UV deglitcher = 5 µs**
				01	V1MON UV deglitcher = 15 µs
				10	V1MON UV deglitcher = 25 µs
				11	V1MON UV deglitcher = 40 µs
		V3MON_UVDGLT_OTP[1:0]	Select V3MON UV deglitcher time	**00**	**V3MON UV deglitcher = 5 µs**
				01	V3MON UV deglitcher = 15 µs
				10	V3MON UV deglitcher = 25 µs
				11	V3MON UV deglitcher = 40 µs

Table 151. Fail-safe OTP bits description*...continued*

Address	Register name	Bit group name	Description	Binary value[1]	Settings
0x2F	OTP_LIMP_OV_DGLT_CFG	V0MON_OVDGLT_OTP	Select V0MON OV deglitcher time (VMON_EXT)	**0**	**V0MON OV deglitcher = 25 µs**
				1	V0MON OV deglitcher = 45 µs
		V1MON_OVDGLT_OTP	Select V1MON OV deglitcher time	**0**	**V1MON OV deglitcher = 25 µs**
				1	V1MON OV deglitcher = 45 µs
		V1_UV_PW_EN_OTP	Enable V1 pre-warning monitor (Typical threshold is 4.6 V)	**0**	**Monitor disabled**
				1	Monitor enabled
		V3MON_OVDGLT_OTP	Select V3MON OV deglitcher time	**0**	**V3MON OV deglitcher = 25 µs**
				1	V3MON OV deglitcher = 45 µs
0x30	OTP_RSTB_IMPACT_CFG	V0UV_RSTB_IMPACT_OTP	Configure VMON_EXT UV impact on RSTB	**0**	**VMON_EXT UV does not assert RSTB**
				1	VMON_EXT UV asserts RSTB
		V0OV_RSTB_IMPACT_OTP	Configure VMON_EXT OV impact on RSTB	0	Default
				0	**VMON_EXT OV does not assert RSTB**
				1	VMON_EXT OV asserts RSTB
		V1UV_RSTB_IMPACT_OTP	Configure V1 UV impact on RSTB	0	Default
				0	**V1 UV does not assert RSTB**
				1	V1 UV asserts RSTB
		V1OV_RSTB_IMPACT_OTP	Configure V1 OV impact on RSTB	0	V1 OV does not assert RSTB
				1	V1 OV asserts RSTB
		V3UV_RSTB_IMPACT_OTP	Configure V3 UV impact on RSTB	**0**	**V3 UV does not assert RSTB**
				1	V3 UV asserts RSTB
		V3OV_RSTB_IMPACT_OTP	Configure V3 OV impact on RSTB	**0**	**V3 OV does not assert RSTB**
				1	V3 OV asserts RSTB

[1] Default values for a blank part are in bold.

25 Package outline

FS24 package is an HVQFN, thermally enhanced, wettable flanks, 5 x 5 x 0.85 mm, 0.5 mm pitch, 32 pins.

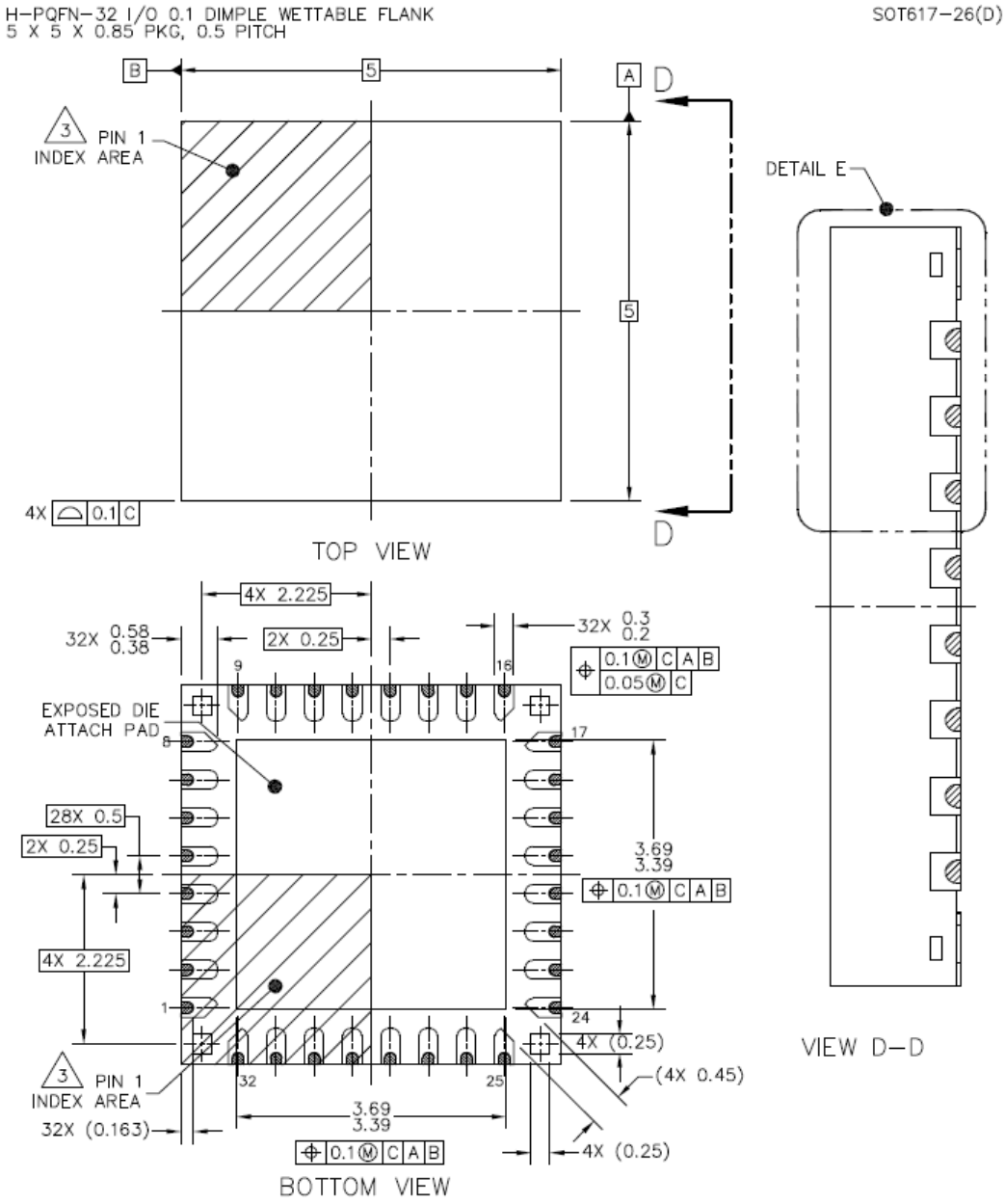


Figure 48. Top and bottom view

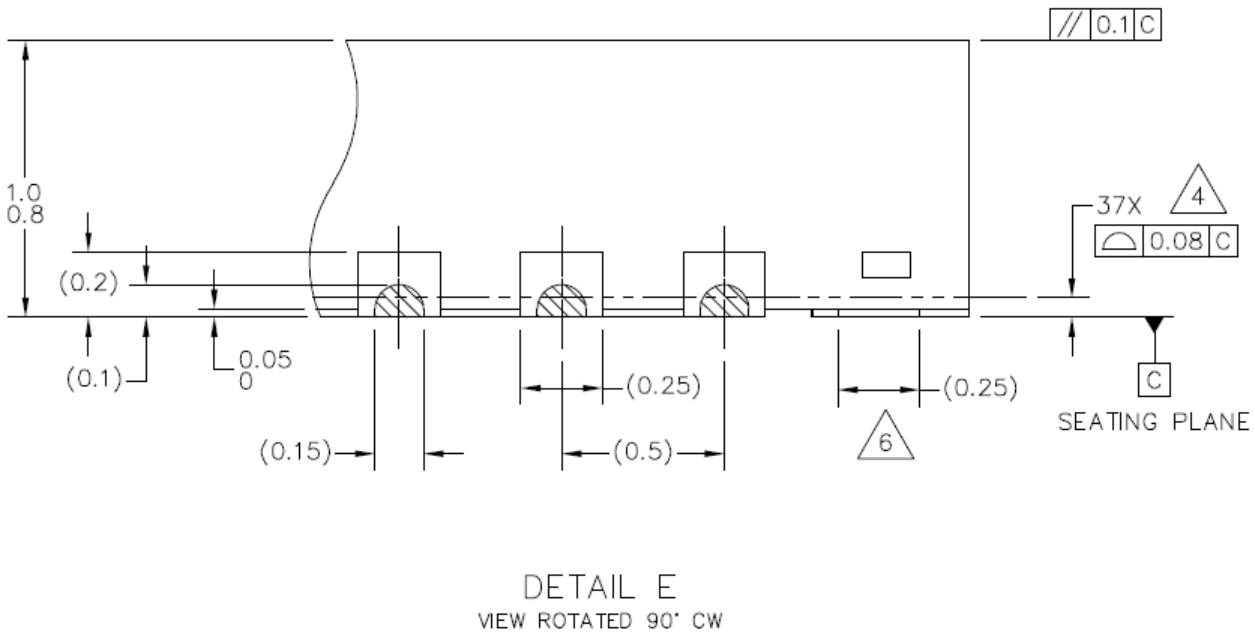


Figure 49. Detail

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

Figure 50. Notes

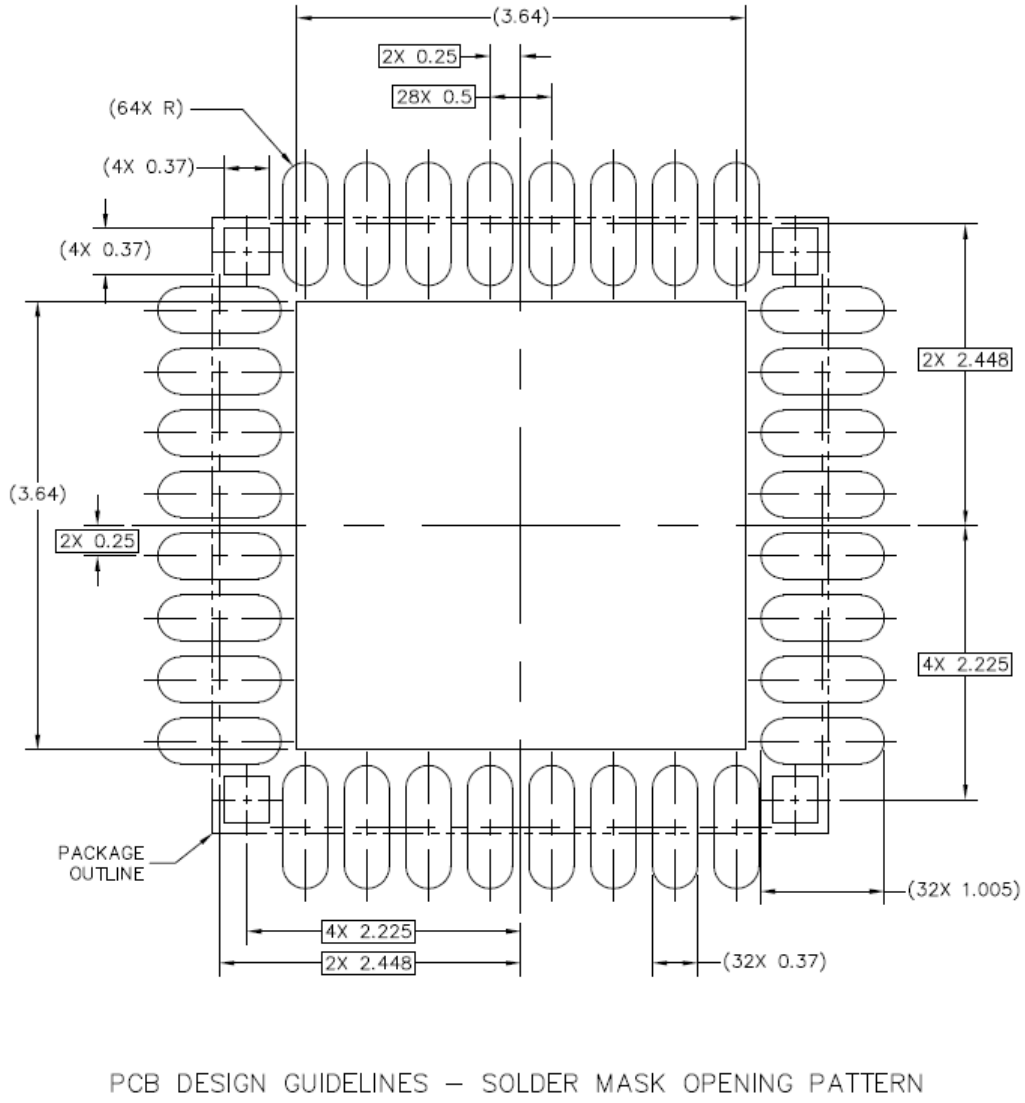


Figure 51. Solder mask opening pattern

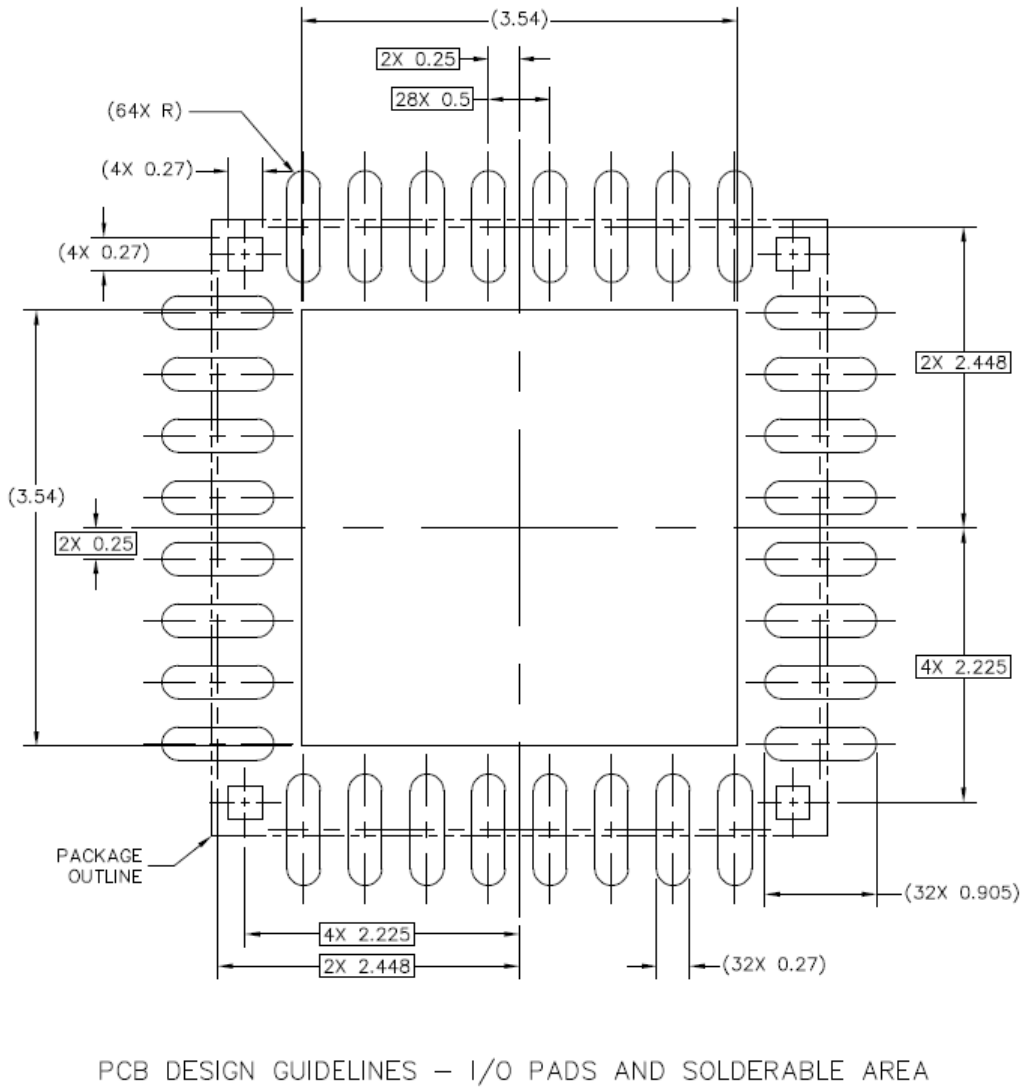


Figure 52. I/O pads solderable area

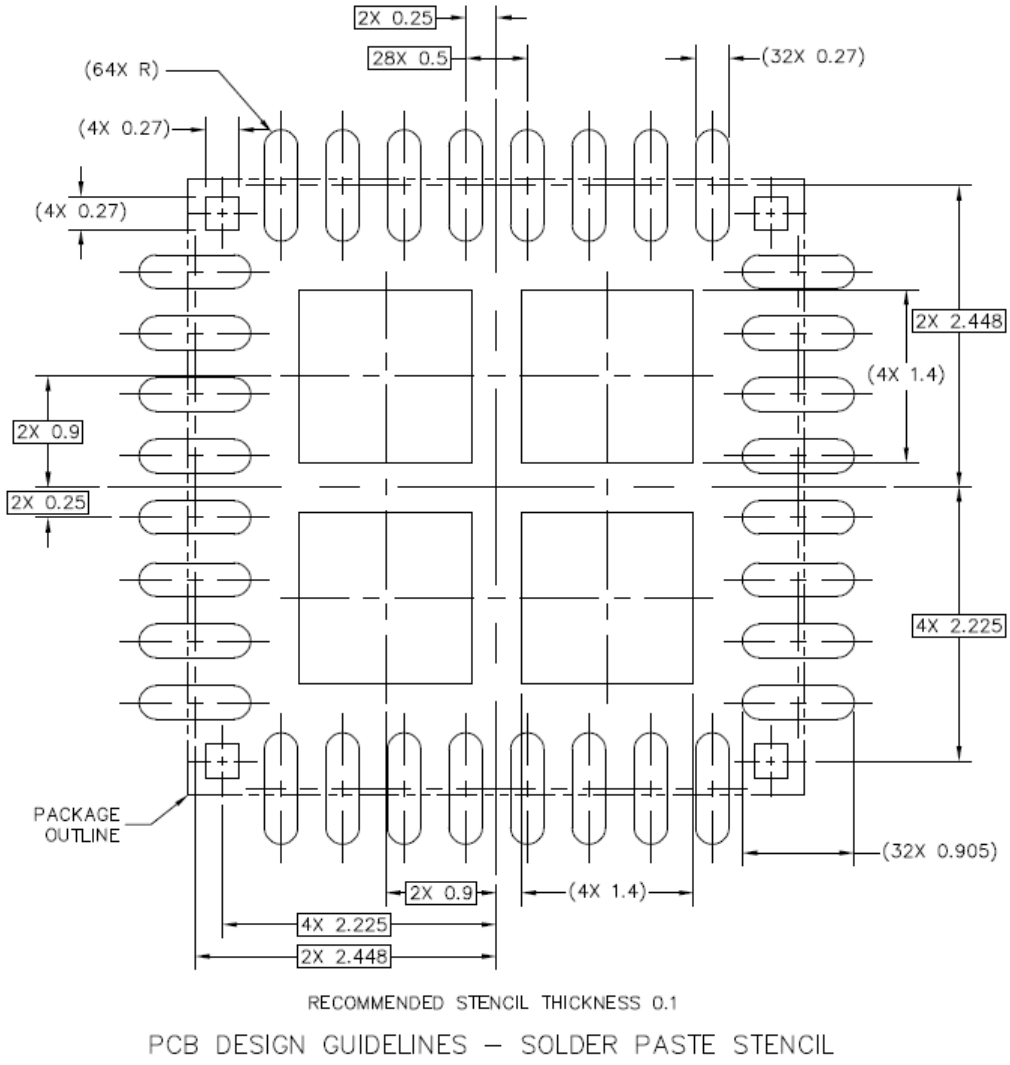


Figure 53. Solder paste stencil

26 Revision history

Table 152. Revision history

Document ID	Release date	Modifications
FS2400 v5.0	16 July 2025	• CIN # 202505018I • Product data sheet • Global: changed package name *QFN* to *HVQFN* • Global: removed or changed non-inclusive language - changed *master* to *controller* and *slave* to *device* • Section 2: updated *Power supplies* and *Configuration and enablement* sections • Section 3: removed *UWB master anchors* item • Figure 1: updated package to *HVQFN32* • Table 1: corrected *Package* column • Table 2: updated package name *HVQFN32EP* to *HVQFN32*, added part *MFS2400AVBAAES* • Table 4: added pin 33 • Section 7.1: updated *Transition to fail-safe during the power up* and *Transitions to Low-power modes* sections • Figure 8: updated • Figure 15: updated • Table 10: updated descriptions of V_{SUP_UVHL} and V_{SUP_UVHH} • Removed duplicate *Pseudo-random modulation* section, formerly 14.1.2.3, along with its figure • Section 14.1.1: updated *thermal shutdown* description • Section 19.3: updated • Table 13: updated italic table description and R_{BUCK_DIS} values, removed t_{VIOV_DGLT} parameter, corrected t_{BUCKHS_OFF} description • Figure 21: added 5 V efficiency • Figure 22: added 5 V efficiency • Figure 23: added 5 V efficiency • Section 14.2.1: updated • Table 17: updated italic table description • Figure 27: updated ECU connector information • Section 16.2.1: updated mode selection transition conditions • Table 19: added $HVIO1_{VIL}$ and $HVIO1_{VIH}$ mode selection characteristics • Section 18.1: updated • Figure 34: corrected conditions for entering *CAN_OFF* state • Section 18.1.1.2: added that the low-power wake-capable receiver is enabled during Low-power mode • Table 25: corrected description for $V_{CAN\_IN\_DIFF\_REC}$ • Section 19.3: updated • Section 19.3.5: updated • Table 35: corrected maximum value for $V0MON_{RPD}$ • Table 38: updated times • Table 44: updated LIMP0 short to high characteristics • Section 19.7: updated • Table 56: changed decimal register addresses to hex • Table 57: changed decimal register addresses to hex • Added link to Section 21 from each main register section • Added link to Table 57 from each Fail-safe register section • Table 72: corrected table title • Table 73: corrected table title and bit number of *VV1_BUCK_S* bit • Table 74: corrected the name of bit 14 • Table 85: removed description of bit 7 • Table 135: corrected *WD_TOKEN* bit description • Section 23.11: corrected typo in bit 15 name, in both tables • Table 148: added bold format to the first two columns • Table 149: corrected *CRC_DIS_OTP* settings, changed hex values to binary, added bit field length information, added bold format for defaults, added footnote explaining bold format for defaults • Table 150: added bold format to the first two columns • Table 151: changed hex values to binary, added bit field length information, added bold format for defaults, added footnote explaining bold format for defaults • Updated legal information
FS2400 v4.0	23 October 2024	• Changed classification from confidential to public • Updated legal information

Table 152. Revision history...*continued*

Document ID	Release date	Modifications
FS2400 v.3	12 January 2024	• Global editing for style and grammar. • Section 2: Under **System support**, updated text to "Four wake-up inputs (40 V capable): WAKEx pins, HVIO1 pin, CAN FD or SPI command" from "Four wake-up inputs (40 V capable): WAKEx pins, HVIO1 pin, CAN FD or SPI activity" • Updated Section 7.5: Added first paragraph • Updated Table 1 and Table 2 • Updated Table 13 – For "R_{HS_BUCK}" and "R_{LS_BUCK}", added "Typical value at Tj = 25 °C. Maximum value at Tj = 150 °C" to Description, deleted "Min" value, changed "Max" value to "350" from "330". – For $I_{OC\_PK\_PFM}$, removed "BUCK_PK_OC_PFM_OTP[2:0] = 010", "BUCK_PK_OC_PFM_OTP[2:0] = 011", and "BUCK_PK_OC_PWM_OTP[2:0] = 100" • Updated Table 21: For Interrupt "EXT_RSTB_WU", changed Mask/Enable to "EXT_RSTB_DIS" from "None" • Updated Table 73: For Bit "0 to 5", updated Description, added "Range 1 …" and "Range 2 ..." and footnote. • Updated Table 129: For Bit "14", updated Description • Updated Table 149 – For Address "0x24", Bit Group Name "VV1_BUCK_OTP" updated Settings for "0x08", "0x1C", "0x28", and "0x28", removed all others. – For Address "0x25", Bit Group Name "VV1_LP_BUCK_OTP" updated Settings for "0x08", "0x1C", "0x28", and "0x28", removed all others. – For Address "0x29", Bit Group Name "CRC_INV_OTP" updated Description. • Updated Figure 3, Figure 10
FS2400 v.2	20231207	Product data sheet
FS2400 v.1	20230614	Preliminary data sheet
FS2400 v.0.3	20230207	Preliminary data sheet
FS2400 v.0.2	20220811	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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