



Customer Information Notification

202504028I : PCA9511A Datasheet Update

Note: This notice is NXP Company
Proprietary.

Issue Date: Jul 11, 2025 **Effective Date:** Jul 14, 2025

Dear PCN EBV,

Here is your personalized communication about an NXP notification.
For detailed information we invite you to [view this notification online](#)

Management summary

NXP notification of datasheet update for PCA9511A for some applications.

Change Category

- | | | | | |
|--|--|--|--|---|
| ☐ Wafer
Fab Process | ☐ Assembly
Process | ☐ Product Marking | ☐ Test
Process | ☐ Design |
| ☐ Wafer
Fab
Materials | ☐ Assembly
Materials | ☐ Mechanical
Specification | ☐ Test
Equipment | ☐ Errata |
| ☐ Wafer
Fab
Location | ☐ Assembly
Location | ☐ Packing/Shipping/Labeling | ☐ Test
Location | ☐ Electrical
spec./Test
coverage |
| ☐ Firmware | ☒ Other: Datasheet | | | |

Notification Overview

Description

New subsection 9.1 Missing ACK event
• Description of the issue and impact
New subsection 9.1.1 Workaround
• Suggestions for workaround the issue

Reason

Datasheet update to provide technical information to deal with the ACK timing vs resistor pull-up (Rup)/Capacitance load (Cload) issue in some applications.

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality

Data Sheet Revision

A new data sheet will be issued

Additional information

Additional documents: [view online](#)

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

Name	Lilia Barrios
Position	Product marketer
e-mail address	lilia.barrios@nxp.com

At NXP Semiconductors we are constantly striving to improve our product and processes to ensure they reach the highest possible Quality Standards. Customer Focus, Passion to Win.

NXP Quality Management Team.

About NXP Semiconductors

NXP Semiconductors N.V. (NASDAQ: NXPI) provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise. These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications.

NXP Semiconductors
High Tech Campus, 5656 AG Eindhoven, The Netherlands

© 2006-2025 NXP Semiconductors. All rights reserved.

12NC	Orderable Part Number	Product Type	Product Description	Package Outline	Package Description	Product Status	Customer Specific Indicator	New 12NC	New Orderable Part Number	New Product Type	New Product Description	Product Line	Notes
935279307112	PCA9511AD.112	PCA9511AD	PCA9511A	SO8	SOT96-1	WIT	No					BLC6	
935279307118	PCA9511AD.118	PCA9511AD	PCA9511A	SO8	SOT96-1	RFS	No					BLC6	
935279308118	PCA9511ADP.118	PCA9511ADP	PCA9511A	(TJSSOP8	SOT505-1	RFS	No					BLC6	

PCA9511A

Hot Swappable I²C-bus and SMBus Bus Buffer

Rev. 5.0 — 1 July 2025

Product data sheet

Document information

Information	Content
Keywords	PCA9511A, I ² C-bus and SMBus buffer, Hot Swappable I ² C-Bus and SMBus Bus Buffer
Abstract	The PCA9511A is a hot swappable I ² C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses.



1 General description

The PCA9511A is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9511A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected (HIGH) or not (LOW).

During insertion, the PCA9511A SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

2 Features

- Bidirectional buffer for SDA and SCL lines increases fan out and prevents SDA and SCL corruption during live board insertion and removal from multipoint backplane systems
- Compatible with I²C-bus Standard-mode, I²C-bus Fast-mode, and SMBus standards
- Built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines (0.6 V threshold) require the bus pull-up voltage and supply voltage (V_{CC}) to be the same
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for $V_{CC} = 0$ V
- 1 V precharge on all SDA and SCL lines
- Supporting clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

3 Applications

The application supports insertion and removal of cPCI, VME, AdvancedTCA cards, and other multipoint backplane cards from an operating system.

4 Feature selection

[Table 1](#) describes the features summary of the PCA95XXA device family.

Table 1. Feature selection chart

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
Idle detect	yes	yes	yes	yes	yes
High-impedance SDA, SCL pins for $V_{CC} = 0$ V	yes	yes	yes	yes	yes
Rise time accelerator circuitry on SDA _n and SCL _n lines	-	yes	yes	yes	yes

Table 1. Feature selection chart...continued

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	yes	-	-
Rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin	-	-	-	yes	yes
Ready open-drain output	yes	yes	-	yes	yes
Two V _{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	-	-	yes	-	-
1 V precharge on all SDA and SCL lines	in only	yes	yes	-	-
92 μ A current source on SCLIN and SDAIN for PICMG applications	-	-	-	yes	-

5 Ordering information

Table 2. Ordering information

 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Type number	Topside mark	Package		
		Name	Description	Version
PCA9511AD	PA9511A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9511ADP	9511A	TSSOP8 ^[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

- Also known as 'MSOP8'.

6 Block diagram

[Figure 1](#) shows the block diagram of PCA9511A.

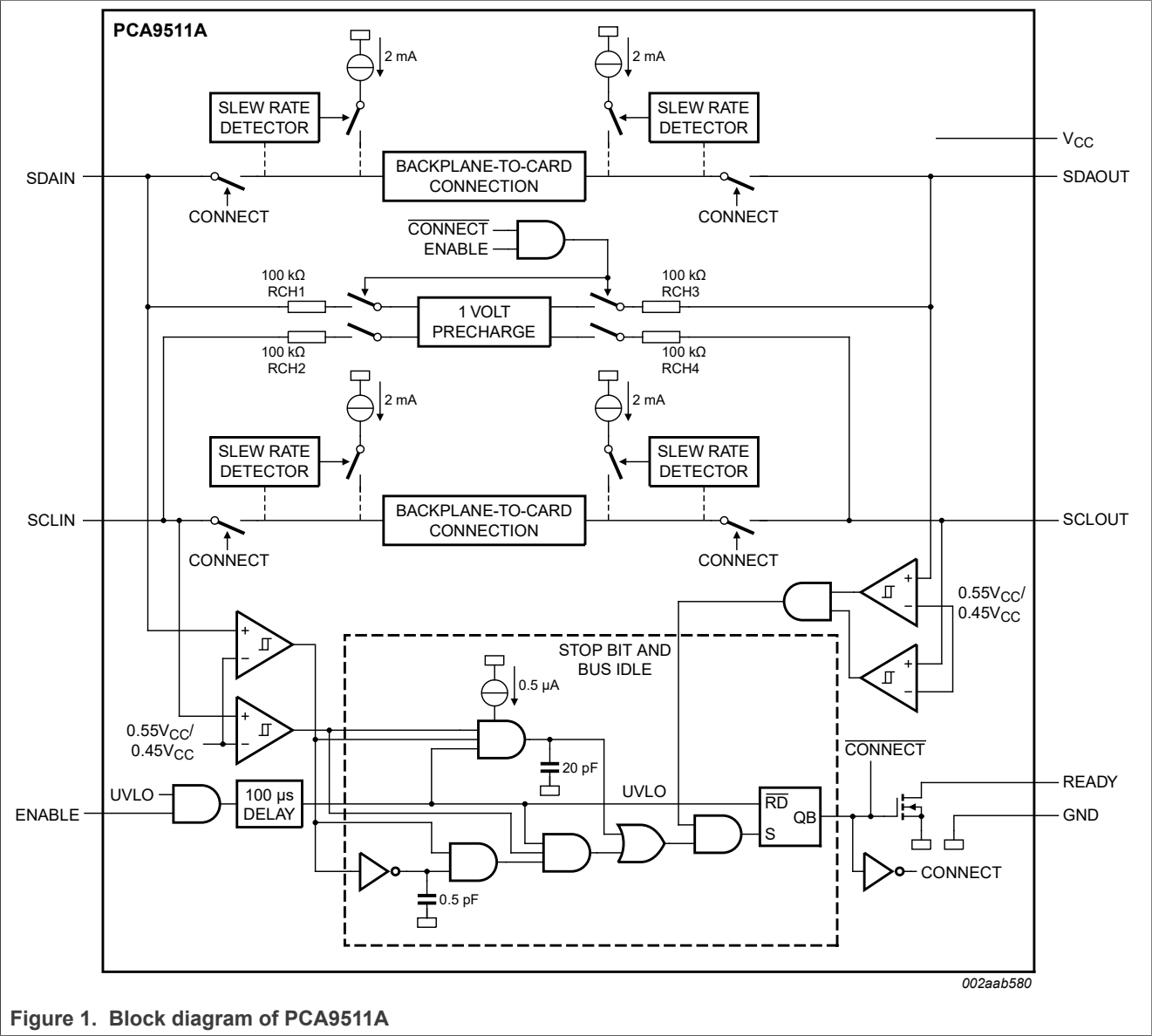


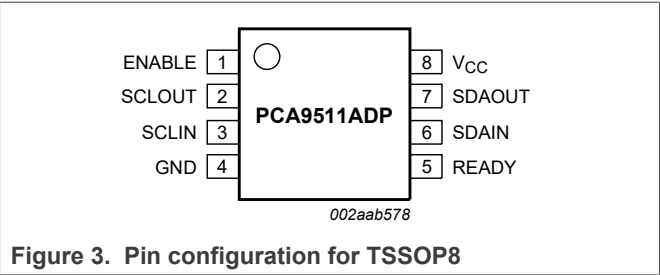
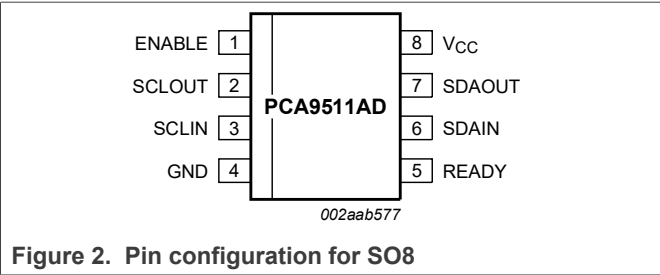
Figure 1. Block diagram of PCA9511A

7 Pinning information

This section provides the pin configuration and pin description of SO8 and TSSOP8 packages.

7.1 Pinning

This section provides the pin configuration detail of SO8 and TSSOP8.



7.2 Pin description

Table 3 provides the pin descriptions for SO8 and TSSOP8 packages of PCA9511.

Table 3. Pin description

Symbol	Pin	Description
ENABLE	1	Chip enable. Grounding this input puts the part in a low current (< 1 μ A) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
SCLOUT	2	Serial clock output to and from the SCL bus on the card.
SCLIN	3	Serial clock input to and from the SCL bus on the backplane.
GND	4	Ground. Connect this pin to a ground plane for best results.
READY	5	Open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected.
SDAIN	6	Serial data input to and from the SDA bus on the backplane.
SDAOUT	7	Serial data output to and from the SDA bus on the card.
V _{CC}	8	Power supply.

8 Functional description

Refer to Figure 1.

8.1 Start-up

An undervoltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the I_{CC} is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH, it enters an initialization state where the internal references are stabilized and the precharge circuit is enabled. At the end of the initialization state the ‘Stop Bit And Bus Idle’ detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state (t_{en}) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 k Ω nominal resistors. This mechanism minimizes the disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

8.2 Connect circuitry

Once the connection circuitry activates, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical. Each pair acts as a bidirectional buffer. These buffers isolate the input capacitance from

the output bus capacitance while maintains the logic levels communication. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. Also, the same is true for the SCL pins. Noise between $0.7 V_{CC}$ and V_{CC} is ignored because a falling edge is only recognized when it falls below $0.7 V_{CC}$ with a slew rate of at least $1.25 V/\mu s$. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver pulls the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below $0.7 V_{CC}$. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate continues. If the first falling pin has a slow slew rate, then the second pin is pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW, they remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin rises up and settles out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least $1.25 V/\mu s$, when the pin voltage exceeds 0.6 V for the PCA9511A, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

8.3 Maximum number of devices in series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. The maximum offset (V_{offset}) is 0.150 V with a 10 k Ω pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is that the I²C-bus specification of 3 mA produces $V_{OL} < 0.4 V$, although if lightly loaded the V_{OL} may be $\sim 0.1 V$. Assuming $V_{OL} = 0.1 V$ and $V_{offset} = 0.1 V$, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line result in firing the rising edge accelerator, introducing false clock edges. It is recommended to limit the number of buffers in a series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns off the pull-down. If the V_{IL} is above $\sim 0.6 V$ and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected.

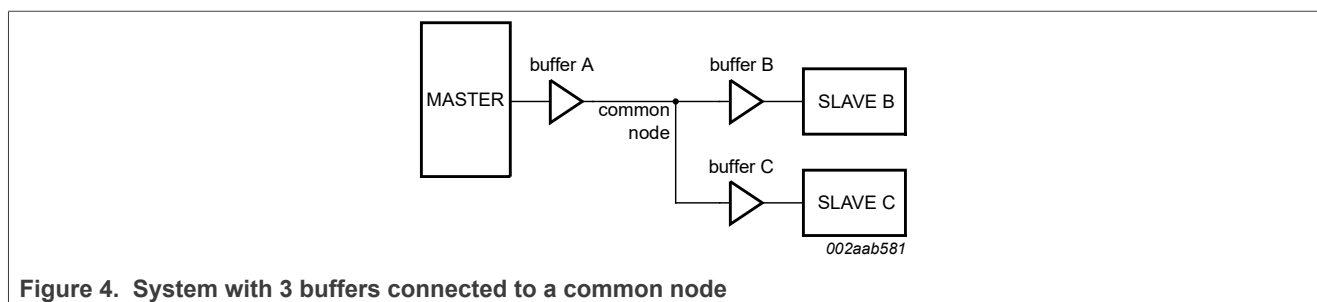


Figure 4. System with 3 buffers connected to a common node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 4. Consider if the V_{OL} at the input of buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of buffer A of 0.3 V and its output, the common node, is $\sim 0.4 V$. The output of buffer B and buffer C would be $\sim 0.5 V$, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is $\sim 0.5 V$. When the Master pull-down turns off, the input of buffer A rises and so does its output,

the common node, because it is the only part driving the node. The common node rises to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V, the accelerators on both buffer A and buffer C fire, contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while, the rising edge accelerators turn off, and the common node returns to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes then falls to ~0.6 V until Slave B is turned off. This does not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurs before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

8.4 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} is negative if the output capacitance is less than the input capacitance and is positive if the output capacitance is greater than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$, and the output turn-on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, V_{CC} and process, as well as the load current and the load capacitance.

8.5 Rise time accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9511A is exceeded. The rising edge rate should be at least 1.25 V/ μ s to guarantee the turn-on of the accelerators. The built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines require the bus pull-up voltage and supply voltage (V_{CC}) to be the same.

8.6 READY digital output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 k Ω to the V_{CC} to provide the pull-up.

8.7 ENABLE low current disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to V_{CC} , the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

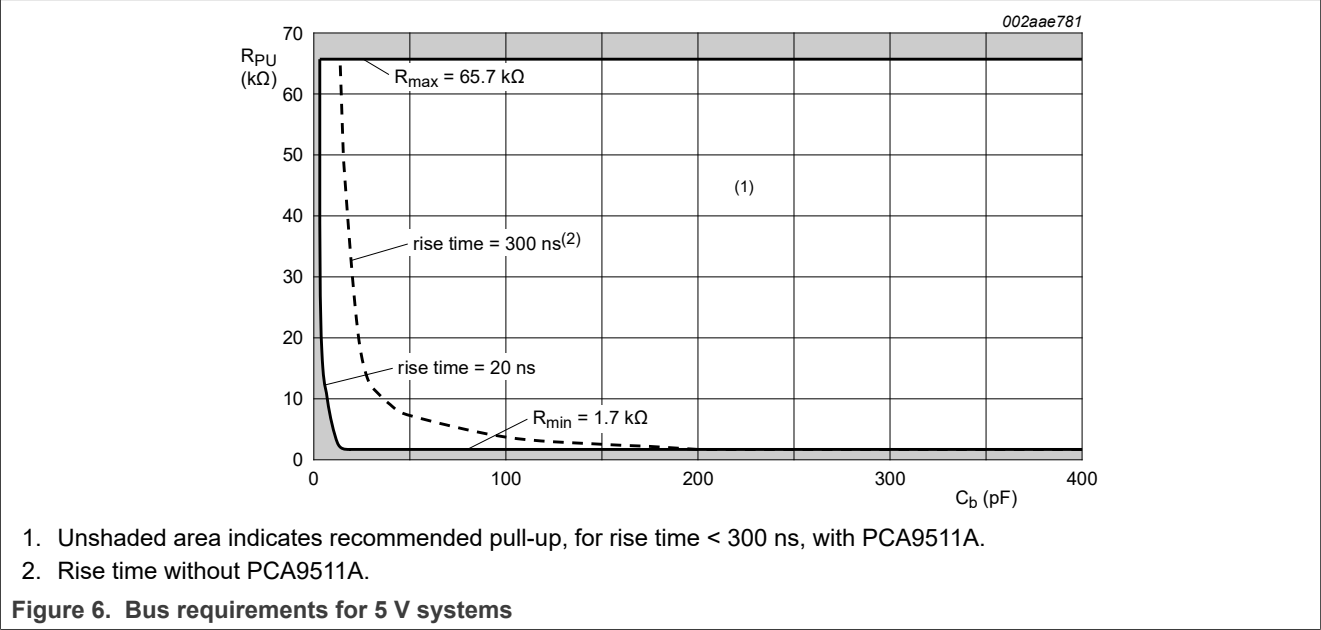
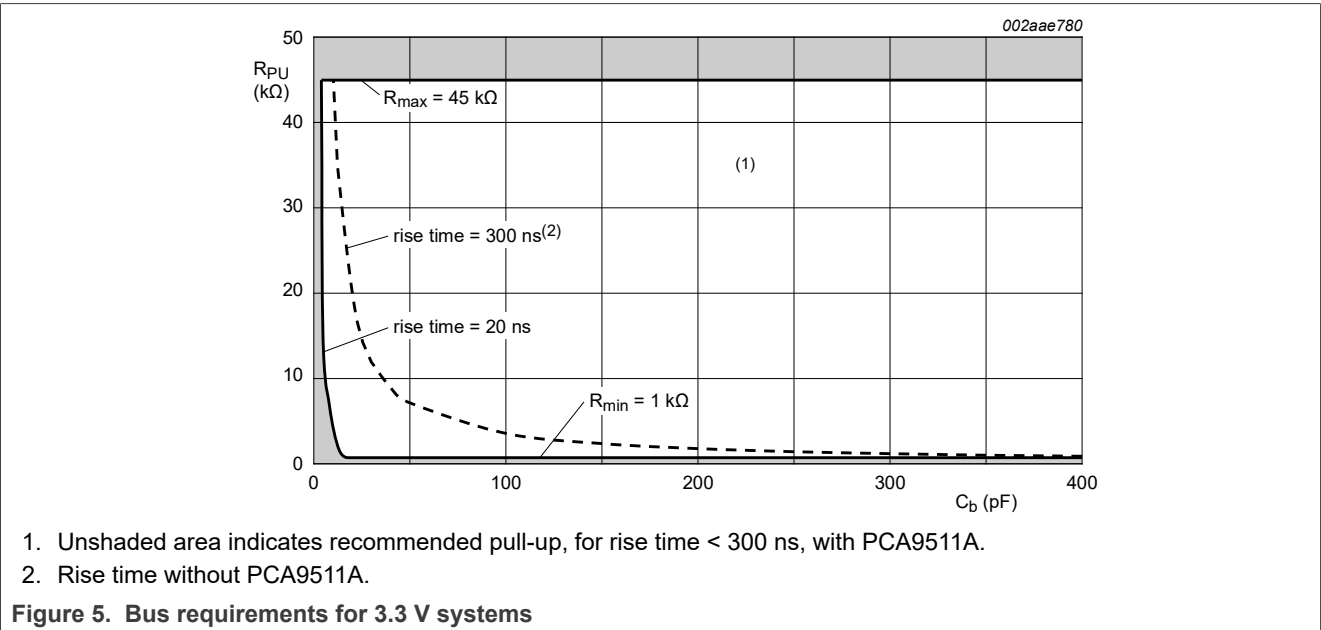
8.8 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/ μ s on the SDA and SCL pins, to activate the boost pull-up currents during rising edges. Choose the maximum resistor value using the formula given in [Equation 1](#):

$$R \leq 800 \times 10^3 \left(\frac{V_{CC(min)}^{-0.6}}{C} \right) \quad (1)$$

Where R is the pull-up resistor value in Ω, V_{CC(min)} is the minimum V_{CC} voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

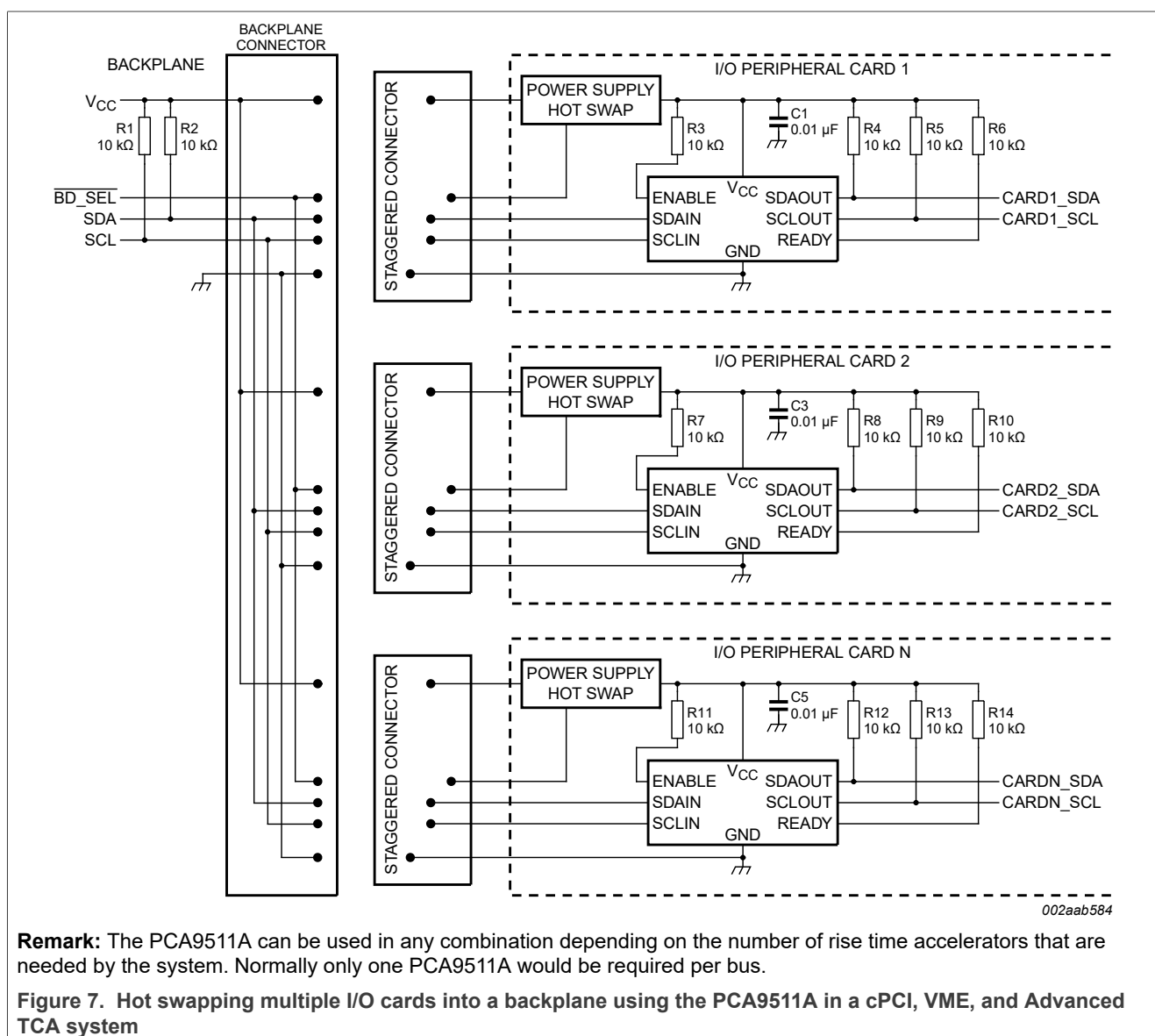
Also, regardless of the bus capacitance, always choose R ≤ 65.7 kΩ for V_{CC} = 5.5 V maximum, R ≤ 45 kΩ for V_{CC} = 3.6 V maximum. The startup circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card. These pull-up values are needed to overcome the precharge voltage. See the curves in [Figure 5](#) and [Figure 6](#) for guidance in resistor pull-up selection.

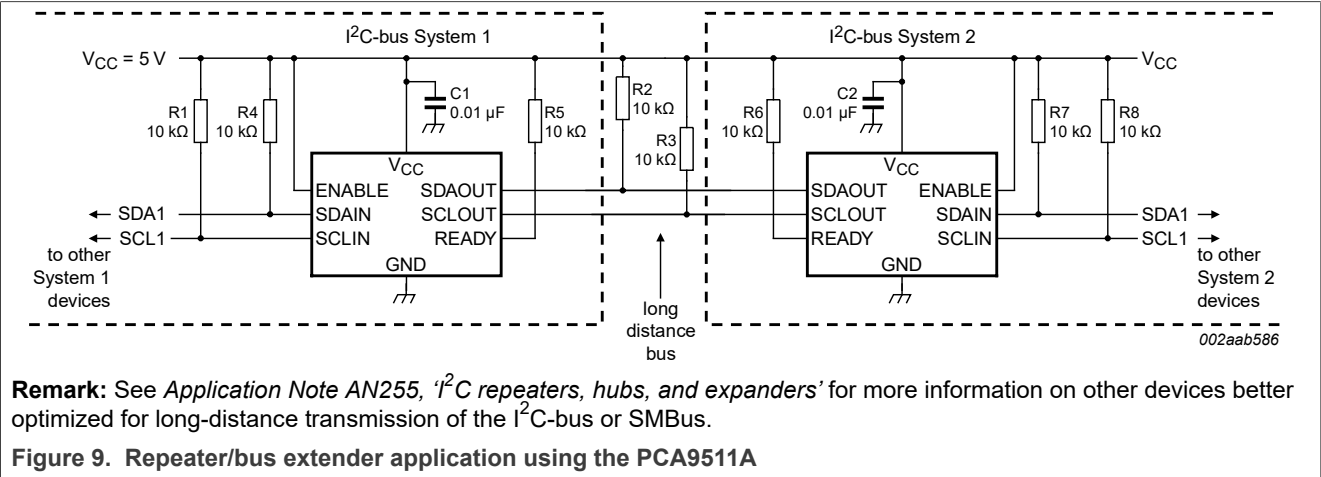
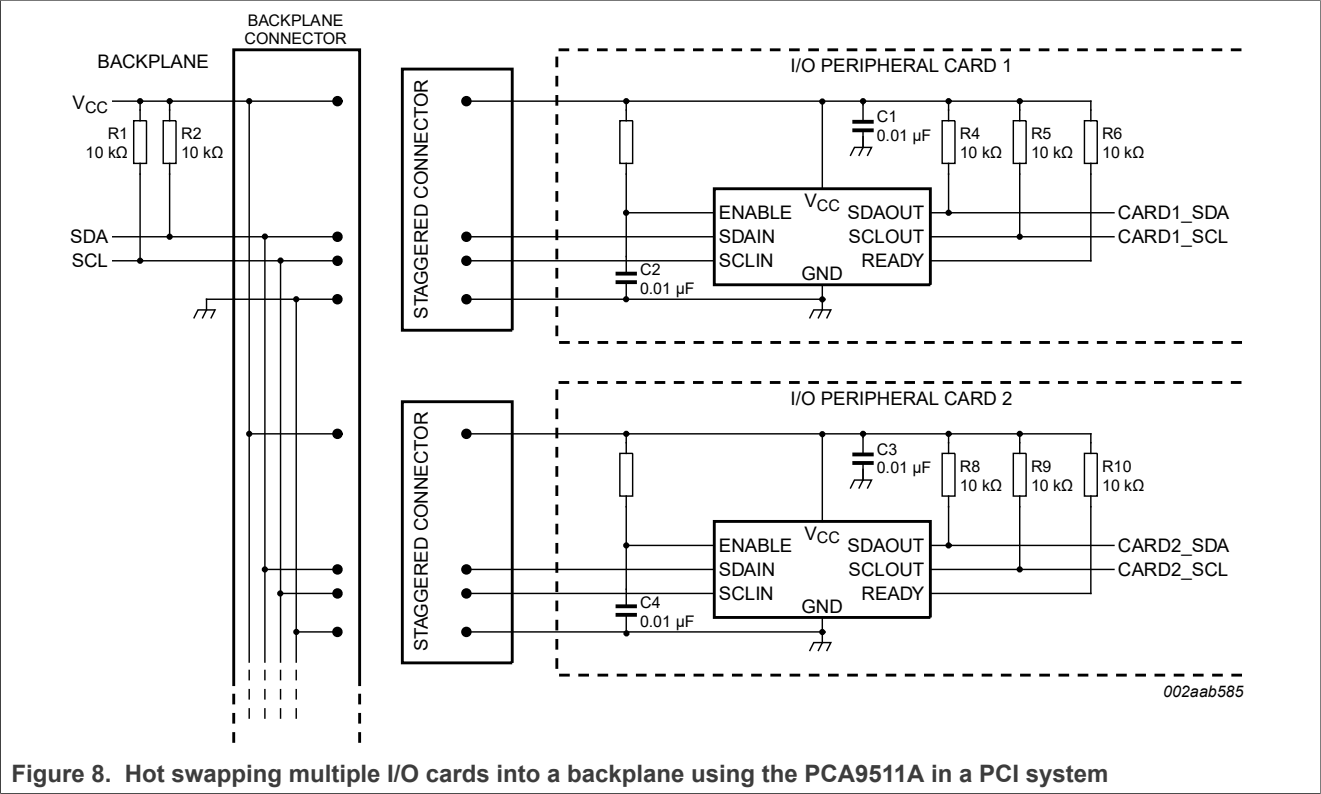


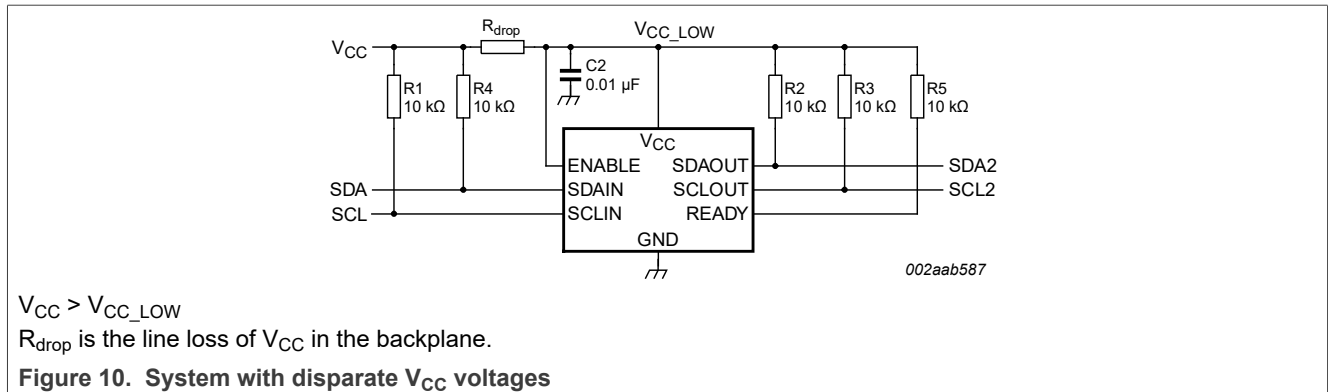
8.9 Hot swapping and capacitance buffering application

Figure 7 through Figure 10 illustrate the usage of the PCA9511A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, if the I/O cards are plugged directly into the backplane, all of the backplane and card capacitances add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note AN10160, 'Hot Swap Bus Buffer' for more information on applications and technical assistance.

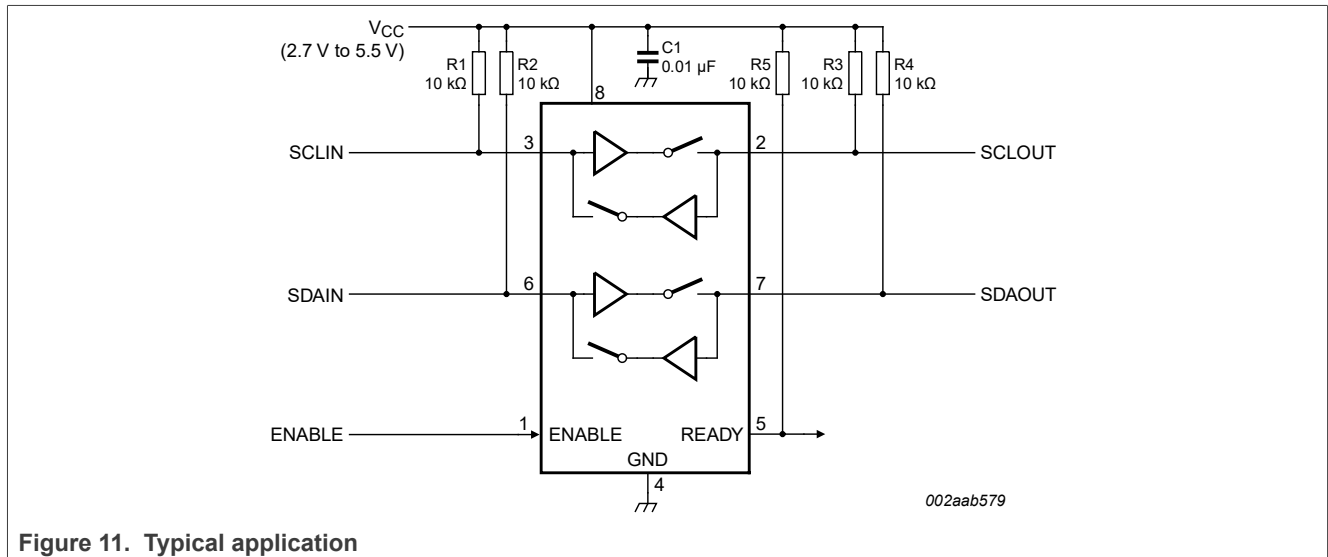






9 Application design-in information

[Figure 11](#) shows the typical application design-in information.



9.1 Missing ACK event

When the target device sends an ACK bit, a logic low on SDA during the ninth clock cycle, with VOL on the bus close to 600 mV, produces a high state on the output port. The rise time accelerators are engaged when the voltage is above 600 mV and the slew rate is above 1.25 V/µs (as described in [Section 8.5](#)). In [Figure 12](#), SDAIN is a target attempting to send an ACK bit. SDAIN pulls to a logic low, but the ACK is not transferred to the other side and SDAOUT remains high unexpectedly. The ACK bit is not transferred through the PCA9511; target and the controller interpret the results as NACK.

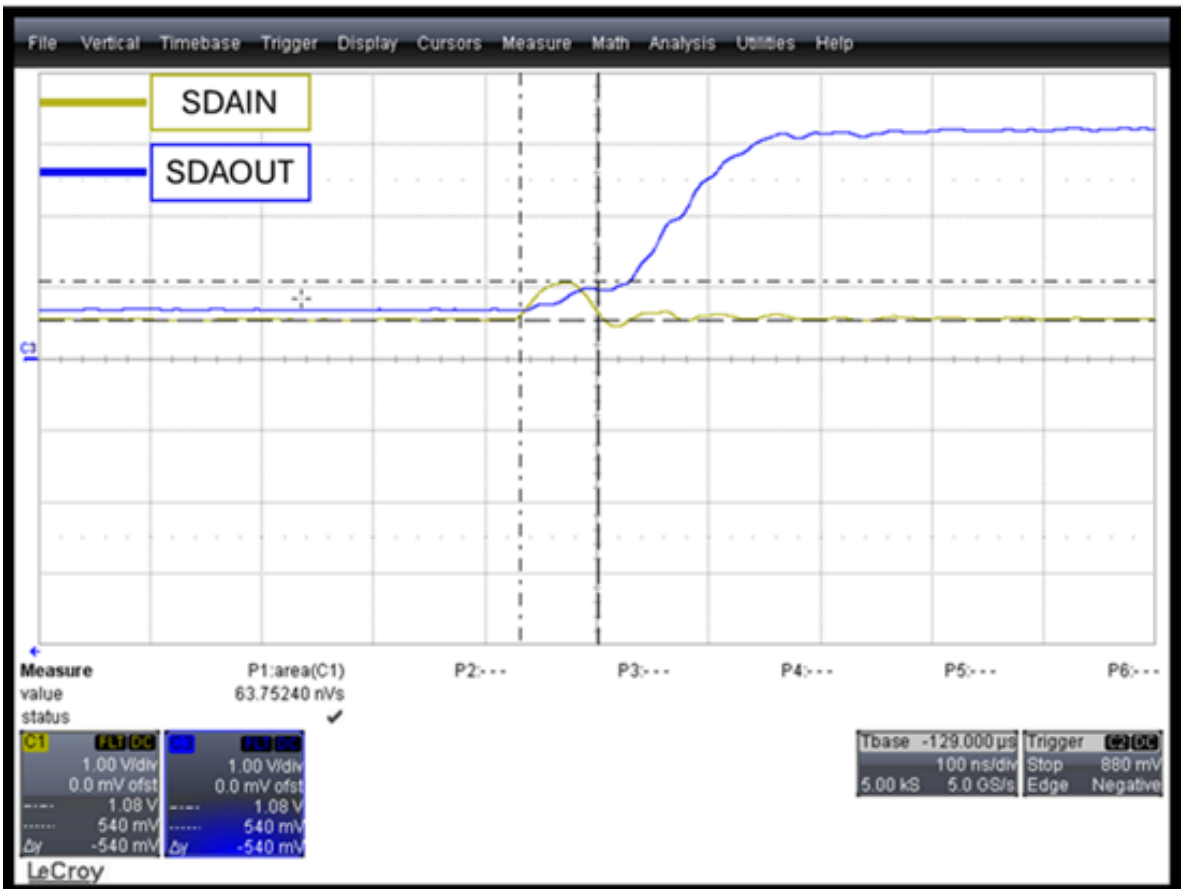


Figure 12. Missing ACK

9.1.1 Workaround

The above-mentioned issue can be mitigated by reducing the glitch magnitude such that it is below 600 mV. One way to accomplish this is by increasing the value of the pull-up resistors on the I2C-bus. Care must be taken to follow the pull-up resistor sizing rules outlined in [Section 8.8](#).

10 Limiting values

[Table 4](#) describes the limiting values In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 4. Limiting values

Symbol	Parameter	Conditions	Note	Min	Max	Unit
V _{CC}	Supply voltage		[1]	-0.5	+7	V
V _n	Voltage on SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE		[1]	-0.5	+7	V
T _{oper}	Operating temperature			-40	+85	°C
T _{stg}	Storage temperature			-65	+150	°C
T _{sp}	Solder point temperature	10 s max.		-	+300	°C
T _{j(max)}	Maximum junction temperature			-	+125	°C

1. Voltages with respect to pin GND.

11 Characteristics

[Table 5](#) describes the electrical characteristics of PCA9511A.

Table 5. Characteristics

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
Power supply							
V_{CC}	Supply voltage		[1]	2.7	-	5.5	V
I_{CC}	Supply current	$V_{CC} = 5.5\text{ V}$; $V_{SDAIN} = V_{SCLIN} = 0\text{ V}$	[1]	-	3.5	6	mA
$I_{CC(sd)}$	Shut-down mode supply current	$V_{ENABLE} = 0\text{ V}$; all other pins at V_{CC} or GND		-	0.1	-	μA
Start-up circuitry							
V_{pch}	Precharge voltage	SDA, SCL floating	[1]	0.8	1.1	1.2	V
$V_{IH(ENABLE)}$	HIGH-level input voltage on pin ENABLE			-	$0.5 \times V_{CC}$	$0.7 \times V_{CC}$	V
$V_{IL(ENABLE)}$	LOW-level input voltage on pin ENABLE			$0.3 \times V_{CC}$	$0.5 \times V_{CC}$	-	V
$I_{I(ENABLE)}$	Input current on pin ENABLE	$V_{ENABLE} = 0\text{ V to }V_{CC}$		-	± 0.1	± 1	μA
t_{en}	Enable time		[2]	-	110	-	μs
$t_{idle(READY)}$	Bus idle time to READY active		[1]	50	105	200	μs
$t_{dis(EN-RDY)}$	Disable time (ENABLE to READY)			-	30	-	ns
$t_{stp(READY)}$	SDAIN to READY delay after STOP		[3]	-	1.2	-	μs
t_{READY}	SCLOUT/SDAOUT to READY delay		[3]	-	0.8	-	μs
$I_{LZ(READY)}$	Off-state leakage current on pin READY	$V_{ENABLE} = V_{CC}$		-	± 0.3	-	μA
$C_{i(ENABLE)}$	Input capacitance on pin ENABLE	$V_I = V_{CC}$ or GND	[4]	-	1.9	4.0	pF
$C_{o(READY)}$	Output capacitance on pin READY	$V_I = V_{CC}$ or GND	[4]	-	2.5	4.0	pF
$V_{OL(READY)}$	LOW-level output voltage on pin READY	$I_{pu} = 3\text{ mA}$; $V_{ENABLE} = V_{CC}$	[1]	-	-	0.4	V
Rise time accelerators							
$I_{trt(pu)}$	Transient boosted pull-up current	positive transition on SDA, SCL; $V_{CC} = 2.7\text{ V}$; slew rate = $1.25\text{ V}/\mu\text{s}$	[5][6]	1	2	-	mA
Input-output connection							

Table 5. Characteristics...continued

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
V_{offset}	Offset voltage	10 k Ω to V_{CC} on SDA, SCL; $V_{CC} = 3.3\text{ V}$	[1][7][9]	0	110	175	mV
t_{PLH}	LOW to HIGH propagation delay	SCL to SCL and SDA to SDA; 10 k Ω to V_{CC} ; $C_L = 100\text{ pF}$ each side		-	0	-	ns
t_{PHL}	HIGH to LOW propagation delay	SCL to SCL and SDA to SDA; 10 k Ω to V_{CC} ; $C_L = 100\text{ pF}$ each side		-	70	-	ns
$C_{i(SCL/SDA)}$	SCL and SDA input capacitance		[4]	-	5	7	pF
V_{OL}	LOW-level output voltage	$V_I = 0\text{ V}$; SDA _n , SCL _n pins; $I_{sink} = 3\text{ mA}$; $V_{CC} = 2.7\text{ V}$	[1]	0	-	0.4	V
I_{LI}	Input leakage current	SDA _n , SCL _n pins; $V_{CC} = 5.5\text{ V}$		-1	-	+1	μA
System characteristics							
f_{SCL}	SCL clock frequency		[4]	0	-	400	kHz
t_{BUF}	Bus free time between a STOP and START condition		[4]	1.3	-	-	μs
$t_{HD,STA}$	Hold time (repeated) START condition		[4]	0.6	-	-	μs
$t_{SU,STA}$	Set-up time for a repeated START condition		[4]	0.6	-	-	μs
$t_{SU,STO}$	Set-up time for STOP condition		[4]	0.6	-	-	μs
$t_{HD,DAT}$	Data hold time		[4]	300	-	-	ns
$t_{SU,DAT}$	Data set-up time		[4]	100	-	-	ns
t_{LOW}	LOW period of the SCL clock		[4]	1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		[4]	0.6	-	-	μs
t_f	Fall time of both SDA and SCL signals		[4][8]	$20 + 0.1 \times C_b$	-	300	ns
t_r	Rise time of both SDA and SCL signals		[4][8]	$20 + 0.1 \times C_b$	-	300	ns

1. This specification applies over the full operating temperature range.
2. The enable time can slow considerably for some parts when temperature is $< -20\text{ °C}$.
3. Delays that can occur after ENABLE and/or idle times have passed.
4. Guaranteed by design, not production tested.
5. $I_{trt(pu)}$ varies with temperature and V_{CC} voltage, as shown in [Section 11.1](#).
6. Input pull-up voltage should not exceed power supply voltage in operating mode because the rise time accelerator clamps the voltage to the positive supply rail.

- 7. The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in [Section 11.1](#).
- 8. C_b = total capacitance of one bus line in pF.
- 9. Force V_{SDAIN} = V_{SCLIN} = 0.1 V, tie SDAOUT and SCLOUT through 10 kΩ resistor to V_{CC} and measure the SDAOUT and SCLOUT output.

11.1 Typical performance characteristics

This section provides the performance characteristics of PCA9511A.

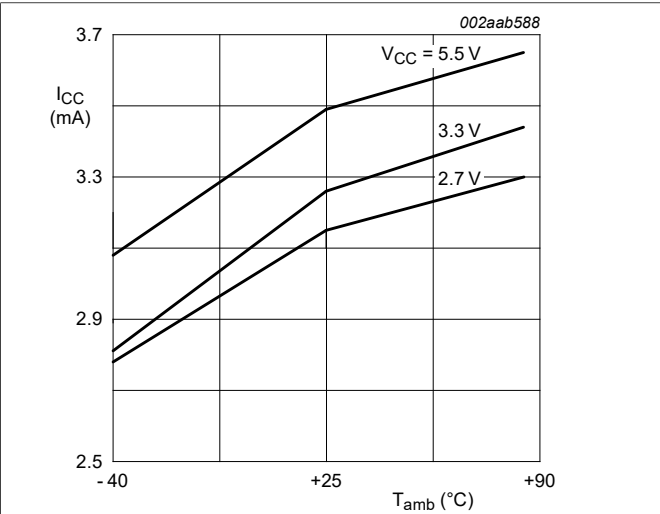


Figure 13. I_{CC} versus temperature

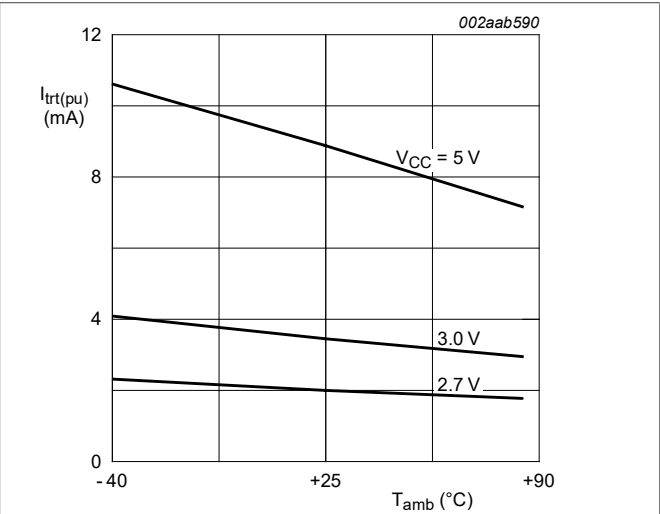
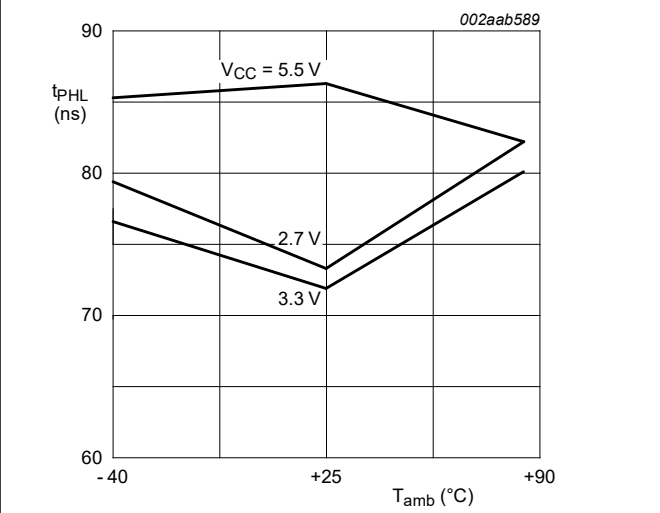


Figure 14. I_{trt(pu)} versus temperature



C_i = C_o > 100 pF; R_{PU(in)} = R_{PU(out)} = 10 kΩ
Figure 15. Input/output t_{PHL} versus temperature

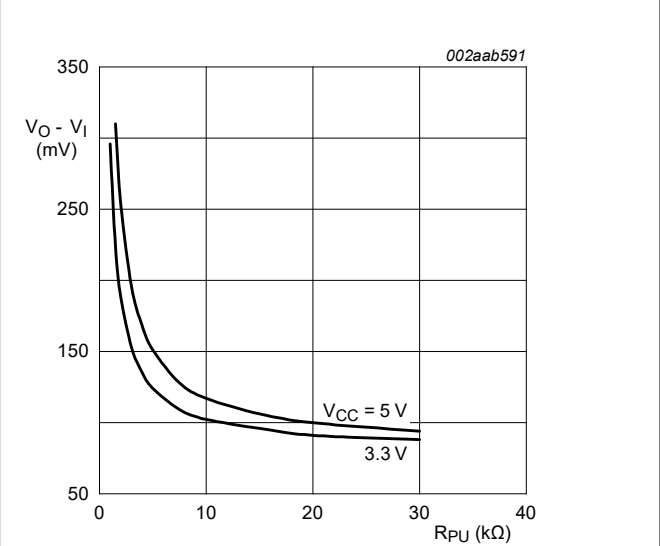
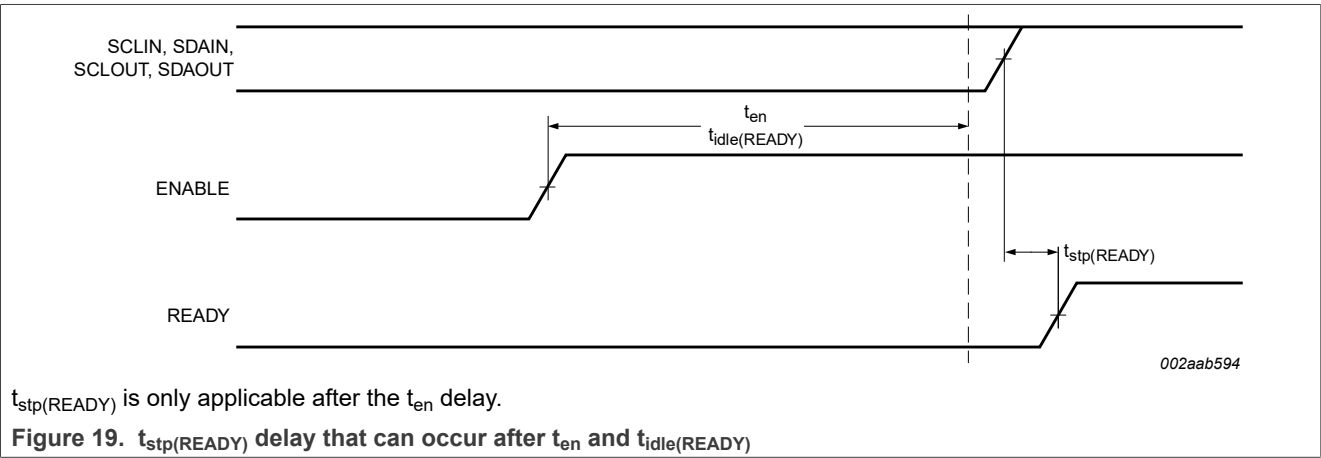
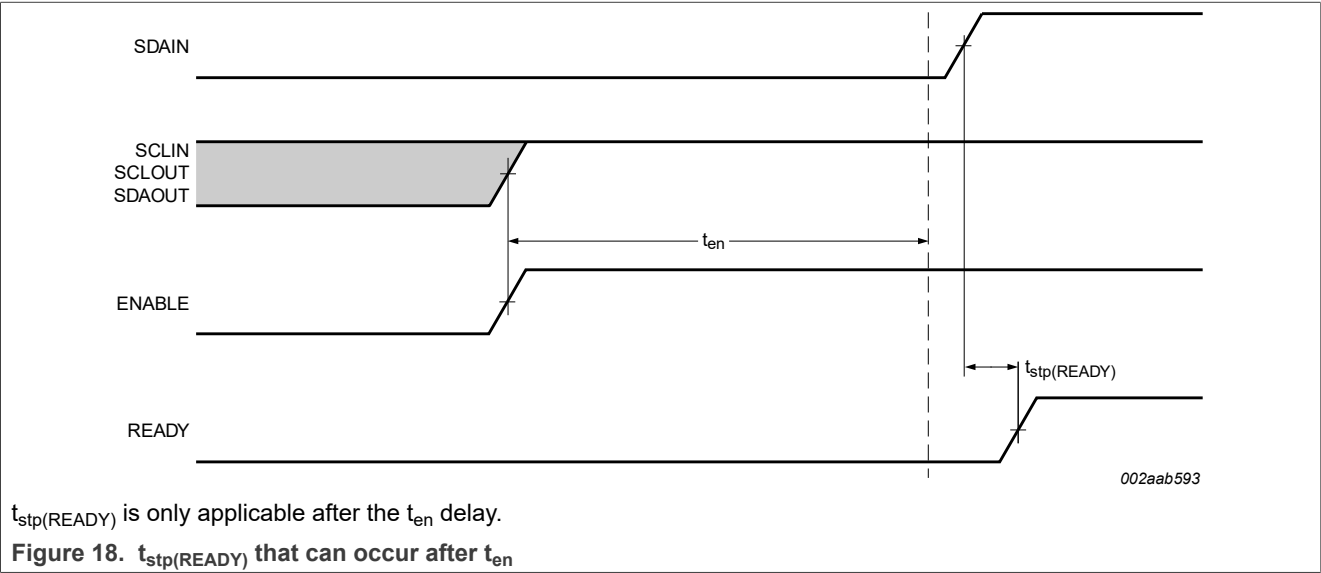
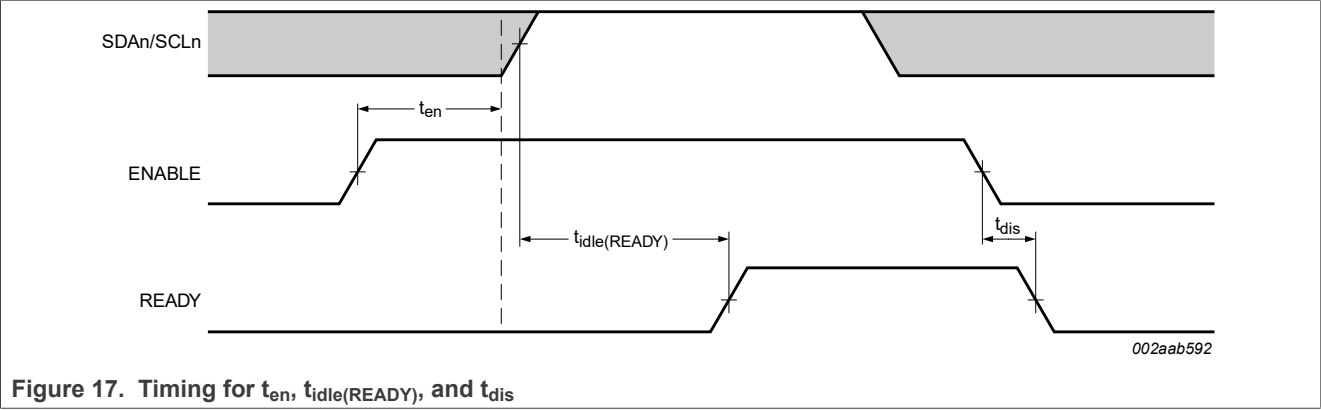


Figure 16. Connection circuitry V_O - V_I

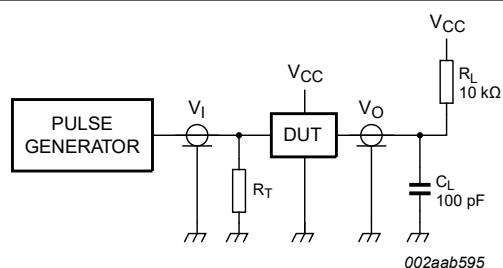
11.2 Timing diagrams

This section provides detailed timing diagrams.



12 Test information

Figure 20 shows the test circuitary diagram.



R_L = load resistor

C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generators.

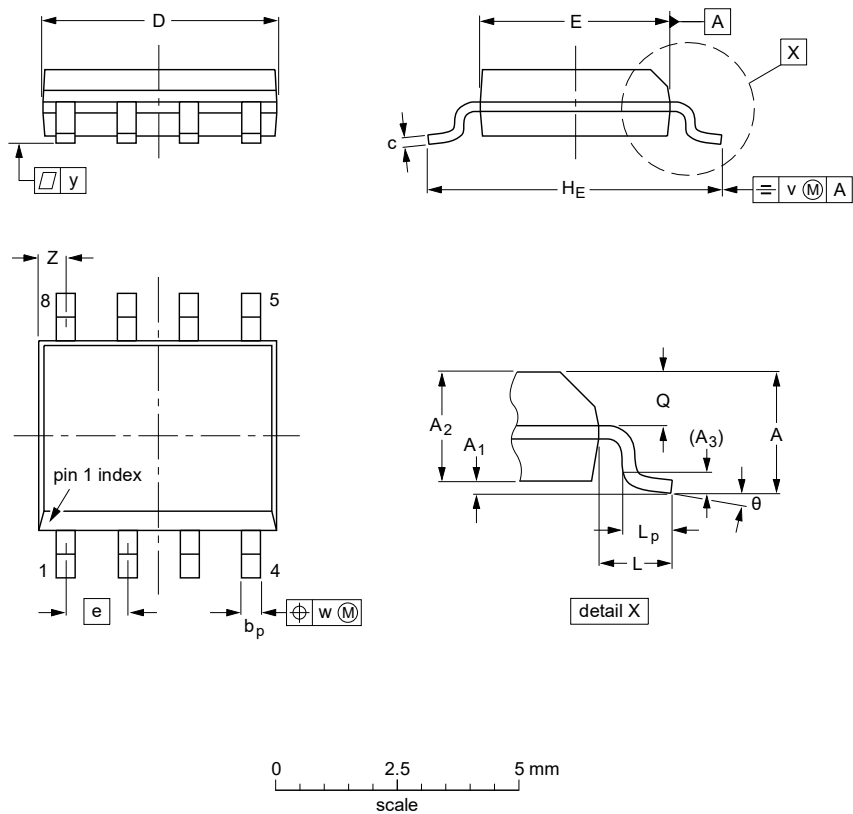
Figure 20. Test circuitry for switching times

13 Package outline

This section provides the package outline for SOT96-1 (SO8) and SOT505-1 (TSSOP8).

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

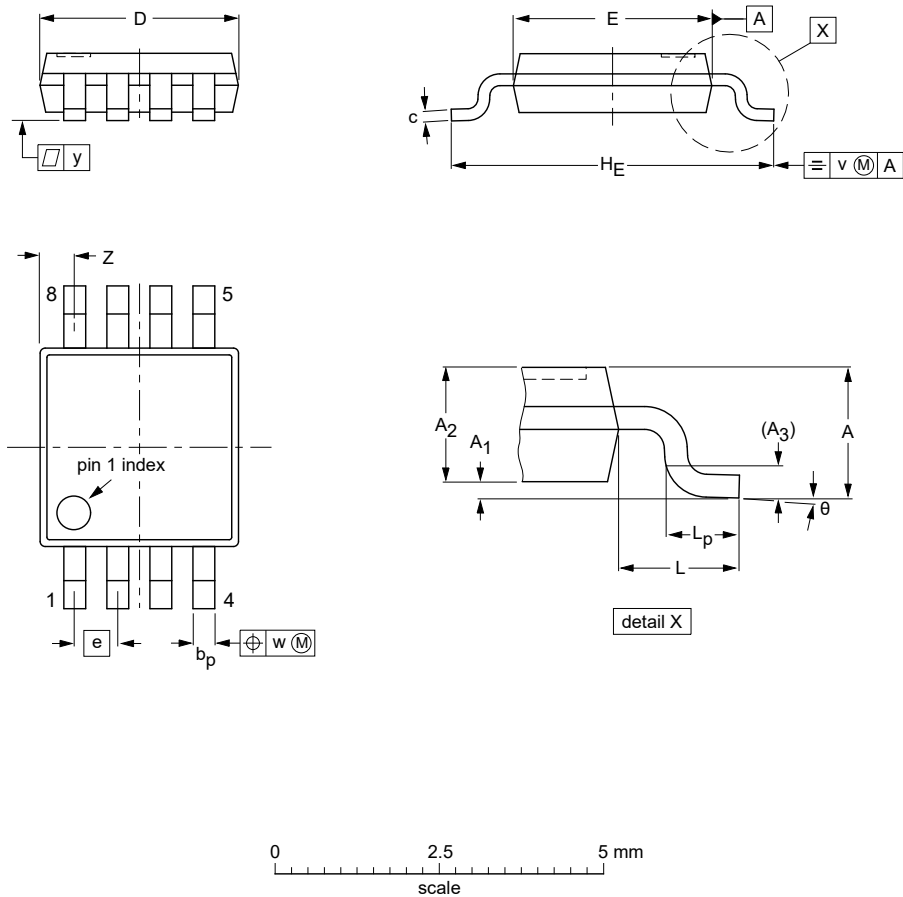
- 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				99-12-27 03-02-18

Figure 21. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						99-04-09 03-02-18

Figure 22. Package outline SOT505-1 (TSSOP8)

14 Soldering of SMD packages

This text provides a brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to printed-circuit boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed-circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, therefore, reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume, and is classified in accordance with [Table 6](#) and [Table 7](#)

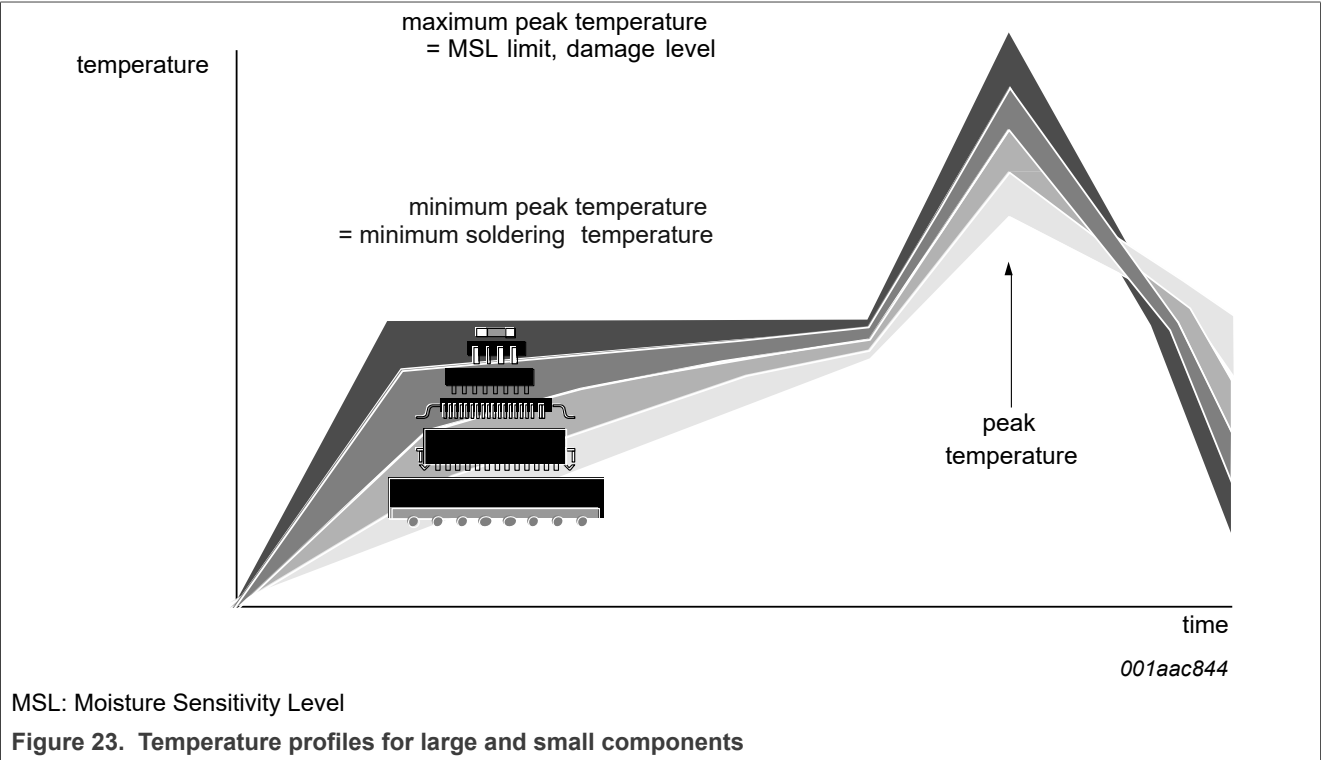
Table 6. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected always.
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

15 Acronyms

Table 8. Acronyms

Acronym	Description
AdvancedTCA	Advanced Telecom Computing Architecture
CDM	Charged device model
cPCI	Compact peripheral component interface
ESD	Electrostatic discharge
HBM	Human body model
I ² C-bus	Inter-IC bus
MM	Machine model
PCI	Peripheral Component Interface
PICMG	PCI industrial computer manufacturers group
SMBus	System management bus
VME	VERSA Module Eurocard

16 Revision history

[Table 9](#) summarizes the revisions to this document.

Table 9. Revision history

Document ID	Revision date	Description
PCA9511A v.5.0	1 July 2025	Updated as per CIN# 202504028I: - Added Section 9.1 - Added Section 9.1.1 - Applied editorial fixes
PCA9511A v.4.0	19 August 2009	PCA9511A v.4.0 release
PCA9511A v.3.0	20 July 2009	PCA9511A v.3.0 release
PCA9511A v.2.0	28 May 20090528	PCA9511A v.2.0 release
PCA9511A v.1.0	15 August 2005	Initial release

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

1	General description	2
2	Features	2
3	Applications	2
4	Feature selection	2
5	Ordering information	3
6	Block diagram	3
7	Pinning information	4
7.1	Pinning	4
7.2	Pin description	5
8	Functional description	5
8.1	Start-up	5
8.2	Connect circuitry	5
8.3	Maximum number of devices in series	6
8.4	Propagation delays	7
8.5	Rise time accelerators	7
8.6	READY digital output	7
8.7	ENABLE low current disable	7
8.8	Resistor pull-up value selection	7
8.9	Hot swapping and capacitance buffering application	9
9	Application design-in information	11
9.1	Missing ACK event	11
9.1.1	Workaround	12
10	Limiting values	12
11	Characteristics	13
11.1	Typical performance characteristics	15
11.2	Timing diagrams	15
12	Test information	17
13	Package outline	17
14	Soldering of SMD packages	20
14.1	Introduction to soldering	20
14.2	Wave and reflow soldering	20
14.3	Wave soldering	20
14.4	Reflow soldering	20
15	Acronyms	22
16	Revision history	22
	Legal information	23

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.