LS1043A

QorIQ LS1043A, LS1023A Data Sheet

Features

- LS1043A contains 32-bit /64-bit ARM® Cortex®-A53 MPCore Processor with the following capabilities:
  - Speed up to 1.6 GHz
  - 32 KB L1 Instruction Cache w/parity
  - 32 KB L1 Data Cache w/ECC
  - Neon SIMD Co-processor
  - ARM v8 Cryptography Extensions
- 1 MB unified I/D L2 Cache w/ECC
- Hierarchical interconnect fabric
  - Hardware Managed Data coherency
  - Up to 400 MHz operation
- One 32-bit DDR3L/DDR4 SDRAM memory controller
  - ECC and interleaving support
  - Up to 1.6 GT/s
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (FMan)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
- Parallel Ethernet interfaces
  - Up to two RGMII interfaces
  - IEEE 1588 support
- Four SerDes lanes for high-speed peripheral interfaces
  - Three PCI Express 2.0 controllers supporting x4 operation
  - One Serial ATA (SATA 3.0) controller
  - Up to four SGMII supporting 1000 Mbit/s
  - Up to two SGMII supporting 2500 Mbit/s
  - Up to one XFI (10 GbE) interface
  - Up to one QSGMII
  - Supports 1000Base-KX
- Additional peripheral interfaces
  - One Quad Serial Peripheral Interface (QSPI) controller, one Deserial Serial Peripheral Interface (DSPI) controller
  - Integrated Flash Controller (IFC) supporting NAND and NOR flash with 28-bit addressing and 16-bit data
  - Three USB 3.0 controllers with integrated PHY
  - Enhanced Secure Digital Host Controller (eSDHC) supporting SD 3.0, eMMC 4.4, and eMMC 4.5 modes
  - uQE supporting TDM/HDLC
  - Four I2C controllers
  - Two 16550 compliant DUARTs and six low-power UARTs (LPUARTs)
  - General Purpose IO (GPIO), eight Flextimers, five Watchdog timer, four independent PWM/counters/timer
  - Trust Architecture
  - Debug supporting run control, data acquisition, high-speed trace, and performance/event monitoring

Table of Contents

1 Introduction

LS1043A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP value-performance line of QorIQ communications processors. Featuring extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.6 GHz.

This chip can be used for networking and wireless access points, industrial gateways, industrial automation, M2M for enterprise, consumer networking and router applications.

This figure shown below represents the block diagram of the LS1043A chip.

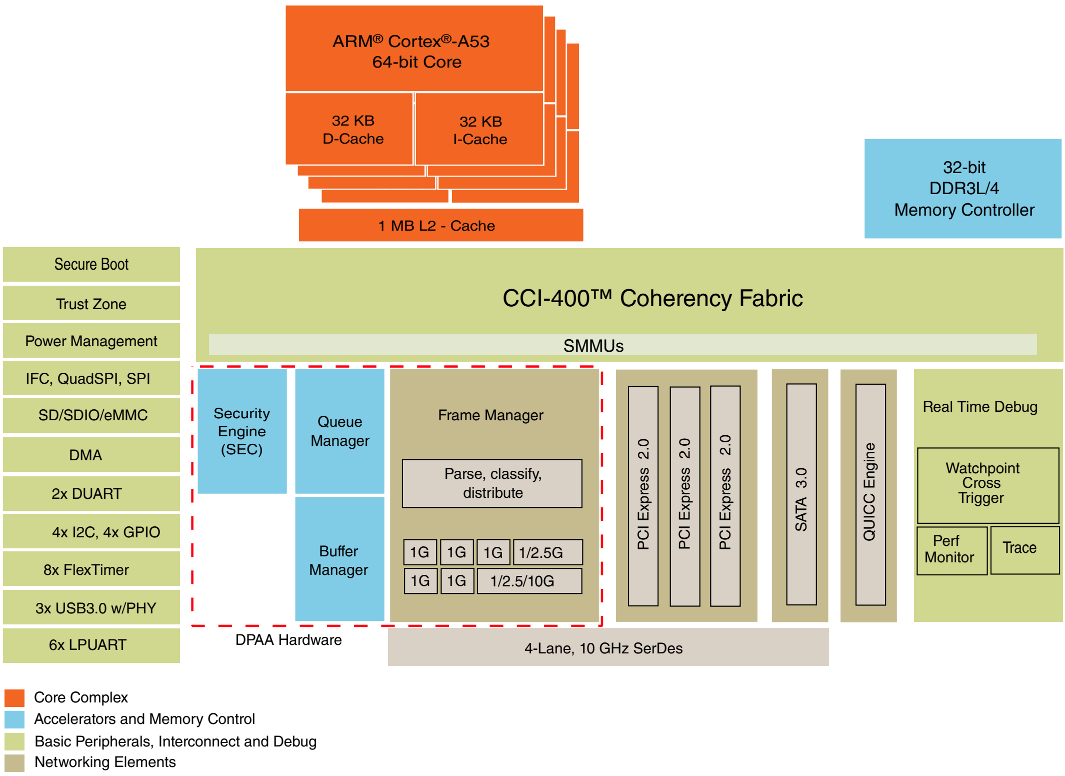

Figure 1. LS1043A Block Diagram

This figure shown below represents the block diagram of the LS1023A chip.

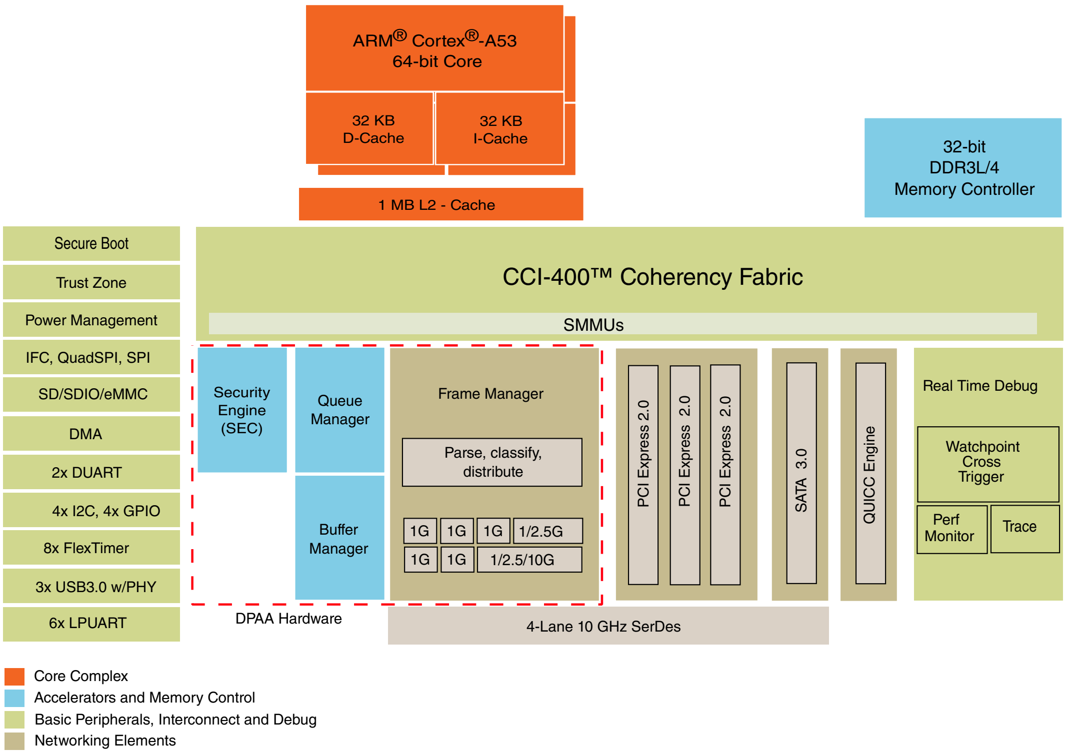

Figure 2. LS1023A Block Diagram

2 Pin assignments

This section describes the ball map diagram and pin list table for both 21x21 and 23x23 packages of LS1043A.

2.1 621 ball layout diagrams

This figure shows the complete view of the LS1043A ball map diagram for the 21x21 package. Figure 4, Figure 5, Figure 6, and Figure 7 show quadrant views.

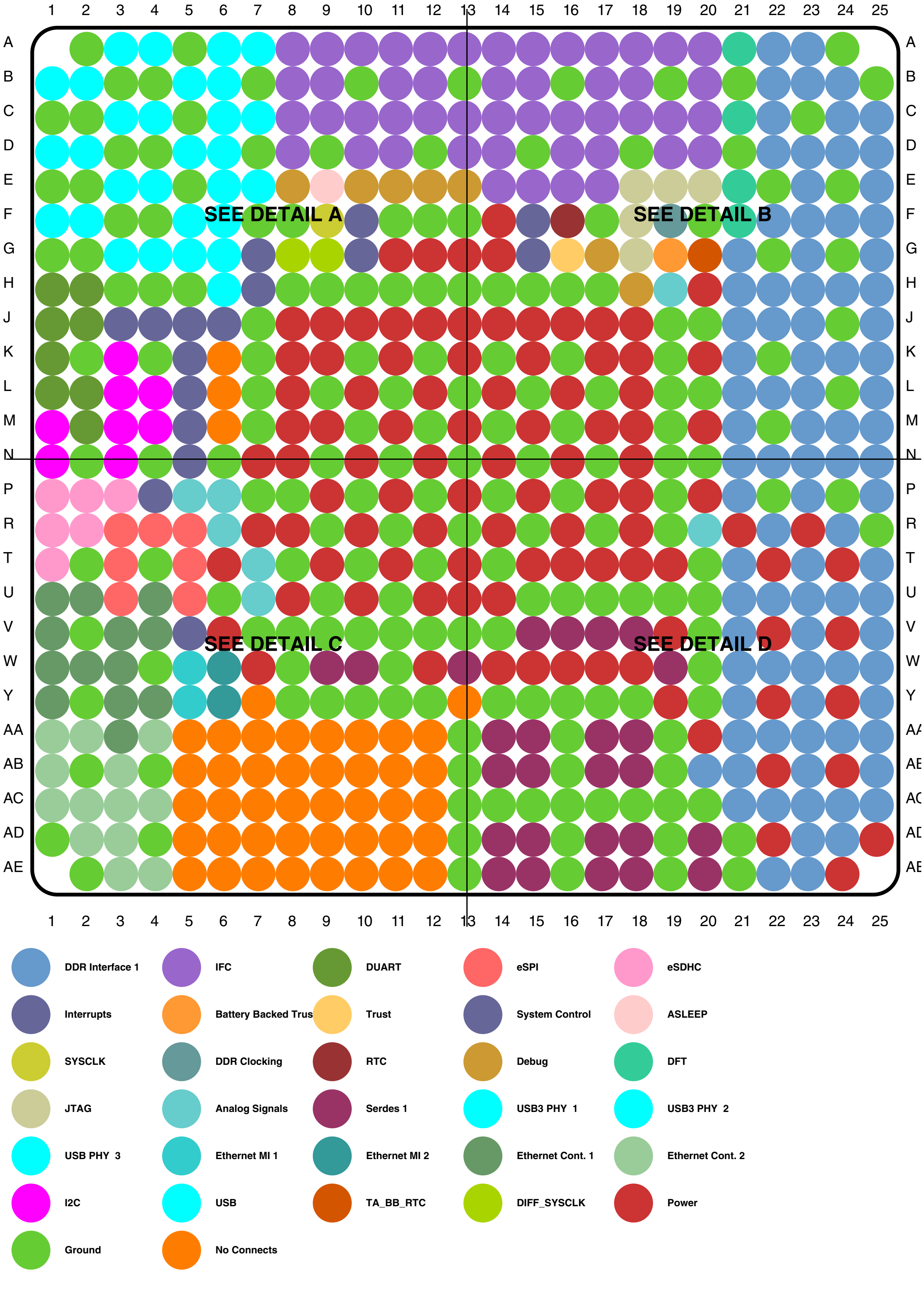

Figure 3. Complete BGA Map for the LS1043A

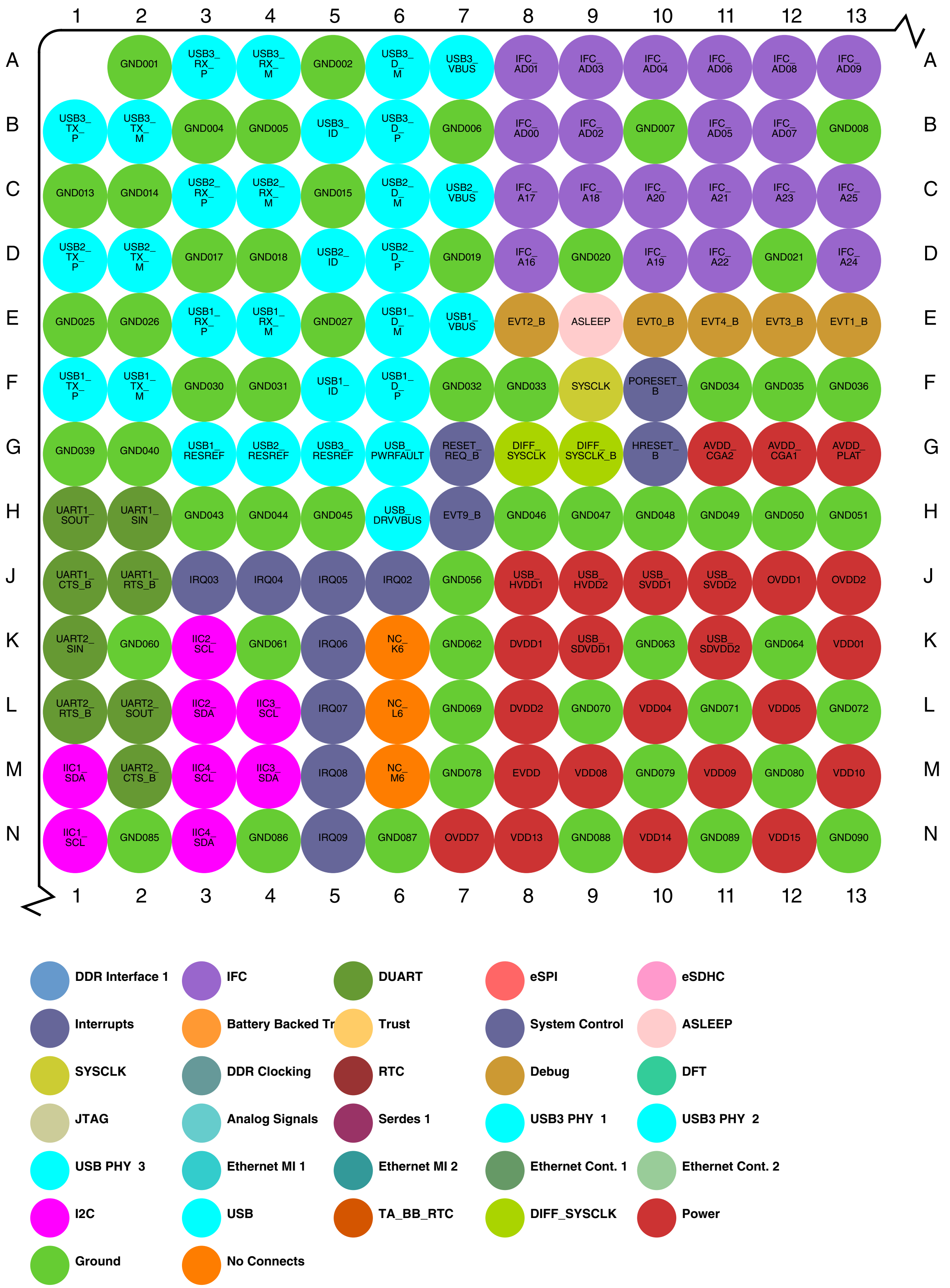

Figure 4. Detail A

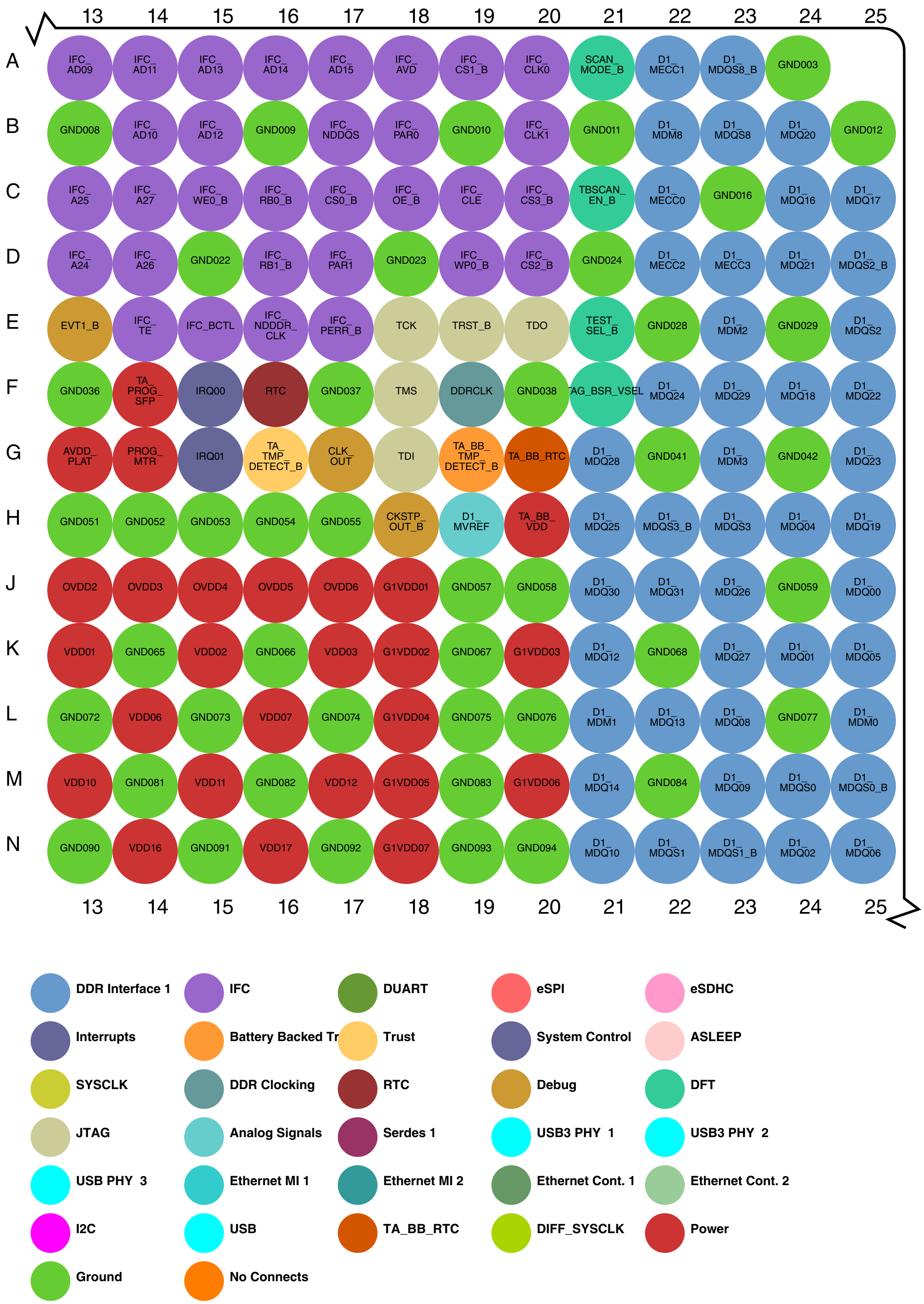

Figure 5. Detail B

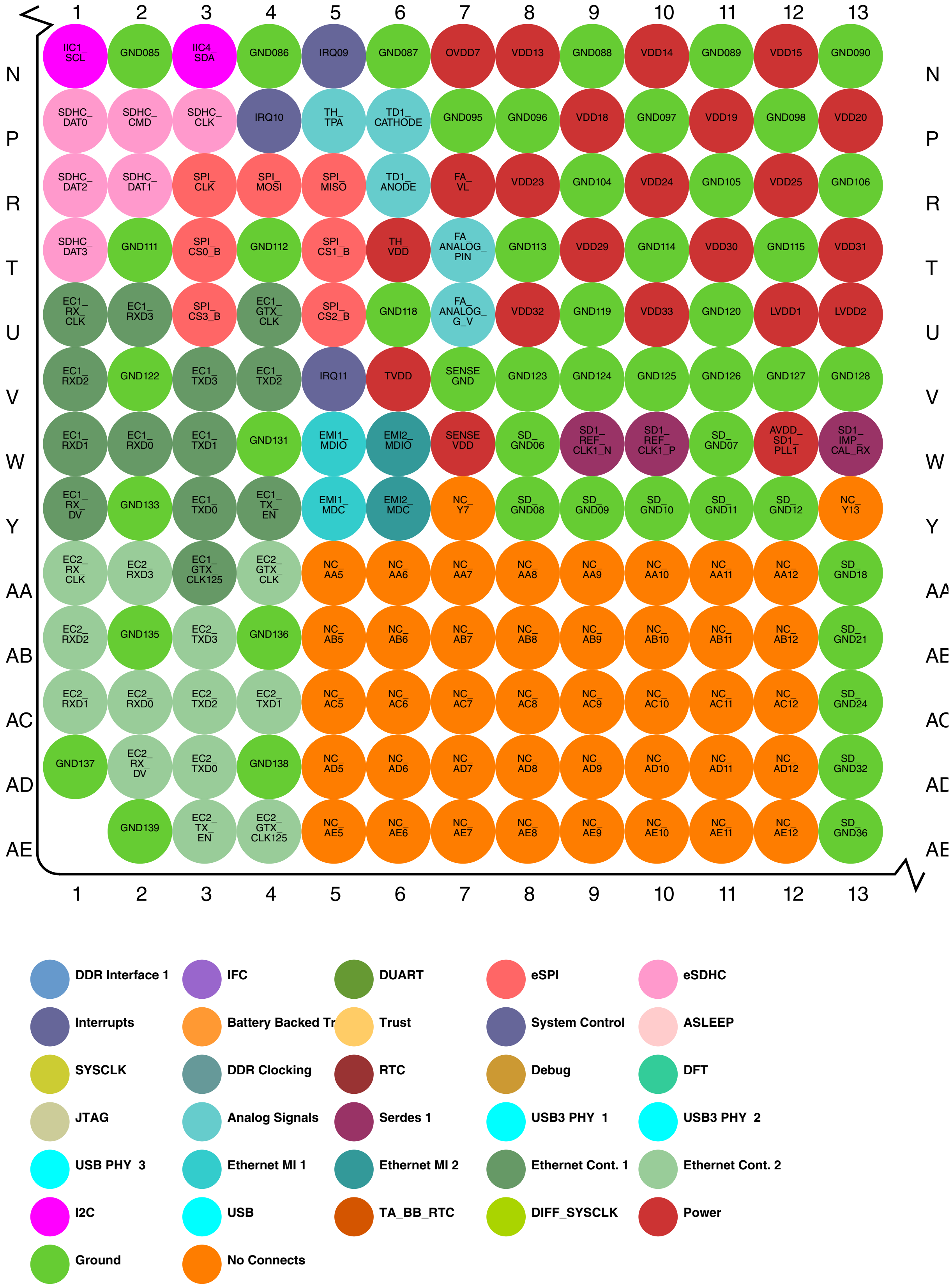

Figure 6. Detail C

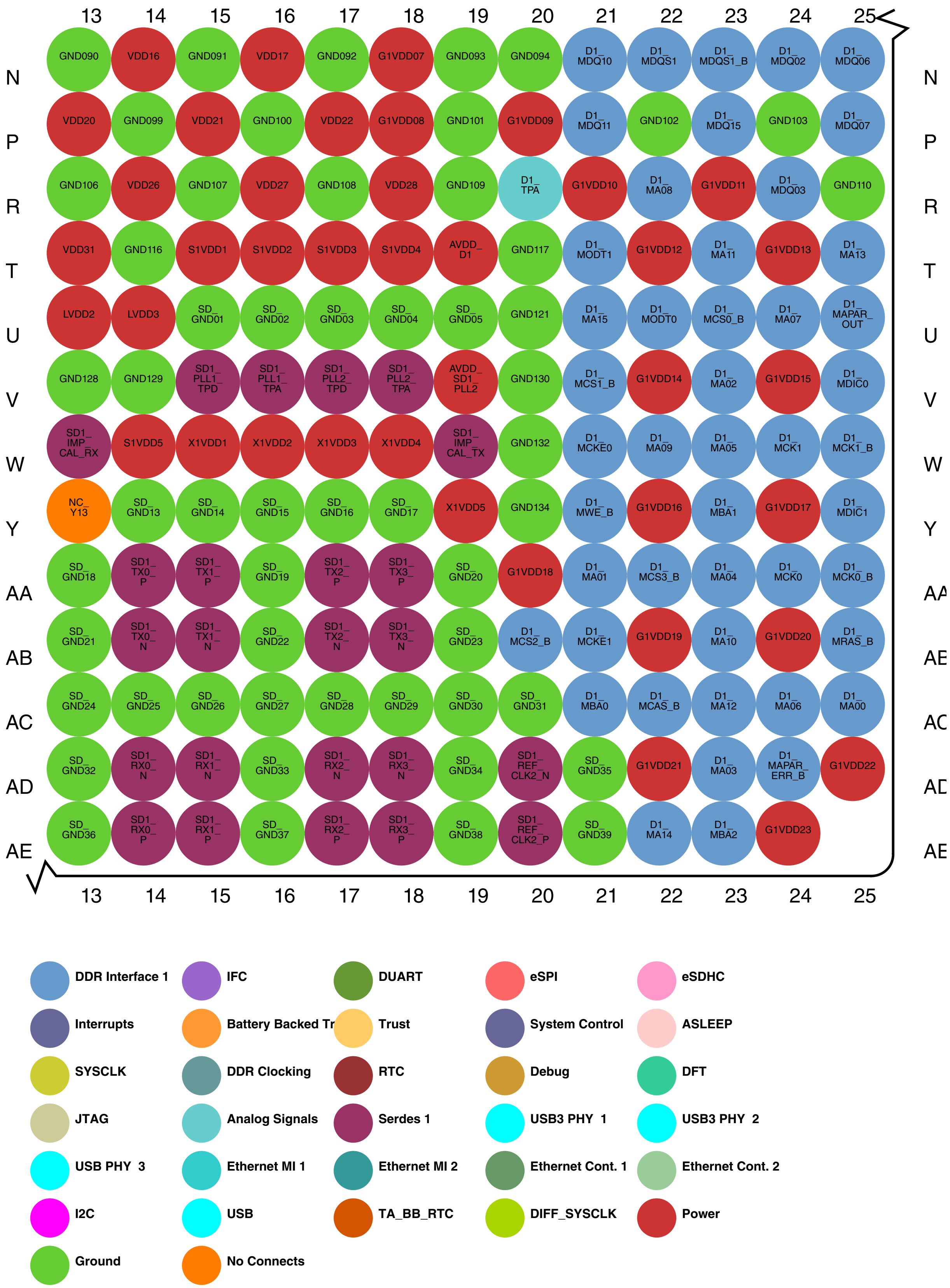

Figure 7. Detail D

2.2 Pinout list (21x21)

This table provides the pinout listing for the LS1043A (21x21) by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	AC25	O	$G1V_{DD}$	---
D1_MA01	Address	AA21	O	$G1V_{DD}$	---
D1_MA02	Address	V23	O	$G1V_{DD}$	---
D1_MA03	Address	AD23	O	$G1V_{DD}$	---
D1_MA04	Address	AA23	O	$G1V_{DD}$	---
D1_MA05	Address	W23	O	$G1V_{DD}$	---
D1_MA06	Address	AC24	O	$G1V_{DD}$	---
D1_MA07	Address	U24	O	$G1V_{DD}$	---
D1_MA08	Address	R22	O	$G1V_{DD}$	---
D1_MA09	Address	W22	O	$G1V_{DD}$	---
D1_MA10	Address	AB23	O	$G1V_{DD}$	---
D1_MA11	Address	T23	O	$G1V_{DD}$	---
D1_MA12	Address	AC23	O	$G1V_{DD}$	---
D1_MA13	Address	T25	O	$G1V_{DD}$	---
D1_MA14	Address	AE22	O	$G1V_{DD}$	25
D1_MA15	Address	U21	O	$G1V_{DD}$	25
D1_MAPAR_ERR_B	Address Parity Error	AD24	I	$G1V_{DD}$	1, 6, 25
D1_MAPAR_OUT	Address Parity Out	U25	O	$G1V_{DD}$	25
D1_MBA0	Bank Select	AC21	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	Y23	O	$G1V_{DD}$	---
D1_MBA2	Bank Select	AE23	O	$G1V_{DD}$	25
D1_MCAS_B	Column Address Strobe	AC22	O	$G1V_{DD}$	25
D1_MCK0	Clock	AA24	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	AA25	O	$G1V_{DD}$	---
D1_MCK1	Clock	W24	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	W25	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	W21	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	AB21	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	U23	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	V21	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select	AB20	O	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCS3_B	Chip Select	AA22	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedence Calibration	V25	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	Y25	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	L25	O	$G1V_{DD}$	1, 25
D1_MDM1	Data Mask	L21	O	$G1V_{DD}$	1, 25
D1_MDM2	Data Mask	E23	O	$G1V_{DD}$	1, 25
D1_MDM3	Data Mask	G23	O	$G1V_{DD}$	1, 25
D1_MDM8	Data Mask	B22	O	$G1V_{DD}$	1, 25
D1_MDQ00	Data	J25	IO	$G1V_{DD}$	---
D1_MDQ01	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ02	Data	N24	IO	$G1V_{DD}$	---
D1_MDQ03	Data	R24	IO	$G1V_{DD}$	---
D1_MDQ04	Data	H24	IO	$G1V_{DD}$	---
D1_MDQ05	Data	K25	IO	$G1V_{DD}$	---
D1_MDQ06	Data	N25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	P25	IO	$G1V_{DD}$	---
D1_MDQ08	Data	L23	IO	$G1V_{DD}$	---
D1_MDQ09	Data	M23	IO	$G1V_{DD}$	---
D1_MDQ10	Data	N21	IO	$G1V_{DD}$	---
D1_MDQ11	Data	P21	IO	$G1V_{DD}$	---
D1_MDQ12	Data	K21	IO	$G1V_{DD}$	---
D1_MDQ13	Data	L22	IO	$G1V_{DD}$	---
D1_MDQ14	Data	M21	IO	$G1V_{DD}$	---
D1_MDQ15	Data	P23	IO	$G1V_{DD}$	---
D1_MDQ16	Data	C24	IO	$G1V_{DD}$	---
D1_MDQ17	Data	C25	IO	$G1V_{DD}$	---
D1_MDQ18	Data	F24	IO	$G1V_{DD}$	---
D1_MDQ19	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ20	Data	B24	IO	$G1V_{DD}$	---
D1_MDQ21	Data	D24	IO	$G1V_{DD}$	---
D1_MDQ22	Data	F25	IO	$G1V_{DD}$	---
D1_MDQ23	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ24	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ25	Data	H21	IO	$G1V_{DD}$	---
D1_MDQ26	Data	J23	IO	$G1V_{DD}$	---
D1_MDQ27	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ28	Data	G21	IO	$G1V_{DD}$	---
D1_MDQ29	Data	F23	IO	$G1V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ30	Data	J21	IO	$G1V_{DD}$	---
D1_MDQ31	Data	J22	IO	$G1V_{DD}$	---
D1_MDQS0	Data Strobe	M24	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	M25	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	N22	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	N23	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	E25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	D25	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	H23	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	H22	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	B23	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	A23	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	C22	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	A22	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	D22	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	D23	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	U22	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination	T21	O	$G1V_{DD}$	2
D1_MRAS_B	Row Address Strobe	AB25	O	$G1V_{DD}$	25
D1_MWE_B	Write Enable	Y21	O	$G1V_{DD}$	25
Integrated Flash Controller					
IFC_A16/QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A17/QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A18/QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5
IFC_A19/QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A20/QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A21/QSPI_B_SCK/ cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A22/QSPI_A_DATA0/ IFC_WP1_B	IFC Address	D11	O	OV_{DD}	1
IFC_A23/QSPI_A_DATA1/ IFC_WP2_B	IFC Address	C12	O	OV_{DD}	1
IFC_A24/QSPI_A_DATA2/ IFC_WP3_B	IFC Address	D13	O	OV_{DD}	1
IFC_A25/GPIO2_25/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	IFC Address	C13	O	OV_{DD}	1
IFC_A26/GPIO2_26/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	IFC Address	D14	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A27/GPIO2_27/ FTM5_EXTCLK/IFC_CS6_B	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	B8	IO	OV_{DD}	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	A8	IO	OV_{DD}	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	B9	IO	OV_{DD}	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	A9	IO	OV_{DD}	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	A10	IO	OV_{DD}	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	B11	IO	OV_{DD}	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	A11	IO	OV_{DD}	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	B12	IO	OV_{DD}	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	A12	IO	OV_{DD}	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A13	IO	OV_{DD}	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	B14	IO	OV_{DD}	4
IFC_AD11/cfg_rcw_src3	IFC Address / Data	A14	IO	OV_{DD}	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	B15	IO	OV_{DD}	4
IFC_AD13/cfg_rcw_src5	IFC Address / Data	A15	IO	OV_{DD}	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A16	IO	OV_{DD}	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A17	IO	OV_{DD}	4
IFC_AVD	IFC Address Valid	A18	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer control	E15	O	OV_{DD}	2
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	C19	O	OV_{DD}	1, 4
IFC_CLK0	IFC Clock	A20	O	OV_{DD}	2
IFC_CLK1	IFC Clock	B20	O	OV_{DD}	2
IFC_CS0_B	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10/ FTM7_CH0	IFC Chip Select	A19	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_11/ FTM7_CH1	IFC Chip Select	D20	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_12/ QSPI_B_DATA3/ FTM7_EXTCLK	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS4_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_RB2_B	IFC Chip Select	C13	O	OV_{DD}	1
IFC_CS5_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_RB3_B	IFC Chip Select	D14	O	OV_{DD}	1
IFC_CS6_B/**IFC_A27**/ GPIO2_27/FTM5_EXTCLK	IFC Chip Select	C14	O	OV_{DD}	1
IFC_NDDDR_CLK	IFC NAND DDR Clock	E16	O	OV_{DD}	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_NDDQS	IFC DQS Strobe	B17	IO	OV_{DD}	---
IFC_OE_B/cfg_eng_use1	IFC Output Enable	C18	O	OV_{DD}	1, 4, 21
IFC_PAR0/GPIO2_13/ QSPI_B_DATA0/FTM6_CH0	IFC Address & Data Parity	B18	IO	OV_{DD}	---
IFC_PAR1/GPIO2_14/ QSPI_B_DATA1/FTM6_CH1	IFC Address & Data Parity	D17	IO	OV_{DD}	---
IFC_PERR_B/GPIO2_15/ QSPI_B_DATA2/ FTM6_EXTCLK	IFC Parity Error	E17	I	OV_{DD}	1
IFC_RB0_B	IFC Ready / Busy CS0	C16	I	OV_{DD}	6
IFC_RB1_B	IFC Ready / Busy CS1	D16	I	OV_{DD}	6
IFC_RB2_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_CS4_B	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_CS5_B	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	C15	O	OV_{DD}	1, 4, 21
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 4, 21
IFC_WP1_B/**IFC_A22**/ QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A23**/ QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A24**/ QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	H1	O	DV_{DD}	1
UART2_CTS_B/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Ready to Send	L1	O	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_SIN/GPIO1_18/ FTM4_CH1/LPUART1_SIN	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO1_16/ LPUART1_SOUT/FTM4_CH0	Transmit Data	L2	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21/FTM4_CH4/ LPUART2_SIN	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19/ LPUART2_SOUT/FTM4_CH2	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit Data	L1	O	DV_{DD}	1
SPI Interface					
SPI_CLK	SPI Clock	R3	O	OV_{DD}	1
SPI_CS0_B/GPIO2_00/ SDHC_DAT4/SDHC_VS	SPI Chip Select	T3	O	OV_{DD}	1
SPI_CS1_B/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	T5	O	OV_{DD}	1
SPI_CS2_B/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	U5	O	OV_{DD}	1
SPI_CS3_B/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	U3	O	OV_{DD}	1
SPI_MISO/ SDHC_CLK_SYNC_IN	Master In Slave Out	R5	I	OV_{DD}	1
SPI_MOSI/ SDHC_CLK_SYNC_OUT	Master Out Slave In	R4	O	OV_{DD}	---
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO4_02/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	Command	K3	I	DV_{DD}	1
SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	Host to Card Clock	P3	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/ **SPI_MISO**	IN	R5	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CLK_SYNC_OUT/ **SPI_MOSI**	OUT	R4	O	OV_{DD}	1
SDHC_CMD/GPIO2_04/ LPUART3_SOUT/FTM4_CH6	Command/Response	P2	IO	EV_{DD}	---
SDHC_CMD_DIR/**SPI_CS1_B**/ GPIO2_01/SDHC_DAT5	DIR	T5	O	OV_{DD}	1
SDHC_DAT0/GPIO2_05/ FTM4_CH7/LPUART3_SIN	Data	P1	IO	EV_{DD}	---
SDHC_DAT0_DIR/ **SPI_CS2_B**/GPIO2_02/ SDHC_DAT6	DIR	U5	O	OV_{DD}	1
SDHC_DAT1/GPIO2_06/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	Data	R2	IO	EV_{DD}	---
SDHC_DAT123_DIR/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7	DIR	U3	O	OV_{DD}	1
SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	Data	R1	IO	EV_{DD}	---
SDHC_DAT3/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	Data	T1	IO	EV_{DD}	---
SDHC_DAT4/**SPI_CS0_B**/ GPIO2_00/SDHC_VS	Data	T3	IO	OV_{DD}	---
SDHC_DAT5/**SPI_CS1_B**/ GPIO2_01/SDHC_CMD_DIR	Data	T5	IO	OV_{DD}	---
SDHC_DAT6/**SPI_CS2_B**/ GPIO2_02/SDHC_DAT0_DIR	Data	U5	IO	OV_{DD}	---
SDHC_DAT7/**SPI_CS3_B**/ GPIO2_03/ SDHC_DAT123_DIR	Data	U3	IO	OV_{DD}	---
SDHC_VS/**SPI_CS0_B**/ GPIO2_00/SDHC_DAT4	VS	T3	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO4_03/FTM3_QD_PHB/ CLK10/QE_SI1_STROBE1/ BRGO3	Write Protect	L3	I	DV_{DD}	1
Programmable Interrupt Controller					
EVT9_B	Interrupt Output	H7	O	OV_{DD}	1, 6, 7
IRQ00	External Interrupt	F15	I	OV_{DD}	1
IRQ01	External Interrupt	G15	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ02	External Interrupt	J6	I	OV_{DD}	1
IRQ03/GPIO1_23/FTM3_CH7/ TDMB_TSYNC/ UC3_RTSB_TXEN	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO1_24/FTM3_CH0/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO1_25/FTM3_CH1/ TDMA_RSYNC/ UC1_CTSB_RXDV	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO1_26/FTM3_CH2/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	External Interrupt	K5	I	DV_{DD}	1
IRQ07/GPIO1_27/FTM3_CH3/ TDMA_TSYNC/ UC1_RTSB_TXEN	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO1_28/FTM3_CH4/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO1_29/FTM3_CH5/ TDMB_RSYNC/ UC3_CTSB_RXDV	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO1_30/FTM3_CH6/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO1_31	External Interrupt	V5	I	LV_{DD}	1
Battery Backed Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	G19	I	$TA\_BB\_V_{DD}$	---
Trust					
TA_TMP_DETECT_B	Tamper Detect	G16	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	G10	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F10	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	G7	O	OV_{DD}	1, 5
Power Management					
ASLEEP/GPIO1_13	Asleep	E9	O	OV_{DD}	1, 4
SYSCLK					
SYSCLK	System Clock	F9	I	OV_{DD}	18
DDR Clocking					
DDRCLK	DDR Controller Clock	F19	I	OV_{DD}	18
RTC					
RTC/GPIO1_14	Real Time Clock	F16	I	OV_{DD}	1
Debug					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
CKSTP_OUT_B	Reserved	H18	O	OV_{DD}	6, 7
CLK_OUT	Clock Out	G17	O	OV_{DD}	2
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	---
EVT2_B	Event 2	E8	IO	OV_{DD}	---
EVT3_B	Event 3	E12	IO	OV_{DD}	---
EVT4_B	Event 4	E11	IO	OV_{DD}	---
EVT5_B/**IIC3_SCL**/GPIO4_10/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_11/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_12/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_13/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	Event 8	N3	IO	DV_{DD}	---
DFT					
JTAG_BSR_VSEL	An IEEE 1149.1 JTAG compliance enable pin. 0: Normal operation. 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.	F21	I	OV_{DD}	36
SCAN_MODE_B	Reserved	A21	I	OV_{DD}	10
TBSCAN_EN_B	An IEEE 1149.1 JTAG compliance enable pin. 0:To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the ARM core debug.	C21	I	OV_{DD}	35
TEST_SEL_B	Reserved	E21	I	OV_{DD}	23
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G18	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TMS	Test Mode Select	F18	I	OV_{DD}	9
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_MVREF	SSTL Reference Voltage	H19	IO	$G1V_{DD}/2$	---
D1_TPA	DDR Controller 1 Test Point Analog	R20	IO		12
FA_ANALOG_G_V	Reserved	U7	IO		15
FA_ANALOG_PIN	Reserved	T7	IO		15
TD1_ANODE	Thermal diode anode	R6	IO		17
TD1_CATHODE	Thermal diode cathode	P6	IO		17
TH_TPA	Thermal Test Point Analog	P5	-	-	12
SerDes					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	W13	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	W19	I	$X1V_{DD}$	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	V16	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	V15	O	$X1V_{DD}$	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	V18	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	V17	O	$X1V_{DD}$	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	W9	I	$S1V_{DD}$	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	W10	I	$S1V_{DD}$	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AD20	I	$S1V_{DD}$	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AE20	I	$S1V_{DD}$	---
SD1_RX0_N	SerDes Receive Data (negative)	AD14	I	$S1V_{DD}$	---
SD1_RX0_P	SerDes Receive Data (positive)	AE14	I	$S1V_{DD}$	---
SD1_RX1_N	SerDes Receive Data (negative)	AD15	I	$S1V_{DD}$	---
SD1_RX1_P	SerDes Receive Data (positive)	AE15	I	$S1V_{DD}$	---
SD1_RX2_N	SerDes Receive Data (negative)	AD17	I	$S1V_{DD}$	---
SD1_RX2_P	SerDes Receive Data (positive)	AE17	I	$S1V_{DD}$	---
SD1_RX3_N	SerDes Receive Data (negative)	AD18	I	$S1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX3_P	SerDes Receive Data (positive)	AE18	I	$S1V_{DD}$	---
SD1_TX0_N	SerDes Transmit Data (negative)	AB14	O	$X1V_{DD}$	---
SD1_TX0_P	SerDes Transmit Data (positive)	AA14	O	$X1V_{DD}$	---
SD1_TX1_N	SerDes Transmit Data (negative)	AB15	O	$X1V_{DD}$	---
SD1_TX1_P	SerDes Transmit Data (positive)	AA15	O	$X1V_{DD}$	---
SD1_TX2_N	SerDes Transmit Data (negative)	AB17	O	$X1V_{DD}$	---
SD1_TX2_P	SerDes Transmit Data (positive)	AA17	O	$X1V_{DD}$	---
SD1_TX3_N	SerDes Transmit Data (negative)	AB18	O	$X1V_{DD}$	---
SD1_TX3_P	SerDes Transmit Data (positive)	AA18	O	$X1V_{DD}$	---
USB3 PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	USB_HV_{DD}	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	USB_HV_{DD}	---
USB1_ID	USB PHY ID Detect	F5	I	-	29
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	27
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	USB_SV_{DD}	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	USB_SV_{DD}	---
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	USB_SV_{DD}	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	USB_SV_{DD}	---
USB1_VBUS	USB PHY VBUS	E7	I	-	28
USB3 PHY 2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	USB_HV_{DD}	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	USB_HV_{DD}	---
USB2_ID	USB PHY ID Detect	D5	I	-	29
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	27
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	USB_SV_{DD}	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	USB_SV_{DD}	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	USB_SV_{DD}	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	USB_SV_{DD}	---
USB2_VBUS	USB PHY VBUS	C7	I	-	28

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
		USB3 PHY 3			
USB3_D_M	USB PHY HS Data (-)	A6	IO	USB_HV_{DD}	---
USB3_D_P	USB PHY HS Data (+)	B6	IO	USB_HV_{DD}	---
USB3_ID	USB PHY ID Detect	B5	I	-	29
USB3_RESREF	USB PHY Impedance Calibration	G5	IO	-	27
USB3_RX_M	USB PHY SS Receive Data (-)	A4	I	USB_SV_{DD}	---
USB3_RX_P	USB PHY SS Receive Data (+)	A3	I	USB_SV_{DD}	---
USB3_TX_M	USB PHY SS Transmit Data (-)	B2	O	USB_SV_{DD}	---
USB3_TX_P	USB PHY SS Transmit Data (+)	B1	O	USB_SV_{DD}	---
USB3_VBUS	USB PHY VBUS	A7	I	-	28
		Ethernet Management Interface 1			
EMI1_MDC/GPIO3_00	Management Data Clock	Y5	O	LV_{DD}	1
EMI1_MDIO/GPIO3_01	Management Data In/Out	W5	IO	LV_{DD}	---
		Ethernet Management Interface 2			
EMI2_MDC/GPIO4_00	Management Data Clock	Y6	O	TV_{DD}	1
EMI2_MDIO/GPIO4_01	Management Data In/Out	W6	IO	TV_{DD}	---
		Ethernet Controller 1			
EC1_GTX_CLK/GPIO3_07/ FTM1_EXTCLK	Transmit Clock Out	U4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO3_08	Reference Clock	AA3	I	LV_{DD}	1
EC1_RXD0/GPIO3_12/ FTM1_CH0	Receive Data	W2	I	LV_{DD}	1
EC1_RXD1/GPIO3_11/ FTM1_CH1	Receive Data	W1	I	LV_{DD}	1
EC1_RXD2/GPIO3_10/ FTM1_CH6	Receive Data	V1	I	LV_{DD}	1
EC1_RXD3/GPIO3_09/ FTM1_CH4	Receive Data	U2	I	LV_{DD}	1
EC1_RX_CLK/GPIO3_13/ FTM1_QD_PHA	Receive Clock	U1	I	LV_{DD}	1
EC1_RX_DV/GPIO3_14/ FTM1_QD_PHB	Receive Data Valid	Y1	I	LV_{DD}	1
EC1_TXD0/GPIO3_05/ FTM1_CH2	Transmit Data	Y3	O	LV_{DD}	1
EC1_TXD1/GPIO3_04/ FTM1_CH3	Transmit Data	W3	O	LV_{DD}	1
EC1_TXD2/GPIO3_03/ FTM1_CH7	Transmit Data	V4	O	LV_{DD}	1
EC1_TXD3/GPIO3_02/ FTM1_CH5	Transmit Data	V3	O	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_TX_EN/GPIO3_06/ FTM1_FAULT	Transmit Enable	Y4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO3_20/ FTM2_EXTCLK	Transmit Clock Out	AA4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO3_21	Reference Clock	AE4	I	LV_{DD}	1
EC2_RXD0/GPIO3_25/ TSEC_1588_TRIG_IN2/ FTM2_CH0	Receive Data	AC2	I	LV_{DD}	1
EC2_RXD1/GPIO3_24/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	Receive Data	AC1	I	LV_{DD}	1
EC2_RXD2/GPIO3_23/ FTM2_CH6	Receive Data	AB1	I	LV_{DD}	1
EC2_RXD3/GPIO3_22/ FTM2_CH4	Receive Data	AA2	I	LV_{DD}	1
EC2_RX_CLK/GPIO3_26/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	Receive Clock	AA1	I	LV_{DD}	1
EC2_RX_DV/GPIO3_27/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	Receive Data Valid	AD2	I	LV_{DD}	1
EC2_TXD0/GPIO3_18/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	Transmit Data	AD3	O	LV_{DD}	1
EC2_TXD1/GPIO3_17/ TSEC_1588_CLK_OUT/ FTM2_CH3	Transmit Data	AC4	O	LV_{DD}	1
EC2_TXD2/GPIO3_16/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	Transmit Data	AC3	O	LV_{DD}	1
EC2_TXD3/GPIO3_15/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	Transmit Data	AB3	O	LV_{DD}	1
EC2_TX_EN/GPIO3_19/ FTM2_FAULT	Transmit Enable	AE3	O	LV_{DD}	1, 14
I2C					
IIC1_SCL	Serial Clock (supports PBL)	N1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	M1	IO	DV_{DD}	7, 8
IIC2_SCL/GPIO4_02/ SDHC_CD_B/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	Serial Clock	K3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO4_03/ SDHC_WP/FTM3_QD_PHB/	Serial Data	L3	IO	DV_{DD}	7, 8

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
CLK10/QE_SI1_STROBE1/ BRGO3					
IIC3_SCL/GPIO4_10/EVT5_B/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	Serial Clock	L4	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_11/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	Serial Data	M4	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_12/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	Serial Clock	M3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_13/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	Serial Data	N3	IO	DV_{DD}	7, 8
USB					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_10/EVT5_B/BRGO4/ FTM8_CH0/CLK11	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_11/EVT6_B/BRGO1/ FTM8_CH1/CLK12_CLK8	PWR Fault	M4	I	DV_{DD}	1
USB3_DRVVBUS/**IIC4_SCL**/ GPIO4_12/EVT7_B/ TDMA_RQ/FTM3_FAULT/ UC1_CDB_RXER	DRV Bus	M3	O	DV_{DD}	1
USB3_PWRFAULT/**IIC4_SDA**/ GPIO4_13/EVT8_B/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	PWR Fault	N3	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_29	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_30	USB_PWRFAULT	G6	I	DV_{DD}	1
Battery Backed RTC					
TA_BB_RTC	Reserved	G20	I	$TA\_BB\_V_{DD}$	33
DSYSCLK					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	G8	I	OV_{DD}	19
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	G9	I	OV_{DD}	19
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**/ QSPI_B_SCK	Power-on-Reset Configuration	C11	I	OV_{DD}	1, 4
cfg_eng_use0/**IFC_WE0_B**	Power-on-Reset Configuration	C15	I	OV_{DD}	1, 4
cfg_eng_use1/**IFC_OE_B**	Power-on-Reset Configuration	C18	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_eng_use2/**IFC_WP0_B**	Power-on-Reset Configuration	D19	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-on-Reset Configuration	B8	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-on-Reset Configuration	A8	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-on-Reset Configuration	B9	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-on-Reset Configuration	A9	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-on-Reset Configuration	A10	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-on-Reset Configuration	B11	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**	Power-on-Reset Configuration	A11	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-on-Reset Configuration	B12	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-on-Reset Configuration	E14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-on-Reset Configuration	A12	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-on-Reset Configuration	A13	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-on-Reset Configuration	B14	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-on-Reset Configuration	A14	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-on-Reset Configuration	B15	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-on-Reset Configuration	A15	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-on-Reset Configuration	A16	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-on-Reset Configuration	A17	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-on-Reset Configuration	C19	I	OV_{DD}	1, 4
General Purpose Input/Output					
GPIO1_13/**ASLEEP**	General Purpose Input/Output	E9	O	OV_{DD}	1, 4
GPIO1_14/**RTC**	General Purpose Input/Output	F16	IO	OV_{DD}	---
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	H1	IO	DV_{DD}	---
GPIO1_16/**UART2_SOUT**/ LPUART1_SOUT/FTM4_CH0	General Purpose Input/Output	L2	IO	DV_{DD}	---
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	H2	IO	DV_{DD}	---
GPIO1_18/**UART2_SIN**/ FTM4_CH1/LPUART1_SIN	General Purpose Input/Output	K1	IO	DV_{DD}	---
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	General Purpose Input/Output	J2	IO	DV_{DD}	---
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	General Purpose Input/Output	L1	IO	DV_{DD}	---
GPIO1_21/**UART1_CTS_B**/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	General Purpose Input/Output	J1	IO	DV_{DD}	---
GPIO1_22/**UART2_CTS_B**/ UART4_SIN/FTM4_CH5/	General Purpose Input/Output	M2	IO	DV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LPUART1_CTS_B/ LPUART4_SIN					
GPIO1_23/**IRQ03**/FTM3_CH7/ TDMB_TSYNC/ UC3_RTSB_TXEN	General Purpose Input/Output	J3	IO	DV_{DD}	---
GPIO1_24/**IRQ04**/FTM3_CH0/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	General Purpose Input/Output	J4	IO	DV_{DD}	---
GPIO1_25/**IRQ05**/FTM3_CH1/ TDMA_RSYNC/ UC1_CTSB_RXDV	General Purpose Input/Output	J5	IO	DV_{DD}	---
GPIO1_26/**IRQ06**/FTM3_CH2/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	General Purpose Input/Output	K5	IO	DV_{DD}	---
GPIO1_27/**IRQ07**/FTM3_CH3/ TDMA_TSYNC/ UC1_RTSB_TXEN	General Purpose Input/Output	L5	IO	DV_{DD}	---
GPIO1_28/**IRQ08**/FTM3_CH4/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	General Purpose Input/Output	M5	IO	DV_{DD}	---
GPIO1_29/**IRQ09**/FTM3_CH5/ TDMB_RSYNC/ UC3_CTSB_RXDV	General Purpose Input/Output	N5	IO	DV_{DD}	---
GPIO1_30/**IRQ10**/FTM3_CH6/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	General Purpose Input/Output	P4	IO	DV_{DD}	---
GPIO1_31/**IRQ11**	General Purpose Input/Output	V5	IO	LV_{DD}	---
GPIO2_00/**SPI_CS0_B**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	T3	IO	OV_{DD}	---
GPIO2_01/**SPI_CS1_B**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	T5	IO	OV_{DD}	---
GPIO2_02/**SPI_CS2_B**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	U5	IO	OV_{DD}	---
GPIO2_03/**SPI_CS3_B**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	U3	IO	OV_{DD}	---
GPIO2_04/**SDHC_CMD**/ LPUART3_SOUT/FTM4_CH6	General Purpose Input/Output	P2	IO	EV_{DD}	---
GPIO2_05/**SDHC_DAT0**/ FTM4_CH7/LPUART3_SIN	General Purpose Input/Output	P1	IO	EV_{DD}	---
GPIO2_06/**SDHC_DAT1**/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	General Purpose Input/Output	R2	IO	EV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_07/**SDHC_DAT2**/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	General Purpose Input/Output	R1	IO	EV_{DD}	---
GPIO2_08/**SDHC_DAT3**/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	General Purpose Input/Output	T1	IO	EV_{DD}	---
GPIO2_09/**SDHC_CLK**/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	General Purpose Input/Output	P3	IO	EV_{DD}	---
GPIO2_10/**IFC_CS1_B**/ FTM7_CH0	General Purpose Input/Output	A19	IO	OV_{DD}	---
GPIO2_11/**IFC_CS2_B**/ FTM7_CH1	General Purpose Input/Output	D20	IO	OV_{DD}	---
GPIO2_12/**IFC_CS3_B**/ QSPI_B_DATA3/ FTM7_EXTCLK	General Purpose Input/Output	C20	IO	OV_{DD}	---
GPIO2_13/**IFC_PAR0**/ QSPI_B_DATA0/FTM6_CH0	General Purpose Input/Output	B18	IO	OV_{DD}	---
GPIO2_14/**IFC_PAR1**/ QSPI_B_DATA1/FTM6_CH1	General Purpose Input/Output	D17	IO	OV_{DD}	---
GPIO2_15/**IFC_PERR_B**/ QSPI_B_DATA2/ FTM6_EXTCLK	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO2_25/**IFC_A25**/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO2_26/**IFC_A26**/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	General Purpose Input/Output	D14	IO	OV_{DD}	---
GPIO2_27/**IFC_A27**/ FTM5_EXTCLK/IFC_CS6_B	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO3_00/**EMI1_MDC**	General Purpose Input/Output	Y5	IO	LV_{DD}	---
GPIO3_01/**EMI1_MDIO**	General Purpose Input/Output	W5	IO	LV_{DD}	---
GPIO3_02/**EC1_TXD3**/ FTM1_CH5	General Purpose Input/Output	V3	IO	LV_{DD}	---
GPIO3_03/**EC1_TXD2**/ FTM1_CH7	General Purpose Input/Output	V4	IO	LV_{DD}	---
GPIO3_04/**EC1_TXD1**/ FTM1_CH3	General Purpose Input/Output	W3	IO	LV_{DD}	---
GPIO3_05/**EC1_TXD0**/ FTM1_CH2	General Purpose Input/Output	Y3	IO	LV_{DD}	---
GPIO3_06/**EC1_TX_EN**/ FTM1_FAULT	General Purpose Input/Output	Y4	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_07/**EC1_GTX_CLK**/ FTM1_EXTCLK	General Purpose Input/Output	U4	IO	LV_{DD}	---
GPIO3_08/**EC1_GTX_CLK125**	General Purpose Input/Output	AA3	IO	LV_{DD}	---
GPIO3_09/**EC1_RXD3**/ FTM1_CH4	General Purpose Input/Output	U2	IO	LV_{DD}	---
GPIO3_10/**EC1_RXD2**/ FTM1_CH6	General Purpose Input/Output	V1	IO	LV_{DD}	---
GPIO3_11/**EC1_RXD1**/ FTM1_CH1	General Purpose Input/Output	W1	IO	LV_{DD}	---
GPIO3_12/**EC1_RXD0**/ FTM1_CH0	General Purpose Input/Output	W2	IO	LV_{DD}	---
GPIO3_13/**EC1_RX_CLK**/ FTM1_QD_PHA	General Purpose Input/Output	U1	IO	LV_{DD}	---
GPIO3_14/**EC1_RX_DV**/ FTM1_QD_PHB	General Purpose Input/Output	Y1	IO	LV_{DD}	---
GPIO3_15/**EC2_TXD3**/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	General Purpose Input/Output	AB3	IO	LV_{DD}	---
GPIO3_16/**EC2_TXD2**/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	General Purpose Input/Output	AC3	IO	LV_{DD}	---
GPIO3_17/**EC2_TXD1**/ TSEC_1588_CLK_OUT/ FTM2_CH3	General Purpose Input/Output	AC4	IO	LV_{DD}	---
GPIO3_18/**EC2_TXD0**/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	General Purpose Input/Output	AD3	IO	LV_{DD}	---
GPIO3_19/**EC2_TX_EN**/ FTM2_FAULT	General Purpose Input/Output	AE3	IO	LV_{DD}	---
GPIO3_20/**EC2_GTX_CLK**/ FTM2_EXTCLK	General Purpose Input/Output	AA4	IO	LV_{DD}	---
GPIO3_21/**EC2_GTX_CLK125**	General Purpose Input/Output	AE4	IO	LV_{DD}	---
GPIO3_22/**EC2_RXD3**/ FTM2_CH4	General Purpose Input/Output	AA2	IO	LV_{DD}	---
GPIO3_23/**EC2_RXD2**/ FTM2_CH6	General Purpose Input/Output	AB1	IO	LV_{DD}	---
GPIO3_24/**EC2_RXD1**/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	General Purpose Input/Output	AC1	IO	LV_{DD}	---
GPIO3_25/**EC2_RXD0**/ TSEC_1588_TRIG_IN2/ FTM2_CH0	General Purpose Input/Output	AC2	IO	LV_{DD}	---
GPIO3_26/**EC2_RX_CLK**/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	General Purpose Input/Output	AA1	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_27/**EC2_RX_DV**/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	General Purpose Input/Output	AD2	IO	LV_{DD}	---
GPIO4_00/**EMI2_MDC**	General Purpose Input/Output	Y6	IO	TV_{DD}	---
GPIO4_01/**EMI2_MDIO**	General Purpose Input/Output	W6	IO	TV_{DD}	---
GPIO4_02/**IIC2_SCL**/ SDHC_CD_B/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	General Purpose Input/Output	K3	IO	DV_{DD}	---
GPIO4_03/**IIC2_SDA**/ SDHC_WP/FTM3_QD_PHB/ CLK10/QE_SI1_STROBE1/ BRGO3	General Purpose Input/Output	L3	IO	DV_{DD}	---
GPIO4_10/**IIC3_SCL**/EVT5_B/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	General Purpose Input/Output	L4	IO	DV_{DD}	---
GPIO4_11/**IIC3_SDA**/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	General Purpose Input/Output	M4	IO	DV_{DD}	---
GPIO4_12/**IIC4_SCL**/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	General Purpose Input/Output	M3	IO	DV_{DD}	---
GPIO4_13/**IIC4_SDA**/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	General Purpose Input/Output	N3	IO	DV_{DD}	---
GPIO4_29/**USB_DRVVBUS**	General Purpose Input/Output	H6	IO	DV_{DD}	---
GPIO4_30/**USB_PWRFAULT**	General Purpose Input/Output	G6	IO	DV_{DD}	---
Frequency Timer Module 1					
FTM1_CH0/**EC1_RXD0**/ GPIO3_12	Channel 0	W2	IO	LV_{DD}	---
FTM1_CH1/**EC1_RXD1**/ GPIO3_11	Channel 1	W1	IO	LV_{DD}	---
FTM1_CH2/**EC1_TXD0**/ GPIO3_05	Channel 2	Y3	IO	LV_{DD}	---
FTM1_CH3/**EC1_TXD1**/ GPIO3_04	Channel 3	W3	IO	LV_{DD}	---
FTM1_CH4/**EC1_RXD3**/ GPIO3_09	Channel 4	U2	IO	LV_{DD}	---
FTM1_CH5/**EC1_TXD3**/ GPIO3_02	Channel 5	V3	IO	LV_{DD}	---
FTM1_CH6/**EC1_RXD2**/ GPIO3_10	Channel 6	V1	IO	LV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM1_CH7/**EC1_TXD2**/GPIO3_03	Channel 7	V4	IO	LV_{DD}	---
FTM1_EXTCLK/**EC1_GTX_CLK**/GPIO3_07	Ext Clock	U4	I	LV_{DD}	1
FTM1_FAULT/**EC1_TX_EN**/GPIO3_06	Fault	Y4	I	LV_{DD}	1
FTM1_QD_PHA/**EC1_RX_CLK**/GPIO3_13	Phase A	U1	I	LV_{DD}	1
FTM1_QD_PHB/**EC1_RX_DV**/GPIO3_14	Phase B	Y1	I	LV_{DD}	1
Frequency Timer Module 2					
FTM2_CH0/**EC2_RXD0**/GPIO3_25/TSEC_1588_TRIG_IN2	Channel 0	AC2	IO	LV_{DD}	---
FTM2_CH1/**EC2_RXD1**/GPIO3_24/TSEC_1588_PULSE_OUT1	Channel 1	AC1	IO	LV_{DD}	---
FTM2_CH2/**EC2_TXD0**/GPIO3_18/TSEC_1588_PULSE_OUT2	Channel 2	AD3	IO	LV_{DD}	---
FTM2_CH3/**EC2_TXD1**/GPIO3_17/TSEC_1588_CLK_OUT	Channel 3	AC4	IO	LV_{DD}	---
FTM2_CH4/**EC2_RXD3**/GPIO3_22	Channel 4	AA2	IO	LV_{DD}	---
FTM2_CH5/**EC2_TXD3**/GPIO3_15/TSEC_1588_ALARM_OUT2	Channel 5	AB3	IO	LV_{DD}	---
FTM2_CH6/**EC2_RXD2**/GPIO3_23	Channel 6	AB1	IO	LV_{DD}	---
FTM2_CH7/**EC2_TXD2**/GPIO3_16/TSEC_1588_ALARM_OUT1	Channel 7	AC3	IO	LV_{DD}	---
FTM2_EXTCLK/**EC2_GTX_CLK**/GPIO3_20	Ext Clock	AA4	I	LV_{DD}	1
FTM2_FAULT/**EC2_TX_EN**/GPIO3_19	Fault	AE3	I	LV_{DD}	1
FTM2_QD_PHA/**EC2_RX_CLK**/GPIO3_26/TSEC_1588_CLK_IN	Phase A	AA1	I	LV_{DD}	1
FTM2_QD_PHB/**EC2_RX_DV**/GPIO3_27/TSEC_1588_TRIG_IN1	Phase B	AD2	I	LV_{DD}	1
Frequency Timer Module 3					

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM3_CH0/**IRQ04**/GPIO1_24/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	Channel 0	J4	IO	DV_{DD}	---
FTM3_CH1/**IRQ05**/GPIO1_25/ TDMA_RSYNC/ UC1_CTSB_RXDV	Channel 1	J5	IO	DV_{DD}	---
FTM3_CH2/**IRQ06**/GPIO1_26/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	Channel 2	K5	IO	DV_{DD}	---
FTM3_CH3/**IRQ07**/GPIO1_27/ TDMA_TSYNC/ UC1_RTSB_TXEN	Channel 3	L5	IO	DV_{DD}	---
FTM3_CH4/**IRQ08**/GPIO1_28/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	Channel 4	M5	IO	DV_{DD}	---
FTM3_CH5/**IRQ09**/GPIO1_29/ TDMB_RSYNC/ UC3_CTSB_RXDV	Channel 5	N5	IO	DV_{DD}	---
FTM3_CH6/**IRQ10**/GPIO1_30/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	Channel 6	P4	IO	DV_{DD}	---
FTM3_CH7/**IRQ03**/GPIO1_23/ TDMB_TSYNC/ UC3_RTSB_TXEN	Channel 7	J3	IO	DV_{DD}	---
FTM3_EXTCLK/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/UC3_CDB_RXER	Ext Clock	N3	I	DV_{DD}	1
FTM3_FAULT/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ UC1_CDB_RXER	Fault	M3	I	DV_{DD}	1
FTM3_QD_PHA/**IIC2_SCL**/ GPIO4_02/SDHC_CD_B/ CLK9/QE_SI1_STROBE0/ BRGO2	Phase A	K3	I	DV_{DD}	1
FTM3_QD_PHB/**IIC2_SDA**/ GPIO4_03/SDHC_WP/CLK10/ QE_SI1_STROBE1/BRGO3	Phase B	L3	I	DV_{DD}	1
Frequency Timer Module 4					
FTM4_CH0/**UART2_SOUT**/ GPIO1_16/LPUART1_SOUT	Channel 0	L2	IO	DV_{DD}	---
FTM4_CH1/**UART2_SIN**/ GPIO1_18/LPUART1_SIN	Channel 1	K1	IO	DV_{DD}	---
FTM4_CH2/**UART1_RTS_B**/ GPIO1_19/UART3_SOUT/ LPUART2_SOUT	Channel 2	J2	IO	DV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM4_CH3/**UART2_RTS_B**/ GPIO1_20/UART4_SOUT/ LPUART4_SOUT/ LPUART1_RTS_B	Channel 3	L1	IO	DV_{DD}	---
FTM4_CH4/**UART1_CTS_B**/ GPIO1_21/UART3_SIN/ LPUART2_SIN	Channel 4	J1	IO	DV_{DD}	---
FTM4_CH5/**UART2_CTS_B**/ GPIO1_22/UART4_SIN/ LPUART1_CTS_B/ LPUART4_SIN	Channel 5	M2	IO	DV_{DD}	---
FTM4_CH6/**SDHC_CMD**/ GPIO2_04/LPUART3_SOUT	Channel 6	P2	IO	EV_{DD}	---
FTM4_CH7/**SDHC_DAT0**/ GPIO2_05/LPUART3_SIN	Channel 7	P1	IO	EV_{DD}	---
FTM4_EXTCLK/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ LPUART5_SIN	Ext Clock	R1	I	EV_{DD}	1
FTM4_FAULT/**SDHC_DAT1**/ GPIO2_06/LPUART5_SOUT/ LPUART2_RTS_B	Fault	R2	I	EV_{DD}	1
FTM4_QD_PHA/**SDHC_DAT3**/ GPIO2_08/LPUART6_SOUT/ LPUART3_RTS_B	Phase A	T1	I	EV_{DD}	1
FTM4_QD_PHB/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ LPUART6_SIN	Phase B	P3	I	EV_{DD}	1
Frequency Timer Module 5					
FTM5_CH0/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ IFC_CS4_B/IFC_RB2_B	Channel 0	C13	IO	OV_{DD}	---
FTM5_CH1/**IFC_A26**/ GPIO2_26/IFC_CS5_B/ IFC_RB3_B	Channel 1	D14	IO	OV_{DD}	---
FTM5_EXTCLK/**IFC_A27**/ GPIO2_27/IFC_CS6_B	Ext Clock	C14	I	OV_{DD}	1
Frequency Timer Module 6					
FTM6_CH0/**IFC_PAR0**/ GPIO2_13/QSPI_B_DATA0	Channel 0	B18	IO	OV_{DD}	---
FTM6_CH1/**IFC_PAR1**/ GPIO2_14/QSPI_B_DATA1	Channel 1	D17	IO	OV_{DD}	---
FTM6_EXTCLK/**IFC_PERR_B**/ GPIO2_15/QSPI_B_DATA2	Ext Clock	E17	I	OV_{DD}	1
Frequency Timer Module 7					
FTM7_CH0/**IFC_CS1_B**/ GPIO2_10	Channel 0	A19	IO	OV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM7_CH1/**IFC_CS2_B**/GPIO2_11	Channel 1	D20	IO	OV_{DD}	---
FTM7_EXTCLK/**IFC_CS3_B**/GPIO2_12/QSPI_B_DATA3	Ext Clock	C20	I	OV_{DD}	1
Frequency Timer Module 8					
FTM8_CH0/**IIC3_SCL**/GPIO4_10/EVT5_B/USB2_DRVVBUS/BRGO4/CLK11	Channel 0	L4	IO	DV_{DD}	---
FTM8_CH1/**IIC3_SDA**/GPIO4_11/EVT6_B/USB2_PWRFAULT/BRGO1/CLK12_CLK8	Channel 1	M4	IO	DV_{DD}	---
LPUART					
LPUART1_CTS_B/**UART2_CTS_B**/GPIO1_22/UART4_SIN/FTM4_CH5/LPUART4_SIN	Clear to send	M2	I	DV_{DD}	1
LPUART1_RTS_B/**UART2_RTS_B**/GPIO1_20/UART4_SOUT/LPUART4_SOUT/FTM4_CH3	Request to send	L1	O	DV_{DD}	1
LPUART1_SIN/**UART2_SIN**/GPIO1_18/FTM4_CH1	Receive data	K1	I	DV_{DD}	1
LPUART1_SOUT/**UART2_SOUT**/GPIO1_16/FTM4_CH0	Transmit data	L2	IO	DV_{DD}	---
LPUART2_CTS_B/**SDHC_DAT2**/GPIO2_07/LPUART5_SIN/FTM4_EXTCLK	Clear to send	R1	I	EV_{DD}	1
LPUART2_RTS_B/**SDHC_DAT1**/GPIO2_06/LPUART5_SOUT/FTM4_FAULT	Request to send	R2	O	EV_{DD}	1
LPUART2_SIN/**UART1_CTS_B**/GPIO1_21/UART3_SIN/FTM4_CH4	Receive data	J1	I	DV_{DD}	1
LPUART2_SOUT/**UART1_RTS_B**/GPIO1_19/UART3_SOUT/FTM4_CH2	Transmit data	J2	IO	DV_{DD}	---
LPUART3_CTS_B/**SDHC_CLK**/GPIO2_09/LPUART6_SIN/FTM4_QD_PHB	Clear to send	P3	I	EV_{DD}	1
LPUART3_RTS_B/**SDHC_DAT3**/GPIO2_08/	Request to send	T1	O	EV_{DD}	1

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LPUART6_SOUT/ FTM4_QD_PHA					
LPUART3_SIN/**SDHC_DAT0**/ GPIO2_05/FTM4_CH7	Receive data	P1	I	EV_{DD}	1
LPUART3_SOUT/ **SDHC_CMD**/GPIO2_04/ FTM4_CH6	Transmit data	P2	IO	EV_{DD}	---
LPUART4_SIN/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B	Receive data	M2	I	DV_{DD}	1
LPUART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit data	L1	IO	DV_{DD}	---
LPUART5_SIN/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ FTM4_EXTCLK	Receive data	R1	I	EV_{DD}	1
LPUART5_SOUT/ **SDHC_DAT1**/GPIO2_06/ FTM4_FAULT/ LPUART2_RTS_B	Transmit data	R2	IO	EV_{DD}	---
LPUART6_SIN/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ FTM4_QD_PHB	Receive data	P3	I	EV_{DD}	1
LPUART6_SOUT/ **SDHC_DAT3**/GPIO2_08/ FTM4_QD_PHA/ LPUART3_RTS_B	Transmit data	T1	IO	EV_{DD}	---
QUICC Engine					
CLK10/**IIC2_SDA**/GPIO4_03/ SDHC_WP/FTM3_QD_PHB/ QE_SI1_STROBE1/BRGO3	QE clock	L3	I	DV_{DD}	1
CLK11/**IIC3_SCL**/GPIO4_10/ EVT5_B/USB2_DRVVBUS/ BRGO4/FTM8_CH0	QE clock	L4	I	DV_{DD}	1
CLK12_CLK8/**IIC3_SDA**/ GPIO4_11/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1	QE clock	M4	I	DV_{DD}	1
CLK9/**IIC2_SCL**/GPIO4_02/ SDHC_CD_B/FTM3_QD_PHA/ QE_SI1_STROBE0/BRGO2	QE clock	K3	I	DV_{DD}	1
QE_SI1_STROBE0/**IIC2_SCL**/ GPIO4_02/SDHC_CD_B/ FTM3_QD_PHA/CLK9/BRGO2	SI strobe	K3	O	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QE_SI1_STROBE1/**IIC2_SDA**/GPIO4_03/SDHC_WP/FTM3_QD_PHB/CLK10/BRGO3	SI strobe	L3	O	DV_{DD}	1
UC1_CDB_RXER/**IIC4_SCL**/GPIO4_12/EVT7_B/USB3_DRVVBUS/TDMA_RQ/FTM3_FAULT	Receive error	M3	I	DV_{DD}	1
UC1_CTSB_RXDV/**IRQ05**/GPIO1_25/FTM3_CH1/TDMA_RSYNC	Receive data	J5	I	DV_{DD}	1
UC1_RTSB_TXEN/**IRQ07**/GPIO1_27/FTM3_CH3/TDMA_TSYNC	Transmit enable	L5	O	DV_{DD}	1
UC1_RXD7/**IRQ04**/GPIO1_24/FTM3_CH0/TDMA_RXD/TDMA_TXD	Receive data	J4	I	DV_{DD}	1
UC1_TXD7/**IRQ06**/GPIO1_26/FTM3_CH2/TDMA_RXD_EXC/TDMA_TXD	Transmit data	K5	O	DV_{DD}	1
UC3_CDB_RXER/**IIC4_SDA**/GPIO4_13/EVT8_B/USB3_PWRFAULT/TDMB_RQ/FTM3_EXTCLK	Receive error	N3	I	DV_{DD}	1
UC3_CTSB_RXDV/**IRQ09**/GPIO1_29/FTM3_CH5/TDMB_RSYNC	Receive data	N5	I	DV_{DD}	1
UC3_RTSB_TXEN/**IRQ03**/GPIO1_23/FTM3_CH7/TDMB_TSYNC	Transmit enable	J3	O	DV_{DD}	1
UC3_RXD7/**IRQ08**/GPIO1_28/FTM3_CH4/TDMB_RXD/TDMB_TXD	Receive data	M5	I	DV_{DD}	1
UC3_TXD7/**IRQ10**/GPIO1_30/FTM3_CH6/TDMB_RXD_EXC/TDMB_TXD	Transmit data	P4	O	DV_{DD}	1
Baud rate generator					
BRGO1/**IIC3_SDA**/GPIO4_11/EVT6_B/USB2_PWRFAULT/FTM8_CH1/CLK12_CLK8	Baud Rate Generator 1	M4	O	DV_{DD}	1
BRGO2/**IIC2_SCL**/GPIO4_02/SDHC_CD_B/FTM3_QD_PHA/CLK9/QE_SI1_STROBE0	Baud Rate Generator 2	K3	O	DV_{DD}	1
BRGO3/**IIC2_SDA**/GPIO4_03/SDHC_WP/FTM3_QD_PHB/CLK10/QE_SI1_STROBE1	Baud Rate Generator 3	L3	O	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
BRGO4/**IIC3_SCL**/GPIO4_10/ EVT5_B/USB2_DRVVBUS/ FTM8_CH0/CLK11	Baud Rate Generator 4	L4	O	DV_{DD}	1
Time Division Multiplexing					
TDMA_RQ/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT/ UC1_CDB_RXER	RQ	M3	O	DV_{DD}	1
TDMA_RSYNC/**IRQ05**/ GPIO1_25/FTM3_CH1/ UC1_CTSB_RXDV	RSYNC	J5	I	DV_{DD}	1
TDMA_RXD/**IRQ04**/ GPIO1_24/FTM3_CH0/ UC1_RXD7/TDMA_TXD	RXD	J4	I	DV_{DD}	1
TDMA_RXD_EXC/**IRQ06**/ GPIO1_26/FTM3_CH2/ TDMA_TXD/UC1_TXD7	Recieve Data	K5	I	DV_{DD}	1
TDMA_TSYNC/**IRQ07**/ GPIO1_27/FTM3_CH3/ UC1_RTSB_TXEN	TSYNC	L5	I	DV_{DD}	1
TDMA_TXD/**IRQ04**/GPIO1_24/ FTM3_CH0/TDMA_RXD/ UC1_RXD7	Transmit Data	J4	O	DV_{DD}	1
TDMA_TXD/**IRQ06**/GPIO1_26/ FTM3_CH2/TDMA_RXD_EXC/ UC1_TXD7	Transmit Data	K5	O	DV_{DD}	1
TDMB_RQ/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK/ UC3_CDB_RXER	RQ	N3	O	DV_{DD}	1
TDMB_RSYNC/**IRQ09**/ GPIO1_29/FTM3_CH5/ UC3_CTSB_RXDV	RSYNC	N5	I	DV_{DD}	1
TDMB_RXD/**IRQ08**/ GPIO1_28/FTM3_CH4/ UC3_RXD7/TDMB_TXD	RXD	M5	I	DV_{DD}	1
TDMB_RXD_EXC/**IRQ10**/ GPIO1_30/FTM3_CH6/ TDMB_TXD/UC3_TXD7	Recieve Data	P4	I	DV_{DD}	1
TDMB_TSYNC/**IRQ03**/ GPIO1_23/FTM3_CH7/ UC3_RTSB_TXEN	TSYNC	J3	I	DV_{DD}	1
TDMB_TXD/**IRQ08**/GPIO1_28/ FTM3_CH4/TDMB_RXD/ UC3_RXD7	Transmit Data	M5	O	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TDMB_TXD/**IRQ10**/GPIO1_30/ FTM3_CH6/TDMB_RXD_EXC/ UC3_TXD7	Transmit Data	P4	O	DV_{DD}	1
TSEC_1588					
TSEC_1588_ALARM_OUT1/ **EC2_TXD2**/GPIO3_16/ FTM2_CH7	Alarm Out	AC3	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3**/GPIO3_15/ FTM2_CH5	Alarm Out	AB3	O	LV_{DD}	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK**/GPIO3_26/ FTM2_QD_PHA	Clock In	AA1	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ **EC2_TXD1**/GPIO3_17/ FTM2_CH3	Clock Out	AC4	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1**/GPIO3_24/ FTM2_CH1	Pulse Out	AC1	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0**/GPIO3_18/ FTM2_CH2	Pulse Out	AD3	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV**/GPIO3_27/ FTM2_QD_PHB	Trigger In	AD2	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0**/GPIO3_25/ FTM2_CH0	Trigger In	AC2	I	LV_{DD}	1
QSPI					
QSPI_A_CS0/**IFC_A16**	Chip Select	D8	O	OV_{DD}	1
QSPI_A_CS1/**IFC_A17**	Chip Select	C8	O	OV_{DD}	1
QSPI_A_DATA0/**IFC_A22**/ IFC_WP1_B	Data	D11	IO	OV_{DD}	---
QSPI_A_DATA1/**IFC_A23**/ IFC_WP2_B	Data	C12	IO	OV_{DD}	---
QSPI_A_DATA2/**IFC_A24**/ IFC_WP3_B	Data	D13	IO	OV_{DD}	---
QSPI_A_DATA3/**IFC_A25**/ GPIO2_25/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	Data	C13	IO	OV_{DD}	---
QSPI_A_SCK/**IFC_A18**	QSPI_A Clock	C9	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A19**	Chip Select	D10	O	OV_{DD}	1
QSPI_B_CS1/**IFC_A20**	Chip Select	C10	O	OV_{DD}	1
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_13/FTM6_CH0	Data	B18	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QSPI_B_DATA1/**IFC_PAR1**/GPIO2_14/FTM6_CH1	Data	D17	IO	OV_{DD}	---
QSPI_B_DATA2/**IFC_PERR_B**/GPIO2_15/FTM6_EXTCLK	Data	E17	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/GPIO2_12/FTM7_EXTCLK	Data	C20	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/GPIO2_12/FTM7_EXTCLK	Data	C20	IO	OV_{DD}	---
QSPI_B_SCK/**IFC_A21**/cfg_dram_type	QSPI_B Clock	C11	O	OV_{DD}	1, 4
Power and Ground Signals					
GND001	GND	A2	---	---	---
GND002	GND	A5	---	---	---
GND003	GND	A24	---	---	---
GND004	GND	B3	---	---	---
GND005	GND	B4	---	---	---
GND006	GND	B7	---	---	---
GND007	GND	B10	---	---	---
GND008	GND	B13	---	---	---
GND009	GND	B16	---	---	---
GND010	GND	B19	---	---	---
GND011	GND	B21	---	---	---
GND012	GND	B25	---	---	---
GND013	GND	C1	---	---	---
GND014	GND	C2	---	---	---
GND015	GND	C5	---	---	---
GND016	GND	C23	---	---	---
GND017	GND	D3	---	---	---
GND018	GND	D4	---	---	---
GND019	GND	D7	---	---	---
GND020	GND	D9	---	---	---
GND021	GND	D12	---	---	---
GND022	GND	D15	---	---	---
GND023	GND	D18	---	---	---
GND024	GND	D21	---	---	---
GND025	GND	E1	---	---	---
GND026	GND	E2	---	---	---
GND027	GND	E5	---	---	---
GND028	GND	E22	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND029	GND	E24	---	---	---
GND030	GND	F3	---	---	---
GND031	GND	F4	---	---	---
GND032	GND	F7	---	---	---
GND033	GND	F8	---	---	---
GND034	GND	F11	---	---	---
GND035	GND	F12	---	---	---
GND036	GND	F13	---	---	---
GND037	GND	F17	---	---	---
GND038	GND	F20	---	---	---
GND039	GND	G1	---	---	---
GND040	GND	G2	---	---	---
GND041	GND	G22	---	---	---
GND042	GND	G24	---	---	---
GND043	GND	H3	---	---	---
GND044	GND	H4	---	---	---
GND045	GND	H5	---	---	---
GND046	GND	H8	---	---	---
GND047	GND	H9	---	---	---
GND048	GND	H10	---	---	---
GND049	GND	H11	---	---	---
GND050	GND	H12	---	---	---
GND051	GND	H13	---	---	---
GND052	GND	H14	---	---	---
GND053	GND	H15	---	---	---
GND054	GND	H16	---	---	---
GND055	GND	H17	---	---	---
GND056	GND	J7	---	---	---
GND057	GND	J19	---	---	---
GND058	GND	J20	---	---	---
GND059	GND	J24	---	---	---
GND060	GND	K2	---	---	---
GND061	GND	K4	---	---	---
GND062	GND	K7	---	---	---
GND063	GND	K10	---	---	---
GND064	GND	K12	---	---	---
GND065	GND	K14	---	---	---
GND066	GND	K16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND067	GND	K19	---	---	---
GND068	GND	K22	---	---	---
GND069	GND	L7	---	---	---
GND070	GND	L9	---	---	---
GND071	GND	L11	---	---	---
GND072	GND	L13	---	---	---
GND073	GND	L15	---	---	---
GND074	GND	L17	---	---	---
GND075	GND	L19	---	---	---
GND076	GND	L20	---	---	---
GND077	GND	L24	---	---	---
GND078	GND	M7	---	---	---
GND079	GND	M10	---	---	---
GND080	GND	M12	---	---	---
GND081	GND	M14	---	---	---
GND082	GND	M16	---	---	---
GND083	GND	M19	---	---	---
GND084	GND	M22	---	---	---
GND085	GND	N2	---	---	---
GND086	GND	N4	---	---	---
GND087	GND	N6	---	---	---
GND088	GND	N9	---	---	---
GND089	GND	N11	---	---	---
GND090	GND	N13	---	---	---
GND091	GND	N15	---	---	---
GND092	GND	N17	---	---	---
GND093	GND	N19	---	---	---
GND094	GND	N20	---	---	---
GND095	GND	P7	---	---	---
GND096	GND	P8	---	---	---
GND097	GND	P10	---	---	---
GND098	GND	P12	---	---	---
GND099	GND	P14	---	---	---
GND100	GND	P16	---	---	---
GND101	GND	P19	---	---	---
GND102	GND	P22	---	---	---
GND103	GND	P24	---	---	---
GND104	GND	R9	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND105	GND	R11	---	---	---
GND106	GND	R13	---	---	---
GND107	GND	R15	---	---	---
GND108	GND	R17	---	---	---
GND109	GND	R19	---	---	---
GND110	GND	R25	---	---	---
GND111	GND	T2	---	---	---
GND112	GND	T4	---	---	---
GND113	GND	T8	---	---	---
GND114	GND	T10	---	---	---
GND115	GND	T12	---	---	---
GND116	GND	T14	---	---	---
GND117	GND	T20	---	---	---
GND118	GND	U6	---	---	---
GND119	GND	U9	---	---	---
GND120	GND	U11	---	---	---
GND121	GND	U20	---	---	---
GND122	GND	V2	---	---	---
GND123	GND	V8	---	---	---
GND124	GND	V9	---	---	---
GND125	GND	V10	---	---	---
GND126	GND	V11	---	---	---
GND127	GND	V12	---	---	---
GND128	GND	V13	---	---	---
GND129	GND	V14	---	---	---
GND130	GND	V20	---	---	---
GND131	GND	W4	---	---	---
GND132	GND	W20	---	---	---
GND133	GND	Y2	---	---	---
GND134	GND	Y20	---	---	---
GND135	GND	AB2	---	---	---
GND136	GND	AB4	---	---	---
GND137	GND	AD1	---	---	---
GND138	GND	AD4	---	---	---
GND139	GND	AE2	---	---	---
SD_GND01	Serdes core logic GND	U15	---	---	34
SD_GND02	Serdes core logic GND	U16	---	---	34
SD_GND03	Serdes core logic GND	U17	---	---	34

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND04	Serdes core logic GND	U18	---	---	34
SD_GND05	Serdes core logic GND	U19	---	---	34
SD_GND06	Serdes core logic GND	W8	---	---	34
SD_GND07	Serdes core logic GND	W11	---	---	34
SD_GND08	Serdes core logic GND	Y8	---	---	34
SD_GND09	Serdes core logic GND	Y9	---	---	34
SD_GND10	Serdes core logic GND	Y10	---	---	34
SD_GND11	Serdes core logic GND	Y11	---	---	34
SD_GND12	Serdes core logic GND	Y12	---	---	34
SD_GND13	Serdes core logic GND	Y14	---	---	34
SD_GND14	Serdes core logic GND	Y15	---	---	34
SD_GND15	Serdes core logic GND	Y16	---	---	34
SD_GND16	Serdes core logic GND	Y17	---	---	34
SD_GND17	Serdes core logic GND	Y18	---	---	34
SD_GND18	Serdes core logic GND	AA13	---	---	34
SD_GND19	Serdes core logic GND	AA16	---	---	34
SD_GND20	Serdes core logic GND	AA19	---	---	34
SD_GND21	Serdes core logic GND	AB13	---	---	34
SD_GND22	Serdes core logic GND	AB16	---	---	34
SD_GND23	Serdes core logic GND	AB19	---	---	34
SD_GND24	Serdes core logic GND	AC13	---	---	34
SD_GND25	Serdes core logic GND	AC14	---	---	34
SD_GND26	Serdes core logic GND	AC15	---	---	34
SD_GND27	Serdes core logic GND	AC16	---	---	34
SD_GND28	Serdes core logic GND	AC17	---	---	34
SD_GND29	Serdes core logic GND	AC18	---	---	34
SD_GND30	Serdes core logic GND	AC19	---	---	34
SD_GND31	Serdes core logic GND	AC20	---	---	34
SD_GND32	Serdes core logic GND	AD13	---	---	34
SD_GND33	Serdes core logic GND	AD16	---	---	34
SD_GND34	Serdes core logic GND	AD19	---	---	34
SD_GND35	Serdes core logic GND	AD21	---	---	34
SD_GND36	Serdes core logic GND	AE13	---	---	34
SD_GND37	Serdes core logic GND	AE16	---	---	34
SD_GND38	Serdes core logic GND	AE19	---	---	34
SD_GND39	Serdes core logic GND	AE21	---	---	34
SENSEGND	GND Sense pin	V7	---	---	---
OVDD1	General I/O supply	J12	---	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
OVDD2	General I/O supply	J13	---	OV_{DD}	---
OVDD3	General I/O supply	J14	---	OV_{DD}	---
OVDD4	General I/O supply	J15	---	OV_{DD}	---
OVDD5	General I/O supply	J16	---	OV_{DD}	---
OVDD6	General I/O supply	J17	---	OV_{DD}	---
OVDD7	General I/O supply	N7	---	OV_{DD}	---
DVDD1	UART/I2C/QE supply - switchable	K8	---	DV_{DD}	---
DVDD2	UART/I2C/QE supply - switchable	L8	---	DV_{DD}	---
EVDD	eSDHC supply - switchable	M8	---	EV_{DD}	---
LVDD1	Ethernet controller 1 & 2 supply	U12	---	LV_{DD}	---
LVDD2	Ethernet controller 1 & 2 supply	U13	---	LV_{DD}	---
LVDD3	Ethernet controller 1 & 2 supply	U14	---	LV_{DD}	---
TVDD	1.2V/LVDD supply for MDIO interface for 10G Fman (EC2)	V6	---	TV_{DD}	---
G1VDD01	DDR supply	J18	---	$G1V_{DD}$	---
G1VDD02	DDR supply	K18	---	$G1V_{DD}$	---
G1VDD03	DDR supply	K20	---	$G1V_{DD}$	---
G1VDD04	DDR supply	L18	---	$G1V_{DD}$	---
G1VDD05	DDR supply	M18	---	$G1V_{DD}$	---
G1VDD06	DDR supply	M20	---	$G1V_{DD}$	---
G1VDD07	DDR supply	N18	---	$G1V_{DD}$	---
G1VDD08	DDR supply	P18	---	$G1V_{DD}$	---
G1VDD09	DDR supply	P20	---	$G1V_{DD}$	---
G1VDD10	DDR supply	R21	---	$G1V_{DD}$	---
G1VDD11	DDR supply	R23	---	$G1V_{DD}$	---
G1VDD12	DDR supply	T22	---	$G1V_{DD}$	---
G1VDD13	DDR supply	T24	---	$G1V_{DD}$	---
G1VDD14	DDR supply	V22	---	$G1V_{DD}$	---
G1VDD15	DDR supply	V24	---	$G1V_{DD}$	---
G1VDD16	DDR supply	Y22	---	$G1V_{DD}$	---
G1VDD17	DDR supply	Y24	---	$G1V_{DD}$	---
G1VDD18	DDR supply	AA20	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AB22	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AB24	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AD22	---	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD22	DDR supply	AD25	---	$G1V_{DD}$	---
G1VDD23	DDR supply	AE24	---	$G1V_{DD}$	---
S1VDD1	SerDes1 core logic supply	T15	---	$S1V_{DD}$	---
S1VDD2	SerDes1 core logic supply	T16	---	$S1V_{DD}$	---
S1VDD3	SerDes1 core logic supply	T17	---	$S1V_{DD}$	---
S1VDD4	SerDes1 core logic supply	T18	---	$S1V_{DD}$	---
S1VDD5	SerDes1 core logic supply	W14	---	$S1V_{DD}$	---
X1VDD1	SerDes1 transceiver supply	W15	---	$X1V_{DD}$	---
X1VDD2	SerDes1 transceiver supply	W16	---	$X1V_{DD}$	---
X1VDD3	SerDes1 transceiver supply	W17	---	$X1V_{DD}$	---
X1VDD4	SerDes1 transceiver supply	W18	---	$X1V_{DD}$	---
X1VDD5	SerDes1 transceiver supply	Y19	---	$X1V_{DD}$	---
FA_VL	Reserved	R7	---	FA_VL	15
PROG_MTR	Reserved	G14	---	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	F14	---	TA_PROG_SFP	31
TH_VDD	Thermal Monitor Unit supply	T6	---	TH_V_{DD}	32
VDD01	Supply for cores and platform	K13	---	V_{DD}	---
VDD02	Supply for cores and platform	K15	---	V_{DD}	---
VDD03	Supply for cores and platform	K17	---	V_{DD}	---
VDD04	Supply for cores and platform	L10	---	V_{DD}	---
VDD05	Supply for cores and platform	L12	---	V_{DD}	---
VDD06	Supply for cores and platform	L14	---	V_{DD}	---
VDD07	Supply for cores and platform	L16	---	V_{DD}	---
VDD08	Supply for cores and platform	M9	---	V_{DD}	---
VDD09	Supply for cores and platform	M11	---	V_{DD}	---
VDD10	Supply for cores and platform	M13	---	V_{DD}	---
VDD11	Supply for cores and platform	M15	---	V_{DD}	---
VDD12	Supply for cores and platform	M17	---	V_{DD}	---
VDD13	Supply for cores and platform	N8	---	V_{DD}	---
VDD14	Supply for cores and platform	N10	---	V_{DD}	---
VDD15	Supply for cores and platform	N12	---	V_{DD}	---
VDD16	Supply for cores and platform	N14	---	V_{DD}	---
VDD17	Supply for cores and platform	N16	---	V_{DD}	---
VDD18	Supply for cores and platform	P9	---	V_{DD}	---
VDD19	Supply for cores and platform	P11	---	V_{DD}	---
VDD20	Supply for cores and platform	P13	---	V_{DD}	---
VDD21	Supply for cores and platform	P15	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD22	Supply for cores and platform	P17	---	V_{DD}	---
VDD23	Supply for cores and platform	R8	---	V_{DD}	---
VDD24	Supply for cores and platform	R10	---	V_{DD}	---
VDD25	Supply for cores and platform	R12	---	V_{DD}	---
VDD26	Supply for cores and platform	R14	---	V_{DD}	---
VDD27	Supply for cores and platform	R16	---	V_{DD}	---
VDD28	Supply for cores and platform	R18	---	V_{DD}	---
VDD29	Supply for cores and platform	T9	---	V_{DD}	---
VDD30	Supply for cores and platform	T11	---	V_{DD}	---
VDD31	Supply for cores and platform	T13	---	V_{DD}	---
VDD32	Supply for cores and platform	U8	---	V_{DD}	---
VDD33	Supply for cores and platform	U10	---	V_{DD}	---
TA_BB_VDD	Battery Backed Security Monitor supply	H20	---	$TA\_BB\_V_{DD}$	---
AVDD_CGA1	CPU Cluster Group A PLL1 supply.	G12	---	AVDD_CGA1	30
AVDD_CGA2	CPU Cluster Group A PLL2 supply.	G11	---	AVDD_CGA2	30
AVDD_PLAT	Platform PLL supply.	G13	---	AVDD_PLAT	30
AVDD_D1	DDR1 PLL supply.	T19	---	AVDD_D1	30
AVDD_SD1_PLL1	SerDes1 PLL 1 supply.	W12	---	AVDD_SD1_PLL1	30
AVDD_SD1_PLL2	SerDes1 PLL 2 supply.	V19	---	AVDD_SD1_PLL2	30
SENSEVDD	Vdd Sense pin	W7	---	SENSEVDD	---
USB_HVDD1	3.3V High Supply	J8	---	USB_HV_{DD}	---
USB_HVDD2	3.3V High Supply	J9	---	USB_HV_{DD}	---
USB_SDVDD1	1.0 V Analog and digital HS supply	K9	---	USB_SDV_{DD}	---
USB_SDVDD2	1.0 V Analog and digital HS supply	K11	---	USB_SDV_{DD}	---
USB_SVDD1	1.0 V Analog and digital SS supply	J10	---	USB_SV_{DD}	---
USB_SVDD2	1.0 V Analog and digital SS supply	J11	---	USB_SV_{DD}	---
No Connection Pins					
NC_AA10	No Connection	AA10	---	---	12
NC_AA11	No Connection	AA11	---	---	12
NC_AA12	No Connection	AA12	---	---	12
NC_AA5	No Connection	AA5	---	---	12
NC_AA6	No Connection	AA6	---	---	12
NC_AA7	No Connection	AA7	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_AA8	No Connection	AA8	---	---	12
NC_AA9	No Connection	AA9	---	---	12
NC_AB10	No Connection	AB10	---	---	12
NC_AB11	No Connection	AB11	---	---	12
NC_AB12	No Connection	AB12	---	---	12
NC_AB5	No Connection	AB5	---	---	12
NC_AB6	No Connection	AB6	---	---	12
NC_AB7	No Connection	AB7	---	---	12
NC_AB8	No Connection	AB8	---	---	12
NC_AB9	No Connection	AB9	---	---	12
NC_AC10	No Connection	AC10	---	---	12
NC_AC11	No Connection	AC11	---	---	12
NC_AC12	No Connection	AC12	---	---	12
NC_AC5	No Connection	AC5	---	---	12
NC_AC6	No Connection	AC6	---	---	12
NC_AC7	No Connection	AC7	---	---	12
NC_AC8	No Connection	AC8	---	---	12
NC_AC9	No Connection	AC9	---	---	12
NC_AD10	No Connection	AD10	---	---	12
NC_AD11	No Connection	AD11	---	---	12
NC_AD12	No Connection	AD12	---	---	12
NC_AD5	No Connection	AD5	---	---	12
NC_AD6	No Connection	AD6	---	---	12
NC_AD7	No Connection	AD7	---	---	12
NC_AD8	No Connection	AD8	---	---	12
NC_AD9	No Connection	AD9	---	---	12
NC_AE10	No Connection	AE10	---	---	12
NC_AE11	No Connection	AE11	---	---	12
NC_AE12	No Connection	AE12	---	---	12
NC_AE5	No Connection	AE5	---	---	12
NC_AE6	No Connection	AE6	---	---	12
NC_AE7	No Connection	AE7	---	---	12
NC_AE8	No Connection	AE8	---	---	12
NC_AE9	No Connection	AE9	---	---	12
NC_K6	No Connection	K6	---	---	12
NC_L6	No Connection	L6	---	---	12
NC_M6	No Connection	M6	---	---	12
NC_Y13	No Connection	Y13	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_Y7	No Connection	Y7	---	---	12

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 200Ω pull-up to respective power-supply.

12. Do not connect. These pins should be left floating.

14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698Ω pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. This pin should be connected to ground through 2-10kΩ resistor when not used.

19. This pin should be connected to ground through 2-10kΩ resistor when SYSCLK input is used as system clock.

21. This pin has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pin should have an optional pull down resistor on board. This is required to support DIFF_SYSCLK/DIFF_SYSCLK_B.

23. This pin must be pulled to OVDD through a 100-ohm to 1k-ohm resistor for a four core LS1043A device and tied to ground for a two core LS1023A device.

25. The alternate signal in DDR4 configuration is mentioned in corresponding Reference Manual.

27. Attach 200 Ohm +/-1% 100-ppm/C precision resistor-to-ground. Voltage range 0-250mV

28. The permissible voltage range is 0 V - 5.25 V.

29. The permissible voltage range for input signal is 0 - 1.8V

30. It is measured at the input of the supply filter and not at the SoC pin.

31. Connect to ground when fuses are read-only.

32. TH_VDD must be tied to OVDD.

33. Recommend that a weak pull-down resistor (2-10 k-ohm) be placed on this pin to GND.

34. SD_GND must be directly connected to GND.

35. This pin is used for debug purposes. It is advised that boards are built with the ability to pull up and pull down this pin.

36. This pin must be pulled down to ground with a resistor of value 4.7k ohm.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

2.3 780 ball layout diagrams

This figure shows the complete view of the LS1043A_23x23 ball map diagram. Figure 9, Figure 10, Figure 11, and Figure 12 show quadrant views.

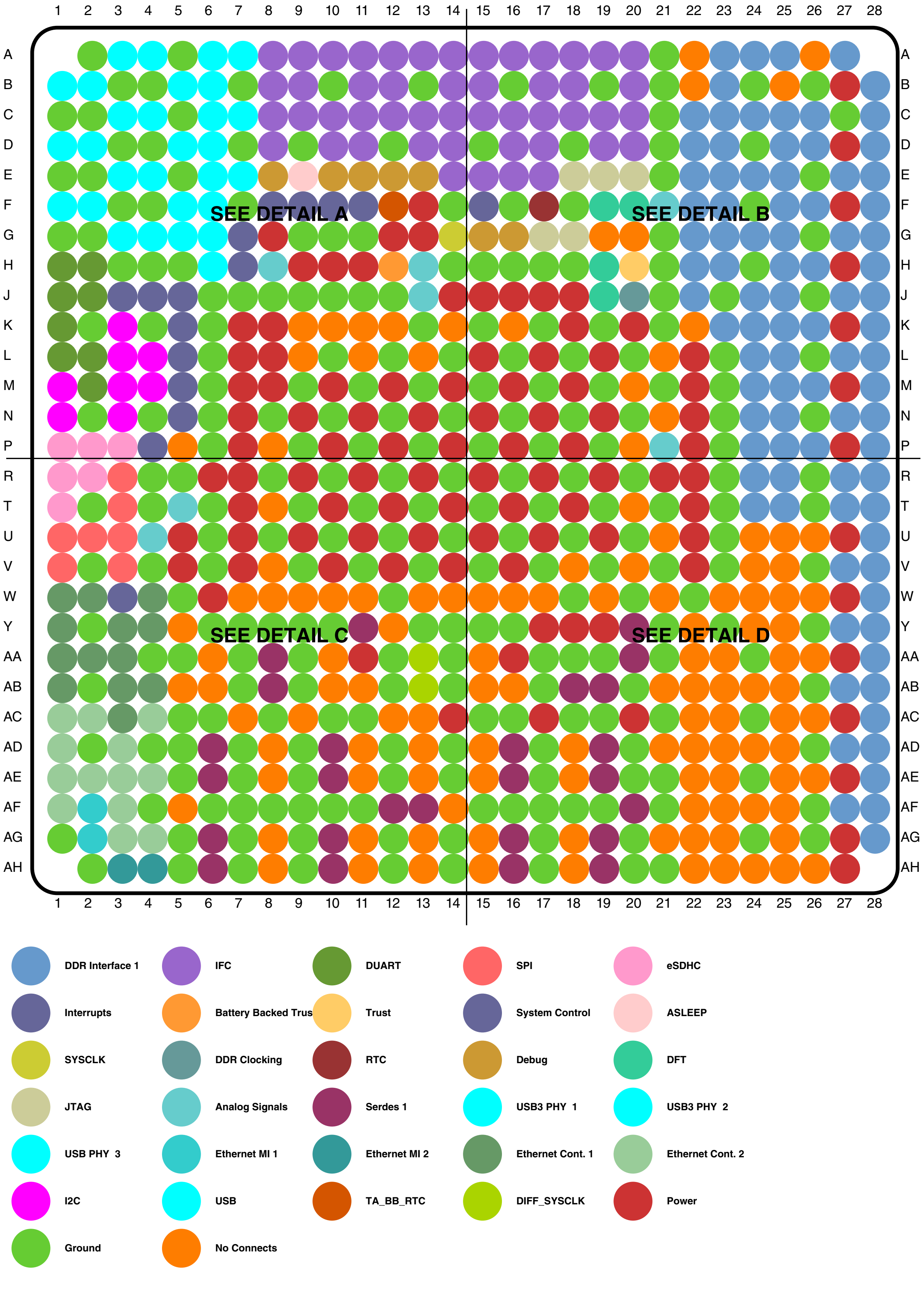

Figure 8. Complete BGA Map for the LS1043A_23x23

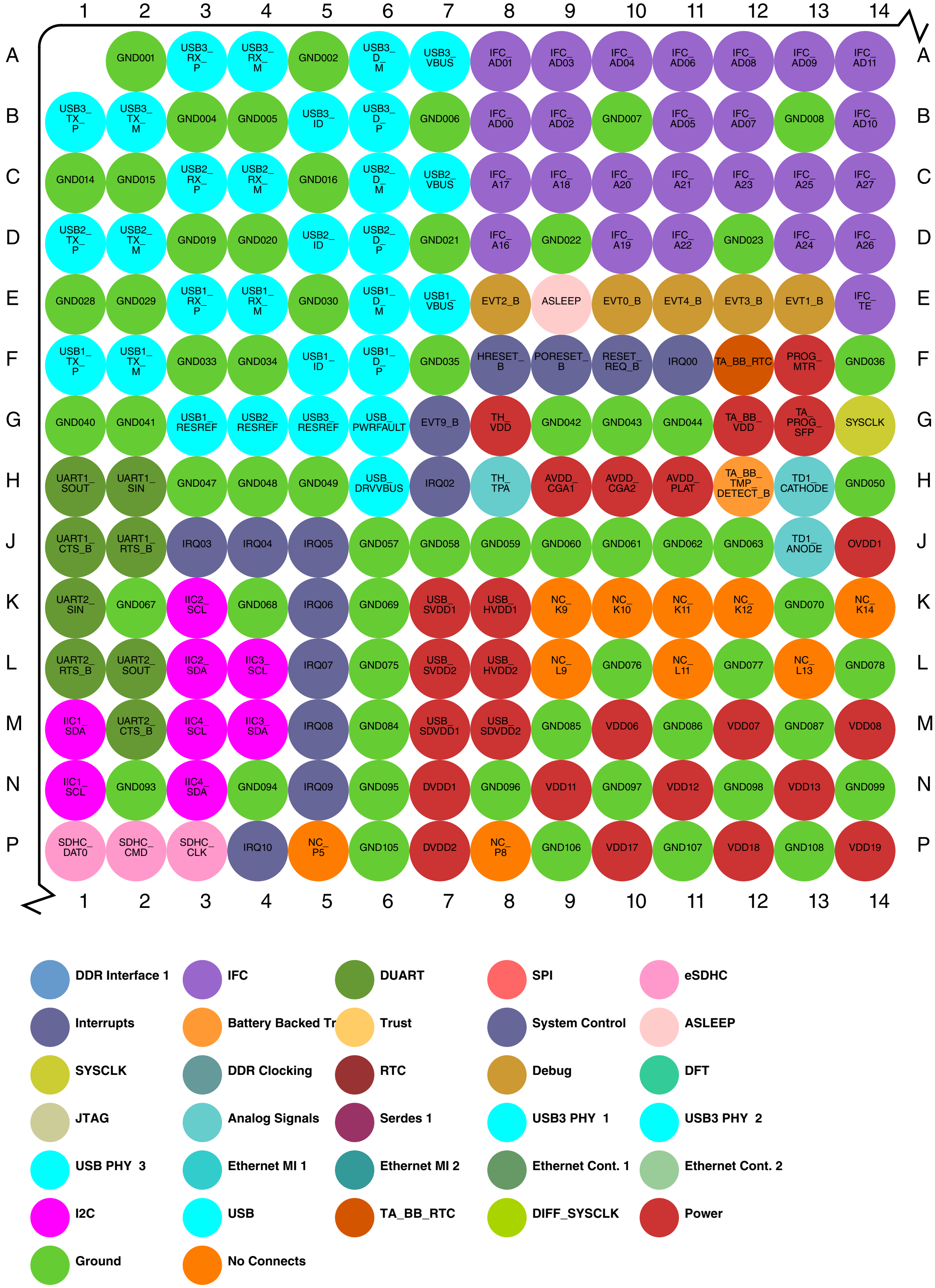

Figure 9. Detail A

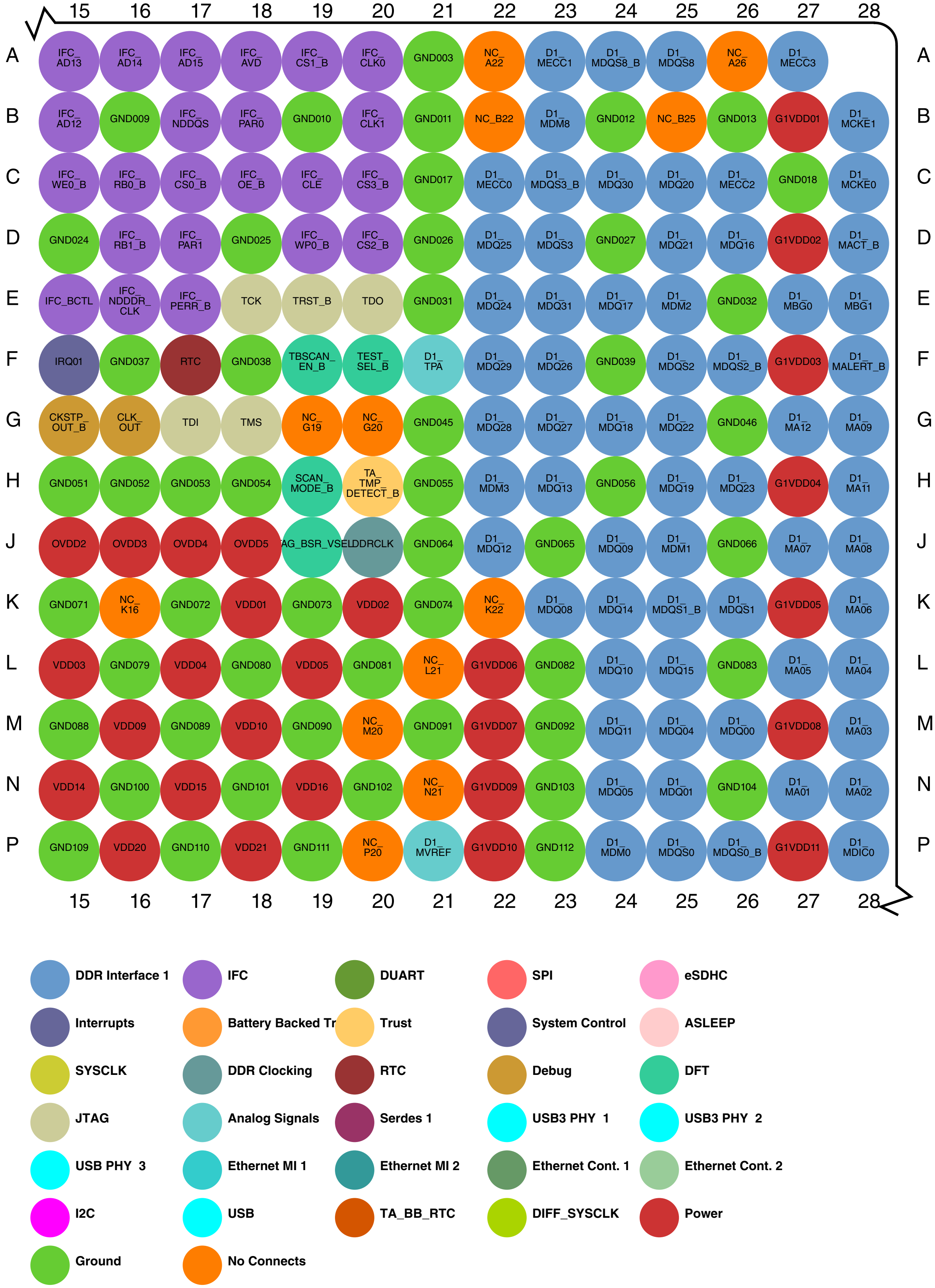

Figure 10. Detail B

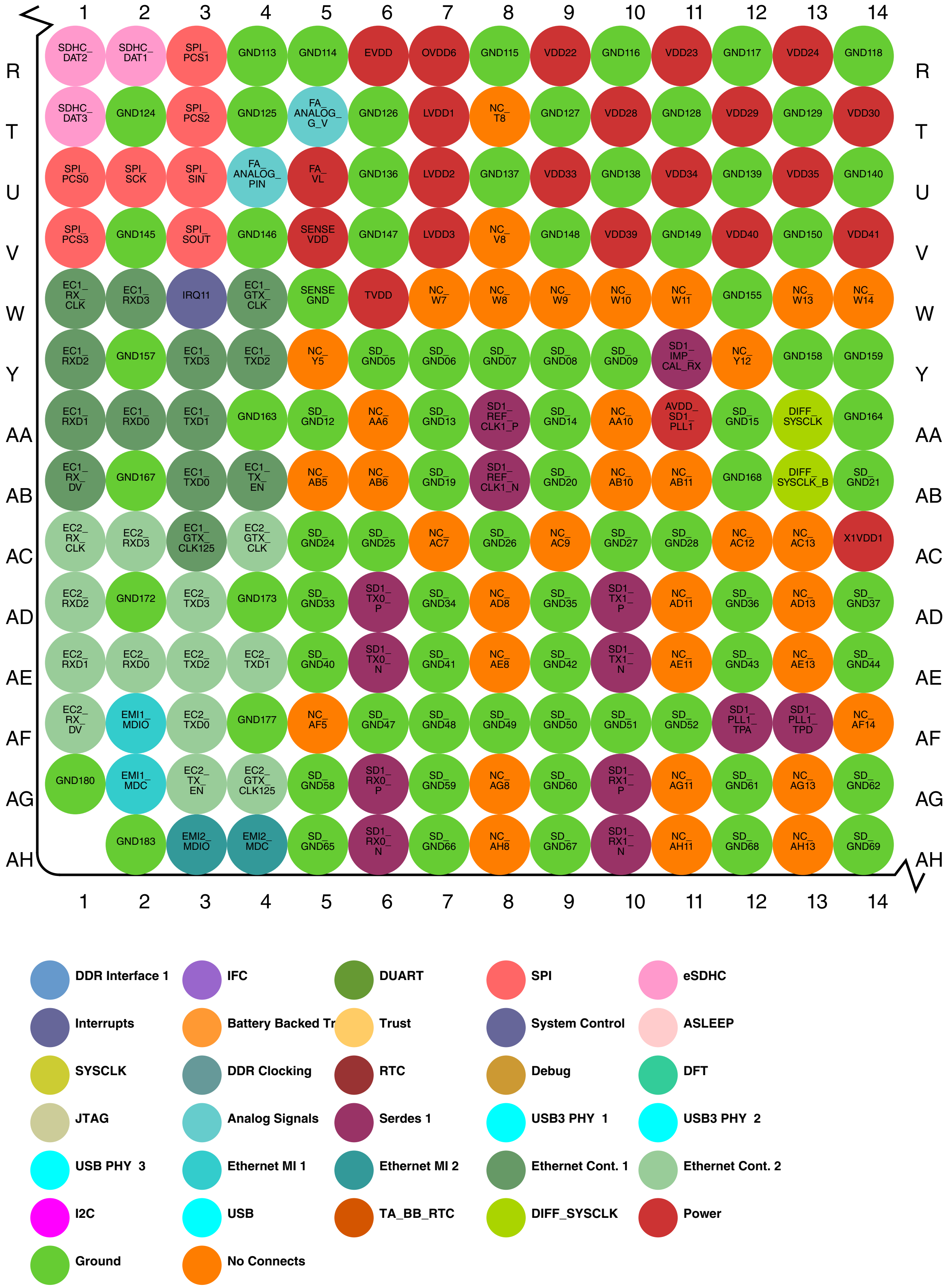

Figure 11. Detail C

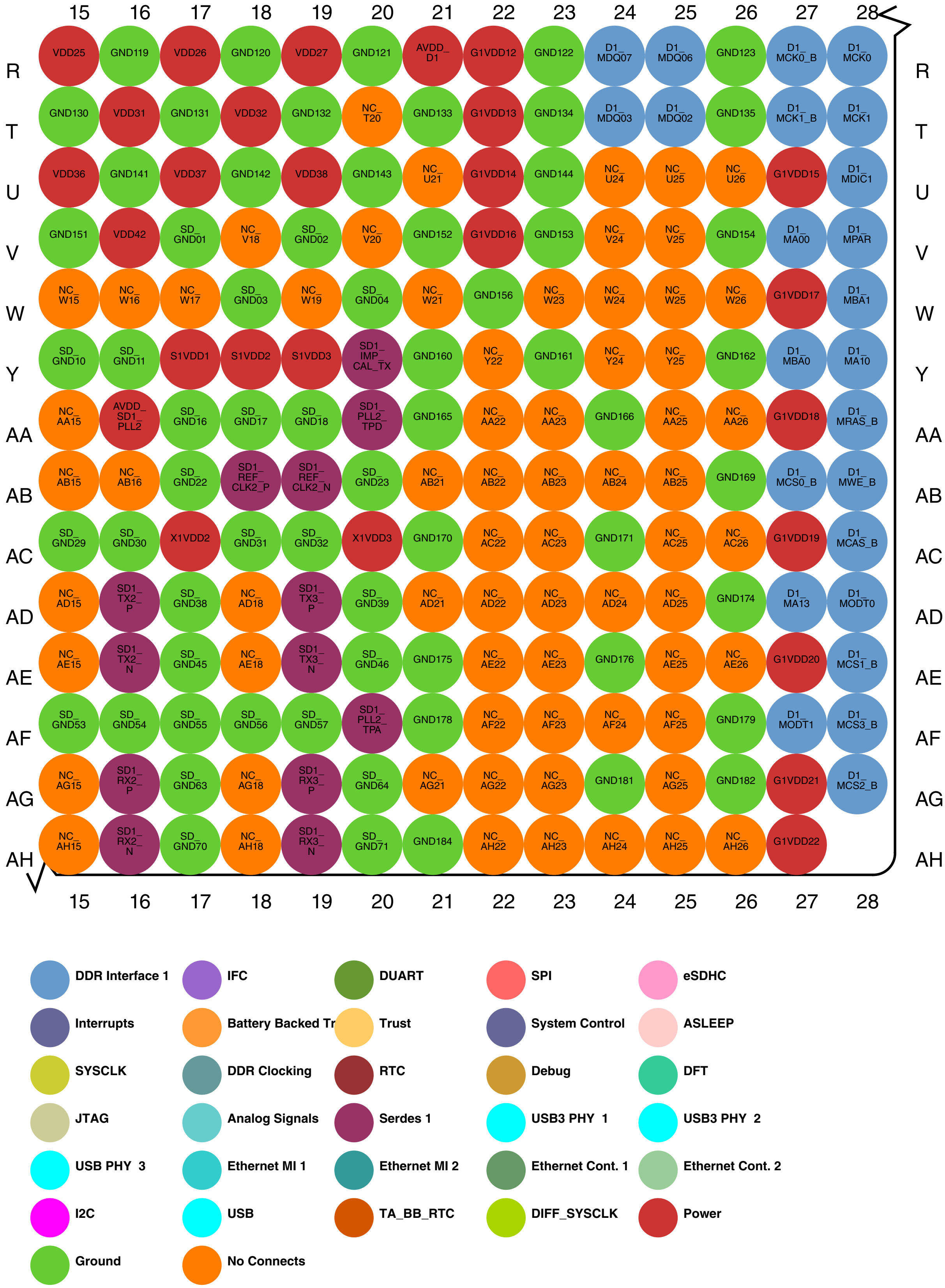

Figure 12. Detail D

2.4 Pinout list

This table provides the pinout listing for the LS1043A_23X23 by bus. Primary functions are **bolded** in the table.

Table 2. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V27	O	$G1V_{DD}$	---
D1_MA01	Address	N27	O	$G1V_{DD}$	---
D1_MA02	Address	N28	O	$G1V_{DD}$	---
D1_MA03	Address	M28	O	$G1V_{DD}$	---
D1_MA04	Address	L28	O	$G1V_{DD}$	---
D1_MA05	Address	L27	O	$G1V_{DD}$	---
D1_MA06	Address	K28	O	$G1V_{DD}$	---
D1_MA07	Address	J27	O	$G1V_{DD}$	---
D1_MA08	Address	J28	O	$G1V_{DD}$	---
D1_MA09	Address	G28	O	$G1V_{DD}$	---
D1_MA10	Address	Y28	O	$G1V_{DD}$	---
D1_MA11	Address	H28	O	$G1V_{DD}$	---
D1_MA12	Address	G27	O	$G1V_{DD}$	---
D1_MA13	Address	AD27	O	$G1V_{DD}$	---
D1_MACT_B	Address	D28	O	$G1V_{DD}$	25
D1_MALERT_B	Address Parity Error	F28	I	$G1V_{DD}$	1, 6, 25
D1_MBA0	Bank Select	Y27	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	---
D1_MBG0	Bank Select	E27	O	$G1V_{DD}$	25
D1_MBG1	Address	E28	O	$G1V_{DD}$	25
D1_MCAS_B	Column Address Strobe	AC28	O	$G1V_{DD}$	25
D1_MCK0	Clock	R28	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	R27	O	$G1V_{DD}$	---
D1_MCK1	Clock	T28	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	T27	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	C28	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	B28	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	AB27	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	AE28	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select	AG28	O	$G1V_{DD}$	---
D1_MCS3_B	Chip Select	AF28	O	$G1V_{DD}$	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	P24	O	$G1V_{DD}$	1, 25
D1_MDM1	Data Mask	J25	O	$G1V_{DD}$	1, 25
D1_MDM2	Data Mask	E25	O	$G1V_{DD}$	1, 25
D1_MDM3	Data Mask	H22	O	$G1V_{DD}$	1, 25
D1_MDM8	Data Mask	B23	O	$G1V_{DD}$	1, 25
D1_MDQ00	Data	M26	IO	$G1V_{DD}$	---
D1_MDQ01	Data	N25	IO	$G1V_{DD}$	---
D1_MDQ02	Data	T25	IO	$G1V_{DD}$	---
D1_MDQ03	Data	T24	IO	$G1V_{DD}$	---
D1_MDQ04	Data	M25	IO	$G1V_{DD}$	---
D1_MDQ05	Data	N24	IO	$G1V_{DD}$	---
D1_MDQ06	Data	R25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	R24	IO	$G1V_{DD}$	---
D1_MDQ08	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ09	Data	J24	IO	$G1V_{DD}$	---
D1_MDQ10	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ11	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ12	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ13	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ14	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ15	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ16	Data	D26	IO	$G1V_{DD}$	---
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	G24	IO	$G1V_{DD}$	---
D1_MDQ19	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ20	Data	C25	IO	$G1V_{DD}$	---
D1_MDQ21	Data	D25	IO	$G1V_{DD}$	---
D1_MDQ22	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ23	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ24	Data	E22	IO	$G1V_{DD}$	---
D1_MDQ25	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ26	Data	F23	IO	$G1V_{DD}$	---
D1_MDQ27	Data	G23	IO	$G1V_{DD}$	---
D1_MDQ28	Data	G22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ30	Data	C24	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ31	Data	E23	IO	$G1V_{DD}$	---
D1_MDQS0	Data Strobe	P25	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	K26	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	D23	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	C23	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	A25	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	C22	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	A23	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	C26	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	A27	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination	AF27	O	$G1V_{DD}$	2
D1_MPAR	Address Parity Out	V28	O	$G1V_{DD}$	25
D1_MRAS_B	Row Address Strobe	AA28	O	$G1V_{DD}$	25
D1_MWE_B	Write Enable	AB28	O	$G1V_{DD}$	25
Integrated Flash Controller					
IFC_A16/QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A17/QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A18/QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5
IFC_A19/QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A20/QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A21/QSPI_B_SCK/ cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A22/QSPI_A_DATA0/ IFC_WP1_B	IFC Address	D11	O	OV_{DD}	1
IFC_A23/QSPI_A_DATA1/ IFC_WP2_B	IFC Address	C12	O	OV_{DD}	1
IFC_A24/QSPI_A_DATA2/ IFC_WP3_B	IFC Address	D13	O	OV_{DD}	1
IFC_A25/GPIO2_25/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	IFC Address	C13	O	OV_{DD}	1
IFC_A26/GPIO2_26/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	IFC Address	D14	O	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A27/GPIO2_27/ FTM5_EXTCLK/IFC_CS6_B	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	B8	IO	OV_{DD}	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	A8	IO	OV_{DD}	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	B9	IO	OV_{DD}	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	A9	IO	OV_{DD}	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	A10	IO	OV_{DD}	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	B11	IO	OV_{DD}	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	A11	IO	OV_{DD}	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	B12	IO	OV_{DD}	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	A12	IO	OV_{DD}	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A13	IO	OV_{DD}	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	B14	IO	OV_{DD}	4
IFC_AD11/cfg_rcw_src3	IFC Address / Data	A14	IO	OV_{DD}	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	B15	IO	OV_{DD}	4
IFC_AD13/cfg_rcw_src5	IFC Address / Data	A15	IO	OV_{DD}	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A16	IO	OV_{DD}	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A17	IO	OV_{DD}	4
IFC_AVD	IFC Address Valid	A18	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer control	E15	O	OV_{DD}	2
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	C19	O	OV_{DD}	1, 4
IFC_CLK0	IFC Clock	A20	O	OV_{DD}	2
IFC_CLK1	IFC Clock	B20	O	OV_{DD}	2
IFC_CS0_B	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10/ FTM7_CH0	IFC Chip Select	A19	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_11/ FTM7_CH1	IFC Chip Select	D20	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_12/ QSPI_B_DATA3/ FTM7_EXTCLK	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS4_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_RB2_B	IFC Chip Select	C13	O	OV_{DD}	1
IFC_CS5_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_RB3_B	IFC Chip Select	D14	O	OV_{DD}	1
IFC_CS6_B/**IFC_A27**/ GPIO2_27/FTM5_EXTCLK	IFC Chip Select	C14	O	OV_{DD}	1
IFC_NDDDR_CLK	IFC NAND DDR Clock	E16	O	OV_{DD}	2

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_NDDQS	IFC DQS Strobe	B17	IO	OV_{DD}	---
IFC_OE_B/cfg_eng_use1	IFC Output Enable	C18	O	OV_{DD}	1, 4, 21
IFC_PAR0/GPIO2_13/ QSPI_B_DATA0/FTM6_CH0	IFC Address & Data Parity	B18	IO	OV_{DD}	---
IFC_PAR1/GPIO2_14/ QSPI_B_DATA1/FTM6_CH1	IFC Address & Data Parity	D17	IO	OV_{DD}	---
IFC_PERR_B/GPIO2_15/ QSPI_B_DATA2/ FTM6_EXTCLK	IFC Parity Error	E17	I	OV_{DD}	1
IFC_RB0_B	IFC Ready / Busy CS0	C16	I	OV_{DD}	6
IFC_RB1_B	IFC Ready / Busy CS1	D16	I	OV_{DD}	6
IFC_RB2_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_CS4_B	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_CS5_B	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	C15	O	OV_{DD}	1, 4, 21
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 4, 21
IFC_WP1_B/**IFC_A22**/ QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A23**/ QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A24**/ QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	H1	O	DV_{DD}	1
UART2_CTS_B/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Ready to Send	L1	O	DV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_SIN/GPIO1_18/ FTM4_CH1/LPUART1_SIN	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO1_16/ LPUART1_SOUT/FTM4_CH0	Transmit Data	L2	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21/FTM4_CH4/ LPUART2_SIN	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19/ LPUART2_SOUT/FTM4_CH2	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit Data	L1	O	DV_{DD}	1
SPI Interface					
SPI_PCS0/GPIO2_00/ SDHC_DAT4/SDHC_VS	SPI Chip Select	U1	O	OV_{DD}	1
SPI_PCS1/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	R3	O	OV_{DD}	1
SPI_PCS2/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	T3	O	OV_{DD}	1
SPI_PCS3/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	V1	O	OV_{DD}	1
SPI_SCK	SPI Clock	U2	O	OV_{DD}	1
SPI_SIN/ SDHC_CLK_SYNC_IN	Master In Slave Out	U3	I	OV_{DD}	1
SPI_SOUT/ SDHC_CLK_SYNC_OUT	Master Out Slave In	V3	IO	OV_{DD}	---
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO4_02/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	Command	K3	I	DV_{DD}	1
SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	Host to Card Clock	P3	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/ **SPI_SIN**	IN	U3	I	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CLK_SYNC_OUT/ **SPI_SOUT**	OUT	V3	O	OV_{DD}	1
SDHC_CMD/GPIO2_04/ LPUART3_SOUT/FTM4_CH6	Command/Response	P2	IO	EV_{DD}	---
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO2_01/SDHC_DAT5	DIR	R3	O	OV_{DD}	1
SDHC_DAT0/GPIO2_05/ FTM4_CH7/LPUART3_SIN	Data	P1	IO	EV_{DD}	---
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO2_02/SDHC_DAT6	DIR	T3	O	OV_{DD}	1
SDHC_DAT1/GPIO2_06/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	Data	R2	IO	EV_{DD}	---
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO2_03/ SDHC_DAT7	DIR	V1	O	OV_{DD}	1
SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	Data	R1	IO	EV_{DD}	---
SDHC_DAT3/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	Data	T1	IO	EV_{DD}	---
SDHC_DAT4/**SPI_PCS0**/ GPIO2_00/SDHC_VS	Data	U1	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO2_01/SDHC_CMD_DIR	Data	R3	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO2_02/SDHC_DAT0_DIR	Data	T3	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO2_03/ SDHC_DAT123_DIR	Data	V1	IO	OV_{DD}	---
SDHC_VS/**SPI_PCS0**/ GPIO2_00/SDHC_DAT4	VS	U1	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO4_03/FTM3_QD_PHB/ CLK10/QE_SI1_STROBE1/ BRGO3	Write Protect	L3	I	DV_{DD}	1
Programmable Interrupt Controller					
EVT9_B	Interrupt Output	G7	O	OV_{DD}	1, 6, 7
IRQ00	External Interrupt	F11	I	OV_{DD}	1
IRQ01	External Interrupt	F15	I	OV_{DD}	1
IRQ02	External Interrupt	H7	I	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ03/GPIO1_23/FTM3_CH7/ TDMB_TSYNC/ UC3_RTSB_TXEN	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO1_24/FTM3_CH0/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO1_25/FTM3_CH1/ TDMA_RSYNC/ UC1_CTSB_RXDV	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO1_26/FTM3_CH2/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	External Interrupt	K5	I	DV_{DD}	1
IRQ07/GPIO1_27/FTM3_CH3/ TDMA_TSYNC/ UC1_RTSB_TXEN	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO1_28/FTM3_CH4/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO1_29/FTM3_CH5/ TDMB_RSYNC/ UC3_CTSB_RXDV	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO1_30/FTM3_CH6/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO1_31	External Interrupt	W3	I	LV_{DD}	1
Battery Backed Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	H12	I	$TA\_BB\_V_{DD}$	---
Trust					
TA_TMP_DETECT_B	Tamper Detect	H20	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	F8	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F9	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	F10	O	OV_{DD}	1, 5
Power Management					
ASLEEP/GPIO1_13	Asleep	E9	O	OV_{DD}	1, 4
SYSCLK					
SYSCLK	System Clock	G14	I	OV_{DD}	18
DDR Clocking					
DDRCLK	DDR Controller Clock	J20	I	OV_{DD}	18
RTC					
RTC/GPIO1_14	Real Time Clock	F17	I	OV_{DD}	1
Debug					
CKSTP_OUT_B	Reserved	G15	O	OV_{DD}	6, 7

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
CLK_OUT	Clock Out	G16	O	OV_{DD}	2
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	---
EVT2_B	Event 2	E8	IO	OV_{DD}	---
EVT3_B	Event 3	E12	IO	OV_{DD}	---
EVT4_B	Event 4	E11	IO	OV_{DD}	---
EVT5_B/**IIC3_SCL**/GPIO4_10/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_11/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_12/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_13/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	Event 8	N3	IO	DV_{DD}	---
DFT					
JTAG_BSR_VSEL	An IEEE 1149.1 JTAG compliance enable pin. 0: Normal operation. 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.	J19	I	OV_{DD}	36
SCAN_MODE_B	Reserved	H19	I	OV_{DD}	10
TBSCAN_EN_B	An IEEE 1149.1 JTAG compliance enable pin. 0:To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the ARM core debug.	F19	I	OV_{DD}	35
TEST_SEL_B	Reserved	F20	I	OV_{DD}	23
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G17	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2
TMS	Test Mode Select	G18	I	OV_{DD}	9

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_MVREF	SSTL Reference Voltage	P21	IO	$G1V_{DD}/2$	---
D1_TPA	DDR Controller 1 Test Point Analog	F21	IO		12
FA_ANALOG_G_V	Reserved	T5	IO		15
FA_ANALOG_PIN	Reserved	U4	IO		15
TD1_ANODE	Thermal diode anode	J13	IO		17
TD1_CATHODE	Thermal diode cathode	H13	IO		17
TH_TPA	Thermal Test Point Analog	H8	-	-	12
SerDes					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y11	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	$X1V_{DD}$	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AF13	O	$X1V_{DD}$	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF20	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AA20	O	$X1V_{DD}$	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AB8	I	$S1V_{DD}$	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AA8	I	$S1V_{DD}$	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	$S1V_{DD}$	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	$S1V_{DD}$	---
SD1_RX0_N	SerDes Receive Data (negative)	AH6	I	$S1V_{DD}$	---
SD1_RX0_P	SerDes Receive Data (positive)	AG6	I	$S1V_{DD}$	---
SD1_RX1_N	SerDes Receive Data (negative)	AH10	I	$S1V_{DD}$	---
SD1_RX1_P	SerDes Receive Data (positive)	AG10	I	$S1V_{DD}$	---
SD1_RX2_N	SerDes Receive Data (negative)	AH16	I	$S1V_{DD}$	---
SD1_RX2_P	SerDes Receive Data (positive)	AG16	I	$S1V_{DD}$	---
SD1_RX3_N	SerDes Receive Data (negative)	AH19	I	$S1V_{DD}$	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX3_P	SerDes Receive Data (positive)	AG19	I	$S1V_{DD}$	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE6	O	$X1V_{DD}$	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD6	O	$X1V_{DD}$	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE10	O	$X1V_{DD}$	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD10	O	$X1V_{DD}$	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE16	O	$X1V_{DD}$	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD16	O	$X1V_{DD}$	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE19	O	$X1V_{DD}$	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD19	O	$X1V_{DD}$	---
USB3 PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	USB_HV_{DD}	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	USB_HV_{DD}	---
USB1_ID	USB PHY ID Detect	F5	I	-	29
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	27
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	USB_SV_{DD}	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	USB_SV_{DD}	---
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	USB_SV_{DD}	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	USB_SV_{DD}	---
USB1_VBUS	USB PHY VBUS	E7	I	-	28
USB3 PHY 2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	USB_HV_{DD}	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	USB_HV_{DD}	---
USB2_ID	USB PHY ID Detect	D5	I	-	29
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	27
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	USB_SV_{DD}	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	USB_SV_{DD}	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	USB_SV_{DD}	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	USB_SV_{DD}	---
USB2_VBUS	USB PHY VBUS	C7	I	-	28

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB3 PHY 3					
USB3_D_M	USB PHY HS Data (-)	A6	IO	USB_HV_{DD}	---
USB3_D_P	USB PHY HS Data (+)	B6	IO	USB_HV_{DD}	---
USB3_ID	USB PHY ID Detect	B5	I	-	29
USB3_RESREF	USB PHY Impedance Calibration	G5	IO	-	27
USB3_RX_M	USB PHY SS Receive Data (-)	A4	I	USB_SV_{DD}	---
USB3_RX_P	USB PHY SS Receive Data (+)	A3	I	USB_SV_{DD}	---
USB3_TX_M	USB PHY SS Transmit Data (-)	B2	O	USB_SV_{DD}	---
USB3_TX_P	USB PHY SS Transmit Data (+)	B1	O	USB_SV_{DD}	---
USB3_VBUS	USB PHY VBUS	A7	I	-	28
Ethernet Management Interface 1					
EMI1_MDC/GPIO3_00	Management Data Clock	AG2	O	LV_{DD}	1
EMI1_MDIO/GPIO3_01	Management Data In/Out	AF2	IO	LV_{DD}	---
Ethernet Management Interface 2					
EMI2_MDC/GPIO4_00	Management Data Clock	AH4	O	TV_{DD}	1
EMI2_MDIO/GPIO4_01	Management Data In/Out	AH3	IO	TV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO3_07/ FTM1_EXTCLK	Transmit Clock Out	W4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO3_08	Reference Clock	AC3	I	LV_{DD}	1
EC1_RXD0/GPIO3_12/ FTM1_CH0	Receive Data	AA2	I	LV_{DD}	1
EC1_RXD1/GPIO3_11/ FTM1_CH1	Receive Data	AA1	I	LV_{DD}	1
EC1_RXD2/GPIO3_10/ FTM1_CH6	Receive Data	Y1	I	LV_{DD}	1
EC1_RXD3/GPIO3_09/ FTM1_CH4	Receive Data	W2	I	LV_{DD}	1
EC1_RX_CLK/GPIO3_13/ FTM1_QD_PHA	Receive Clock	W1	I	LV_{DD}	1
EC1_RX_DV/GPIO3_14/ FTM1_QD_PHB	Receive Data Valid	AB1	I	LV_{DD}	1
EC1_TXD0/GPIO3_05/ FTM1_CH2	Transmit Data	AB3	O	LV_{DD}	1
EC1_TXD1/GPIO3_04/ FTM1_CH3	Transmit Data	AA3	O	LV_{DD}	1
EC1_TXD2/GPIO3_03/ FTM1_CH7	Transmit Data	Y4	O	LV_{DD}	1
EC1_TXD3/GPIO3_02/ FTM1_CH5	Transmit Data	Y3	O	LV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_TX_EN/GPIO3_06/ FTM1_FAULT	Transmit Enable	AB4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO3_20/ FTM2_EXTCLK	Transmit Clock Out	AC4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO3_21	Reference Clock	AG4	I	LV_{DD}	1
EC2_RXD0/GPIO3_25/ TSEC_1588_TRIG_IN2/ FTM2_CH0	Receive Data	AE2	I	LV_{DD}	1
EC2_RXD1/GPIO3_24/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	Receive Data	AE1	I	LV_{DD}	1
EC2_RXD2/GPIO3_23/ FTM2_CH6	Receive Data	AD1	I	LV_{DD}	1
EC2_RXD3/GPIO3_22/ FTM2_CH4	Receive Data	AC2	I	LV_{DD}	1
EC2_RX_CLK/GPIO3_26/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	Receive Clock	AC1	I	LV_{DD}	1
EC2_RX_DV/GPIO3_27/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	Receive Data Valid	AF1	I	LV_{DD}	1
EC2_TXD0/GPIO3_18/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	Transmit Data	AF3	O	LV_{DD}	1
EC2_TXD1/GPIO3_17/ TSEC_1588_CLK_OUT/ FTM2_CH3	Transmit Data	AE4	O	LV_{DD}	1
EC2_TXD2/GPIO3_16/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	Transmit Data	AE3	O	LV_{DD}	1
EC2_TXD3/GPIO3_15/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	Transmit Data	AD3	O	LV_{DD}	1
EC2_TX_EN/GPIO3_19/ FTM2_FAULT	Transmit Enable	AG3	O	LV_{DD}	1, 14
I2C					
IIC1_SCL	Serial Clock (supports PBL)	N1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	M1	IO	DV_{DD}	7, 8
IIC2_SCL/GPIO4_02/ SDHC_CD_B/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	Serial Clock	K3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO4_03/ SDHC_WP/FTM3_QD_PHB/	Serial Data	L3	IO	DV_{DD}	7, 8

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
CLK10/QE_SI1_STROBE1/ BRGO3					
IIC3_SCL/GPIO4_10/EVT5_B/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	Serial Clock	L4	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_11/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	Serial Data	M4	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_12/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	Serial Clock	M3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_13/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	Serial Data	N3	IO	DV_{DD}	7, 8
USB					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_10/EVT5_B/BRGO4/ FTM8_CH0/CLK11	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_11/EVT6_B/BRGO1/ FTM8_CH1/CLK12_CLK8	PWR Fault	M4	I	DV_{DD}	1
USB3_DRVVBUS/**IIC4_SCL**/ GPIO4_12/EVT7_B/ TDMA_RQ/FTM3_FAULT/ UC1_CDB_RXER	DRV Bus	M3	O	DV_{DD}	1
USB3_PWRFAULT/**IIC4_SDA**/ GPIO4_13/EVT8_B/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	PWR Fault	N3	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_29	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_30	USB_PWRFAULT	G6	I	DV_{DD}	1
Battery Backed RTC					
TA_BB_RTC	Reserved	F12	I	$TA\_BB\_V_{DD}$	33
DSYSCLK					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AA13	I	OV_{DD}	19
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AB13	I	OV_{DD}	19
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**/ QSPI_B_SCK	Power-on-Reset Configuration	C11	I	OV_{DD}	1, 4
cfg_eng_use0/**IFC_WE0_B**	Power-on-Reset Configuration	C15	I	OV_{DD}	1, 4
cfg_eng_use1/**IFC_OE_B**	Power-on-Reset Configuration	C18	I	OV_{DD}	1, 4

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_eng_use2/**IFC_WP0_B**	Power-on-Reset Configuration	D19	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-on-Reset Configuration	B8	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-on-Reset Configuration	A8	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-on-Reset Configuration	B9	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-on-Reset Configuration	A9	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-on-Reset Configuration	A10	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-on-Reset Configuration	B11	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**	Power-on-Reset Configuration	A11	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-on-Reset Configuration	B12	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-on-Reset Configuration	E14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-on-Reset Configuration	A12	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-on-Reset Configuration	A13	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-on-Reset Configuration	B14	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-on-Reset Configuration	A14	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-on-Reset Configuration	B15	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-on-Reset Configuration	A15	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-on-Reset Configuration	A16	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-on-Reset Configuration	A17	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-on-Reset Configuration	C19	I	OV_{DD}	1, 4
General Purpose Input/Output					
GPIO1_13/**ASLEEP**	General Purpose Input/Output	E9	O	OV_{DD}	1, 4
GPIO1_14/**RTC**	General Purpose Input/Output	F17	IO	OV_{DD}	---
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	H1	IO	DV_{DD}	---
GPIO1_16/**UART2_SOUT**/ LPUART1_SOUT/FTM4_CH0	General Purpose Input/Output	L2	IO	DV_{DD}	---
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	H2	IO	DV_{DD}	---
GPIO1_18/**UART2_SIN**/ FTM4_CH1/LPUART1_SIN	General Purpose Input/Output	K1	IO	DV_{DD}	---
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	General Purpose Input/Output	J2	IO	DV_{DD}	---
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	General Purpose Input/Output	L1	IO	DV_{DD}	---
GPIO1_21/**UART1_CTS_B**/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	General Purpose Input/Output	J1	IO	DV_{DD}	---
GPIO1_22/**UART2_CTS_B**/ UART4_SIN/FTM4_CH5/	General Purpose Input/Output	M2	IO	DV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LPUART1_CTS_B/ LPUART4_SIN					
GPIO1_23/**IRQ03**/FTM3_CH7/ TDMB_TSYNC/ UC3_RTSB_TXEN	General Purpose Input/Output	J3	IO	DV_{DD}	---
GPIO1_24/**IRQ04**/FTM3_CH0/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	General Purpose Input/Output	J4	IO	DV_{DD}	---
GPIO1_25/**IRQ05**/FTM3_CH1/ TDMA_RSYNC/ UC1_CTSB_RXDV	General Purpose Input/Output	J5	IO	DV_{DD}	---
GPIO1_26/**IRQ06**/FTM3_CH2/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	General Purpose Input/Output	K5	IO	DV_{DD}	---
GPIO1_27/**IRQ07**/FTM3_CH3/ TDMA_TSYNC/ UC1_RTSB_TXEN	General Purpose Input/Output	L5	IO	DV_{DD}	---
GPIO1_28/**IRQ08**/FTM3_CH4/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	General Purpose Input/Output	M5	IO	DV_{DD}	---
GPIO1_29/**IRQ09**/FTM3_CH5/ TDMB_RSYNC/ UC3_CTSB_RXDV	General Purpose Input/Output	N5	IO	DV_{DD}	---
GPIO1_30/**IRQ10**/FTM3_CH6/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	General Purpose Input/Output	P4	IO	DV_{DD}	---
GPIO1_31/**IRQ11**	General Purpose Input/Output	W3	IO	LV_{DD}	---
GPIO2_00/**SPI_PCS0**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO2_01/**SPI_PCS1**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	R3	IO	OV_{DD}	---
GPIO2_02/**SPI_PCS2**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	T3	IO	OV_{DD}	---
GPIO2_03/**SPI_PCS3**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	V1	IO	OV_{DD}	---
GPIO2_04/**SDHC_CMD**/ LPUART3_SOUT/FTM4_CH6	General Purpose Input/Output	P2	IO	EV_{DD}	---
GPIO2_05/**SDHC_DAT0**/ FTM4_CH7/LPUART3_SIN	General Purpose Input/Output	P1	IO	EV_{DD}	---
GPIO2_06/**SDHC_DAT1**/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	General Purpose Input/Output	R2	IO	EV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_07/**SDHC_DAT2**/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	General Purpose Input/Output	R1	IO	EV_{DD}	---
GPIO2_08/**SDHC_DAT3**/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	General Purpose Input/Output	T1	IO	EV_{DD}	---
GPIO2_09/**SDHC_CLK**/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	General Purpose Input/Output	P3	IO	EV_{DD}	---
GPIO2_10/**IFC_CS1_B**/ FTM7_CH0	General Purpose Input/Output	A19	IO	OV_{DD}	---
GPIO2_11/**IFC_CS2_B**/ FTM7_CH1	General Purpose Input/Output	D20	IO	OV_{DD}	---
GPIO2_12/**IFC_CS3_B**/ QSPI_B_DATA3/ FTM7_EXTCLK	General Purpose Input/Output	C20	IO	OV_{DD}	---
GPIO2_13/**IFC_PAR0**/ QSPI_B_DATA0/FTM6_CH0	General Purpose Input/Output	B18	IO	OV_{DD}	---
GPIO2_14/**IFC_PAR1**/ QSPI_B_DATA1/FTM6_CH1	General Purpose Input/Output	D17	IO	OV_{DD}	---
GPIO2_15/**IFC_PERR_B**/ QSPI_B_DATA2/ FTM6_EXTCLK	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO2_25/**IFC_A25**/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO2_26/**IFC_A26**/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	General Purpose Input/Output	D14	IO	OV_{DD}	---
GPIO2_27/**IFC_A27**/ FTM5_EXTCLK/IFC_CS6_B	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO3_00/**EMI1_MDC**	General Purpose Input/Output	AG2	IO	LV_{DD}	---
GPIO3_01/**EMI1_MDIO**	General Purpose Input/Output	AF2	IO	LV_{DD}	---
GPIO3_02/**EC1_TXD3**/ FTM1_CH5	General Purpose Input/Output	Y3	IO	LV_{DD}	---
GPIO3_03/**EC1_TXD2**/ FTM1_CH7	General Purpose Input/Output	Y4	IO	LV_{DD}	---
GPIO3_04/**EC1_TXD1**/ FTM1_CH3	General Purpose Input/Output	AA3	IO	LV_{DD}	---
GPIO3_05/**EC1_TXD0**/ FTM1_CH2	General Purpose Input/Output	AB3	IO	LV_{DD}	---
GPIO3_06/**EC1_TX_EN**/ FTM1_FAULT	General Purpose Input/Output	AB4	IO	LV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_07/**EC1_GTX_CLK**/ FTM1_EXTCLK	General Purpose Input/Output	W4	IO	LV_{DD}	---
GPIO3_08/**EC1_GTX_CLK125**	General Purpose Input/Output	AC3	IO	LV_{DD}	---
GPIO3_09/**EC1_RXD3**/ FTM1_CH4	General Purpose Input/Output	W2	IO	LV_{DD}	---
GPIO3_10/**EC1_RXD2**/ FTM1_CH6	General Purpose Input/Output	Y1	IO	LV_{DD}	---
GPIO3_11/**EC1_RXD1**/ FTM1_CH1	General Purpose Input/Output	AA1	IO	LV_{DD}	---
GPIO3_12/**EC1_RXD0**/ FTM1_CH0	General Purpose Input/Output	AA2	IO	LV_{DD}	---
GPIO3_13/**EC1_RX_CLK**/ FTM1_QD_PHA	General Purpose Input/Output	W1	IO	LV_{DD}	---
GPIO3_14/**EC1_RX_DV**/ FTM1_QD_PHB	General Purpose Input/Output	AB1	IO	LV_{DD}	---
GPIO3_15/**EC2_TXD3**/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	General Purpose Input/Output	AD3	IO	LV_{DD}	---
GPIO3_16/**EC2_TXD2**/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	General Purpose Input/Output	AE3	IO	LV_{DD}	---
GPIO3_17/**EC2_TXD1**/ TSEC_1588_CLK_OUT/ FTM2_CH3	General Purpose Input/Output	AE4	IO	LV_{DD}	---
GPIO3_18/**EC2_TXD0**/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	General Purpose Input/Output	AF3	IO	LV_{DD}	---
GPIO3_19/**EC2_TX_EN**/ FTM2_FAULT	General Purpose Input/Output	AG3	IO	LV_{DD}	---
GPIO3_20/**EC2_GTX_CLK**/ FTM2_EXTCLK	General Purpose Input/Output	AC4	IO	LV_{DD}	---
GPIO3_21/**EC2_GTX_CLK125**	General Purpose Input/Output	AG4	IO	LV_{DD}	---
GPIO3_22/**EC2_RXD3**/ FTM2_CH4	General Purpose Input/Output	AC2	IO	LV_{DD}	---
GPIO3_23/**EC2_RXD2**/ FTM2_CH6	General Purpose Input/Output	AD1	IO	LV_{DD}	---
GPIO3_24/**EC2_RXD1**/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	General Purpose Input/Output	AE1	IO	LV_{DD}	---
GPIO3_25/**EC2_RXD0**/ TSEC_1588_TRIG_IN2/ FTM2_CH0	General Purpose Input/Output	AE2	IO	LV_{DD}	---
GPIO3_26/**EC2_RX_CLK**/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	General Purpose Input/Output	AC1	IO	LV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_27/**EC2_RX_DV**/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	General Purpose Input/Output	AF1	IO	LV_{DD}	---
GPIO4_00/**EMI2_MDC**	General Purpose Input/Output	AH4	IO	TV_{DD}	---
GPIO4_01/**EMI2_MDIO**	General Purpose Input/Output	AH3	IO	TV_{DD}	---
GPIO4_02/**IIC2_SCL**/ SDHC_CD_B/FTM3_QD_PHA/ CLK9/QE_SI1_STROBE0/ BRGO2	General Purpose Input/Output	K3	IO	DV_{DD}	---
GPIO4_03/**IIC2_SDA**/ SDHC_WP/FTM3_QD_PHB/ CLK10/QE_SI1_STROBE1/ BRGO3	General Purpose Input/Output	L3	IO	DV_{DD}	---
GPIO4_10/**IIC3_SCL**/EVT5_B/ USB2_DRVVBUS/BRGO4/ FTM8_CH0/CLK11	General Purpose Input/Output	L4	IO	DV_{DD}	---
GPIO4_11/**IIC3_SDA**/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1/CLK12_CLK8	General Purpose Input/Output	M4	IO	DV_{DD}	---
GPIO4_12/**IIC4_SCL**/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ FTM3_FAULT/ UC1_CDB_RXER	General Purpose Input/Output	M3	IO	DV_{DD}	---
GPIO4_13/**IIC4_SDA**/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/FTM3_EXTCLK/ UC3_CDB_RXER	General Purpose Input/Output	N3	IO	DV_{DD}	---
GPIO4_29/**USB_DRVVBUS**	General Purpose Input/Output	H6	IO	DV_{DD}	---
GPIO4_30/**USB_PWRFAULT**	General Purpose Input/Output	G6	IO	DV_{DD}	---
Frequency Timer Module 1					
FTM1_CH0/**EC1_RXD0**/ GPIO3_12	Channel 0	AA2	IO	LV_{DD}	---
FTM1_CH1/**EC1_RXD1**/ GPIO3_11	Channel 1	AA1	IO	LV_{DD}	---
FTM1_CH2/**EC1_TXD0**/ GPIO3_05	Channel 2	AB3	IO	LV_{DD}	---
FTM1_CH3/**EC1_TXD1**/ GPIO3_04	Channel 3	AA3	IO	LV_{DD}	---
FTM1_CH4/**EC1_RXD3**/ GPIO3_09	Channel 4	W2	IO	LV_{DD}	---
FTM1_CH5/**EC1_TXD3**/ GPIO3_02	Channel 5	Y3	IO	LV_{DD}	---
FTM1_CH6/**EC1_RXD2**/ GPIO3_10	Channel 6	Y1	IO	LV_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM1_CH7/**EC1_TXD2**/ GPIO3_03	Channel 7	Y4	IO	LV_{DD}	---
FTM1_EXTCLK/ **EC1_GTX_CLK**/GPIO3_07	Ext Clock	W4	I	LV_{DD}	1
FTM1_FAULT/**EC1_TX_EN**/ GPIO3_06	Fault	AB4	I	LV_{DD}	1
FTM1_QD_PHA/ **EC1_RX_CLK**/GPIO3_13	Phase A	W1	I	LV_{DD}	1
FTM1_QD_PHB/**EC1_RX_DV**/ GPIO3_14	Phase B	AB1	I	LV_{DD}	1
Frequency Timer Module 2					
FTM2_CH0/**EC2_RXD0**/ GPIO3_25/ TSEC_1588_TRIG_IN2	Channel 0	AE2	IO	LV_{DD}	---
FTM2_CH1/**EC2_RXD1**/ GPIO3_24/ TSEC_1588_PULSE_OUT1	Channel 1	AE1	IO	LV_{DD}	---
FTM2_CH2/**EC2_TXD0**/ GPIO3_18/ TSEC_1588_PULSE_OUT2	Channel 2	AF3	IO	LV_{DD}	---
FTM2_CH3/**EC2_TXD1**/ GPIO3_17/ TSEC_1588_CLK_OUT	Channel 3	AE4	IO	LV_{DD}	---
FTM2_CH4/**EC2_RXD3**/ GPIO3_22	Channel 4	AC2	IO	LV_{DD}	---
FTM2_CH5/**EC2_TXD3**/ GPIO3_15/ TSEC_1588_ALARM_OUT2	Channel 5	AD3	IO	LV_{DD}	---
FTM2_CH6/**EC2_RXD2**/ GPIO3_23	Channel 6	AD1	IO	LV_{DD}	---
FTM2_CH7/**EC2_TXD2**/ GPIO3_16/ TSEC_1588_ALARM_OUT1	Channel 7	AE3	IO	LV_{DD}	---
FTM2_EXTCLK/ **EC2_GTX_CLK**/GPIO3_20	Ext Clock	AC4	I	LV_{DD}	1
FTM2_FAULT/**EC2_TX_EN**/ GPIO3_19	Fault	AG3	I	LV_{DD}	1
FTM2_QD_PHA/ **EC2_RX_CLK**/GPIO3_26/ TSEC_1588_CLK_IN	Phase A	AC1	I	LV_{DD}	1
FTM2_QD_PHB/**EC2_RX_DV**/ GPIO3_27/ TSEC_1588_TRIG_IN1	Phase B	AF1	I	LV_{DD}	1
Frequency Timer Module 3					

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Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM3_CH0/**IRQ04**/GPIO1_24/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	Channel 0	J4	IO	DV_{DD}	---
FTM3_CH1/**IRQ05**/GPIO1_25/ TDMA_RSYNC/ UC1_CTSB_RXDV	Channel 1	J5	IO	DV_{DD}	---
FTM3_CH2/**IRQ06**/GPIO1_26/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	Channel 2	K5	IO	DV_{DD}	---
FTM3_CH3/**IRQ07**/GPIO1_27/ TDMA_TSYNC/ UC1_RTSB_TXEN	Channel 3	L5	IO	DV_{DD}	---
FTM3_CH4/**IRQ08**/GPIO1_28/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	Channel 4	M5	IO	DV_{DD}	---
FTM3_CH5/**IRQ09**/GPIO1_29/ TDMB_RSYNC/ UC3_CTSB_RXDV	Channel 5	N5	IO	DV_{DD}	---
FTM3_CH6/**IRQ10**/GPIO1_30/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	Channel 6	P4	IO	DV_{DD}	---
FTM3_CH7/**IRQ03**/GPIO1_23/ TDMB_TSYNC/ UC3_RTSB_TXEN	Channel 7	J3	IO	LV_{DD}	---
FTM3_EXTCLK/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT/ TDMB_RQ/UC3_CDB_RXER	Ext Clock	N3	I	DV_{DD}	1
FTM3_FAULT/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS/TDMA_RQ/ UC1_CDB_RXER	Fault	M3	I	DV_{DD}	1
FTM3_QD_PHA/**IIC2_SCL**/ GPIO4_02/SDHC_CD_B/ CLK9/QE_SI1_STROBE0/ BRGO2	Phase A	K3	I	DV_{DD}	1
FTM3_QD_PHB/**IIC2_SDA**/ GPIO4_03/SDHC_WP/CLK10/ QE_SI1_STROBE1/BRGO3	Phase B	L3	I	DV_{DD}	1
Frequency Timer Module 4					
FTM4_CH0/**UART2_SOUT**/ GPIO1_16/LPUART1_SOUT	Channel 0	L2	IO	DV_{DD}	---
FTM4_CH1/**UART2_SIN**/ GPIO1_18/LPUART1_SIN	Channel 1	K1	IO	DV_{DD}	---
FTM4_CH2/**UART1_RTS_B**/ GPIO1_19/UART3_SOUT/ LPUART2_SOUT	Channel 2	J2	IO	DV_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM4_CH3/**UART2_RTS_B**/ GPIO1_20/UART4_SOUT/ LPUART4_SOUT/ LPUART1_RTS_B	Channel 3	L1	IO	DV_{DD}	---
FTM4_CH4/**UART1_CTS_B**/ GPIO1_21/UART3_SIN/ LPUART2_SIN	Channel 4	J1	IO	DV_{DD}	---
FTM4_CH5/**UART2_CTS_B**/ GPIO1_22/UART4_SIN/ LPUART1_CTS_B/ LPUART4_SIN	Channel 5	M2	IO	DV_{DD}	---
FTM4_CH6/**SDHC_CMD**/ GPIO2_04/LPUART3_SOUT	Channel 6	P2	IO	EV_{DD}	---
FTM4_CH7/**SDHC_DAT0**/ GPIO2_05/LPUART3_SIN	Channel 7	P1	IO	EV_{DD}	---
FTM4_EXTCLK/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ LPUART5_SIN	Ext Clock	R1	I	EV_{DD}	1
FTM4_FAULT/**SDHC_DAT1**/ GPIO2_06/LPUART5_SOUT/ LPUART2_RTS_B	Fault	R2	I	EV_{DD}	1
FTM4_QD_PHA/**SDHC_DAT3**/ GPIO2_08/LPUART6_SOUT/ LPUART3_RTS_B	Phase A	T1	I	EV_{DD}	1
FTM4_QD_PHB/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ LPUART6_SIN	Phase B	P3	I	EV_{DD}	1
Frequency Timer Module 5					
FTM5_CH0/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ IFC_CS4_B/IFC_RB2_B	Channel 0	C13	IO	OV_{DD}	---
FTM5_CH1/**IFC_A26**/ GPIO2_26/IFC_CS5_B/ IFC_RB3_B	Channel 1	D14	IO	OV_{DD}	---
FTM5_EXTCLK/**IFC_A27**/ GPIO2_27/IFC_CS6_B	Ext Clock	C14	I	OV_{DD}	1
Frequency Timer Module 6					
FTM6_CH0/**IFC_PAR0**/ GPIO2_13/QSPI_B_DATA0	Channel 0	B18	IO	OV_{DD}	---
FTM6_CH1/**IFC_PAR1**/ GPIO2_14/QSPI_B_DATA1	Channel 1	D17	IO	OV_{DD}	---
FTM6_EXTCLK/**IFC_PERR_B**/ GPIO2_15/QSPI_B_DATA2	Ext Clock	E17	I	OV_{DD}	1
Frequency Timer Module 7					
FTM7_CH0/**IFC_CS1_B**/ GPIO2_10	Channel 0	A19	IO	OV_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM7_CH1/**IFC_CS2_B**/ GPIO2_11	Channel 1	D20	IO	OV_{DD}	---
FTM7_EXTCLK/**IFC_CS3_B**/ GPIO2_12/QSPI_B_DATA3	Ext Clock	C20	I	OV_{DD}	1
Frequency Timer Module 8					
FTM8_CH0/**IIC3_SCL**/ GPIO4_10/EVT5_B/ USB2_DRVVBUS/BRGO4/ CLK11	Channel 0	L4	IO	DV_{DD}	---
FTM8_CH1/**IIC3_SDA**/ GPIO4_11/EVT6_B/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Channel 1	M4	IO	DV_{DD}	---
LPUART					
LPUART1_CTS_B/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART4_SIN	Clear to send	M2	I	DV_{DD}	1
LPUART1_RTS_B/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3	Request to send	L1	O	DV_{DD}	1
LPUART1_SIN/**UART2_SIN**/ GPIO1_18/FTM4_CH1	Receive data	K1	I	DV_{DD}	1
LPUART1_SOUT/ **UART2_SOUT**/GPIO1_16/ FTM4_CH0	Transmit data	L2	IO	DV_{DD}	---
LPUART2_CTS_B/ **SDHC_DAT2**/GPIO2_07/ LPUART5_SIN/ FTM4_EXTCLK	Clear to send	R1	I	EV_{DD}	1
LPUART2_RTS_B/ **SDHC_DAT1**/GPIO2_06/ LPUART5_SOUT/ FTM4_FAULT	Request to send	R2	O	EV_{DD}	1
LPUART2_SIN/ **UART1_CTS_B**/GPIO1_21/ UART3_SIN/FTM4_CH4	Receive data	J1	I	DV_{DD}	1
LPUART2_SOUT/ **UART1_RTS_B**/GPIO1_19/ UART3_SOUT/FTM4_CH2	Transmit data	J2	IO	DV_{DD}	---
LPUART3_CTS_B/ **SDHC_CLK**/GPIO2_09/ LPUART6_SIN/ FTM4_QD_PHB	Clear to send	P3	I	EV_{DD}	1
LPUART3_RTS_B/ **SDHC_DAT3**/GPIO2_08/	Request to send	T1	O	EV_{DD}	1

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Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LPUART6_SOUT/ FTM4_QD_PHA					
LPUART3_SIN/**SDHC_DAT0**/ GPIO2_05/FTM4_CH7	Receive data	P1	I	EV_{DD}	1
LPUART3_SOUT/ **SDHC_CMD**/GPIO2_04/ FTM4_CH6	Transmit data	P2	IO	EV_{DD}	---
LPUART4_SIN/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B	Receive data	M2	I	DV_{DD}	1
LPUART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit data	L1	IO	DV_{DD}	---
LPUART5_SIN/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ FTM4_EXTCLK	Receive data	R1	I	EV_{DD}	1
LPUART5_SOUT/ **SDHC_DAT1**/GPIO2_06/ FTM4_FAULT/ LPUART2_RTS_B	Transmit data	R2	IO	EV_{DD}	---
LPUART6_SIN/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ FTM4_QD_PHB	Receive data	P3	I	EV_{DD}	1
LPUART6_SOUT/ **SDHC_DAT3**/GPIO2_08/ FTM4_QD_PHA/ LPUART3_RTS_B	Transmit data	T1	IO	EV_{DD}	---
QUICC Engine					
CLK10/**IIC2_SDA**/GPIO4_03/ SDHC_WP/FTM3_QD_PHB/ QE_SI1_STROBE1/BRGO3	CLK9	L3	I	DV_{DD}	1
CLK11/**IIC3_SCL**/GPIO4_10/ EVT5_B/USB2_DRVVBUS/ BRGO4/FTM8_CH0	Clock 11	L4	I	DV_{DD}	1
CLK12_CLK8/**IIC3_SDA**/ GPIO4_11/EVT6_B/ USB2_PWRFAULT/BRGO1/ FTM8_CH1	CLK8	M4	I	DV_{DD}	1
CLK9/**IIC2_SCL**/GPIO4_02/ SDHC_CD_B/FTM3_QD_PHA/ QE_SI1_STROBE0/BRGO2	CLK9	K3	I	DV_{DD}	1
QE_SI1_STROBE0/**IIC2_SCL**/ GPIO4_02/SDHC_CD_B/ FTM3_QD_PHA/CLK9/BRGO2	SI Strobe	K3	O	DV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QE_SI1_STROBE1/**IIC2_SDA**/GPIO4_03/SDHC_WP/FTM3_QD_PHB/CLK10/BRGO3	SI Strobe	L3	O	DV_{DD}	1
UC1_CDB_RXER/**IIC4_SCL**/GPIO4_12/EVT7_B/USB3_DRVVBUS/TDMA_RQ/FTM3_FAULT	Receive Error	M3	I	DV_{DD}	1
UC1_CTSB_RXDV/**IRQ05**/GPIO1_25/FTM3_CH1/TDMA_RSYNC	Receive Data	J5	I	DV_{DD}	1
UC1_RTSB_TXEN/**IRQ07**/GPIO1_27/FTM3_CH3/TDMA_TSYNC	Transmit Enable	L5	O	DV_{DD}	1
UC1_RXD7/**IRQ04**/GPIO1_24/FTM3_CH0/TDMA_RXD/TDMA_TXD	Receive Data	J4	I	DV_{DD}	1
UC1_TXD7/**IRQ06**/GPIO1_26/FTM3_CH2/TDMA_RXD_EXC/TDMA_TXD	Transmit Data	K5	O	DV_{DD}	1
UC3_CDB_RXER/**IIC4_SDA**/GPIO4_13/EVT8_B/USB3_PWRFAULT/TDMB_RQ/FTM3_EXTCLK	Receive Error	N3	I	DV_{DD}	1
UC3_CTSB_RXDV/**IRQ09**/GPIO1_29/FTM3_CH5/TDMB_RSYNC	Receive Data	N5	I	DV_{DD}	1
UC3_RTSB_TXEN/**IRQ03**/GPIO1_23/FTM3_CH7/TDMB_TSYNC	Transmit Enable	J3	O	DV_{DD}	1
UC3_RXD7/**IRQ08**/GPIO1_28/FTM3_CH4/TDMB_RXD/TDMB_TXD	Receive Data	M5	I	DV_{DD}	1
UC3_TXD7/**IRQ10**/GPIO1_30/FTM3_CH6/TDMB_RXD_EXC/TDMB_TXD	Transmit Data	P4	O	DV_{DD}	1
Baud rate generator					
BRGO1/**IIC3_SDA**/GPIO4_11/EVT6_B/USB2_PWRFAULT/FTM8_CH1/CLK12_CLK8	Baud Rate Generator 1	M4	O	DV_{DD}	1
BRGO2/**IIC2_SCL**/GPIO4_02/SDHC_CD_B/FTM3_QD_PHA/CLK9/QE_SI1_STROBE0	Baud Rate Generator 2	K3	O	DV_{DD}	1
BRGO3/**IIC2_SDA**/GPIO4_03/SDHC_WP/FTM3_QD_PHB/CLK10/QE_SI1_STROBE1	Baud Rate Generator 3	L3	O	DV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
BRGO4/**IIC3_SCL**/GPIO4_10/ EVT5_B/USB2_DRVVBUS/ FTM8_CH0/CLK11	Baud Rate Generator 4	L4	O	DV_{DD}	1
Time Division Multiplexing					
TDMA_RQ/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT/ UC1_CDB_RXER	RQ	M3	O	DV_{DD}	1
TDMA_RSYNC/**IRQ05**/ GPIO1_25/FTM3_CH1/ UC1_CTSB_RXDV	RSYNC	J5	I	DV_{DD}	1
TDMA_RXD/**IRQ04**/ GPIO1_24/FTM3_CH0/ UC1_RXD7/TDMA_TXD	RXD	J4	I	DV_{DD}	1
TDMA_RXD_EXC/**IRQ06**/ GPIO1_26/FTM3_CH2/ TDMA_TXD/UC1_TXD7	Recieve Data	K5	I	DV_{DD}	1
TDMA_TSYNC/**IRQ07**/ GPIO1_27/FTM3_CH3/ UC1_RTSB_TXEN	TSYNC	L5	I	DV_{DD}	1
TDMA_TXD/**IRQ04**/GPIO1_24/ FTM3_CH0/TDMA_RXD/ UC1_RXD7	Transmit Data	J4	O	DV_{DD}	1
TDMA_TXD/**IRQ06**/GPIO1_26/ FTM3_CH2/TDMA_RXD_EXC/ UC1_TXD7	Transmit Data	K5	O	DV_{DD}	1
TDMB_RQ/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK/ UC3_CDB_RXER	RQ	N3	O	DV_{DD}	1
TDMB_RSYNC/**IRQ09**/ GPIO1_29/FTM3_CH5/ UC3_CTSB_RXDV	RSYNC	N5	I	DV_{DD}	1
TDMB_RXD/**IRQ08**/ GPIO1_28/FTM3_CH4/ UC3_RXD7/TDMB_TXD	RXD	M5	I	DV_{DD}	1
TDMB_RXD_EXC/**IRQ10**/ GPIO1_30/FTM3_CH6/ TDMB_TXD/UC3_TXD7	Recieve Data	P4	I	DV_{DD}	1
TDMB_TSYNC/**IRQ03**/ GPIO1_23/FTM3_CH7/ UC3_RTSB_TXEN	TSYNC	J3	I	DV_{DD}	1
TDMB_TXD/**IRQ08**/GPIO1_28/ FTM3_CH4/TDMB_RXD/ UC3_RXD7	Transmit Data	M5	O	DV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TDMB_TXD/**IRQ10**/GPIO1_30/ FTM3_CH6/TDMB_RXD_EXC/ UC3_TXD7	Transmit Data	P4	O	DV_{DD}	1
TSEC_1588					
TSEC_1588_ALARM_OUT1/ **EC2_TXD2**/GPIO3_16/ FTM2_CH7	Alarm Out	AE3	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3**/GPIO3_15/ FTM2_CH5	Alarm Out	AD3	O	LV_{DD}	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK**/GPIO3_26/ FTM2_QD_PHA	Clock In	AC1	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ **EC2_TXD1**/GPIO3_17/ FTM2_CH3	Clock Out	AE4	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1**/GPIO3_24/ FTM2_CH1	Pulse Out	AE1	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0**/GPIO3_18/ FTM2_CH2	Pulse Out	AF3	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV**/GPIO3_27/ FTM2_QD_PHB	Trigger In	AF1	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0**/GPIO3_25/ FTM2_CH0	Trigger In	AE2	I	LV_{DD}	1
QSPI					
QSPI_A_CS0/**IFC_A16**	Chip Select	D8	O	OV_{DD}	1, 5
QSPI_A_CS1/**IFC_A17**	Chip Select	C8	O	OV_{DD}	1, 5
QSPI_A_DATA0/**IFC_A22**/ IFC_WP1_B	Data	D11	IO	OV_{DD}	---
QSPI_A_DATA1/**IFC_A23**/ IFC_WP2_B	Data	C12	IO	OV_{DD}	---
QSPI_A_DATA2/**IFC_A24**/ IFC_WP3_B	Data	D13	IO	OV_{DD}	---
QSPI_A_DATA3/**IFC_A25**/ GPIO2_25/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	Data	C13	IO	OV_{DD}	---
QSPI_A_SCK/**IFC_A18**	Serial Clock	C9	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A19**	Chip Select	D10	O	OV_{DD}	1, 5
QSPI_B_CS1/**IFC_A20**	Chip Select	C10	O	OV_{DD}	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_13/FTM6_CH0	Data	B18	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_14/FTM6_CH1	Data	D17	IO	OV_{DD}	---
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_15/ FTM6_EXTCLK	Data	E17	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_12/FTM7_EXTCLK	Data	C20	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_12/FTM7_EXTCLK	Data	C20	IO	OV_{DD}	---
QSPI_B_SCK/**IFC_A21**/ cfg_dram_type	Serial Clock	C11	O	OV_{DD}	1, 4
Power and Ground Signals					
GND001	GND	A2	---	---	---
GND002	GND	A5	---	---	---
GND003	GND	A21	---	---	---
GND004	GND	B3	---	---	---
GND005	GND	B4	---	---	---
GND006	GND	B7	---	---	---
GND007	GND	B10	---	---	---
GND008	GND	B13	---	---	---
GND009	GND	B16	---	---	---
GND010	GND	B19	---	---	---
GND011	GND	B21	---	---	---
GND012	GND	B24	---	---	---
GND013	GND	B26	---	---	---
GND014	GND	C1	---	---	---
GND015	GND	C2	---	---	---
GND016	GND	C5	---	---	---
GND017	GND	C21	---	---	---
GND018	GND	C27	---	---	---
GND019	GND	D3	---	---	---
GND020	GND	D4	---	---	---
GND021	GND	D7	---	---	---
GND022	GND	D9	---	---	---
GND023	GND	D12	---	---	---
GND024	GND	D15	---	---	---
GND025	GND	D18	---	---	---
GND026	GND	D21	---	---	---
GND027	GND	D24	---	---	---
GND028	GND	E1	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND029	GND	E2	---	---	---
GND030	GND	E5	---	---	---
GND031	GND	E21	---	---	---
GND032	GND	E26	---	---	---
GND033	GND	F3	---	---	---
GND034	GND	F4	---	---	---
GND035	GND	F7	---	---	---
GND036	GND	F14	---	---	---
GND037	GND	F16	---	---	---
GND038	GND	F18	---	---	---
GND039	GND	F24	---	---	---
GND040	GND	G1	---	---	---
GND041	GND	G2	---	---	---
GND042	GND	G9	---	---	---
GND043	GND	G10	---	---	---
GND044	GND	G11	---	---	---
GND045	GND	G21	---	---	---
GND046	GND	G26	---	---	---
GND047	GND	H3	---	---	---
GND048	GND	H4	---	---	---
GND049	GND	H5	---	---	---
GND050	GND	H14	---	---	---
GND051	GND	H15	---	---	---
GND052	GND	H16	---	---	---
GND053	GND	H17	---	---	---
GND054	GND	H18	---	---	---
GND055	GND	H21	---	---	---
GND056	GND	H24	---	---	---
GND057	GND	J6	---	---	---
GND058	GND	J7	---	---	---
GND059	GND	J8	---	---	---
GND060	GND	J9	---	---	---
GND061	GND	J10	---	---	---
GND062	GND	J11	---	---	---
GND063	GND	J12	---	---	---
GND064	GND	J21	---	---	---
GND065	GND	J23	---	---	---
GND066	GND	J26	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND067	GND	K2	---	---	---
GND068	GND	K4	---	---	---
GND069	GND	K6	---	---	---
GND070	GND	K13	---	---	---
GND071	GND	K15	---	---	---
GND072	GND	K17	---	---	---
GND073	GND	K19	---	---	---
GND074	GND	K21	---	---	---
GND075	GND	L6	---	---	---
GND076	GND	L10	---	---	---
GND077	GND	L12	---	---	---
GND078	GND	L14	---	---	---
GND079	GND	L16	---	---	---
GND080	GND	L18	---	---	---
GND081	GND	L20	---	---	---
GND082	GND	L23	---	---	---
GND083	GND	L26	---	---	---
GND084	GND	M6	---	---	---
GND085	GND	M9	---	---	---
GND086	GND	M11	---	---	---
GND087	GND	M13	---	---	---
GND088	GND	M15	---	---	---
GND089	GND	M17	---	---	---
GND090	GND	M19	---	---	---
GND091	GND	M21	---	---	---
GND092	GND	M23	---	---	---
GND093	GND	N2	---	---	---
GND094	GND	N4	---	---	---
GND095	GND	N6	---	---	---
GND096	GND	N8	---	---	---
GND097	GND	N10	---	---	---
GND098	GND	N12	---	---	---
GND099	GND	N14	---	---	---
GND100	GND	N16	---	---	---
GND101	GND	N18	---	---	---
GND102	GND	N20	---	---	---
GND103	GND	N23	---	---	---
GND104	GND	N26	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND105	GND	P6	---	---	---
GND106	GND	P9	---	---	---
GND107	GND	P11	---	---	---
GND108	GND	P13	---	---	---
GND109	GND	P15	---	---	---
GND110	GND	P17	---	---	---
GND111	GND	P19	---	---	---
GND112	GND	P23	---	---	---
GND113	GND	R4	---	---	---
GND114	GND	R5	---	---	---
GND115	GND	R8	---	---	---
GND116	GND	R10	---	---	---
GND117	GND	R12	---	---	---
GND118	GND	R14	---	---	---
GND119	GND	R16	---	---	---
GND120	GND	R18	---	---	---
GND121	GND	R20	---	---	---
GND122	GND	R23	---	---	---
GND123	GND	R26	---	---	---
GND124	GND	T2	---	---	---
GND125	GND	T4	---	---	---
GND126	GND	T6	---	---	---
GND127	GND	T9	---	---	---
GND128	GND	T11	---	---	---
GND129	GND	T13	---	---	---
GND130	GND	T15	---	---	---
GND131	GND	T17	---	---	---
GND132	GND	T19	---	---	---
GND133	GND	T21	---	---	---
GND134	GND	T23	---	---	---
GND135	GND	T26	---	---	---
GND136	GND	U6	---	---	---
GND137	GND	U8	---	---	---
GND138	GND	U10	---	---	---
GND139	GND	U12	---	---	---
GND140	GND	U14	---	---	---
GND141	GND	U16	---	---	---
GND142	GND	U18	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND143	GND	U20	---	---	---
GND144	GND	U23	---	---	---
GND145	GND	V2	---	---	---
GND146	GND	V4	---	---	---
GND147	GND	V6	---	---	---
GND148	GND	V9	---	---	---
GND149	GND	V11	---	---	---
GND150	GND	V13	---	---	---
GND151	GND	V15	---	---	---
GND152	GND	V21	---	---	---
GND153	GND	V23	---	---	---
GND154	GND	V26	---	---	---
GND155	GND	W12	---	---	---
GND156	GND	W22	---	---	---
GND157	GND	Y2	---	---	---
GND158	GND	Y13	---	---	---
GND159	GND	Y14	---	---	---
GND160	GND	Y21	---	---	---
GND161	GND	Y23	---	---	---
GND162	GND	Y26	---	---	---
GND163	GND	AA4	---	---	---
GND164	GND	AA14	---	---	---
GND165	GND	AA21	---	---	---
GND166	GND	AA24	---	---	---
GND167	GND	AB2	---	---	---
GND168	GND	AB12	---	---	---
GND169	GND	AB26	---	---	---
GND170	GND	AC21	---	---	---
GND171	GND	AC24	---	---	---
GND172	GND	AD2	---	---	---
GND173	GND	AD4	---	---	---
GND174	GND	AD26	---	---	---
GND175	GND	AE21	---	---	---
GND176	GND	AE24	---	---	---
GND177	GND	AF4	---	---	---
GND178	GND	AF21	---	---	---
GND179	GND	AF26	---	---	---
GND180	GND	AG1	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND181	GND	AG24	---	---	---
GND182	GND	AG26	---	---	---
GND183	GND	AH2	---	---	---
GND184	GND	AH21	---	---	---
SD_GND01	Serdes core logic GND	V17	---	---	34
SD_GND02	Serdes core logic GND	V19	---	---	34
SD_GND03	Serdes core logic GND	W18	---	---	34
SD_GND04	Serdes core logic GND	W20	---	---	34
SD_GND05	Serdes core logic GND	Y6	---	---	34
SD_GND06	Serdes core logic GND	Y7	---	---	34
SD_GND07	Serdes core logic GND	Y8	---	---	34
SD_GND08	Serdes core logic GND	Y9	---	---	34
SD_GND09	Serdes core logic GND	Y10	---	---	34
SD_GND10	Serdes core logic GND	Y15	---	---	34
SD_GND11	Serdes core logic GND	Y16	---	---	34
SD_GND12	Serdes core logic GND	AA5	---	---	34
SD_GND13	Serdes core logic GND	AA7	---	---	34
SD_GND14	Serdes core logic GND	AA9	---	---	34
SD_GND15	Serdes core logic GND	AA12	---	---	34
SD_GND16	Serdes core logic GND	AA17	---	---	34
SD_GND17	Serdes core logic GND	AA18	---	---	34
SD_GND18	Serdes core logic GND	AA19	---	---	34
SD_GND19	Serdes core logic GND	AB7	---	---	34
SD_GND20	Serdes core logic GND	AB9	---	---	34
SD_GND21	Serdes core logic GND	AB14	---	---	34
SD_GND22	Serdes core logic GND	AB17	---	---	34
SD_GND23	Serdes core logic GND	AB20	---	---	34
SD_GND24	Serdes core logic GND	AC5	---	---	34
SD_GND25	Serdes core logic GND	AC6	---	---	34
SD_GND26	Serdes core logic GND	AC8	---	---	34
SD_GND27	Serdes core logic GND	AC10	---	---	34
SD_GND28	Serdes core logic GND	AC11	---	---	34
SD_GND29	Serdes core logic GND	AC15	---	---	34
SD_GND30	Serdes core logic GND	AC16	---	---	34
SD_GND31	Serdes core logic GND	AC18	---	---	34
SD_GND32	Serdes core logic GND	AC19	---	---	34
SD_GND33	Serdes core logic GND	AD5	---	---	34
SD_GND34	Serdes core logic GND	AD7	---	---	34

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND35	Serdes core logic GND	AD9	---	---	34
SD_GND36	Serdes core logic GND	AD12	---	---	34
SD_GND37	Serdes core logic GND	AD14	---	---	34
SD_GND38	Serdes core logic GND	AD17	---	---	34
SD_GND39	Serdes core logic GND	AD20	---	---	34
SD_GND40	Serdes core logic GND	AE5	---	---	34
SD_GND41	Serdes core logic GND	AE7	---	---	34
SD_GND42	Serdes core logic GND	AE9	---	---	34
SD_GND43	Serdes core logic GND	AE12	---	---	34
SD_GND44	Serdes core logic GND	AE14	---	---	34
SD_GND45	Serdes core logic GND	AE17	---	---	34
SD_GND46	Serdes core logic GND	AE20	---	---	34
SD_GND47	Serdes core logic GND	AF6	---	---	34
SD_GND48	Serdes core logic GND	AF7	---	---	34
SD_GND49	Serdes core logic GND	AF8	---	---	34
SD_GND50	Serdes core logic GND	AF9	---	---	34
SD_GND51	Serdes core logic GND	AF10	---	---	34
SD_GND52	Serdes core logic GND	AF11	---	---	34
SD_GND53	Serdes core logic GND	AF15	---	---	34
SD_GND54	Serdes core logic GND	AF16	---	---	34
SD_GND55	Serdes core logic GND	AF17	---	---	34
SD_GND56	Serdes core logic GND	AF18	---	---	34
SD_GND57	Serdes core logic GND	AF19	---	---	34
SD_GND58	Serdes core logic GND	AG5	---	---	34
SD_GND59	Serdes core logic GND	AG7	---	---	34
SD_GND60	Serdes core logic GND	AG9	---	---	34
SD_GND61	Serdes core logic GND	AG12	---	---	34
SD_GND62	Serdes core logic GND	AG14	---	---	34
SD_GND63	Serdes core logic GND	AG17	---	---	34
SD_GND64	Serdes core logic GND	AG20	---	---	34
SD_GND65	Serdes core logic GND	AH5	---	---	34
SD_GND66	Serdes core logic GND	AH7	---	---	34
SD_GND67	Serdes core logic GND	AH9	---	---	34
SD_GND68	Serdes core logic GND	AH12	---	---	34
SD_GND69	Serdes core logic GND	AH14	---	---	34
SD_GND70	Serdes core logic GND	AH17	---	---	34
SD_GND71	Serdes core logic GND	AH20	---	---	34
SENSEGND	GND Sense pin	W5	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
OVDD1	General I/O supply	J14	---	OV_{DD}	---
OVDD2	General I/O supply	J15	---	OV_{DD}	---
OVDD3	General I/O supply	J16	---	OV_{DD}	---
OVDD4	General I/O supply	J17	---	OV_{DD}	---
OVDD5	General I/O supply	J18	---	OV_{DD}	---
OVDD6	General I/O supply	R7	---	OV_{DD}	---
DVDD1	UART/I2C/QE supply - switchable	N7	---	DV_{DD}	---
DVDD2	UART/I2C/QE supply - switchable	P7	---	DV_{DD}	---
EVDD	eSDHC supply - switchable	R6	---	EV_{DD}	---
LVDD1	Ethernet controller 1 & 2 supply	T7	---	LV_{DD}	---
LVDD2	Ethernet controller 1 & 2 supply	U7	---	LV_{DD}	---
LVDD3	Ethernet controller 1 & 2 supply	V7	---	LV_{DD}	---
TVDD	1.2V/LVDD supply for MDIO interface for 10G Fman (EC2)	W6	---	TV_{DD}	---
G1VDD01	DDR supply	B27	---	$G1V_{DD}$	---
G1VDD02	DDR supply	D27	---	$G1V_{DD}$	---
G1VDD03	DDR supply	F27	---	$G1V_{DD}$	---
G1VDD04	DDR supply	H27	---	$G1V_{DD}$	---
G1VDD05	DDR supply	K27	---	$G1V_{DD}$	---
G1VDD06	DDR supply	L22	---	$G1V_{DD}$	---
G1VDD07	DDR supply	M22	---	$G1V_{DD}$	---
G1VDD08	DDR supply	M27	---	$G1V_{DD}$	---
G1VDD09	DDR supply	N22	---	$G1V_{DD}$	---
G1VDD10	DDR supply	P22	---	$G1V_{DD}$	---
G1VDD11	DDR supply	P27	---	$G1V_{DD}$	---
G1VDD12	DDR supply	R22	---	$G1V_{DD}$	---
G1VDD13	DDR supply	T22	---	$G1V_{DD}$	---
G1VDD14	DDR supply	U22	---	$G1V_{DD}$	---
G1VDD15	DDR supply	U27	---	$G1V_{DD}$	---
G1VDD16	DDR supply	V22	---	$G1V_{DD}$	---
G1VDD17	DDR supply	W27	---	$G1V_{DD}$	---
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
S1VDD1	SerDes1 core logic supply	Y17	---	$S1V_{DD}$	---
S1VDD2	SerDes1 core logic supply	Y18	---	$S1V_{DD}$	---
S1VDD3	SerDes1 core logic supply	Y19	---	$S1V_{DD}$	---
X1VDD1	SerDes1 transceiver supply	AC14	---	$X1V_{DD}$	---
X1VDD2	SerDes1 transceiver supply	AC17	---	$X1V_{DD}$	---
X1VDD3	SerDes1 transceiver supply	AC20	---	$X1V_{DD}$	---
FA_VL	Reserved	U5	---	FA_VL	15
PROG_MTR	Reserved	F13	---	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	31
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	32
VDD01	Supply for cores and platform	K18	---	V_{DD}	---
VDD02	Supply for cores and platform	K20	---	V_{DD}	---
VDD03	Supply for cores and platform	L15	---	V_{DD}	---
VDD04	Supply for cores and platform	L17	---	V_{DD}	---
VDD05	Supply for cores and platform	L19	---	V_{DD}	---
VDD06	Supply for cores and platform	M10	---	V_{DD}	---
VDD07	Supply for cores and platform	M12	---	V_{DD}	---
VDD08	Supply for cores and platform	M14	---	V_{DD}	---
VDD09	Supply for cores and platform	M16	---	V_{DD}	---
VDD10	Supply for cores and platform	M18	---	V_{DD}	---
VDD11	Supply for cores and platform	N9	---	V_{DD}	---
VDD12	Supply for cores and platform	N11	---	V_{DD}	---
VDD13	Supply for cores and platform	N13	---	V_{DD}	---
VDD14	Supply for cores and platform	N15	---	V_{DD}	---
VDD15	Supply for cores and platform	N17	---	V_{DD}	---
VDD16	Supply for cores and platform	N19	---	V_{DD}	---
VDD17	Supply for cores and platform	P10	---	V_{DD}	---
VDD18	Supply for cores and platform	P12	---	V_{DD}	---
VDD19	Supply for cores and platform	P14	---	V_{DD}	---
VDD20	Supply for cores and platform	P16	---	V_{DD}	---
VDD21	Supply for cores and platform	P18	---	V_{DD}	---
VDD22	Supply for cores and platform	R9	---	V_{DD}	---
VDD23	Supply for cores and platform	R11	---	V_{DD}	---
VDD24	Supply for cores and platform	R13	---	V_{DD}	---
VDD25	Supply for cores and platform	R15	---	V_{DD}	---
VDD26	Supply for cores and platform	R17	---	V_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD27	Supply for cores and platform	R19	---	V_{DD}	---
VDD28	Supply for cores and platform	T10	---	V_{DD}	---
VDD29	Supply for cores and platform	T12	---	V_{DD}	---
VDD30	Supply for cores and platform	T14	---	V_{DD}	---
VDD31	Supply for cores and platform	T16	---	V_{DD}	---
VDD32	Supply for cores and platform	T18	---	V_{DD}	---
VDD33	Supply for cores and platform	U9	---	V_{DD}	---
VDD34	Supply for cores and platform	U11	---	V_{DD}	---
VDD35	Supply for cores and platform	U13	---	V_{DD}	---
VDD36	Supply for cores and platform	U15	---	V_{DD}	---
VDD37	Supply for cores and platform	U17	---	V_{DD}	---
VDD38	Supply for cores and platform	U19	---	V_{DD}	---
VDD39	Supply for cores and platform	V10	---	V_{DD}	---
VDD40	Supply for cores and platform	V12	---	V_{DD}	---
VDD41	Supply for cores and platform	V14	---	V_{DD}	---
VDD42	Supply for cores and platform	V16	---	V_{DD}	---
TA_BB_VDD	Battery Backed Security Monitor Supply	G12	---	TA_BB_V_{DD}	---
AVDD_CGA1	CPU Cluster Group A PLL1 supply.	H9	---	AVDD_CGA1	30
AVDD_CGA2	CPU Cluster Group A PLL2 supply.	H10	---	AVDD_CGA2	30
AVDD_PLAT	Platform PLL supply.	H11	---	AVDD_PLAT	30
AVDD_D1	DDR1 PLL supply.	R21	---	AVDD_D1	30
AVDD_SD1_PLL1	SerDes1 PLL 1 supply.	AA11	---	AVDD_SD1_PLL1	30
AVDD_SD1_PLL2	SerDes1 PLL 2 supply.	AA16	---	AVDD_SD1_PLL2	30
SENSEVDD	Vdd Sense pin	V5	---	SENSEVDD	---
USB_HVDD1	3.3V High Supply	K8	---	USB_HV$_{DD}$	---
USB_HVDD2	3.3V High Supply	L8	---	USB_HV$_{DD}$	---
USB_SDVDD1	1.0 V Analog and digital HS supply	M7	---	USB_SDV$_{DD}$	---
USB_SDVDD2	1.0 V Analog and digital HS supply	M8	---	USB_SDV$_{DD}$	---
USB_SVDD1	1.0 V Analog and digital SS supply	K7	---	USB_SV$_{DD}$	---
USB_SVDD2	1.0 V Analog and digital SS supply	L7	---	USB_SV$_{DD}$	---
No Connection Pins					
NC_A22	No Connection	A22	---	---	---
NC_A26	No Connection	A26	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_AA10	No Connection	AA10	---	---	---
NC_AA15	No Connection	AA15	---	---	---
NC_AA22	No Connection	AA22	---	---	---
NC_AA23	No Connection	AA23	---	---	---
NC_AA25	No Connection	AA25	---	---	---
NC_AA26	No Connection	AA26	---	---	---
NC_AA6	No Connection	AA6	---	---	---
NC_AB10	No Connection	AB10	---	---	---
NC_AB11	No Connection	AB11	---	---	---
NC_AB15	No Connection	AB15	---	---	---
NC_AB16	No Connection	AB16	---	---	---
NC_AB21	No Connection	AB21	---	---	---
NC_AB22	No Connection	AB22	---	---	---
NC_AB23	No Connection	AB23	---	---	---
NC_AB24	No Connection	AB24	---	---	---
NC_AB25	No Connection	AB25	---	---	---
NC_AB5	No Connection	AB5	---	---	---
NC_AB6	No Connection	AB6	---	---	---
NC_AC12	No Connection	AC12	---	---	---
NC_AC13	No Connection	AC13	---	---	---
NC_AC22	No Connection	AC22	---	---	---
NC_AC23	No Connection	AC23	---	---	---
NC_AC25	No Connection	AC25	---	---	---
NC_AC26	No Connection	AC26	---	---	---
NC_AC7	No Connection	AC7	---	---	---
NC_AC9	No Connection	AC9	---	---	---
NC_AD11	No Connection	AD11	---	---	---
NC_AD13	No Connection	AD13	---	---	---
NC_AD15	No Connection	AD15	---	---	---
NC_AD18	No Connection	AD18	---	---	---
NC_AD21	No Connection	AD21	---	---	---
NC_AD22	No Connection	AD22	---	---	---
NC_AD23	No Connection	AD23	---	---	---
NC_AD24	No Connection	AD24	---	---	---
NC_AD25	No Connection	AD25	---	---	---
NC_AD8	No Connection	AD8	---	---	---
NC_AE11	No Connection	AE11	---	---	---
NC_AE13	No Connection	AE13	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_AE15	No Connection	AE15	---	---	---
NC_AE18	No Connection	AE18	---	---	---
NC_AE22	No Connection	AE22	---	---	---
NC_AE23	No Connection	AE23	---	---	---
NC_AE25	No Connection	AE25	---	---	---
NC_AE26	No Connection	AE26	---	---	---
NC_AE8	No Connection	AE8	---	---	---
NC_AF14	No Connection	AF14	---	---	---
NC_AF22	No Connection	AF22	---	---	---
NC_AF23	No Connection	AF23	---	---	---
NC_AF24	No Connection	AF24	---	---	---
NC_AF25	No Connection	AF25	---	---	---
NC_AF5	No Connection	AF5	---	---	---
NC_AG11	No Connection	AG11	---	---	---
NC_AG13	No Connection	AG13	---	---	---
NC_AG15	No Connection	AG15	---	---	---
NC_AG18	No Connection	AG18	---	---	---
NC_AG21	No Connection	AG21	---	---	---
NC_AG22	No Connection	AG22	---	---	---
NC_AG23	No Connection	AG23	---	---	---
NC_AG25	No Connection	AG25	---	---	---
NC_AG8	No Connection	AG8	---	---	---
NC_AH11	No Connection	AH11	---	---	---
NC_AH13	No Connection	AH13	---	---	---
NC_AH15	No Connection	AH15	---	---	---
NC_AH18	No Connection	AH18	---	---	---
NC_AH22	No Connection	AH22	---	---	---
NC_AH23	No Connection	AH23	---	---	---
NC_AH24	No Connection	AH24	---	---	---
NC_AH25	No Connection	AH25	---	---	---
NC_AH26	No Connection	AH26	---	---	---
NC_AH8	No Connection	AH8	---	---	---
NC_B22	No Connection	B22	---	---	---
NC_B25	No Connection	B25	---	---	---
NC_G19	No Connection	G19	---	---	---
NC_G20	No Connection	G20	---	---	---
NC_K10	No Connection	K10	---	---	---
NC_K11	No Connection	K11	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_K12	No Connection	K12	---	---	---
NC_K14	No Connection	K14	---	---	---
NC_K16	No Connection	K16	---	---	---
NC_K22	No Connection	K22	---	---	---
NC_K9	No Connection	K9	---	---	---
NC_L11	No Connection	L11	---	---	---
NC_L13	No Connection	L13	---	---	---
NC_L21	No Connection	L21	---	---	---
NC_L9	No Connection	L9	---	---	---
NC_M20	No Connection	M20	---	---	---
NC_N21	No Connection	N21	---	---	---
NC_P20	No Connection	P20	---	---	---
NC_P5	No Connection	P5	---	---	---
NC_P8	No Connection	P8	---	---	---
NC_T20	No Connection	T20	---	---	---
NC_T8	No Connection	T8	---	---	---
NC_U21	No Connection	U21	---	---	---
NC_U24	No Connection	U24	---	---	---
NC_U25	No Connection	U25	---	---	---
NC_U26	No Connection	U26	---	---	---
NC_V18	No Connection	V18	---	---	---
NC_V20	No Connection	V20	---	---	---
NC_V24	No Connection	V24	---	---	---
NC_V25	No Connection	V25	---	---	---
NC_V8	No Connection	V8	---	---	---
NC_W10	No Connection	W10	---	---	---
NC_W11	No Connection	W11	---	---	---
NC_W13	No Connection	W13	---	---	---
NC_W14	No Connection	W14	---	---	---
NC_W15	No Connection	W15	---	---	---
NC_W16	No Connection	W16	---	---	---
NC_W17	No Connection	W17	---	---	---
NC_W19	No Connection	W19	---	---	---
NC_W21	No Connection	W21	---	---	---
NC_W23	No Connection	W23	---	---	---
NC_W24	No Connection	W24	---	---	---
NC_W25	No Connection	W25	---	---	---
NC_W26	No Connection	W26	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_W7	No Connection	W7	---	---	---
NC_W8	No Connection	W8	---	---	---
NC_W9	No Connection	W9	---	---	---
NC_Y12	No Connection	Y12	---	---	---
NC_Y22	No Connection	Y22	---	---	---
NC_Y24	No Connection	Y24	---	---	---
NC_Y25	No Connection	Y25	---	---	---
NC_Y5	No Connection	Y5	---	---	---

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 200Ω pull-up to respective power-supply.

12. Do not connect. These pins should be left floating.

14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698Ω pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. This pin should be connected to ground through 2-10kΩ resistor when not used.

19. This pin should be connected to ground through 2-10kΩ resistor when SYSCLK input is used as system clock.

21. This pin has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pin should have an optional pull down resistor on board. This is required to support DIFF_SYSCLK/DIFF_SYSCLK_B.

23. This pin must be pulled to OVDD through a 100-ohm to 1k-ohm resistor for a four core LS1043A device and tied to ground for a two core LS1023A device.

25. The alternate signal in DDR4 configuration is mentioned in corresponding Reference Manual.

27. Attach 200 Ohm +/-1% 100-ppm/C precision resistor-to-ground. Voltage range 0-250mV.

28. The permissible voltage range is 0 V - 5.25 V.

29. The permissible voltage range for input signal is 0 - 1.8 V.

30. It is measured at the input of the supply filter and not at the SoC pin.

31. Connect to ground when fuses are read-only.

32. TH_VDD must be tied to OVDD.

33. Recommend that a weak pull-down resistor (2-10 kΩ) be placed on this pin to GND.

34. SD_GND must be directly connected to GND.

35. This pin is used for debug purposes. It is advised that boards are built with the ability to pull up and pull down this pin.

36. This pin must be pulled down to ground with a resistor of value 4.7kohm.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 3. Absolute maximum ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3 to 1.08	V	4
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1, AV_{DD}_PLAT	-0.3 to 1.98	V	9
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)	AVDD_SD1_PLL1 AVDD_SD1_PLL2	-0.3 to 1.48	V	—
SFP Fuse Programming	TA_PROG_SFP	-0.3 to 1.98	V	—
Thermal Unit Monitor supply	TH_V_{DD}	-0.3 to 1.98	V	—
IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1, eSDHC[4-7]/VS/DAT123_DIR/DAT0_DIR/CMD_DIR/SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7, POR signals	OV_{DD}	-0.3 to 1.98	V	—

Table continues on the next page...

Table 3. Absolute maximum ratings[1] (continued)

Characteristic	Symbol	Max Value	Unit	Notes
DUART1/2, I^2C, DMA, QE, LPUART1, LPUART2_SOUT/SIN, LPUART4, GPIO1, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control (DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5	DV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	-
eSDHC[0-3]/CLK/CMD, GPIO2, LPUART2_CTS_B,LPUART2_RTS_B, LPUART3, LPUART5, LPUART6, FTM4_CH6/7, FTM4_EXTCLK/FAULT/QD_PHA/QD_PHB,	EV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	—
DDR3L DRAM I/O voltage DDR4 DRAM I/O voltage	$G1V_{DD}$	-0.3 to 1.42 -0.3 to 1.26	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{DD}$	-0.3 to 1.08	V	—
Pad power supply for SerDes transmitter	$X1V_{DD}$	-0.3 to 1.48	V	—
Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)	LV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
Ethernet management interface 2 (EMI2), GPIO4	TV_{DD}	-0.3 to 2.75 -0.3 to 1.98 -0.3 to 1.32	V	—
USB PHY Transceiver supply voltage	USB_HV_{DD}	-0.3 to 3.63	V	6
	USB_SDV_{DD}	-0.3 to 1.08	V	7
	USB_SV_{DD}	-0.3 to 1.08	V	8
Battery Backed Security Monitor supply	$TA\_BB\_V_{DD}$	-0.3 to 1.08	V	—
Storage temperature range	T_{STG}	-55 to 150	°C	--
Notes: See next table.				

This table provides the absolute maximum ratings for input signal voltage levels.

Table 4. Absolute maximum ratings for input signal voltage levels[1]

Interface Input signals	Symbol	Max DC V_input range (MAX_DC_IN)	Max undershoot and overshoot voltage range (MAX_OV_RNG)	Unit	Notes
DDR4 and DDR3L DRAM signals	MV_{IN}	GND to ($G1V_{DD}$ x 1.05)	-0.3 to ($G1V_{DD}$ x 1.1)	V	2, 3, 11
DDR3L DRAM reference	$D1\_MV_{REF}$	GND to ($G1V_{DD}$/2 x 1.05)	-0.3 to ($G1V_{DD}$/2 x 1.1)	V	2, 3
Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)	LV_{IN}	GND to (LV_{DD} x 1.1)	-0.3 to (LV_{DD} x 1.15)	V	2, 3
IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2,	OV_{IN}	GND to (OV_{DD} x 1.1)	-0.3 to (OV_{DD} x 1.15)	V	2, 3

Table continues on the next page...

Table 4. Absolute maximum ratings for input signal voltage levels[1] (continued)

Interface Input signals	Symbol	Max DC V_input range (MAX_DC_IN)	Max undershoot and overshoot voltage range (MAX_OV_RNG)	Unit	Notes
GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/CMD_DIR/ SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7, POR signals					
eSDHC[0-3]/CLK/CMD, GPIO2, LPUART2_CTS_B,LPUART2_RTS_B, LPUART3, LPUART5, LPUART6, FTM4_CH6/7, FTM4_EXTCLK/ FAULT/QD_PHA/QD_PHB	EV_{IN}	GND to (EV_{DD} x 1.1)	-0.3 to (EV_{DD} x 1.15)	V	2, 3
DUART1/2, I2C, DMA, QE, LPUART1, LPUART2_SOUT/SIN, LPUART4, GPIO1, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control (DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5	DV_{IN}	GND to (DV_{DD} x 1.1)	-0.3 to (DV_{DD} x 1.15)	V	2, 3
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{IN}$	GND to ($S1V_{DD}$ x 1.05)	-0.3 to ($S1V_{DD}$ x 1.1)	V	2, 3
USB PHY Transceiver signals	USB_HV_{IN}	GND to (USB_HV_{DD} x 1.05)	-0.3 to (USB_HV_{DD} x 1.15)	V	2, 3, 6
	USB_SV_{IN}	GND to (USB_SV_{DD} x 1.1)	-0.3 to (USB_SV_{DD} x 1.15)	V	2, 3, 8
	USB_SDV_{IN}	GND to (USB_SDV_{DD} x 1.1)	-0.3 to (USB_SDV_{DD} x 1.15)	V	2, 3, 7
Ethernet management interface 2 (EMI2), GPIO4	$TVDD_{IN}$	GND to ($TVDD_{DD}$ x 1.05)	-0.3 to ($TVDD_{DD}$ x 1.1)	V	2, 3

Notes:

1. Functional operating conditions are given in Recommended operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** The input voltage level of the signals must not exceed corresponding Max DC V_input range (MAX_DC_IN). For example DDR4 and DDR3L DRAM signals (MV_{IN}) must not exceed 5% of $G1V_{DD}$. Similarly, DDR3L DRAM reference ($D1\_MV_{REF}$) must not exceed 5% of ($G1V_{DD}$/2).

3. **Caution:** In case of overshoot/undershoot, the voltage may exceed corresponding MAX_DC_IN level, but it must not exceed corresponding MAX_OV_RNG for more than 10% of the Unit interval of the functional frequency. See the Overshoot/ Undershoot voltage figure in Recommended operating conditions

4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

6. Transceiver supply for USBPHY

7. Analog and Digital HS supply for USBPHY.

8. Analog and Digital SS supply for USBPHY.

9. AVDD_PLAT, AVDD_CGA1, AVDD_CGA2 and AVDD_D1 are measured at the input to the filter and not at the pin of the device. See the application note titled *LS1043A QorIQ Integrated Processor Design Checklist* (document AN5012).

10. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.

Table 4. Absolute maximum ratings for input signal voltage levels[1]

Interface Input signals	Symbol	Max DC V_input range (MAX_DC_IN)	Max undershoot and overshoot voltage range (MAX_OV_RNG)	Unit	Notes
11. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards.					

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 5. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	V_{DD}	0.9 V ± 30 mV 1.0 V ± 30 mV	V	3, 4, 5, 10
Battery backed security monitor supply	$TA\_BB\_V_{DD}$	0.9 V ± 30 mV 1.0 V ± 30 mV	V	10
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1, AV_{DD}_PLAT	1.8 V ± 90 mV	V	—
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)	AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2	1.35 V ± 67 mV	V	—
SFP Fuse Programming	TA_PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	
IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1, eSDHC[4-7]/VS/DAT123_DIR/DAT0_DIR/CMD_DIR/SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7, POR signals	OV_{DD}	1.8 V ± 90 mV	V	—
DUART1/2, I^2C, DMA, QE, LPUART1, LPUART2_SOUT/SIN, LPUART4, GPIO1, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control (DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5	DV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	6
eSDHC[0-3]/CLK/CMD, GPIO2, LPUART2_CTS_B,LPUART2_RTS_B, LPUART3, LPUART5,	EV_{DD}	3.3 V ±165 mV 1.8 V ± 90 mV	V	—

Table continues on the next page...

Table 5. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
LPUART6, FTM4_CH6/7, FTM4_EXTCLK/FAULT/QD_PHA/ QD_PHB					
DDR DRAM I/O voltage	DDR4	$G1V_{DD}$	1.2V ± 60 mV	V	—
	DDR3L		1.35 V ± 67 mV		
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		$S1V_{DD}$	0.9 V + 50 mV / - 30 mV 1.0 V + 50 mV / - 30 mV	V	10
Pad power supply for SerDes transmitters		$X1V_{DD}$	1.35 V ± 67 mV	V	—
Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)		LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2), GPIO4		TV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 1.2V ± 60 mV	V	
USB PHY Transceiver supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	6
		USB_SV_{DD}	0.9 V + 50 mV / - 30 mV 1.0 V + 50 mV / - 30 mV	V	8, 10
		USB_SDV_{DD}	0.9 V + 50 mV / - 30 mV 1.0 V + 50 mV / - 30 mV	V	7, 10
Input voltage	DDR3L and DDR4 DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	—
	DDR3L DRAM reference	$D1\_MV_{REF}$	$G1V_{DD}$/2 ± 1%	V	—
	Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)	LV_{IN}	GND to LV_{DD}	V	—
	IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7, POR signals	OV_{IN}	GND to OV_{DD}	V	—
	DUART1/2, I^2C, DMA, QE, LPUART1, LPUART2_SOUT/SIN,	DV_{IN}	GND to DV_{DD}	V	—

Table continues on the next page...

Table 5. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
	LPUART4, GPIO1, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control (DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5				
	eSDHC[0-3]/CLK/CMD, GPIO2, LPUART2_CTS_B,LPUART2_RTS_B, LPUART3, LPUART5, LPUART6, FTM4_CH6/7, FTM4_EXTCLK/FAULT/QD_PHA/QD_PHB	EV_{IN}	GND to EV_{DD}	V	—
	Main power supply for internal circuitry of SerDes	$S1V_{IN}$	GND to $S1V_{DD}$	V	—
	Ethernet management interface 2 (EMI2), GPIO4	TV_{IN}	GND to TV_{DD}	V	—
PHY Transceiver signals	USB Transceiver supply for USBPHY	USB_HV_{IN}	GND to USB_HV_{DD}	V	6
	Analog and Digital SS supply for USBPHY	USB_SV_{IN}	GND to USB_SV_{DD}	V	8
	Analog and Digital HS supply for USBPHY	USB_SDV_{IN}	0.3 to USB_SDV_{DD}	V	7
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105(max)	°C	—
	Extended temperature	T_A, T_J	T_A = -40 (min) to T_J = 105(max)	°C	9
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 105(max)	°C	2

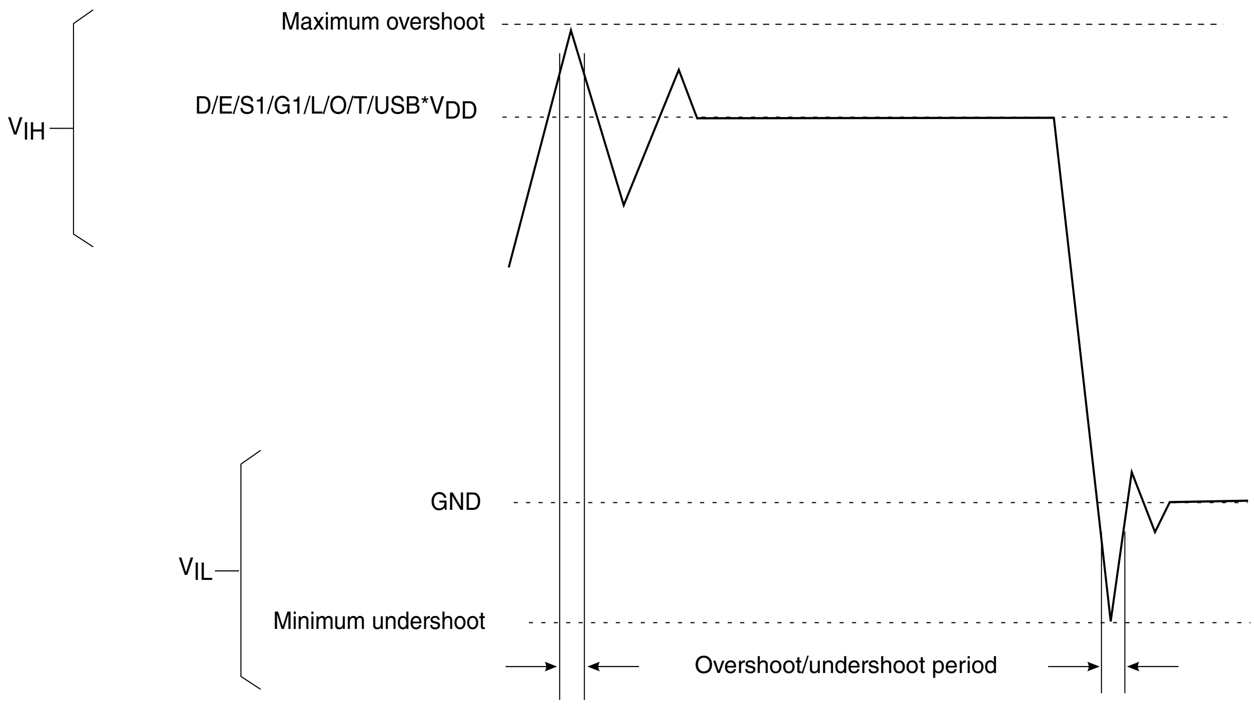
Notes:

1. RGMII is supported at 2.5 V or 1.8 V only.
2. TA_PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, TA_PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.
3. For supply filtering requirements, refer to "LS1043A QorIQ Integrated Processor Design Checklist (AN5012)".
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
5. Operation at 1.08V is allowable for up to 25 ms at initial power on.
6. Transceiver supply for USBPHY
7. Analog and Digital HS supply for USBPHY
8. Analog and Digital SS supply for USBPHY
9. Only valid in case of 1.0 V operation

Table 5. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
10. For part numbering nomenclature refer to Part numbering nomenclature.				

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 13. Overshoot/Undershoot voltage for $G1V_{DD}/OV_{DD}/S1V_{DD}/DV_{DD}/TV_{DD}/ LV_{DD}/EV_{DD}/ USB*V_{DD}$

See Table 5 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 5. The input voltage threshold scales with respect to the associated I/O supply voltage. DV_{DD}, EV_{DD}, OV_{DD}, and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied $D1\_MV_{REF}$ signal (nominally set to $G1V_{DD}/2$) as is appropriate for the SSTL_1.35/SSTL_1.2 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 6. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR4 signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
DDR3L signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.35 V	1
Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)	30	50	70	LV_{DD} = 2.5 V	
	30	45	60	LV_{DD} = 1.8 V	
MDC of Ethernet management interface 2 (EMI 2)	45	65	100	TV_{DD} = 1.2 V	-
	40	55	75	TV_{DD} = 1.8 V	
	40	60	90	TV_{DD} = 2.5 V	
MDIO of Ethernet management interface 2 (EMI 2)	30	40	60	TV_{DD} = 1.2 V	-
	25	33	44	TV_{DD} = 1.8 V	
	25	40	57	TV_{DD} = 2.5 V	
IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1, eSDHC[4-7]/VS/DAT123_DIR/ DAT0_DIR/CMD_DIR/SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7, POR signals	30	45	60	OV_{DD} = 1.8 V	-
DUART1/2, I^2C, DMA, QE, LPUART1, LPUART2_SOUT/SIN, LPUART4, GPIO1, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control (DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5	45	65	90	DV_{DD} = 3.3 V	-
	40	55	75	DV_{DD} = 1.8 V	
eSDHC[0-3]/CLK/CMD, GPIO2, LPUART2_CTS_B,LPUART2_RTS_B, LPUART3, LPUART5, LPUART6, FTM4_CH6/7, FTM4_EXTCLK/FAULT/QD_PHA/QD_PHB	45	65	90	EV_{DD} = 3.3 V	-
	40	55	75	EV_{DD} = 1.8 V	

1. The drive strength of the DDR4 or DDR3L interface in half-strength mode is at T_j = 105 °C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.1.4 General AC timing specifications

This table lists the AC timing specifications for the sections that are not covered under the specific interface sections.

Table 7. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1
1. Rise time refers to the signal transitions from 10% to 90% of supply and fall time refers to the signal transitions from 90% to 10% of supply.					

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure the proper device operation. For power up, these requirements are as follows:

1. AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, OV_{DD}, DV_{DD}, LV_{DD}, EV_{DD}, USB_HV_{DD}, TV_{DD}

   Drive TA_PROG_SFP = GND

   PORESET_B input must be driven asserted and held during this step.

2. V_{DD}, $S1V_{DD}$, TA_BB_V_{DD}, USB_SDV_{DD}, USB_SV_{DD}

   The 3.3 V (USB_HV_{DD}) in **Step 1** and 1.0 V (USB_SDV_{DD}, USB_SV_{DD}) in **Step 2** supplies can power up in any sequence, provided all these USB supplies ramp up within 10 ms with respect to each other.

3. a. When using DDR3L : $G1V_{DD}$, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 ramps up in Step 3.
   b. When using DDR4 : $G1V_{DD}$ ramps up in Step 3, whereas $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 may ramp up with Step 1 supplies.

AV_{DD}_SD1_PLL1 and AV_{DD}_SD1_PLL2 are derived from $X1V_{DD}$

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value.

NOTE

If using Trust Architecture Security Monitor battery backed features, prior to VDD ramping up to the 0.5 V level, ensure that OVDD is ramped to recommended operational voltage and SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is running. These clock should have a minimum frequency of 800 Hz and a maximum frequency no greater than the supported system clock frequency for the device.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time meets as listed in Table 27.

NOTE

- While V_{DD} is ramping up, current may be supplied from V_{DD} through the LS1043A processor to $G1V_{DD}$.
- Ramp rate requirements should meet as listed in Table 16.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. This value is based on design estimates and is preliminary.

For secure boot fuse programming, use the following steps:

1. After the negation of PORESET_B signal, drive TA_PROG_SFP = 1.8 V after a required minimum delay as listed in Table 8.
2. After the fuse programming is complete, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 8. For additional details, see the section Security fuse processor.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.

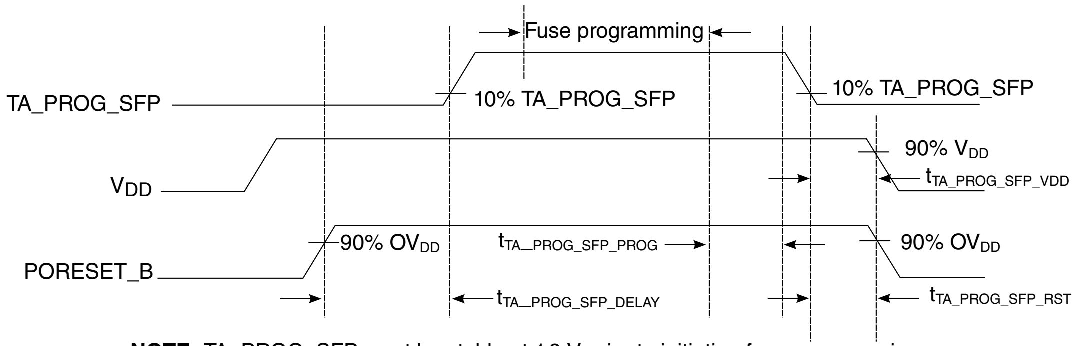


Figure 14. TA_PROG_SFP timing diagram

This table provides the information on the shut down and start up sequence parameters for TA_PROG_SFP.

Table 8. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	100	—	SYSCLKs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	—	us	2
$t_{TA\_PROG\_SFP\_VDD}$	0	—	us	3
$t_{TA\_PROG\_SFP\_RST}$	0	—	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

3. Delay required from TA_PROG_SFP ramp-down complete to V_{DD} ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} reaches 90% V_{DD}.

4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only six secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power down requirements

The shut down cycle must complete such that power supply values are below 0.4 V before a new start up cycle can be started.

If performing secure boot fuse programming as per the requirements listed in Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or shut down (V_{DD} ramp down) per the required timing specified in Power sequencing.

3.4 Power characteristics

This table shows the power dissipations of the V_{DD} supply for various operating platform clock frequencies versus the core and DDR clock frequencies. Note that these numbers are based on design estimates only and are preliminary.

Table 9. LS1043A core power dissipation (V_{DD} = 0.9 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1200	300	1300	0.9	0.9	65	Typical	2.44	0.36	2.80	2, 3
					105	Thermal	3.63	0.39	4.02	4, 7
						Maximum	4.29	0.39	4.68	5, 6, 7
1000	300	1300	0.9	0.9	65	Typical	2.34	0.36	2.70	2, 3
					105	Thermal	3.53	0.39	3.92	4, 7
						Maximum	3.95	0.39	4.34	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform at 100% activity factor.

5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.

6. Maximum and Maximum power is provided for power supply design sizing.

7. Thermal and maximum power are based on worst case processed device.

8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

Table 10. LS1043A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1600	400	1600	1.0	1.0	65	Typical	3.79	0.39	4.18	2, 3
					105	Thermal	6.67	0.39	7.06	4, 7
						Maximum	7.41	0.39	7.80	5, 6, 7
1400	300	1600	1.0	1.0	65	Typical	3.30	0.36	3.69	2, 3
					105	Thermal	5.18	0.39	5.57	4, 7
						Maximum	5.77	0.39	6.16	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	3.18	0.36	3.57	2, 3
					105	Thermal	5.06	0.39	5.45	4, 7
						Maximum	5.65	0.39	6.04	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	3.06	0.36	3.45	2, 3
					105	Thermal	4.94	0.39	5.33	4, 7
						Maximum	5.48	0.39	5.87	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform at 100% activity factor.

5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.

6. Maximum and Maximum power is provided for power supply design sizing.

7. Thermal and maximum power are based on worst case processed device.

8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

Table 11. LS1023A core power dissipation (V_{DD} = 0.9 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1200	300	1300	0.9	0.9	65	Typical	2.19	0.36	2.55	2, 3
					105	Thermal	3.18	0.39	3.57	4, 7
						Maximum	3.48	0.39	3.87	5, 6, 7
1000	300	1300	0.9	0.9	65	Typical	2.13	0.36	2.49	2, 3

Table continues on the next page...

Table 11. LS1023A core power dissipation (V_{DD} = 0.9 V) (continued)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
					105	Thermal	3.12	0.39	3.51	4, 7
						Maximum	3.40	0.39	3.79	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform at 100% activity factor.

5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.

6. Maximum power is provided for power supply design sizing.

7. Thermal and maximum power are based on worst case processed device.

8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

Table 12. LS1023A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1600	400	1600	1.0	1.0	65	Typical	3.30	0.39	3.69	2, 3
					105	Thermal	5.69	0.39	6.08	4, 7
						Maximum	6.16	0.39	6.55	5, 6, 7
1400	300	1600	1.0	1.0	65	Typical	2.86	0.39	3.25	2, 3
					105	Thermal	4.42	0.39	4.81	4, 7
						Maximum	4.80	0.39	5.19	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	2.78	0.39	3.17	2, 3
					105	Thermal	4.35	0.39	4.74	4, 7
						Maximum	4.73	0.39	5.12	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	2.71	0.39	3.10	2, 3
					105	Thermal	4.27	0.39	4.66	4, 7
						Maximum	4.64	0.39	5.03	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

Table 12. LS1023A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
2. Typical power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform with 100% activity factor.										
3. Typical power based on nominal, processed device.										
4. Thermal power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform at 100% activity factor.										
5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.										
6. Maximum power is provided for power supply design sizing.										
7. Thermal and maximum power are based on worst case processed device.										
8. Total $S1V_{DD}$ Power conditions:										
a. SerDes Lane 1, XFI@ 10G										
b. SerDes Lane 2 - 4, PCIe@ 5G										

3.5 Low power mode saving estimation

Refer to this table for low power mode savings.

Table 13. Low power mode savings, 0.9 V, 65C[1, 2, 3]

Mode	Core Frequency = 1.0 GHz	Core Frequency = 1.2 GHz	Units	Comments	Notes
PW15	0.03	0.04	Watts	Saving realized moving from run --> PW15 state, single core. ARM in STANDBYWFI/WFE	4
SWLPM20	0.16	0.19	Watts	Saving realized moving from PW15 --> SWLPM20 state, 4 cores. ARM in STANDBYWFI/WFE	5, 6
Notes:					
1. Power for VDD only					
2. Typical power assumes Dhrystone running with activity factor of 80%					
3. Typical power based on nominal process distribution for this device					
4. PW15 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores					
5. SWLPM20 has all platform clocks disabled					
6. SWLPM20 power saving with all the 4 cores in STANDBYWFI/WFE					

Table 14. Low power mode savings, 1.0 V, 65C[1, 2, 3]

Mode	Core Frequency = 1.0 GHz	Core Frequency = 1.2 GHz	Core Frequency = 1.4 GHz	Core Frequency = 1.6 GHz	Units	Comments	Notes
PW15	0.04	0.05	0.06	0.06	Watts	Saving realized moving from run --> PW15 state, single core. ARM in STANDBYWFI/WFE	4
SWLPM20	0.20	0.24	0.31	0.36	Watts	Saving realized moving from PW15 --> SWLPM20 state, 4 cores. ARM in STANDBYWFI/WFE	5, 6

Notes:

1. Power for VDD only
2. Typical power assumes Dhrystone running with activity factor of 80%
3. Typical power based on nominal process distribution for this device
4. PW15 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores
5. SWLPM20 has all platform clocks disabled
6. SWLPM20 power saving with all the 4 cores in STANDBYWFI/WFE

3.6 I/O power dissipation

This table provides the estimated I/O power numbers for each block: DDR, PCI Express, IFC, Ethernet controller, SGMII, eSDHC, USB, eSPI, DUART, IIC, SATA and GPIO. Note that these numbers are based on design estimates only.

Table 15. I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
DDR3L	1600 MT/s data rate	G1VDD (1.35 V)	630	1250	mW	1, 2, 6
DDR4	1600 MT/s data rate	G1VDD (1.2 V)	490	990	mW	1, 8, 9
PCI Express	x1, 2.5 GT/s	X1VDD (1.35 V)	80	86	mW	1, 4, 7
	x2, 2.5 GT/s		132	137		
	x4, 2.5 GT/s		237	242		
	x1, 5 GT/s		80	86		
	x2, 5 GT/s		133	138		
	x4, 5 GT/s		239	244		
SGMII	x1, 1.25 GBaud	X1VDD (1.35 V)	77	82	mW	1, 4, 7
	x2, 1.25 GBaud		127	136		
	x3, 1.25 GBaud		177	186		
	x4, 1.25 GBaud		227	235		

Table continues on the next page...

Table 15. I/O power supply estimated values (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
	x1, 3.125 GBaud		80	85		
	x2, 3.125 GBaud		132	140		
QSGMII	x1, 5 GBaud	X1VDD (1.35 V)	80	85	mW	1, 4, 7
XFI	x1, 10 GBaud	X1VDD (1.35 V)	81	87	mW	1, 4, 7
SATA (per port)	3.0 GBaud	X1VDD (1.35 V)	73	78	mW	1, 4, 7
	6.0 GBaud		74	79		
IFC	16-bit, 100 MHz	OVDD (1.8 V)	60	84	mW	1, 3, 7
EC1	RGMII	LVDD (2.5 V)	24	71	mW	1, 3, 7
	RGMII	LVDD (1.8 V)	17	42	mW	1, 3, 7
EC2	RGMII	LVDD (2.5 V)	24	71	mW	1, 3, 7
	RGMII	LVDD (1.8 V)	17	42		
eSDHC		EVDD (3.3 V)	19	39	mW	1, 3, 7
		EVDD (1.8 V)	19	42		
USB1, USB2, USB3		USB_HVDD (3.3 V)	138	201	mW	1, 3, 7
		USB_SVDD (1.0 V)	111	153		
		USB_SDVDD (1.0 V)	12	24		
SPI		OVDD (1.8 V)	8	14	mW	1, 3, 7
I2C		DVDD (3.3 V)	17	18	mW	1, 3, 7
		DVDD (1.8 V)	9	9		
DUART		DVDD (3.3 V)	18	23	mW	1, 3, 7
		DVDD (1.8 V)	9	10		
IEEE1588		LVDD (2.5 V)	14	34	mW	1, 3, 7
		LVDD (1.8 V)	10	21		
QE		DVDD (3.3 V)	39	79	mW	1, 3, 7
		DVDD (1.8 V)	19	31		
GPIO	x8	3.3 V	5	8	mW	1, 3, 5, 7
		2.5 V	4	7		
		1.8 V	3	5		
System Control		OVDD (1.8 V)	16	17	mW	1, 3, 7
PLL core and system		AVDD_CGA1, AVDD_CGA2, AVDD_PLAT (1.8 V)	30	30	mW	1, 3, 7
PLL DDR		AVDD_D1 (1.8 V)	30	40	mW	1, 3, 7
PLL SerDes		AVDD_SD1_PLL1, AVDD_SD1_PLL2 (1.35 V)	50	50	mW	1, 3, 7
PROG_SFP		PROG_SFP (1.8 V)	173	-	mW	1, 10
TH_VDD		TH_VDD (1.8 V)	18	-	mW	1
QSPI		OVDD (1.8 V)	2	5	mW	1
JTAG + DFT		OVDD (1.8 V)	10	15	mW	1

Table continues on the next page...

Table 15. I/O power supply estimated values (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
1. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming at 65° C junction temperature. 2. Typical DDR power numbers are based on 2 Rank DIMM with 40% utilization. 3. Assuming 15 pF total capacitance load per pin. 4. The total power numbers of X1VDD is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the X1VDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes. 5. GPIOs are supported on OV_{DD}, LV_{DD}, DV_{DD}, TV_{DD} and EV_{DD} power rails. 6. Maximum DDR3L/DDR4 power numbers are based on 2 Ranks DIMM with 100% utilization. 7. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105ºC junction temperature. 8. Typical DDR4 power numbers are based on single Rank DIMM with 40% utilization. 9. Maximum DDR4 power numbers are based on single Rank DIMM with 100% utilization. 10. The max power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.						

3.7 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 16. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/$G1V_{DD}$/ $S1V_{DD}$/$X1V_{DD}$/LV_{DD}/EV_{DD}/TV_{DD} all core and platform V_{DD} supplies, D*n*_MV_{REF}, TA_PROG_SFP, and all AV_{DD} supplies.)	--	25	V/ms	1, 2
Required ramp rate for PROG_SFP	--	25	V/ms	1,2
Required ramp rate for USB_HVDD	--	26.7	V/ms	1,2
Notes: 1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. 2. Over full recommended operating temperature range. See Table 5.				

3.8 Input clocks

3.8.1 System clock (SYSCLK)

This section describes the system clock DC electrical characteristics and AC timing specifications.

3.8.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 17. SYSCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.

2. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 5.

3.8.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 18. SYSCLK AC timing specifications[1, 7]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	64.0	—	100.0	MHz	2, 5, 6
SYSCLK cycle time	t_{SYSCLK}	10.0	—	15.6	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.

2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.

Table 18. SYSCLK AC timing specifications[1, 7]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.						
4. Phase noise is calculated as FFT of TIE jitter.						
5. The 64 MHz SYSCLK reference frequency support is specifically for QE requirements. It provides support for profibus for Industrial markets.						
6. The 100 MHz reference frequency is needed if USB is used. The reference clock to USB PHY is selectable between SYSCLK or DIFF_SYSCLK/DIF_SYSCLK_B. The selected clock must meet the clock specifications as mentioned in USB 3.0 reference clock requirements .						
7. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 5.						

3.8.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 19. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2
Notes:				
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 18.				
2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.				
3. At recommended operating conditions with OVDD = 1.8 V. See Table 5.				

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.8.3 Real-time clock timing (RTC)

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed. .

3.8.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 1.8 V.

Table 20. EC*n*_GTX_CLK125 DC electrical characteristics (LVDD = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	—	V	2
Input low voltage	V_{IL}	—	—	0.6	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3
Notes:						
1. For recommended operating conditions, refer to table Table 5.						
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 5.						
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.						

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V.

Table 21. EC*n*_GTX_CLK125 DC electrical characteristics (LVDD = 2.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	—	V	2
Input low voltage	V_{IL}	—	—	0.7	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3
Notes:						
1. For recommended operating conditions, refer to table Table 5.						
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 5.						

Table 21. ECn_GTX_CLK125 DC electrical characteristics (LVDD = 2.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.						

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 22. ECn_GTX_CLK125 AC timing specifications [1, 4]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}		8		ns	—
EC*n*_GTX_CLK125 rise and fall time LV_{DD} = 1.8 V LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	0.54 0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	4
EC*n*_GTX_CLK125 jitter	—	—	—	± 150	ps	4

Notes:

1. At recommended operating conditions with LV_{DD} = 1.8V/ 2.5V. See Table 5.

2. Rise and fall times for EC*n*_GTX_CLK125 are measured from 20% to 80% LV_{DD}

4. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.8.5 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.8.5.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 23. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

Table 23. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.						
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 5.						
3. At recommended operating conditions with OV_{DD} = 1.8 V. see Table 5.						

3.8.5.2 DDRCLK AC timing specifications

This table provides the DDRCLK AC timing specifications.

Table 24. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	64.0	—	100.0	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	10	—	15.6	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V. See Table 5.

3.8.6 Differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

Single Source clocking mode requires single onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/DIFF_SYSCLK_B).

This Differential clock pair input provides clock to Core, Platform, DDR and USB PLL's

This figure shows a receiver reference diagram of the Differential System clock.

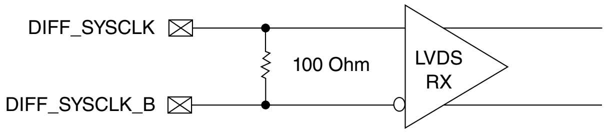


Figure 15. LVDS receiver

This section provides the differential system clock DC and AC timing specifications.

3.8.6.1 Differential system clock DC timing characteristics

The Differential System clock receiver voltage requirements are as specified in the Recommended operating conditions table.

The Differential system clock can also be single-ended. For this, DIFF_SYSCLK_B should be connected to OV_{DD}/2.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) DC specifications.

Table 25. Differential system clock DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage swing	V_{id}	100	-	600	mV	2
Input common mode voltage	V_{icm}	50	-	1570	mV	-
Power supply current	I_{cc}	-	-	5	mA	-
Input capacitance	C_{in}	1.45	1.5	1.55	pF	-
Note: 1. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 5 for details. 2. Input differential voltage swing (Vid) specified is equal to **|VDIFF_SYSCLK_P - VDIFF_SYSCLK_N|**						

3.8.6.2 Differential system clock AC timing specifications

Spread Spectrum clocking is not supported on Differential System clock pair input.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) AC specifications.

Table 26. Differential system clock AC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
DIFF_SYSCLK/DIFF_SYSCLK_B frequency range	t_{DIFF_SYSCLK}	-	100	-	MHz	-
DIFF_SYSCLK/DIFF_SYSCLK_B frequency tolerance	t_{DIFF_TOL}	-300	-	+300	ppm	-

Table continues on the next page...

Table 26. Differential system clock AC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Duty cycle	t_{DIFF_DUTY}	40	50	60	%	-
Clock period jitter (peak to peak)	t_{DIFF_TJ}	-	-	100	ps	1
Slew rate	t_{DIFF_slew}	0.5	-	4	V/ns	-

Note:

1. This is evaluated with supply noise profile at +/- 5% sine wave

2. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 5

3. The 100 MHz reference frequency is needed if USB is used. The reference clock to USB PHY is selectable between SYSCLK or DIFF_SYSCLK/DIF_SYSCLK_B. The selected clock must meet the clock specifications as mentioned in USB 3.0 reference clock requirements .

3.8.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, and IFC, see the specific interface section.

3.9 RESET initialization

This table provides the AC timing specifications for the RESET initialization timing.

Table 27. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B after VDD is stable	1	—	ms	1
Required input assertion time of HRESET_B	32	—	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	—	10	SYSCLK	4,5
Maximum rise/fall time of PORESET_B	—	1	SYSCLK	4,6
PLL input setup time with stable SYSCLK before HRESET_B negation	100	—	μs	—
Input setup time for POR configs with respect to negation of PORESET_B	4	—	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

2. SYSCLK is the primary clock input for the chip.

Table 27. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.				
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.				
5. For HRESET_B the rise/fall time should not exceed 10 SYSCLKs. Rise time refers to signal transitions from 20% to 70% of OVDD. Fall time refers to transitions from 70% to 20% of OVDD.				
6. For PORESET_B the rise/fall time should not exceed 1 SYSCLK. Rise time refers to signal transitions from 20% to 70% of OVDD. Fall time refers to transitions from 70% to 20% of OVDD.				

This table provides the phase-locked loop (PLL) lock times.

Table 28. PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (Core, platform, DDR only)	—	100	μs	—

3.10 DDR4 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 and DDR3L SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM and the $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.10.1 DDR4 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 29. DDR3L SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.35 V)[1, 9]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$D1\_MV_{REF}$	0.49 x $G1V_{DD}$	0.51 x $G1V_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	$D1\_MV_{REF}$ + 0.090	$G1V_{DD}$	V	5
Input low voltage	V_{IL}	GND	$D1\_MV_{REF}$ - 0.090	V	5
Output high current (V_{OUT} = 0.641V)	I_{OH}	-	-23.3	mA	7, 8
Output low current (V_{OUT} =0.641 V)	I_{OL}	23.3	-	mA	7, 8

Table continues on the next page...

Table 29. DDR3L SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.35 V)[1, 9] (continued)

Parameter	Symbol	Min	Max	Unit	Note
I/O leakage current	I_{OZ}	-165	165	μA	6

Notes:

1. $G1V_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The voltage supply of DRAM and memory controller may or may not be from the same source.

2. $D1\_MV_{REF}$ is expected to be equal to 0.5 x $G1V_{DD}$ and to track $G1V_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $D1\_MV_{REF}$ may not exceed the $D1\_MV_{REF}$ DC level by more than ±1% of $G1V_{DD}$ (that is, ±13.5mV).

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $D1\_MV_{REF}$ with a min value of $D1\_MV_{REF}$ - 0.04 and a max value of $D1\_MV_{REF}$ + 0.04. V_{TT} should track variations in the DC level of $D1\_MV_{REF}$.

4. The voltage regulator for $D1\_MV_{REF}$ must meet the specifications listed below in table "Current draw characteristics for D1_MVREF1".

5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.

6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$.

7. See the IBIS model for the complete output IV curve characteristics.

8. I_{OH} and I_{OL} are measured at $G1V_{DD}$ = 1.282 V.

9. For recommended operating conditions, refer to Table 5.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 30. DDR4 SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.2 V)[1, 8]

Parameter	Symbol	Min	Max	Unit	Note
Input low	V_{IL}	-	0.7 x $G1V_{DD}$ - 0.175	V	1, 3, 7
Input high	V_{IH}	0.7 x $G1V_{DD}$ + 0.175	-	V	1, 3, 7
Output high current (V_{OUT} = 0.57V)	I_{OH}	-	-20.7	mA	4, 5
Output low current (V_{OUT} =0.57V)	I_{OL}	20.7	-	mA	4, 5
I/O leakage current	I_{OZ}	-165	165	μA	6

Notes:

1. $G1V_{DD}$ is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.

2. V_{TT} and VREFCA are applied directly to the DRAM device. Both VTT and VREFCA voltages must track G1VDD/2.

3. Input capacitance load for MDQ, MDQS, and MDQS_B are available in the IBIS models.

4. I_{OH} and I_{OL} are measured at $G1V_{DD}$ = 1.14 V.

5. Refer to the IBIS model for the complete output IV curve characteristics.

6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$.

7. Internal Vref for data must be set to 0.7 x $G1V_{DD}$.

8. For recommended operating conditions, refer to Table 5.

This table provides the current draw characteristics for $D1\_MV_{REF}$.

Table 31. Current draw characteristics for $D1\_MV_{REF}$[1]

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3L SDRAM for $D1\_MV_{REF}$	I_{D1_MVREF}	-	500	μA	-
Note: 1. For recommended operating conditions, refer to Table 5.					

3.10.2 DDR4 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 and DDR3L memories. Note that the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM. The required $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.10.2.1 DDR4 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 32. DDR3L SDRAM interface input AC timing specifications[1]

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	-	D1_MVREF- 0.135	V	-
	≤ 1200 MT/s data rate			D1_MVREF- 0.160		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	D1_MVREF+ 0.135	-	V	-
	≤ 1200 MT/s data rate		D1_MVREF+ 0.160			
Notes: 1. For recommended operating conditions, see Table 5.						

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 33. DDR4 SDRAM interface input AC timing specifications[1]

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≤ 1600 MT/s data rate	V_{ILAC}	-	0.7 x G1VDD - 0.175	V	-

Table continues on the next page...

Table 33. DDR4 SDRAM interface input AC timing specifications[1] (continued)

Parameter		Symbol	Min	Max	Unit	Notes
AC input high voltage	≤ 1600 MT/s data rate	V_{IHAC}	0.7 x G1VDD + 0.175	-	V	-

Notes:

1. For recommended operating conditions, see Table 5.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L and DDR4 SDRAM.

Table 34. DDR4 and DDR3L SDRAM interface input AC timing specifications[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}			ps	
1600 MT/s data rate		-112	112		1
1300 MT/s data rate		-125	125		1
1200 MT/s data rate		-142	142		1, 4
1000 MT/s data rate		-170	170		1, 4
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}			ps	
1600 MT/s data rate		-200	200		2
1300 MT/s data rate		-250	250		2
1200 MT/s data rate		-275	275		2, 4
1000 MT/s data rate		-300	300		2, 4

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 5.

4. DDR3L only

This figure shows the DDR4 and DDR3L SDRAM interface input timing diagram.

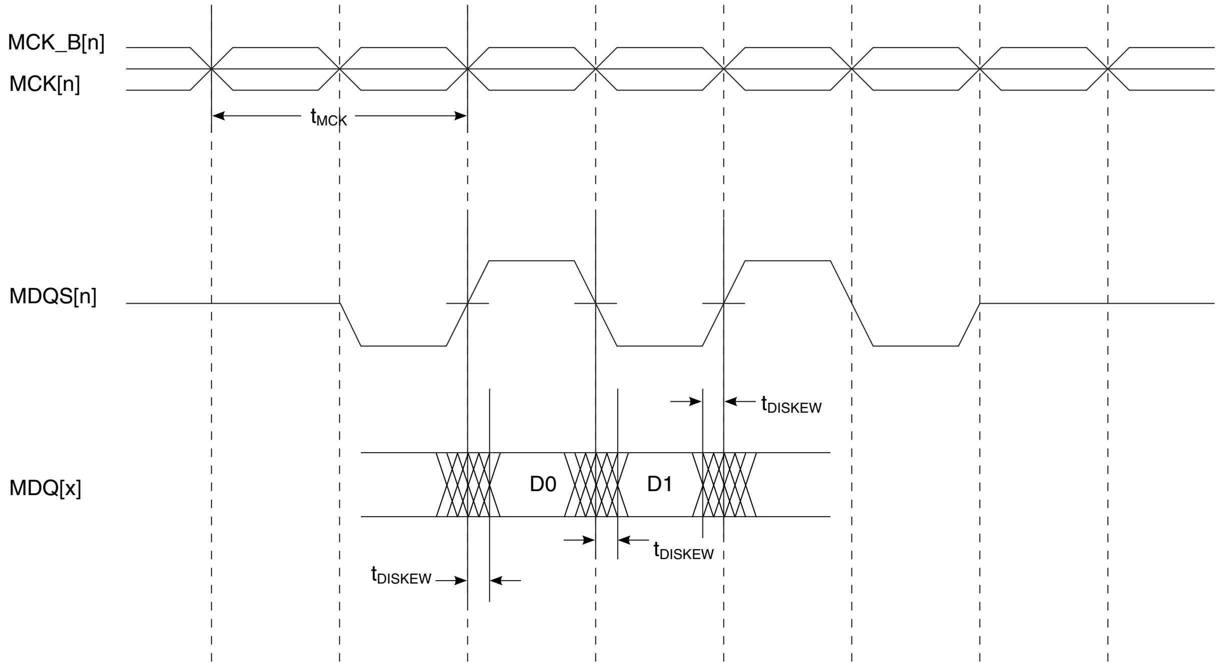


Figure 16. DDR4 and DDR3L SDRAM Interface Input Timing Diagram

3.10.2.2 DDR4 and DDR3L SDRAM interface output AC timing specifications

This table provides the output AC timing targets for the DDR4 and DDR3L SDRAM interface.

Table 35. DDR4 and DDR3L SDRAM interface output AC timing specifications[8]

Parameter		Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time		t_{MCK}	1250	2000	ps	2
ADDR/CMD/CNTL output setup with respect to MCK	1600 MT/s data rate	t_{DDKHAS}	495	—	ps	3
	1300 MT/s data rate		606	—		
	1200 MT/s data rate		675	—		3, 6
	1000 MT/s data rate		744	—		3, 6
ADDR/CMD/CNTL output hold with respect to MCK	1600 MT/s data rate	t_{DDKHAX}	495	—	ps	3
	1300 MT/s data rate		606	—		
	1200 MT/s data rate		675	—		3, 6

Table continues on the next page...

Table 35. DDR4 and DDR3L SDRAM interface output AC timing specifications[8] (continued)

Parameter		Symbol[1]	Min	Max	Unit	Notes
	1000 MT/s data rate		744	—		3, 6
MCK to MDQS Skew ≥ 1000 MT/s data rate, ≤ 1600 MT/s data rate		t_{DDKHMH}	-245	245	ps	4, 7
MDQ/MECC/MDM output Data eye	1600 MT/s data rate	$t_{DDKXDEYE}$,	400	—	ps	5
	1300 MT/s data rate		500	—		
	1200 MT/s data rate		550	—		5, 6
	1000 MT/s data rate		600	—		5, 6
MDQS preamble		t_{DDKHMP}	900 x t_{MCK}	—	ps	—
MDQS postamble		t_{DDKHME}	400 x t_{MCK}	600 x t_{MCK}	ps	—

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. DDR3L only.

7. Note that it is required to program the start value of the MDQS adjust for write leveling.

8. For recommended operating conditions, refer to table Table 5.

NOTE

For the ADDR/CMD setup and hold specifications in Recommended operating conditions, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR4 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

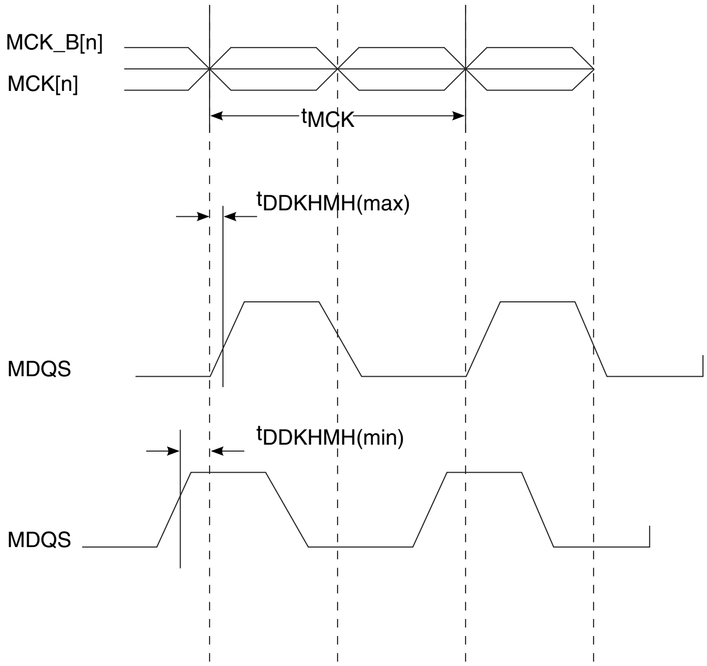


Figure 17. t_{DDKHMH} timing diagram

This figure shows the DDR4 and DDR3L SDRAM output timing diagram.

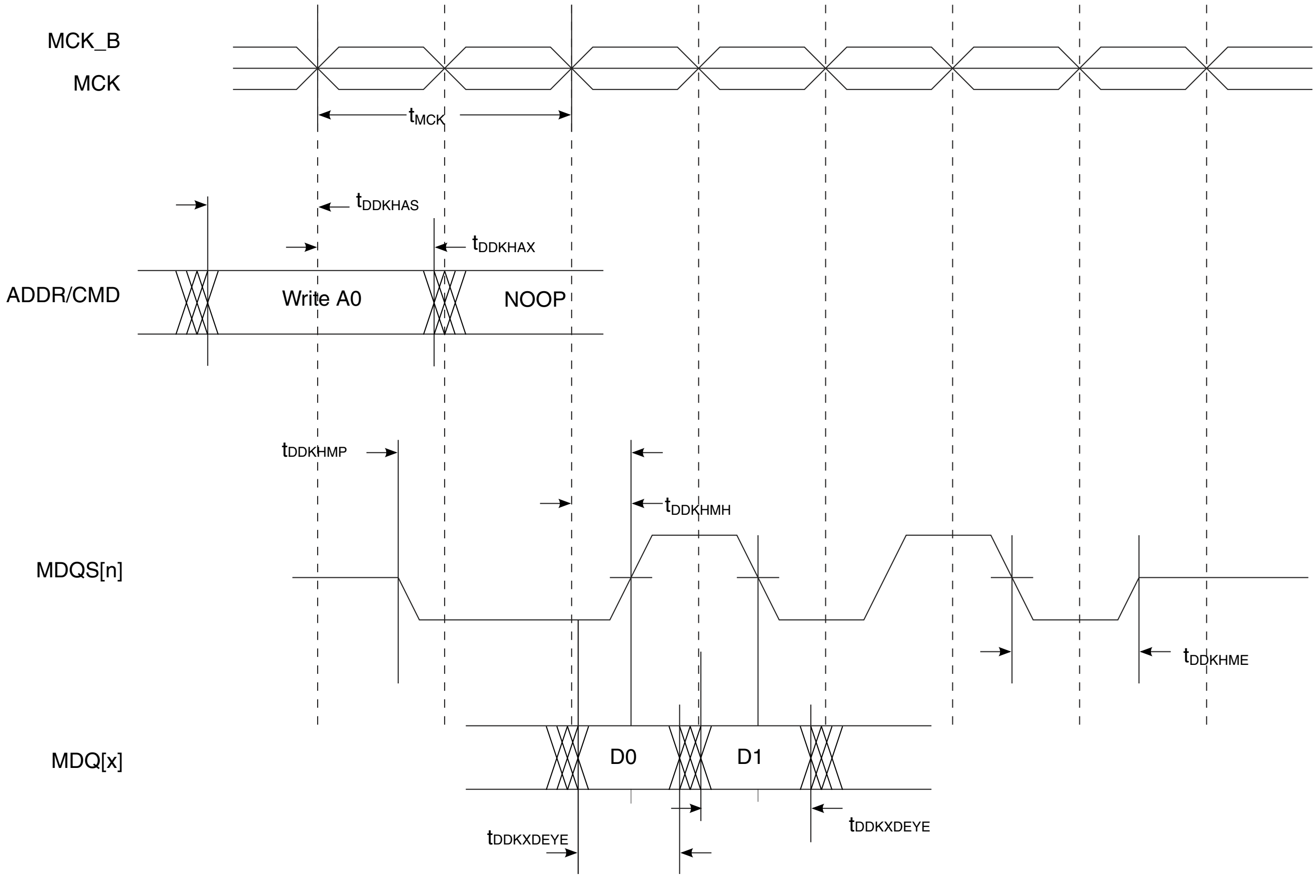


Figure 18. DDR4 and DDR3L output timing diagram

3.11 Ethernet interface, Ethernet management interface, IEEE Std 1588™

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, and IEEE Std 1588 interfaces.

3.11.1 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 19, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 94.

3.11.1.1 SGMII clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.11.1.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.11.1.2.1 SGMII and SGMII 2.5G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N)as shown in SGMII and SGMII 2.5G transmit DC specifications.

Table 36. SGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	LNmTECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		LNmTECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		LNmTECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		LNmTECR0[AMP_RED]=0b000010
		213.1	333.0	482.9		LNmTECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		LNmTECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		LNmTECR0[AMP_RED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD} \rvert = \lvert V_{SD\_TXn\_P} - V_{SD\_TXn\_N} \rvert$. $\lvert V_{OD} \rvert$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \lvert V_{OD} \rvert$.
3. The $\lvert V_{OD} \rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 5.
5. Example amplitude reduction setting for SGMII on lane A: LNaTECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

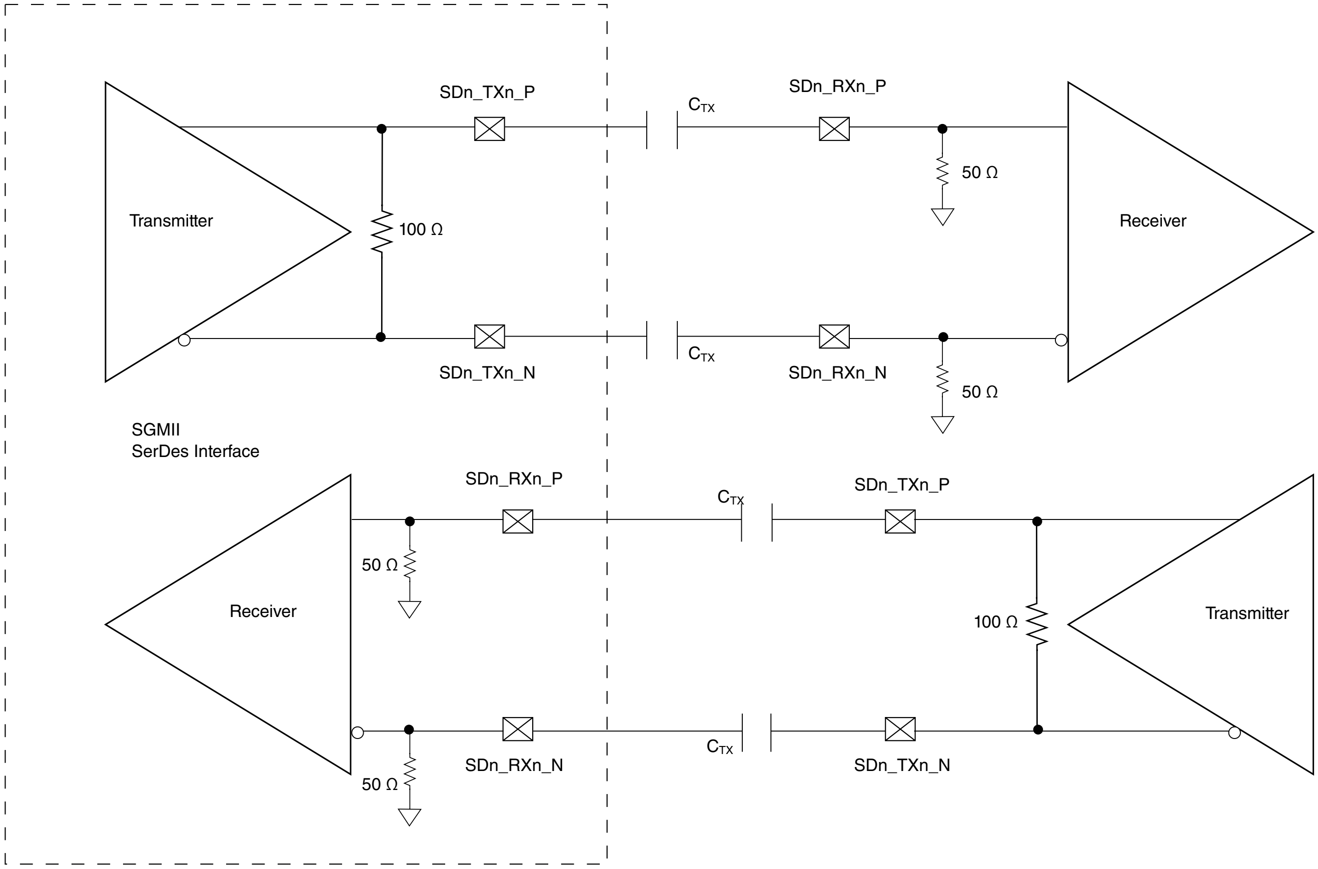


Figure 19. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

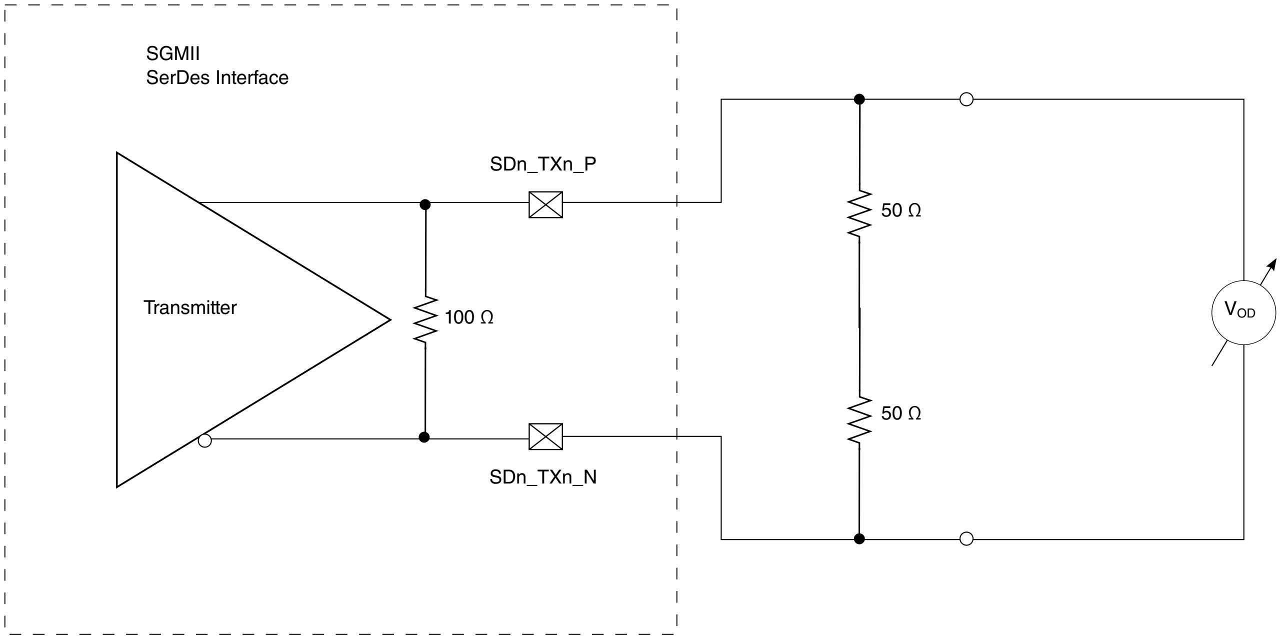


Figure 20. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 37. SGMII 2.5G transmitter DC electrical characteristics ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	-
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes:						
1. For recommended operating conditions, see Table 5.						

3.11.1.2.2 SGMII and SGMII 2.5G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 38. SGMII DC receiver electrical characteristics ($S1V_{DD}$)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp\text{-}p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		

Table continues on the next page...

Table 38. SGMII DC receiver electrical characteristics ($S1V_{DD}$)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-
Notes:						
1. Input must be externally AC coupled.						
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.						
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.						
4. For recommended operating conditions, see Table 5.						
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.						

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 39. SGMII 2.5G receiver DC timing specifications ($S1V_{DD}$)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp-p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-
Notes:						
1. For recommended operating conditions, see Table 5.						

3.11.1.3 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

3.11.1.3.1 SGMII and SGMII 2.5G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 40. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Table continues on the next page...

Table 40. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See SGMII and SGMII 2.5G receiver AC timing Specification for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 5.

3.11.1.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

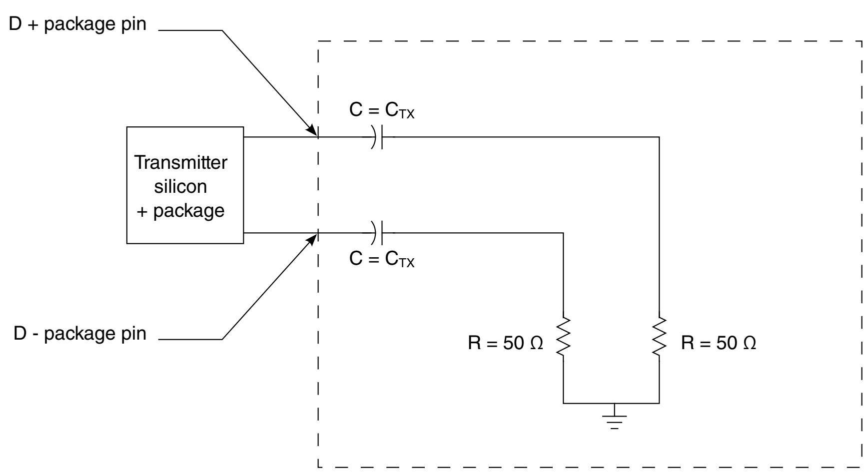


Figure 21. SGMII AC test/measurement load

3.11.1.3.3 SGMII and SGMII 2.5G receiver AC timing Specification

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 41. SGMII Receive AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1

Table continues on the next page...

Table 41. SGMII Receive AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver

2.Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of the figure given below. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 5.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

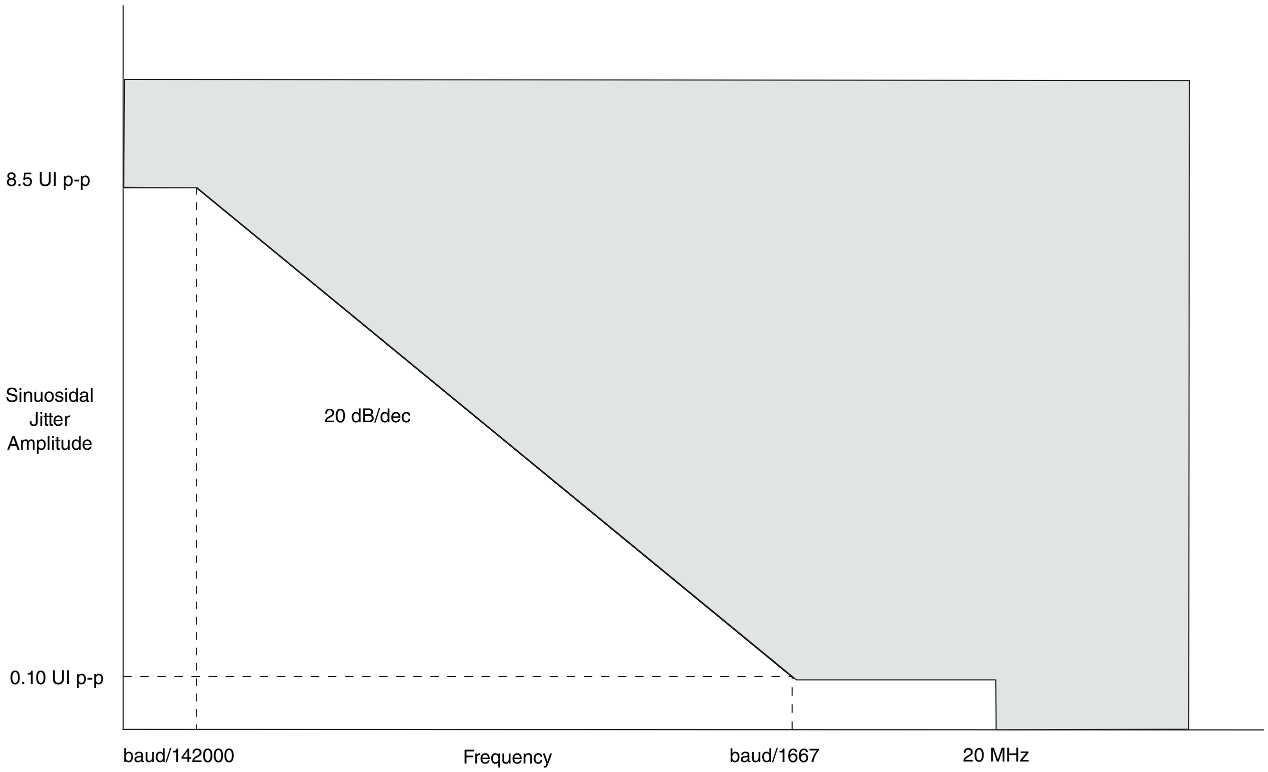


Figure 22. Single-frequency sinusoidal jitter limits

3.11.2 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.11.2.1 QSGMII clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

For more information on these specifications, see SerDes reference clocks.

3.11.2.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the QSGMII interface.

3.11.2.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 42. QSGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	900	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 5.						

3.11.2.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 43. QSGMII receiver DC timing specifications ($S1V_{DD}$)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	-	900	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 5.						

3.11.2.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.11.2.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 44. QSGMII transmit AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p	-
Total jitter tolerance	J_T	-	-	0.30	UI p-p	-

Notes:

1. For recommended operating conditions, see Table 5.

3.11.2.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

Table 45. QSGMII receive AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	$R_{SJ\text{-}max}$	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	$R_{SJ\text{-}hf}$	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-

Notes:

1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 5.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

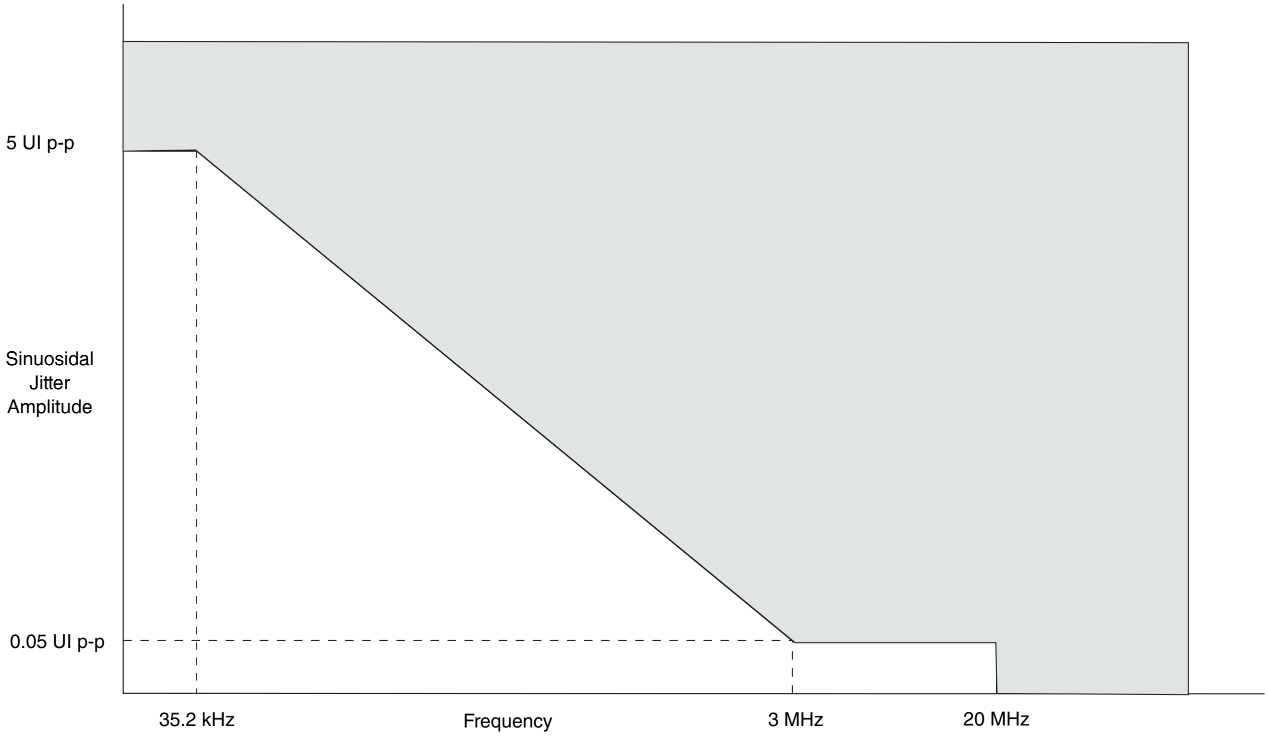


Figure 23. QSGMII single-frequency sinusoidal jitter limits

3.11.3 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.11.3.1 XFI clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

Only SerDes PLL1 (SD1_REF_CLK1_P and SD1_REF_CLK1_N) is allowed be used for XFI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.11.3.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.11.3.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 46. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX\text{-}DIFF}$	360	-	770	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 5.						

3.11.3.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 47. XFI receiver DC electrical characteristics ($S1V_{DD}$)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\text{-}DIFF}$	110	-	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	-
1. Measured at receiver 2. For recommended operating conditions, see Table 5.						

3.11.3.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.11.3.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 48. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
Notes:					
1. For recommended operating conditions, see Table 5.					

3.11.3.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 49. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	$T_{NON\text{-}EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2
1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J						
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.						
3. For recommended operating conditions, see Table 5.						

This figure shows the sinusoidal jitter tolerance of XFI receiver.

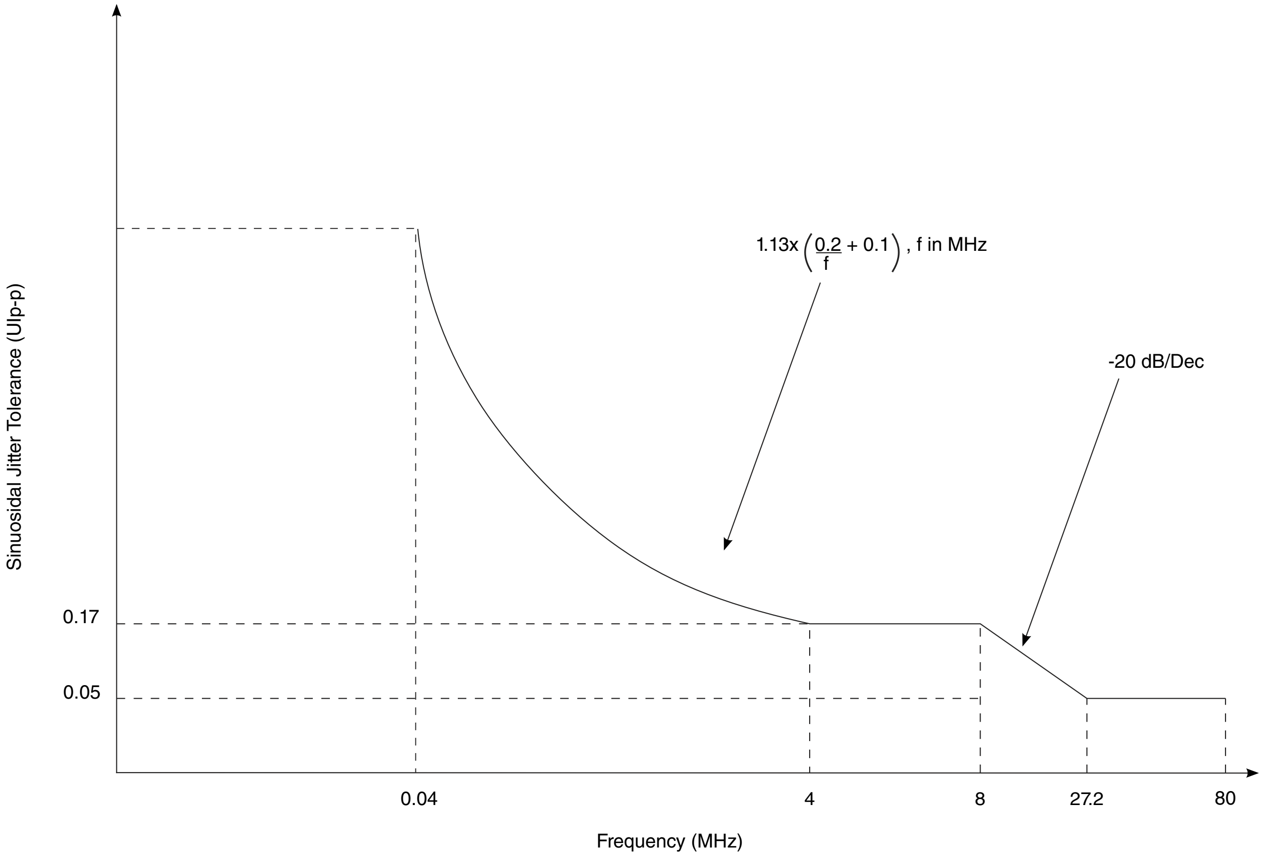


Figure 24. XFI host receiver input sinusoidal jitter tolerance

3.11.4 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC-coupled operation is supported.

3.11.4.1 1000Base-KX DC electrical characteristics

3.11.4.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TXn_P and SD1_TXn_N).

Table 50. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-
Notes: 1. SRDSxLNmTECR0[AMP_RED]=00_0000. 2. For recommended operating conditions, see Table 5.						

3.11.4.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 51. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-
Notes: 1. For recommended operating conditions, see Table 5.						

3.11.4.2 1000Base-KX AC electrical characteristics

3.11.4.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 52. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1
Notes: 1. Total jitter is specified at a BER of 10^{-12}. 2. For recommended operating conditions, see Table 5.						

3.11.4.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 53. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	$R_{SJ\text{-}max}$	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2

Notes:

1. Random jitter is specified at a BER of 10^{-12}.

2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.

3. Per IEEE 802.3ap-clause 70.

4. The AC specifications do not include Refclk jitter.

5. For recommended operating conditions, see Table 5.

3.11.5 RGMII electrical specifications

This section describes the electrical characteristics for the RGMII interface.

3.11.5.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 2.5 V.

Table 54. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN}=0 V or LV_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (LV_{DD} = min,I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	3

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.

2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.

Table 54. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
3. The symbol LV_{DD}, in this case, represents the LV_{DD} and symbol referenced in Table 5.					
4. For recommended operating conditions, see Table 5.					

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 1.8 V.

Table 55. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (LV_{IN} = 0 V or LV_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	3
Notes:					
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} values found in Table 5.					
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.					
3. The symbol LV_{DD}, in this case, represents the LV_{DD} symbol referenced in Table 5.					
4. For recommended operating conditions, see Table 5.					

3.11.5.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 56. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500	0	500	ps	7
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%-80%) LV_{DD} = 2.5V LV_{DD} = 1.8V	t_{RGTR}	—	—	— 0.75 0.54	ns	5, 6
Fall time (20%-80%) LV_{DD} = 2.5V LV_{DD} = 1.8V	t_{RGTF}	—	—	— 0.75 0.54	ns	5, 6
Notes:						

Table 56. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).						
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.						
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.						
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.						
5. Applies to inputs and outputs.						
6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.						
7. The frequency of EC*n*_RX_CLK (input) should not exceed the frequency of EC*n*_GTX_CLK (output) by more than 300 ppm.						
8. For recommended operating conditions, see Table 5.						

This figure shows the RGMII AC timing and multiplexing diagrams.

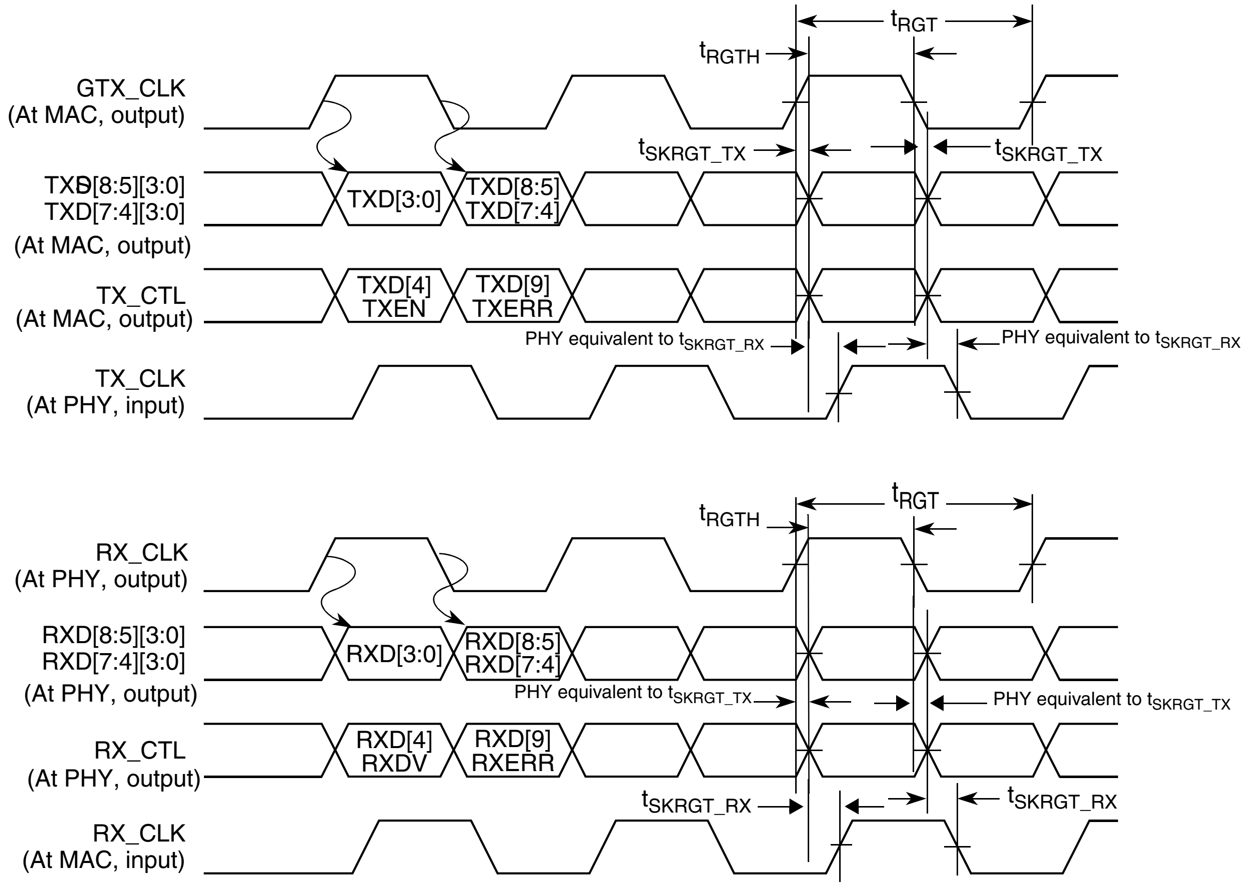


Figure 25. RGMII AC timing and multiplexing diagrams

Warning

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.6 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet Management Interface (EMI) interface.

Both the interfaces (EMI1 and EMI2) interface timing is compatible with IEEE Std 802.3™ clause 22.

3.11.6.1 Ethernet management interface 1 (EMI1)

This section describes the electrical characteristics for the EMI1 interface.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.11.6.1.1 EMI1 DC electrical characteristics

This section describes the DC electrical characteristics for EMI1_MDIO and EMI1_MDC. The pins are available on LV_{DD}. For operating voltages, see Table 5.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 2.5 V.

Table 57. EMI1 DC electrical characteristics (LV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 or LV_{IN} = LV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 5.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} symbols referenced in Table 5.
4. For recommended operating conditions, see Table 5.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 1.8 V.

Table 58. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	3

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} respective values found in Table 5.
2. The symbol LV_{IN} represents the LV_{IN} symbols referenced in Table 5.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} symbols referenced in Table 5.
4. For recommended operating conditions, see Table 5.

3.11.6.1.2 EMI1 AC timing specifications

This table provides the EMI1 AC timing specifications.

Table 59. EMI1 AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 4.8	—	(5 x t_{enet_clk}) + 4.6	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	2.75	—	—	ns	5

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.

4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).

5. For more details, see the application note titled *QorIQ LS1043A Design Checklist* (document AN5012).

6. For recommended operating conditions, see Table 5.

This figure shows the Ethernet management interface 1 timing diagram

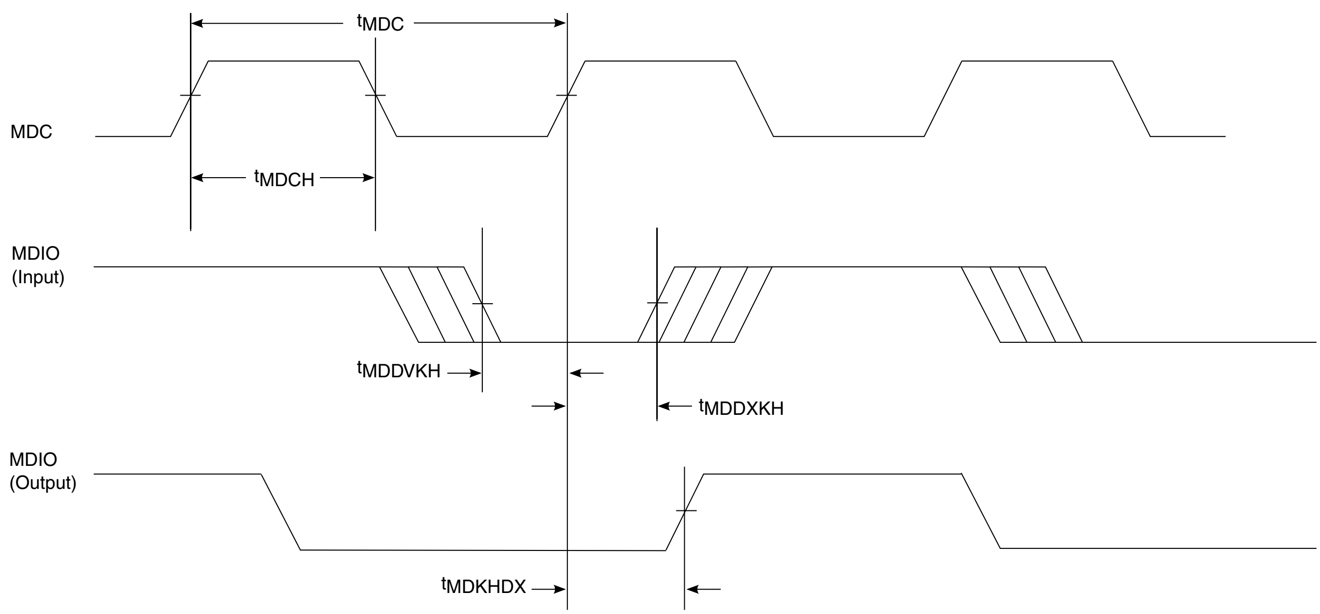


Figure 26. Ethernet management interface 1 timing diagram

3.11.6.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.11.6.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. For operating voltages, see Recommended operating conditions .

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 2.5 V.

Table 60. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 or TV_{IN} = TV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Recommended operating conditions.

2. The symbol V_{IN}, in this case, represents the TV_{IN} symbols referenced in Recommended operating conditions.

3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.

4. For recommended operating conditions, see Table 5.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.8 V.

Table 61. EMI2 DC electrical characteristics (TV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 V or TV_{IN} = TV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	3

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max TV_{IN} respective values found in Recommended operating conditions.

2. The symbol TV_{IN} represents the TV_{IN} symbols referenced in Recommended operating conditions.

3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.

4. For recommended operating conditions, see Table 5.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.2 V.

Table 62. EMI2 DC electrical characteristics (TV_{DD} = 1.2 V) [4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	—
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4		mA	—
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 100 uA)	V_{OL}	—	0.2	V	—
Input Capacitance	C_{IN}	—	10	pF	—

Notes:

1. For recommended operating conditions, see Table 5.

3.11.6.2.2 EMI2 AC timing specifications

This table provides the EMI2 AC timing specifications.

Table 63. EMI2 AC timing specifications at 2.5 MHz[7]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 115	—	(5 x t_{enet_clk}) + 115	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	90	—	—	ns	6
MDIO to MDC hold time	t_{MDDXKH}	2.75	—	—	ns	5

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 115 ns. Note that the reference is measured from falling edge of the clock.

4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).

5. For more details, see the application note titled *LS1043A Design Checklist* (document AN5012).

6. The setup time t_{MDDVKH} is measured at

a) 470pf load @ 1.2 V in open-drain configuration.

b) 300pf load @ 1.2 V in push-pull configuration.

7. For recommended operating conditions, see Table 5

This table provides the EMI2 AC timing specifications.

Table 64. EMI2 AC timing specifications at 10 MHz (TV_{DD} = 1.2V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	10	MHz	2
MDC clock pulse width high	t_{MDCH}	35	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 30	—	(5 x t_{enet_clk}) + 20	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	30	—	—	ns	6
MDIO to MDC hold time	t_{MDDXKH}	2.75	—	—	ns	5

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 115 ns. Note that the reference is measured from falling edge of the clock.

4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).

5. For more details, see the application note titled *LS1043A Design Checklist* (document AN5012).

6. The setup time t_{MDDVKH} is measured at 75pf load.

7. Valid for open-drain and push-pull configuration.

8. For recommended operating conditions, see Table 5

This figure shows the Ethernet management interface 2 timing diagram

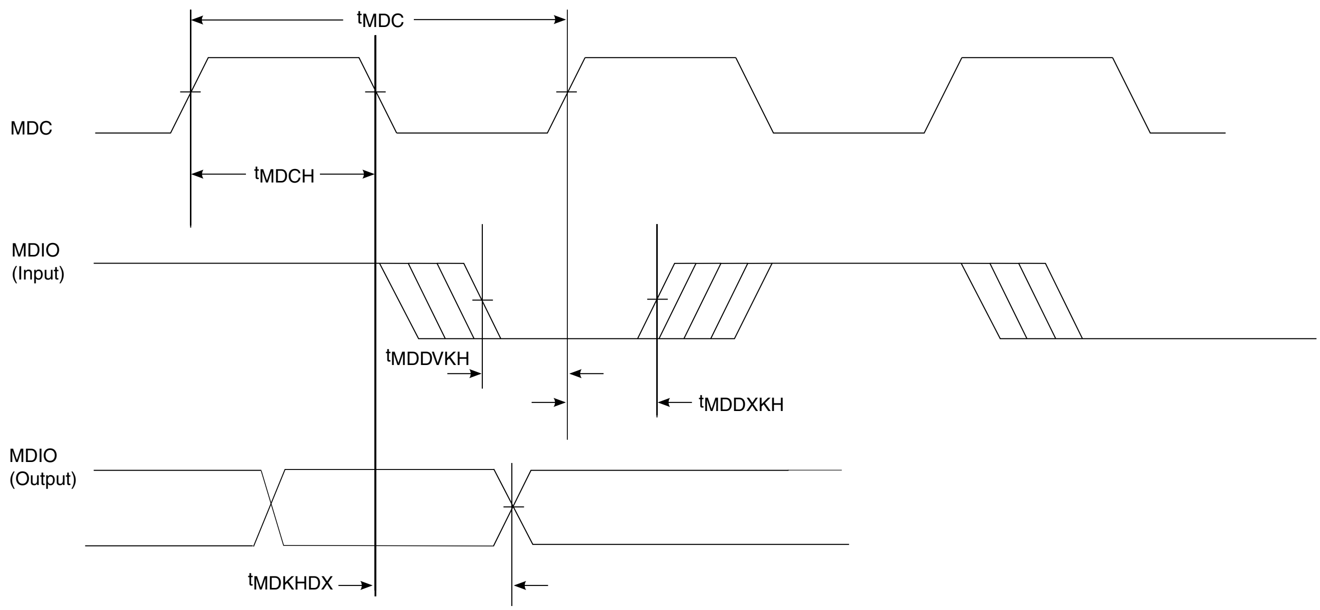


Figure 27. Ethernet management interface 2 timing diagram

3.11.7 IEEE 1588 electrical specifications

3.11.7.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 65. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 66. IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.11.7.2 IEEE 1588 AC timing specifications

This table provides the IEEE 1588 AC timing specifications.

Table 67. IEEE 1588 AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	5.0	—	T_{RX_CLK} x 7	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK_IN (20%-80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK_IN (80%-20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	—	—	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK\_MAX}$	—	—	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of the ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

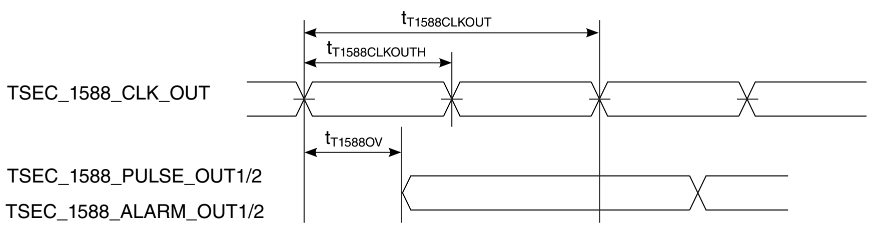
2. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.

4. There are three input clock sources for 1588: TSEC_1588_CLK_IN, RTC, and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$.

5. For recommended operating conditions, see Table 5.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 28. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

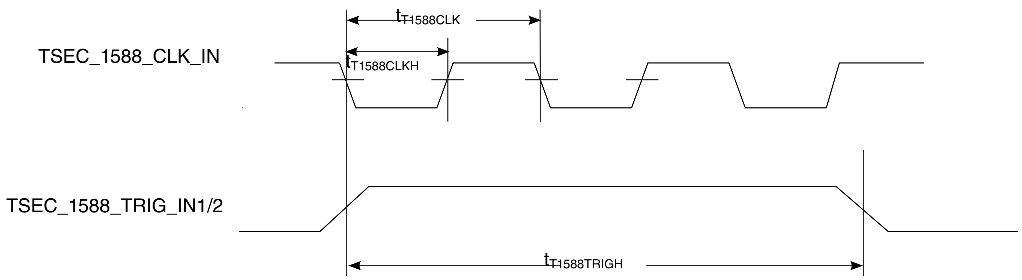


Figure 29. IEEE 1588 input AC timing

3.12 QUICC engine specifications

The rise/fall time on QUICC engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}. Fall time refers to transitions from 90% to 10% of V_{DD}.

3.12.1 HDLC interface

This section describes the DC and AC electrical specifications for the high-level data link control (HDLC) interface.

3.12.1.1 HDLC and Synchronous UART DC electrical characteristics

This table provides the DC electrical characteristics for the HDLC and Synchronous UART protocols when DV_{DD} = 3.3 V.

Table 68. HDLC and Synchronous UART DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for the HDLC and Synchronous UART protocols when DV_{DD} = 1.8 V.

Table 69. HDLC and Synchronous UART DC electrical characteristics (DV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OH} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.12.1.2 HDLC and Synchronous UART AC timing specifications

This table provides the input and output AC timing specifications for HDLC and Synchornous UART protocols.

Table 70. HDLC AC timing specifications[2]

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	5.5	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	10.5	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns	1
Outputs-External clock High Impedance	t_{HEKHOX}	1	8	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs-External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	—	ns	—
Inputs-External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 5.

This table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 71. Synchronous UART AC timing specifications[2]

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	11	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	14	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	11	ns	1

Table continues on the next page...

Table 71. Synchronous UART AC timing specifications[2] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-External clock High Impedance	t_{HEKHOX}	1	14	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs-External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	—	ns	—
Inputs-External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2. For recommended operating conditions, see Table 5.

This figure shows the AC test load.

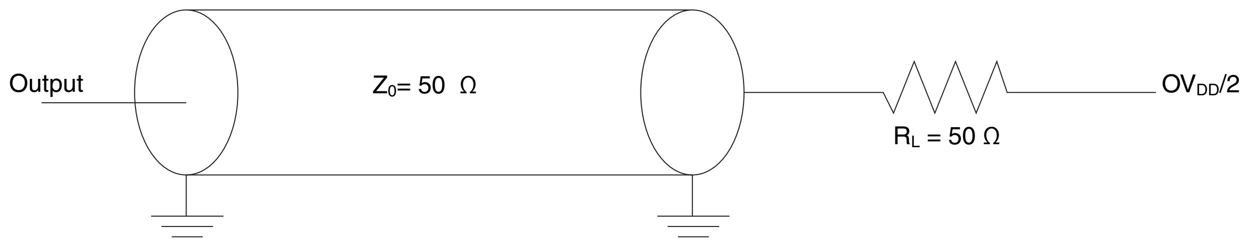


Figure 30. AC test load

These figures represent the AC timing from Table 70 and Table 71. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with an external clock.

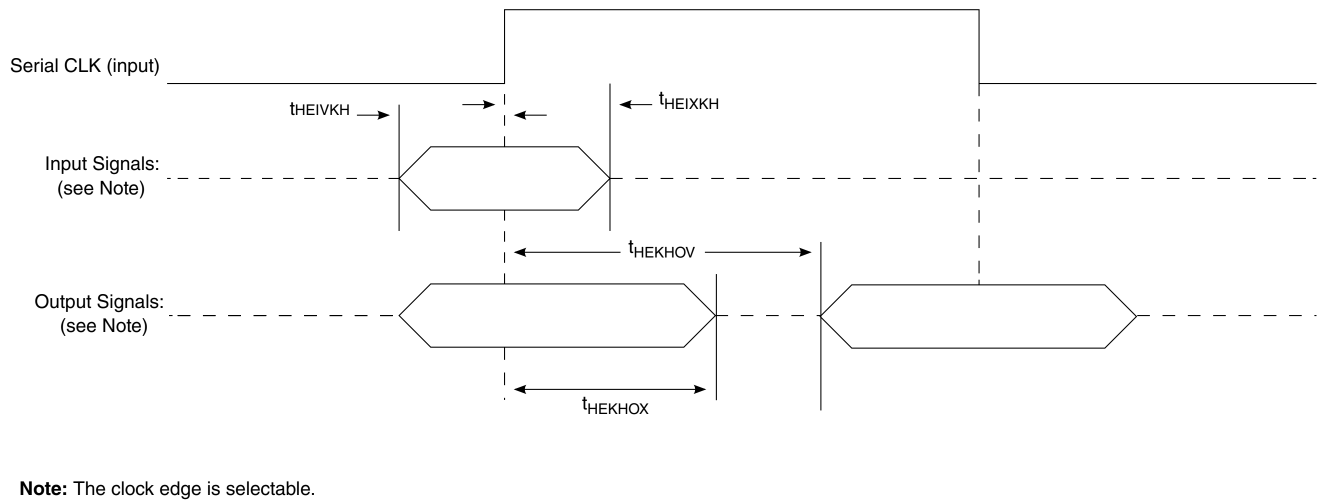


Figure 31. AC timing (external clock) diagram

This figure shows the timing with an internal clock.

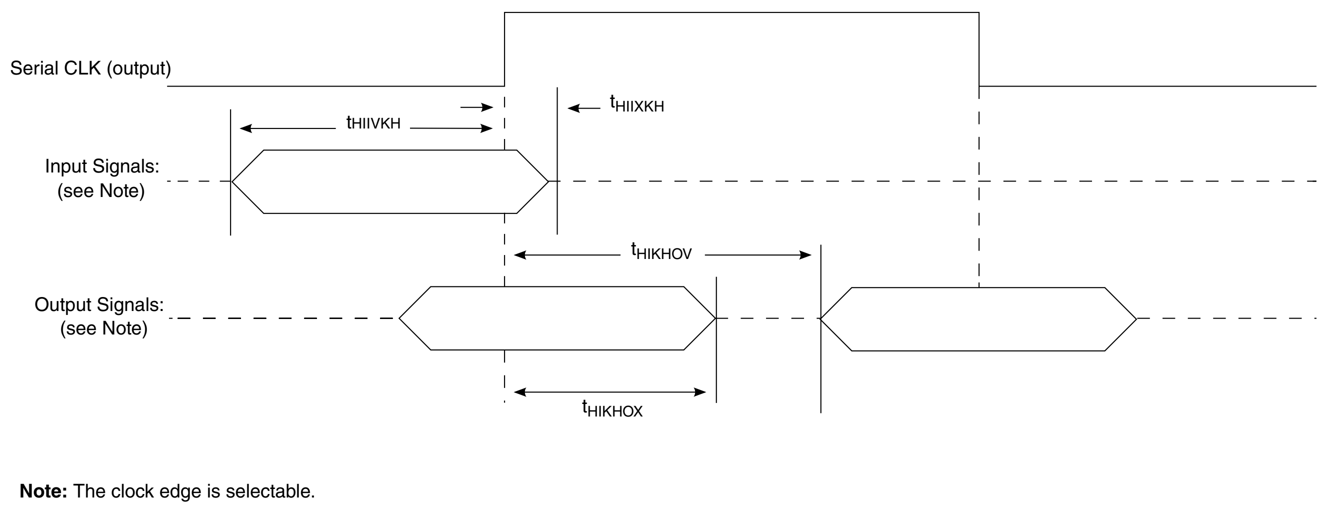


Figure 32. AC timing (internal clock) diagram

3.12.2 Time-division-multiplexed and serial interface (TDM/SI)

This section describes the DC and AC electrical specifications for the TDM/SI.

3.12.2.1 TDM/SI DC electrical characteristics

This table provides the TDM/SI DC electrical characteristics when DV_{DD} = 3.3 V.

Table 72. TDM/SI DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the TDM/SI DC electrical characteristics when DV_{DD} = 1.8 V.

Table 73. TDM/SI DC electrical characteristics (DV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OH} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.12.2.2 TDM/SI AC timing specifications

This table provides the TDM/SI input and output AC timing specifications.

Table 74. TDM/SI AC timing specifications [1]

Parameter	Symbol [1]	Min	Max	Unit
TDM/SI outputs-External clock delay	t_{SEKHOV}	2	12.75	ns
TDM/SI outputs-External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs-External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs-External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure shows the AC test load for the TDM/SI.

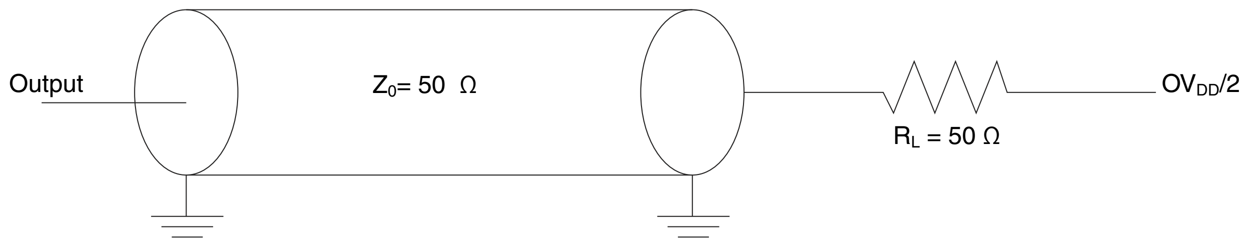
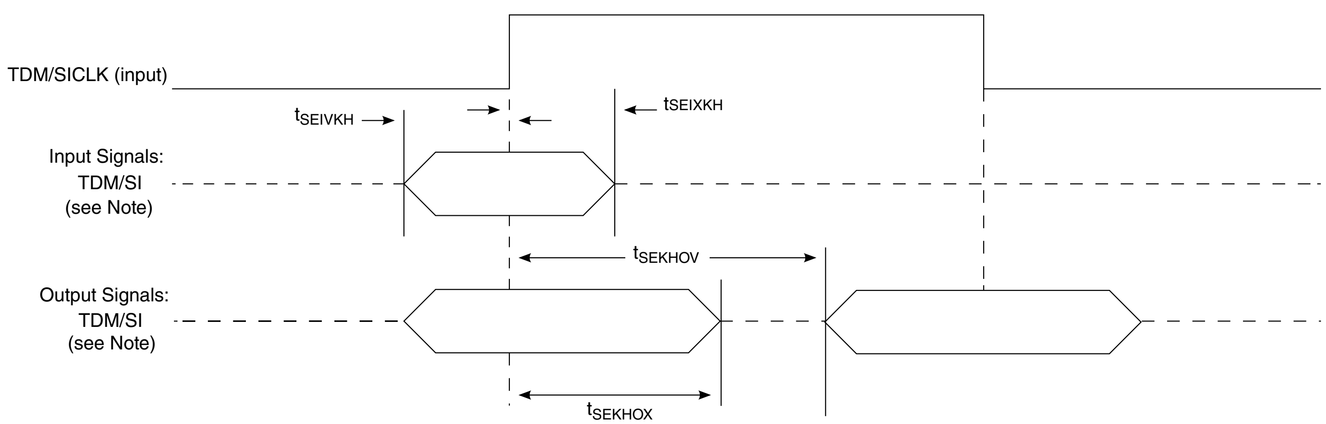


Figure 33. TDM/SI AC test load

This figure represents the AC timing from Table 74. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the TDM/SI timing with an external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC timing (external clock) diagram

3.13 USB 3.0 interface

This section describes the DC and AC electrical specifications for the USB 3.0 interface.

3.13.1 USB 3.0 PHY transceiver supply DC voltage

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at USB_HV_{DD} = 3.3 V.

Table 75. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 5.
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.13.2 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 76. USB 3.0 transmitter DC electrical characteristics[1]

Characteristic	Symbol	Min	Nom	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800	1000	1200	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400	—	1200	$mV_{p\text{-}p}$
Tx de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3	—	4	dB
Differential impedance	Z_{diffTX}	72	100	120	Ohm
Tx common mode impedance	$R_{TX\text{-}DC}$	18	—	30	Ohm
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	—	—	200	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	—	10	mV

Note:

1. For recommended operating conditions, see Table 5.

This table provides the USB 3.0 receiver DC electrical characteristics at the Rx package pins.

Table 77. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Differential Rx input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72	100	120	Ohm	—
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18	—	30	Ohm	—
DC input CM input impedance for V > 0 during reset or power down	ZRX-HIGH-IMP-DC	25 K	—	—	Ohm	—

Table continues on the next page...

Table 77. USB 3.0 receiver DC electrical characteristics (continued)

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
LFPS detect threshold	$VRX\text{-}IDLE\text{-}DET\text{-}DC\text{-}DIFF_{pp}$	100	—	300	mV	1
Note:						
1. Below the minimum is noise. Must wake up above the maximum.						

3.13.3 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 78. USB 3.0 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Speed	—	—	5.0	—	Gb/s	—
Transmitter eye	$t_{TX\text{-}Eye}$	0.625	—	—	UI	—
Unit interval	UI	199.94	—	200.06	ps	2
AC coupling capacitor	AC coupling capacitor	75	—	200	nF	—
Note:						
1. For recommended operating conditions, see Table 5.						
2. UI does not account for SSC-caused variations.						

This table provides the USB 3.0 receiver AC timing specifications at Rx package pins.

Table 79. USB 3.0 receiver AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Unit interval	UI	199.94	—	200.06	ps	2
Notes:						
1. For recommended operating conditions, see Table 5.						
2. UI does not account for SSC-caused variations.						

3.13.4 USB 3.0 reference clock requirements

USB 3.0 SSPHY needs a reference clock. There are two options for the reference clock: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B.

This table summarizes the requirements of the reference clock provided to the USB 3.0 SSPHY. 100 MHz reference clock is required with the following specifications:

Table 80. Reference clock requirements[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency offset	FREF_OFFSET	-300	—	300	ppm	—
Reference clock random jitter (RMS)	RMSJREF_CLK	—	—	3	ps	1, 2
Reference clock deterministic jitter	DJREF_CLK	—	—	150	ps	3
Notes:						
1. 1.5 MHz to Nyquist frequency. For 100 MHz reference clock, the Nyquist frequency is 50 MHz.						
2. The peak-to-peak Rj specification is calculated as 14.069 times the RMS Rj for 10-12 BER.						
3. DJ across all frequencies.						
4. SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B must meet the clock specification mentioned in this table when used as a clock source for USB PHY.						

3.13.5 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 81. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Period	tPeriod	20	—	100	ns	—
Peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS}$	800	—	1200	mV	—
Low-power peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS-LP}$	400	—	600	mV	—
Rise/fall time	$t_{RiseFall20-80}$	—	—	4	ns	1
Duty cycle	Duty cycle	40	—	60	%	1
Note:						
1. Measured at compliance TP1. See Figure 35 for details.						

This figure shows the Tx normative setup with reference channel as per USB 3.0 specifications.

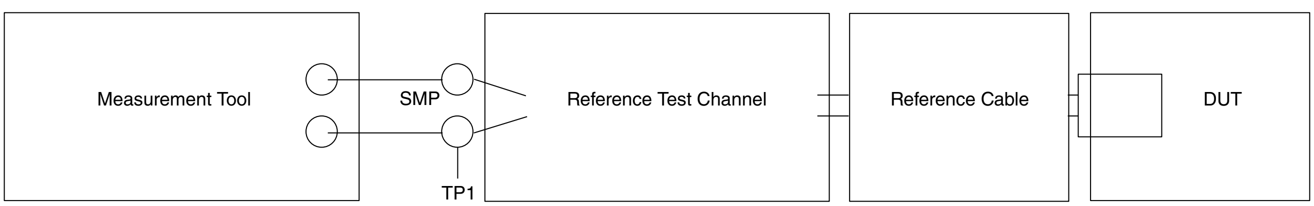


Figure 35. Tx normative setup

3.14 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.14.1 IFC DC electrical characteristics

This table provides the DC electrical characteristics for the IFC when operating at OV_{DD}= 1.8 V.

Table 82. IFC DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.32	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.14.2 Integrated Flash Controller AC Timing Specifications

This section describes the AC timing specifications for the integrated flash controller.

3.14.2.1 Test Condition

Figure below provides the AC test load for the integrated flash controller.

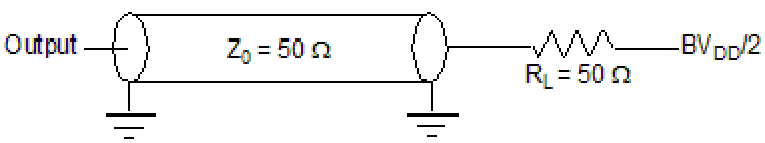


Figure 36. Integrated Flash Controller AC Test Load

3.14.2.2 IFC AC Timing Specifications (GPCM/GASIC)

Table below describes the input AC timing specifications of the IFC-GPCM and IFC-GASIC interface.

Table 83. Integrated Flash Controller Input Timing Specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 5

Figure below shows the input AC timing diagram for IFC-GPCM, IFC-GASIC interface.

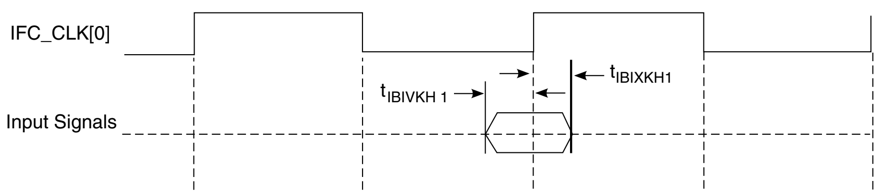


Figure 37. IFC-GPCM, IFC-GASIC Input AC Timings

Table below describes the output AC timing specifications of IFC-GPCM and IFC-GASIC interface .

Table 84. Integrated Flash Controller IFC-GPCM and IFC-GASIC interface Output Timing Specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. Output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 5

Figure below shows the output AC timing diagram for IFC-GPCM, IFC-GASIC interface.

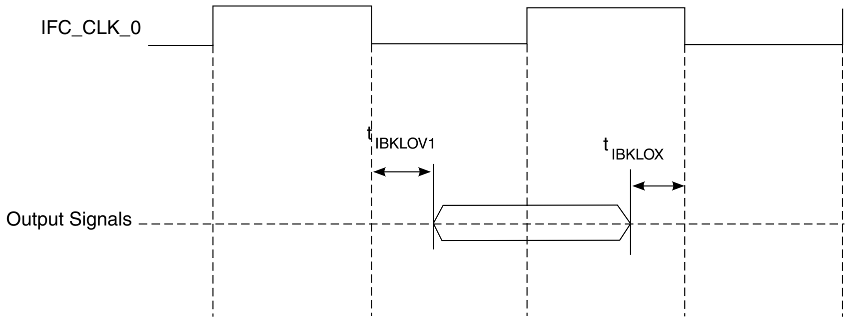


Figure 38. IFC-GPCM, IFC-GASIC Signals

3.14.2.3 IFC AC Timing Specifications (NOR)

Table below describes the input timing specifications of the IFC-NOR interface.

Table 85. Integrated Flash Controller Input Timing Specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH2}$	(1 x t_{IP_CLK}) + 1	-	ns	1

NOTE

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

2. For recommended operating conditions, see Table 5.

Figure below shows the AC input timing diagram for input signals of IFC-NOR interface. Here TRAD is a programmable delay parameter, refer to IFC section of for more information.

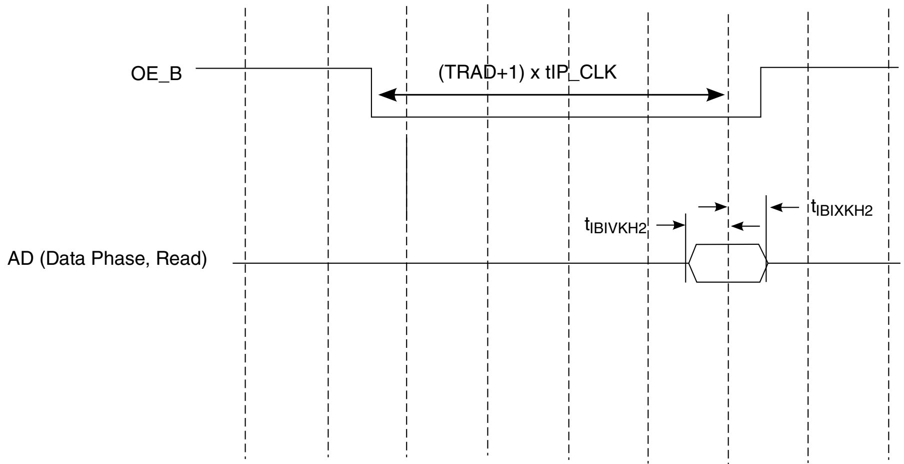


Figure 39. IFC-NOR Interface Input AC Timings

Table below describes the output AC timing specifications of IFC-NOR interface .

Table 86. Integrated Flash Controller IFC-NOR Interface Output Timing Specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1
NOTE:					
1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.					
2. For recommended operating conditions, see Table 5					

Figure below shows the AC timing diagram for output signals of IFC-NOR interface. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is suppose to change TACO (a programmable delay, refer to IFC section of for more information) time after CS_B. Because of skew between the signals, OE_B may change anywhere within time window defined by tIBKLOV2. This concept applies to other output signalsof IFC-NOR interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. Here is the list of IFC-NOR output signals NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD(Address phase).

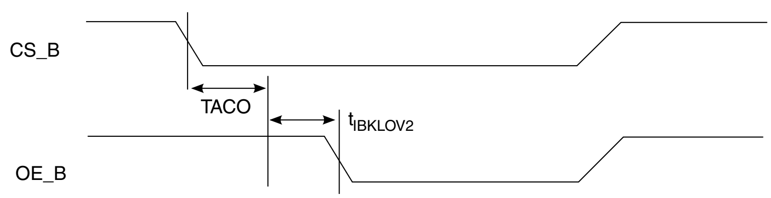


Figure 40. IFC-NOR Interface Output AC Timings

3.14.2.4 IFC AC Timing Specifications (NAND)

Table below describes the input timing specifications of the IFC-NAND interface.

Table 87. Integrated Flash Controller Input Timing Specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1
NOTE:					
1. t_{IP_CLK} is the period of ip clock on which IFC is running.					
2. For recommended operating conditions, see					

Figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter, refer to IFC section of for more information.

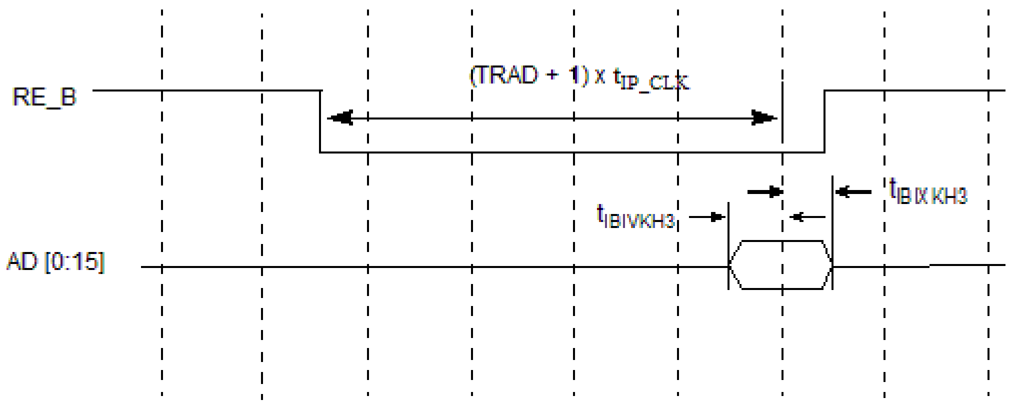


Figure 41. IFC-NAND Interface Input AC Timings

NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

Table below describes the output AC timing specifications of IFC-NAND interface.

Table 88. Integrated Flash Controller IFC-NAND Interface Output Timing Specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

Table continues on the next page...

Table 88. Integrated Flash Controller IFC-NAND Interface Output Timing Specifications (OV_{DD} = 1.8 V)[2] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
NOTE: 1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change. 2. For recommended operating conditions, see Table 5					

Figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs have been illustrated here by taking timings between two signals, CS_B and CLE as an example. CLE is suppose to change TCCST (a programmable delay, refer to IFC section of for more information) time after CS_B. Because of skew between the signals CLE may change anywhere within time window defined by $t_{IBKLOV3}$. This concept applies to other output signals of IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. Here is the list of output signals NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, AD.

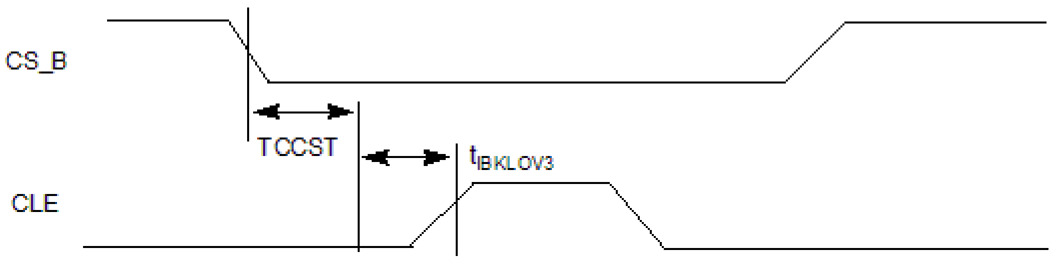


Figure 42. IFC-NAND Interface Output AC Timings

3.14.2.5 IFC-NAND SDR AC Timing Specifications

Table below describes the AC timing specifications of IFC-NAND SDR interface. These specifications are compliant to SDR mode of ONFI specification revision 3.0.

Table 89. Integrated Flash Controller IFC-NAND SDR Interface AC Timing Specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes	Fig
Address cycle to data loading time	tADL	O	TADLE - 1500(ps)	TADLE + 1500(ps)	t_{IP_CLK}		Figure 43
ALE hold time	tALH	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}		Figure 44
ALE setup time	tALS	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}		Figure 44
ALE to RE_n delay	tAR	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}		Figure 45
CE_n hold time	tCH	O	5 + 1500(ps)	-	ns		Figure 44

Table continues on the next page...

Table 89. Integrated Flash Controller IFC-NAND SDR Interface AC Timing Specifications (OVDD = 1.8 V) (continued)

CE_n high to input hi-Z	tCHZ	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}		Figure 46
CLE hold time	tCLH	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}		Figure 44
CLE to RE_n delay	tCLR	O	TWHRE - 1500(ps)	TWHRE - 1500(ps)	t_{IP_CLK}		Figure 47
CLE setup time	tCLS	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}		Figure 44
CE_n high to input hold	tCOH	I	150 - 1500(ps)	-	ns		Figure 46
CE_n setup time	tCS	O	TCS - 1500(ps)	TCS + 1500(ps)	t_{IP_CLK}		Figure 44
Data hold time	tDH	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}		Figure 44
Data setup time	tDS	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}		Figure 44
Busy time for Set Features and Get Features	tFEAT	O	-	FTOCNT	t_{IP_CLK}		Figure 48
Output hi-Z to RE_n low	tIR	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}		Figure 49
Interface and Timing Mode Change time	tITC	O	-	FTOCNT	t_{IP_CLK}		Figure 48
RE_n cycle time	tRC	O	TRP + TREH - 1500(ps)	TRP + TREH + 1500(ps)	t_{IP_CLK}		Figure 46
RE_n access time	tREA	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}		Figure 46
RE_n high hold time	tREH	I	TREH	TREH	t_{IP_CLK}		Figure 46
RE_n high to input hold	tRHOH	I	0	-	ns		Figure 46
RE_n high to WE_n low	tRHW	O	100 + 1500(ps)	-	ns		Figure 50
RE_n high to input hi-Z	tRHZ	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}		Figure 46
RE_n low to input data hold	tRLOH	I	0	-	ns		Figure 51
RE_n pulse width	tRP	O	TRP	TRP	t_{IP_CLK}		Figure 46
Ready to data input cycle (data only)	tRR	O	TRR - 1500(ps)	TRR + 1500(ps)	t_{IP_CLK}		Figure 46
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	tRST (raw NAND)	O	-	FTOCNT	t_{IP_CLK}		Figure 52
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	tRST2 (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}		Figure 52
(WE_n high or CLK rising edge) to SR[6] low	tWB	O	TWBE + TWH - 1500(ps)	TWBE + TWH + 1500(ps)	t_{IP_CLK}		Figure 44
WE_n cycle time	tWC	O	TWP + TWH	TWP + TWH	t_{IP_CLK}		Figure 53
WE_n high hold time	tWH	O	TWH	TWH	t_{IP_CLK}		Figure 53

Table continues on the next page...

Table 89. Integrated Flash Controller IFC-NAND SDR Interface AC Timing Specifications (OVDD = 1.8 V) (continued)

Command, address, or data input cycle to data output cycle	tWHR	O	TWHRE + TWH - 1500(ps)	TWHRE + TWH + 1500(ps)	t_{IP_CLK}		Figure 54
WE_n pulse width	tWP	O	TWP	TWP	t_{IP_CLK}		Figure 44
WP_n transition to command cycle	tWW	O	TWW - 1500(ps)	TWW + 1500(ps)	t_{IP_CLK}		Figure 55
Data Input hold	tIBIXKH4	I	1	-	t_{IP_CLK}		Figure 56

NOTE:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.

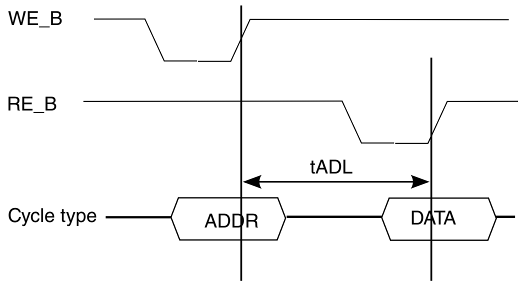


Figure 43. tADL Timing

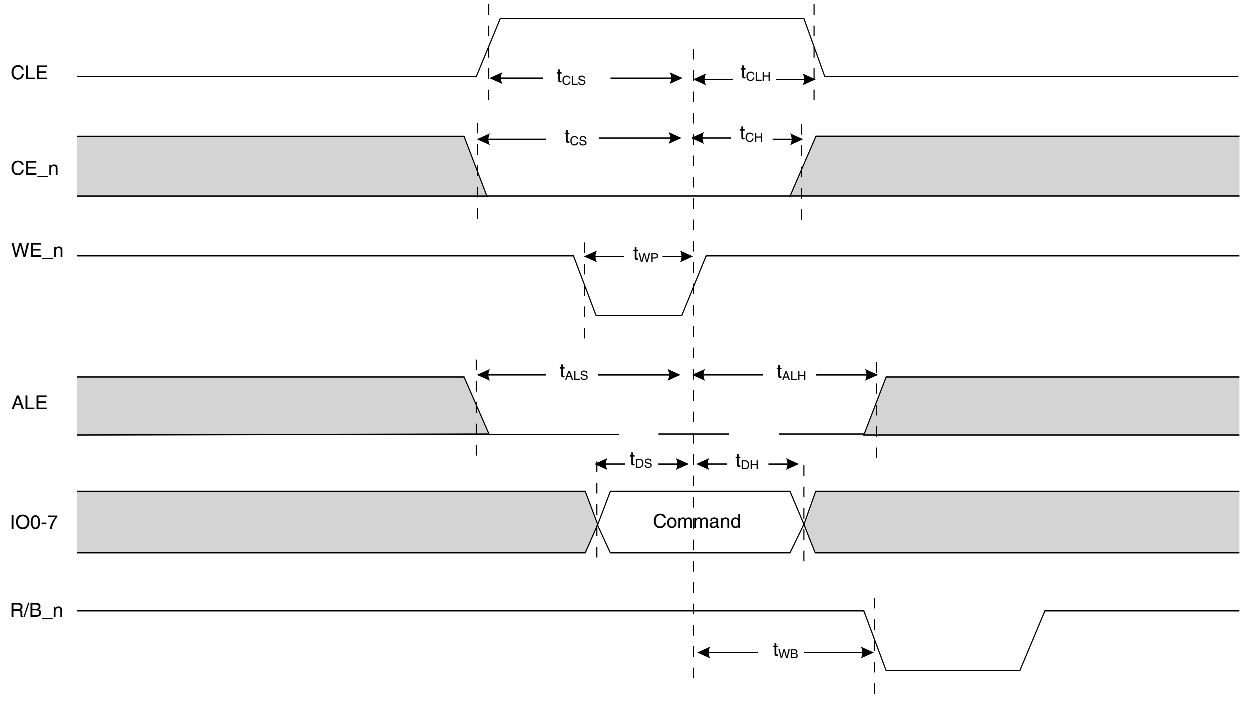


Figure 44. Command Cycle

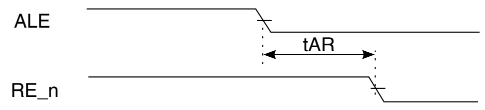


Figure 45. tAR Timings

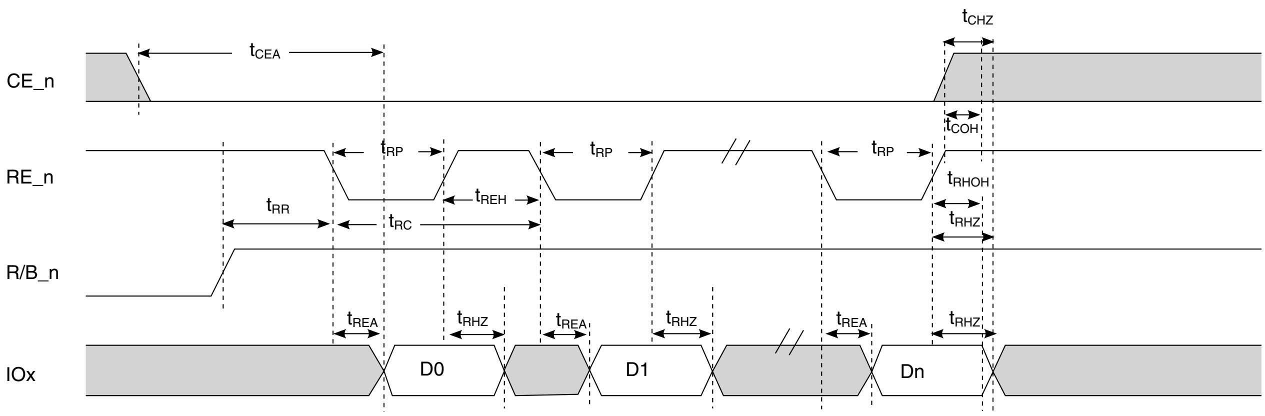


Figure 46. Data Input Cycle Timings

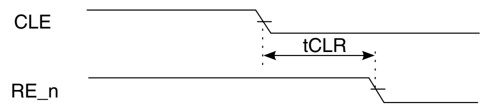


Figure 47. tCLR Timings

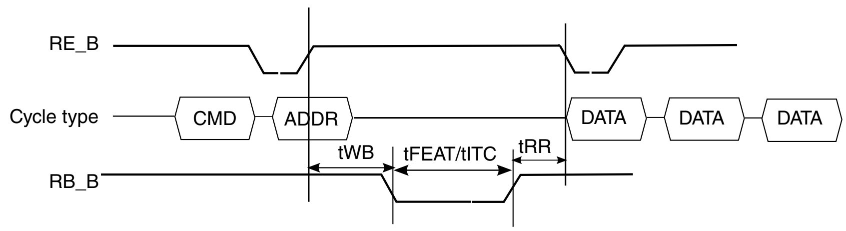


Figure 48. tWB, tFEAT, tITC, tRR Timings

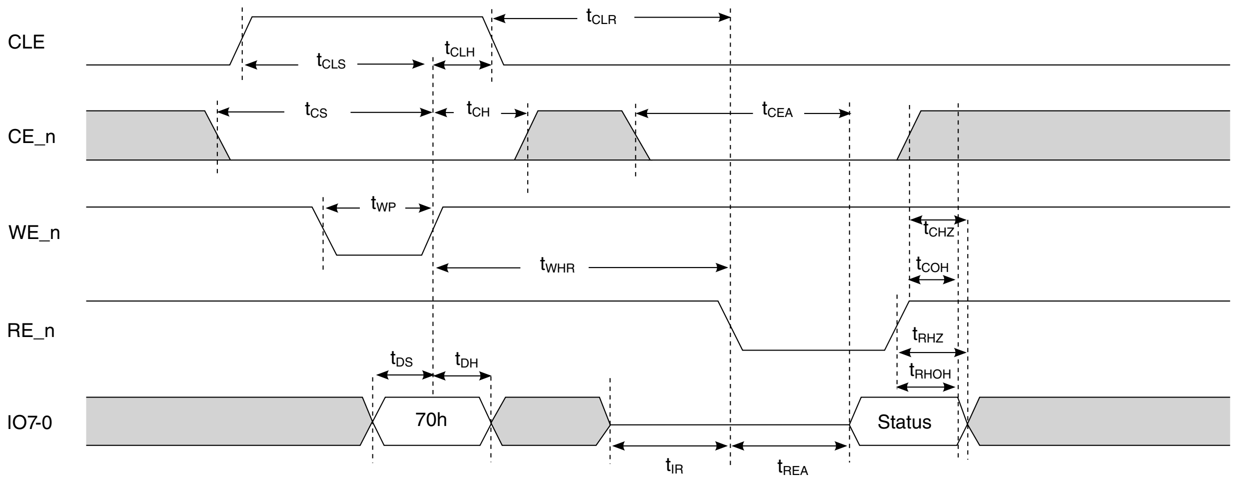


Figure 49. Read StatusTimings

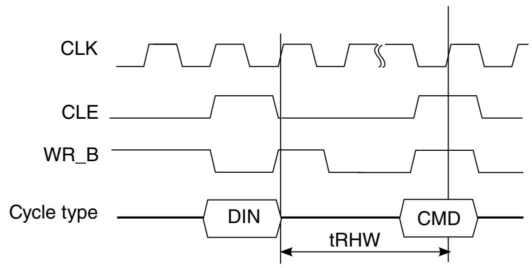


Figure 50. tRHW Timings

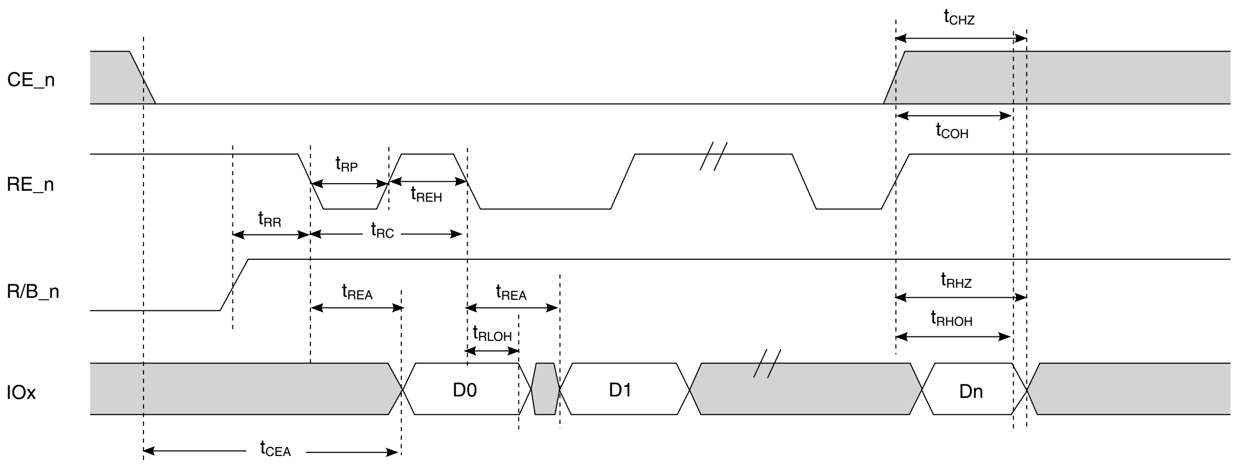


Figure 51. EDO Mode Data Input CycleTimings

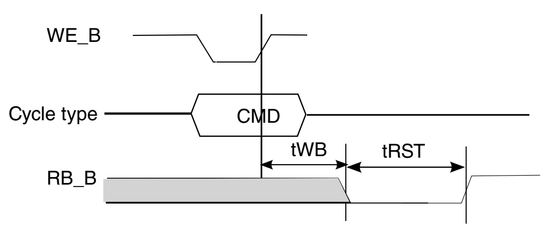


Figure 52. tWB, tRST Timings

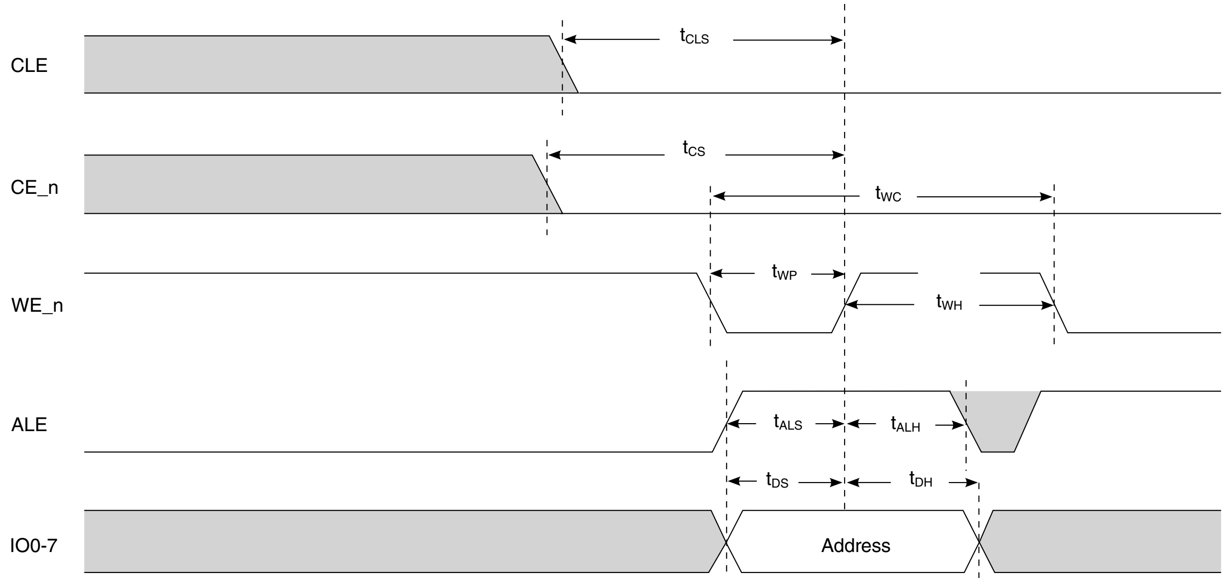


Figure 53. Address Latch Timings

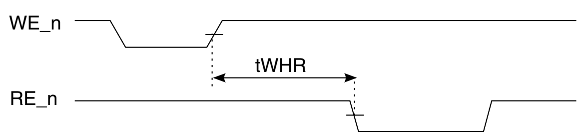


Figure 54. tWHR Timings

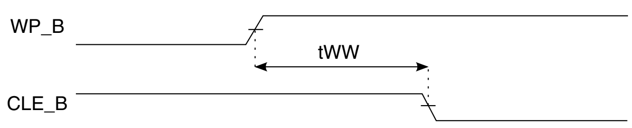


Figure 55. tWW Timings

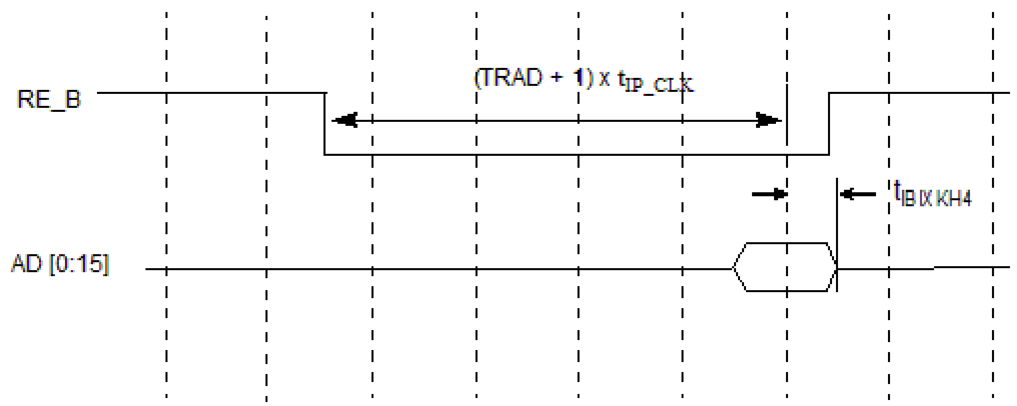


Figure 56. tIBIXKH4 Timings

3.14.2.6 IFC-NAND NVDDR AC Timing Specification

Table below describes the AC timing specifications of IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 90. Integrated Flash Controller IFC-NAND NVDDR Interface AC Timing Specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes	Fig
Access window of DQ[7:0] from CLK	tAC	I	3 - 150 (ps)	20 + 150 (ps)	ns		Figure 60
Address cycle to data loading time	tADL	I	TADL	-	t_{IP_CLK}		Figure 61
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast	tCADf	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}		Figure 57
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow	tCADs	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}		Figure 57
Command/address DQ hold time	tCAH	O	2 + 150 (ps)	-	ns		Figure 57
CLE and ALE hold time	tCALH	O	2 + 150 (ps)	-	ns		Figure 57
CLE and ALE setup time	tCALS	O	2 + 150 (ps)	-	ns		Figure 57
Command/address DQ setup time	tCAS	O	2 + 150 (ps)	-	ns		Figure 57
CE# hold time	tCH	O	2 + 150 (ps)	-	ns		Figure 57
Average clock cycle time, also known as tCK	tCK(avg) or tCK	O	10	-	ns		Figure 57
Absolute clock period, measured from rising edge to the next consecutive rising edge	tCK(abs)	O	tCK(avg) + tJIT(per) min	tCK(avg) + tJIT(per) max	ns		Figure 57
Clock cycle high	tCKH(abs)	O	0.45	0.55	tCK		Figure 57
Clock cycle low	tCKL(abs)	O	0.45	0.55	tCK		Figure 57
Data input end to W/R# high B16	tCKWR	O	TCKWR - 150 (ps)	TCKWR + 150 (ps)	t_{IP_CLK}		Figure 60

Table continues on the next page...

Table 90. Integrated Flash Controller IFC-NAND NVDDR Interface AC Timing Specifications (OVDD = 1.8 V) (continued)

CE# setup time	tCS	O	TCS - 150 (ps)	TCS + 150 (ps)	t_{IP_CLK}		Figure 59
Data DQ hold time	tDH	O	1050	-	ps		Figure 59
Access window of DQS from CLK	tDQSCK	I	-	20 + 150 (ps)	ns		Figure 60
W/R# low to DQS/DQ driven by device	tDQSD	I	-150 (ps)	18 + 150 (ps)	ns		Figure 60
DQS output high pulse width	tDQSH	O	0.45	0.55	tCK		Figure 59
W/R# high to DQS/DQ tri-state by device	tDQSHZ	O	RHZ - 150 (ps)	RHZ + 150 (ps)	t_{IP_CLK}		Figure 57
DQS output low pulse width	tDQSL	O	0.45	0.55	tCK		Figure 59
DQS-DQ skew, DQS to last DQ valid, per ac cess (1.0V)	tDQSQ	I	-	1000	ps		Figure 60
DQS-DQ skew, DQS to last DQ valid, per access (0.9V)				930			
Data output to first DQS latching transition	tDQSS	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK		Figure 59
Data DQ setup time	tDS	O	1050	-	ps		Figure 59
DQS falling edge to CLK rising - hold time	tDSH	O	0.2 + 150 (ps)	-	tCK		Figure 59
DQS falling edge to CLK rising - setup time	tDSS	O	0.2 + 150 (ps)	-	tCK		Figure 59
Input data valid window	tDVW	I	tDVW = tQH - tDQSQ	-	ns		Figure 60
Busy time for Set Features and Get Features	tFEAT	I	-	FTOCNT	t_{IP_CLK}		Figure 62
Half-clock period	tHP	O	tHP = min(tCKL, tCKH)	-	ns		Figure 60
Interface and Timing Mode Change time	tITC	I	-	FTOCNT	t_{IP_CLK}		Figure 62
The deviation of a given tCK(abs) from tCK(avg)	tJIT(per)	O	-0.5	0.5	ns		-
DQ-DQS hold, DQS to first DQ to go non-valid, per access	tQH	I	tQH = tHP - tQHS	-	t_{IP_CLK}		Figure 60
Data hold skew factor	tQHS	I	-	1 + 150(ps)	ns		-
Data input cycle to command, address, or data output cycle	tRHW	O	TRHW	-	t_{IP_CLK}		Figure 63
Ready to data input cycle (data only)	tRR	I	TRR	-	t_{IP_CLK}		Figure 62

Table continues on the next page...

Table 90. Integrated Flash Controller IFC-NAND NVDDR Interface AC Timing Specifications (OVDD = 1.8 V) (continued)

Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	tRST (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}		Figure 64
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	tRST2 (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}		Figure 64
CLK rising edge to SR[6] low	tWB	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}		Figure 64
Command, address or data output cycle to data input cycle	tWHR	O	TWHR	-	t_{IP_CLK}		Figure 65
DQS write preamble	tWPRE	O	1.5	-	tCK		Figure 59
DQS write postamble	tWPST	O	1.5	-	tCK		Figure 59
W/R# low to data input cycle	tWRCK	I	TWRCK - 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}		Figure 60
WP# transition to command cycle	tWW	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}		Figure 66
NOTE: 1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.							

Following diagrams show the AC timing diagram for IFC-NAND NVDDR interface.

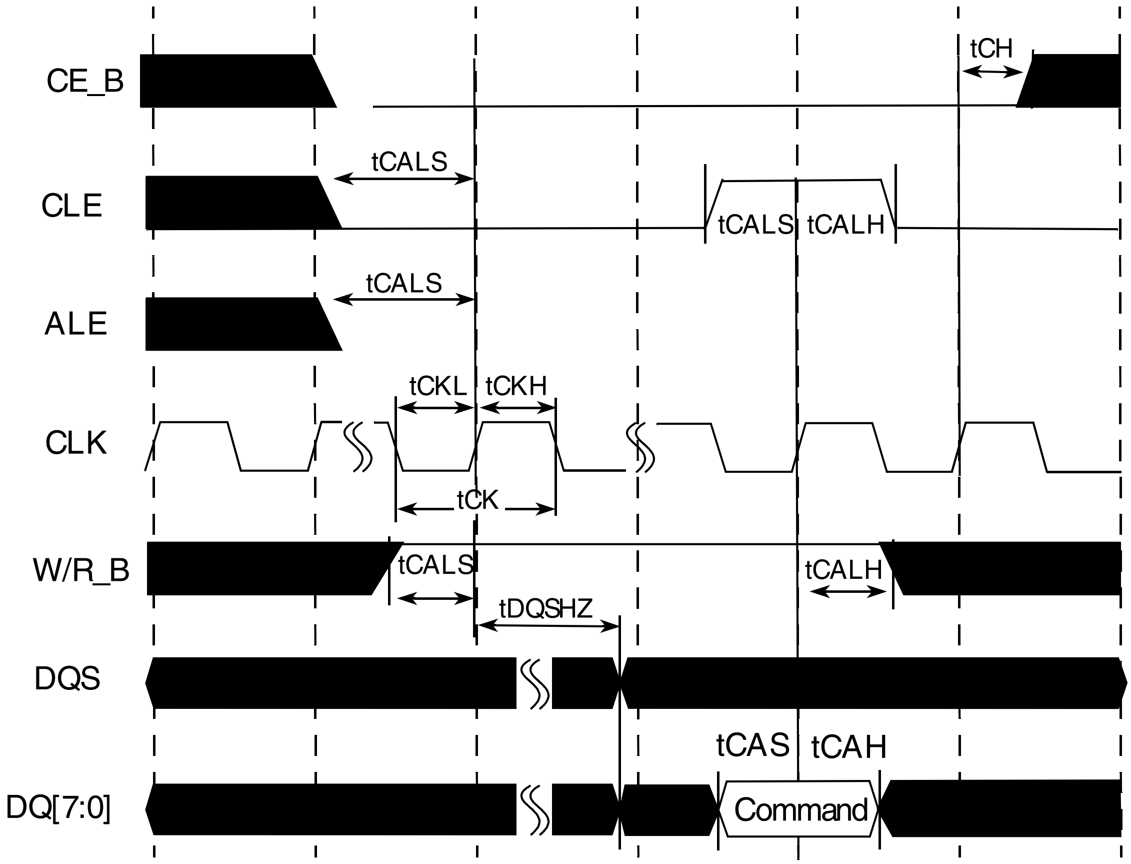


Figure 57. Command Cycle

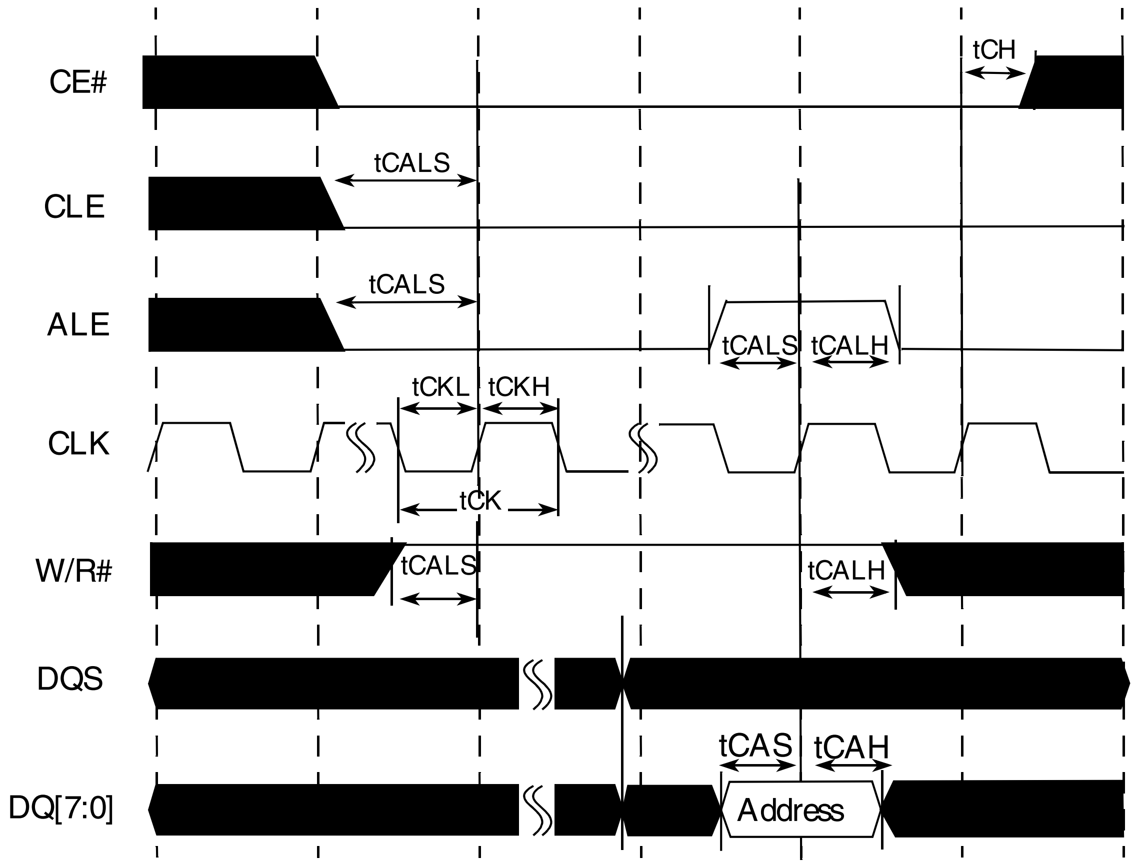


Figure 58. Address Cycle

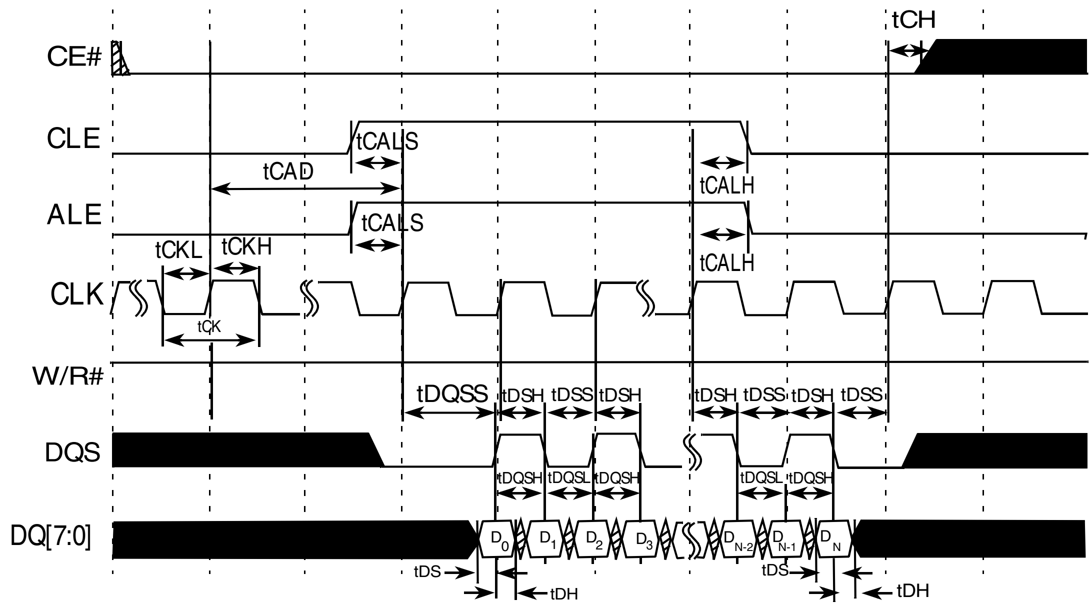


Figure 59. Write Cycle

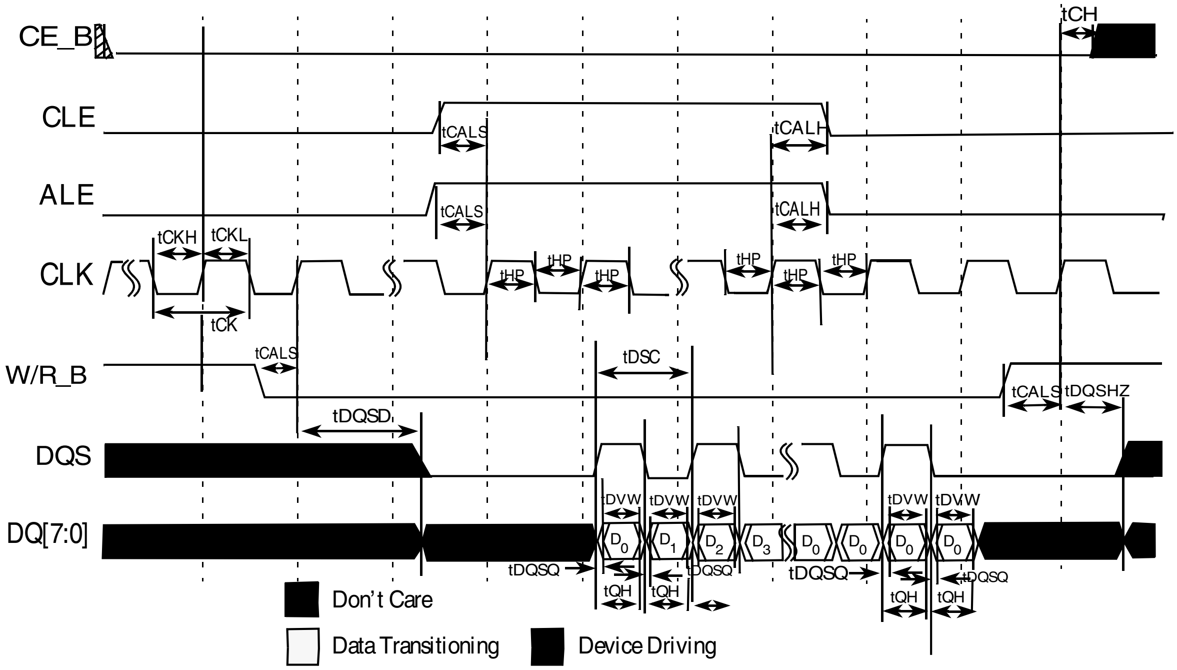


Figure 60. Read Cycle

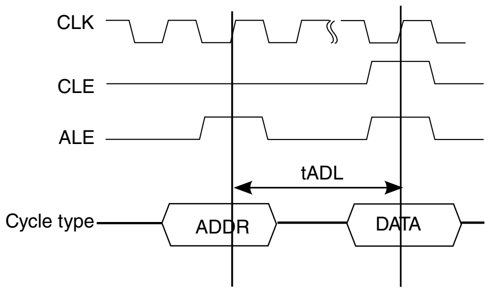


Figure 61. tADL Timings

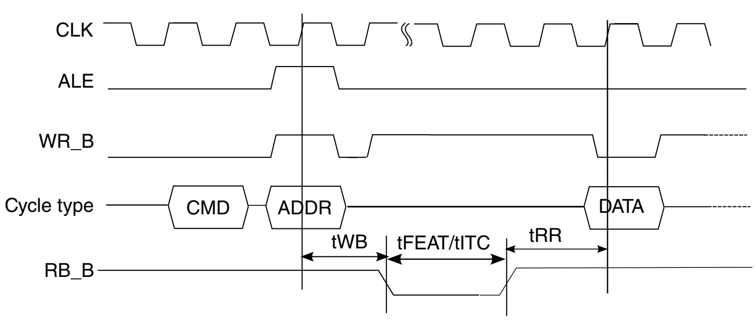


Figure 62. tWB, tFEAT, tITC, tRR Timings

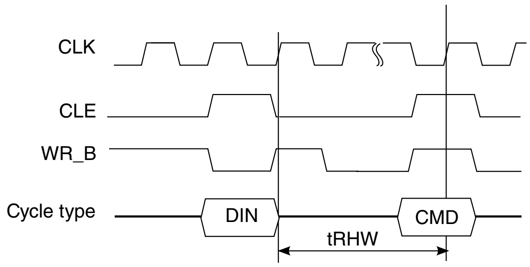


Figure 63. tRHW Timings

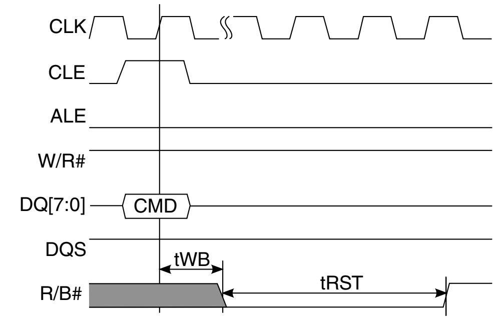


Figure 64. tWB, tRST Timings

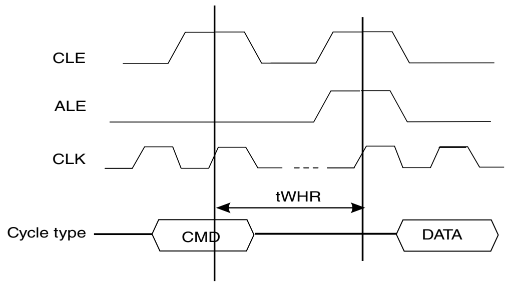


Figure 65. tWHR Timings

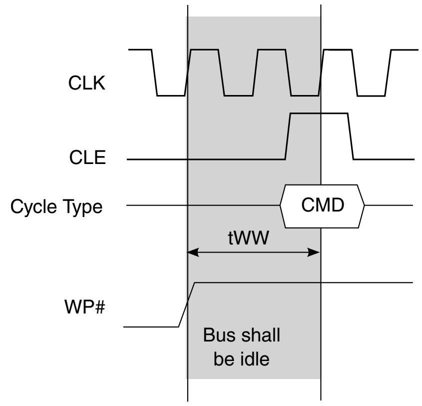


Figure 66. tWW Timings

3.15 LPUART interface

This section describes the DC and AC electrical specifications for the LPUART interface.

3.15.1 LPUART DC electrical characteristics

This table provides the DC electrical characteristics for the LPUART interface when operating at D/EV_{DD} = 3.3 V.

Table 91. LPUART DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/ EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (D/EV_{IN} = 0 V or D/EV_{IN} = D/EV_{DD})	I_{IN}	—	±50	μA	—
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max D/EV_{DD} respective values found in Table 5.
2. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for the LPUART interface when operating at D/EV_{DD} = 1.8 V.

Table 92. LPUART DC electrical characteristics (DV_{DD}/EV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/ EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (D/EV_{IN} = 0 V or D/EV_{IN} = D/EV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (D/EV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (D/EV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max D/EV_{DD} respective values found in Table 5.
2. The symbol D/EV_{IN} represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.15.2 LPUART AC timing specifications

This table provides the AC timing specifications for the LPUART interface.

Table 93. LPUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 32 x 8192)	baud	1, 3, 4
Maximum baud rate	f_{PLAT}/(2 x 4)	baud	1, 2, 4

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. Every bit can be over sampled with a sample clock rate of 8 and 64 times (software configurable) and each bit is the majority of the values sampled at the sample rate divided by two, (sample rate/2)+1 and (sample rate/2)+2.
4. The 1-to-0 transition during a data word can cause a resynchronization of the sample point.

3.16 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.16.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 3.3 V.

Table 94. DUART DC electrical characteristics (3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 95. DUART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 5.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.16.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 96. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3.17 Flextimer interface

This section describes the DC and AC electrical characteristics for the Flextimer interface. There are Flextimer pins on various power supplies in this device.

3.17.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for Flextimer pins operating at D/ EV_{DD} = 3.3 V.

Table 97. Flextimer DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= D/EV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the DV_{IN}/EV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for Flextimer pins operating at D/ EV_{DD} = 1.8 V.

Table 98. Flextimer DC electrical characteristics (DV_{DD}/EV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = D/EV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (D/EV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (D/EV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the DV_{IN}/EV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for Flextimer pins operating at LV_{DD} = 2.5 V.

Table 99. Flextimer DC electrical characteristics (2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2

Table continues on the next page...

Table 99. Flextimer DC electrical characteristics (2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for Flextimer pins operating at L/OV_{DD} = 1.8 V.

Table 100. Flextimer DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = L/OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (L/OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (L/OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max L/OV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.17.2 Flextimer AC timing specifications

This table provides the Flextimer AC timing specifications.

Table 101. Flextimer AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
Flextimer inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs should be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 5.

This figure provides the AC test load for the Flextimer.

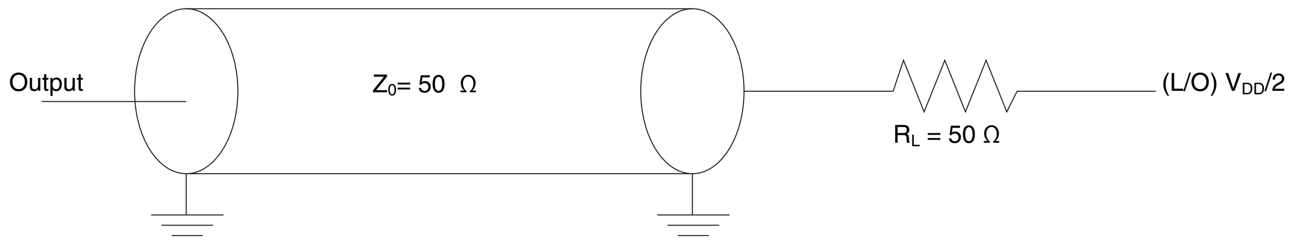


Figure 67. Flextimer AC test load

3.18 SPI interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.18.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 102. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.18.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 103. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit
SCK Clock Pulse Width	t_{SDC}	—	40%	60%	t_{SCK}
CS to SCK Delay	t_{CSC}	Master	16	—	ns
After SCK Delay	t_{ASC}	Master	16	—	ns
Data Setup Time for Inputs	t_{NIIVKH}	Master	8	—	ns
Data Hold Time for Inputs	t_{NIIXKH}	Master	0	—	ns
Data Valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	—	7	ns
Data Hold Time for Outputs	t_{NIKHOX}	Master	0	—	ns

This figure shows the SPI timing master when CPHA = 0.

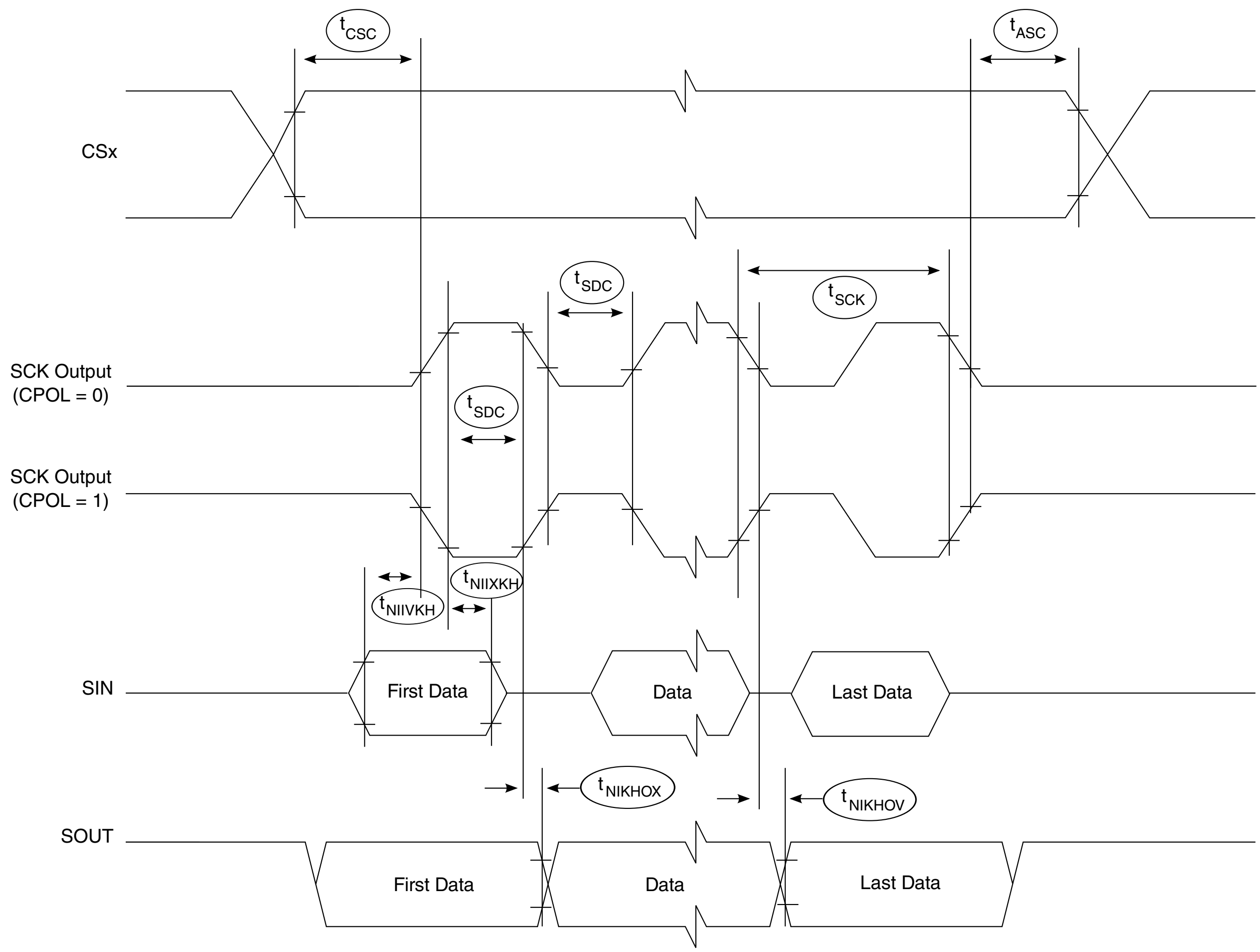


Figure 68. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

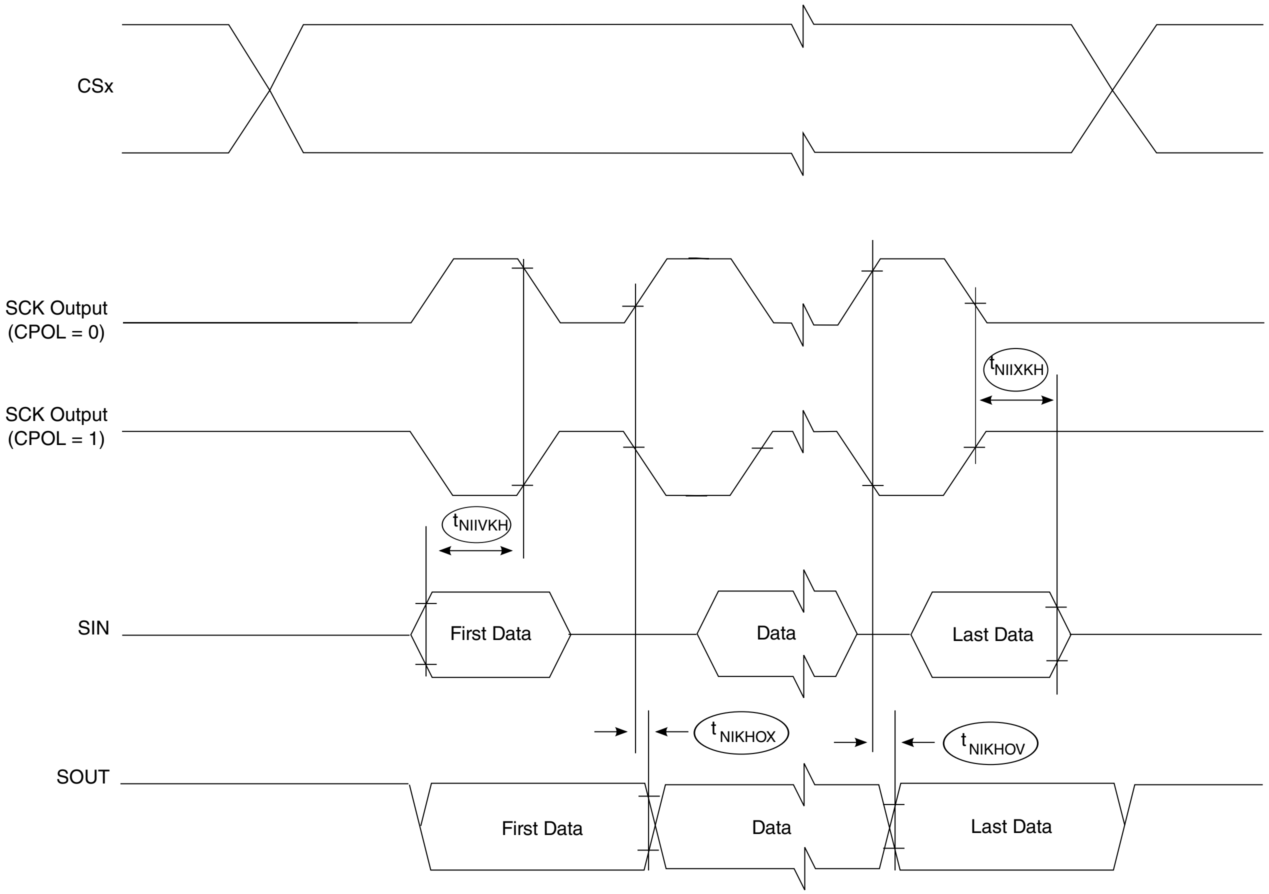


Figure 69. SPI timing master, CPHA = 1

3.19 QuadSPI interface

This section describes the DC and AC electrical characteristics for the QuadSPI interface.

3.19.1 QuadSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QuadSPI interface operating at OV_{DD} = 1.8 V.

Table 104. QuadSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage	V_{OH}	1.35	—	V	—

Table continues on the next page...

Table 104. QuadSPI DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
(OV_{DD} = min, I_{OH} = -0.5 mA)					
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.19.2 QuadSPI AC timing specifications

This section describes the QuadSPI timing specifications in SDR mode. All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing figures in this section.

3.19.2.1 QuadSPI timing SDR mode

This table provides the QuadSPI input and output timing in SDR mode.

Table 105. SDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock frequency	F_{SCK}	—	62.5	MHz
Clock rise/fall time	T_{RISE}/T_{FALL}	1	—	ns
CS output hold time	$t_{NIKHOX2}$	-3.4	—	ns
CS output delay	$t_{NIKHOV2}$	—	3.5	ns
Setup time for incoming data	t_{NIIVKH}	8.6	—	ns
Hold time requirement for incoming data	t_{NIIXKH}	0.4	—	ns
Output data valid	t_{NIKHOV} t_{NIKLOV}	—	4.5	ns
Output data hold	t_{NIKHOX} t_{NIKLOX}	-4.4	—	ns

This figure shows the QuadSPI AC timing in SDR mode.

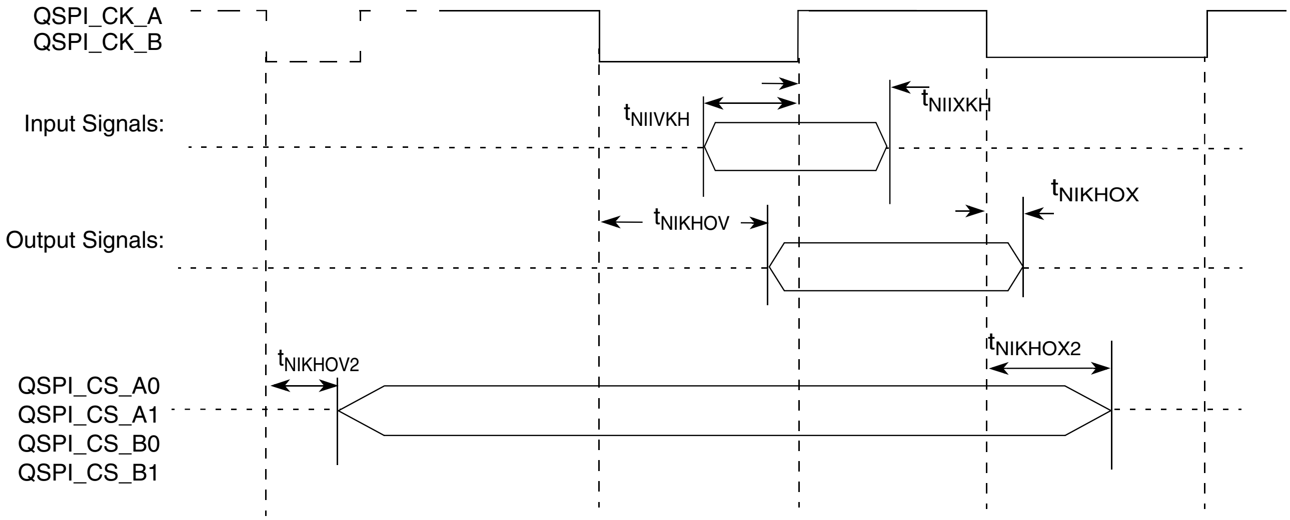


Figure 70. QuadSPI AC timing — SDR mode

3.20 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.20.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 106. eSDHC interface DC electrical characteristics[3]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.625 x D/EV_{DD}	-	V	1
Input low voltage	V_{IL}	-	-	0.25 x D/EV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = -100 μA at D/EV_{DD} min	0.75 x D/EV_{DD}	-	V	-
Output low voltage	V_{OL}	I_{OL} = 100 μA at D/EV_{DD} min	-	0.125 x D/EV_{DD}	V	-
Output low voltage	V_{OL}	I_{OL} = 2 mA	-	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	-	-10	10	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max D/EV_{IN} values found in the Recommended operating conditions table..

2. Open-drain mode is for MMC cards only.

3. At Recommended operating conditions with D/EV_{DD}=3.3V.

4. Interface signals are distributed over different voltages (D/EV_{DD}), ensure that voltage is set to 3.3V when in operation.

Table 107. eSDHC interface DC electrical characteristics (dual-voltage cards)[2]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.7 * O/D/EV_{DD}	-	V	1
Input low voltage	V_{IL}	-	-	0.2 * O/D/EV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = -100 µA at O/D/EV_{DD} min	O/D/EV_{DD} - 0.2	-	V	-
Output low voltage	V_{OL}	I_{OL} = 100 µA at O/D/EV_{DD} min	-	0.2	V	-
Output low voltage	V_{OL}	I_{OL} = 2 mA	-	0.3	V	4
Input/output leakage current	I_{IN}/I_{OZ}	-	-10	10	µA	4

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max O/D/EV_{IN} values found in the Recommended operating conditions tableReplace with xref to Recommended operating conditions table.

2. At Recommended operating conditions for 1.8V or 3.3V.

3. Interface signals are distributed over different voltages (O/D/EV_{DD}), ensure that voltage is set to a common level when in operation.

4. Open-drain mode is for MMC cards only.

3.20.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 71, Figure 72, and Figure 73.

Table 108. eSDHC AC timing specifications (high-speed mode)[6]

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency:	SD/SDIO (full-speed/high-speed mode)	f_{SHSCK}	0	25/50	MHz	2, 4
	MMC (full-speed/ high-speed mode)			20/52		
SDHC_CLK clock low time (full-speed/high-speed mode)		t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)		t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times		t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK		$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK		$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

Table 108. eSDHC AC timing specifications (high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).					
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-20MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.					
3. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.					
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.					
5. The parameter values apply to both full-speed and high-speed modes.					
6. At recommended operating conditions with OV_{DD}/EV_{DD}=1.8V or 3.3V.					

This figure provides the eSDHC clock input timing diagram.

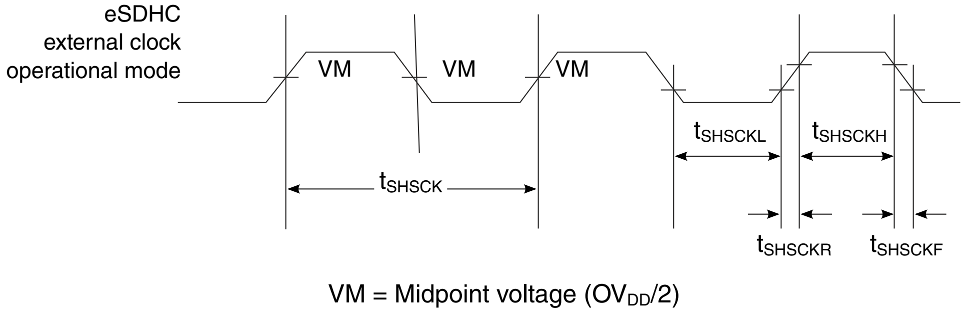


Figure 71. eSDHC clock input timing diagram

This figure provides the input AC timing diagram for high-speed mode.

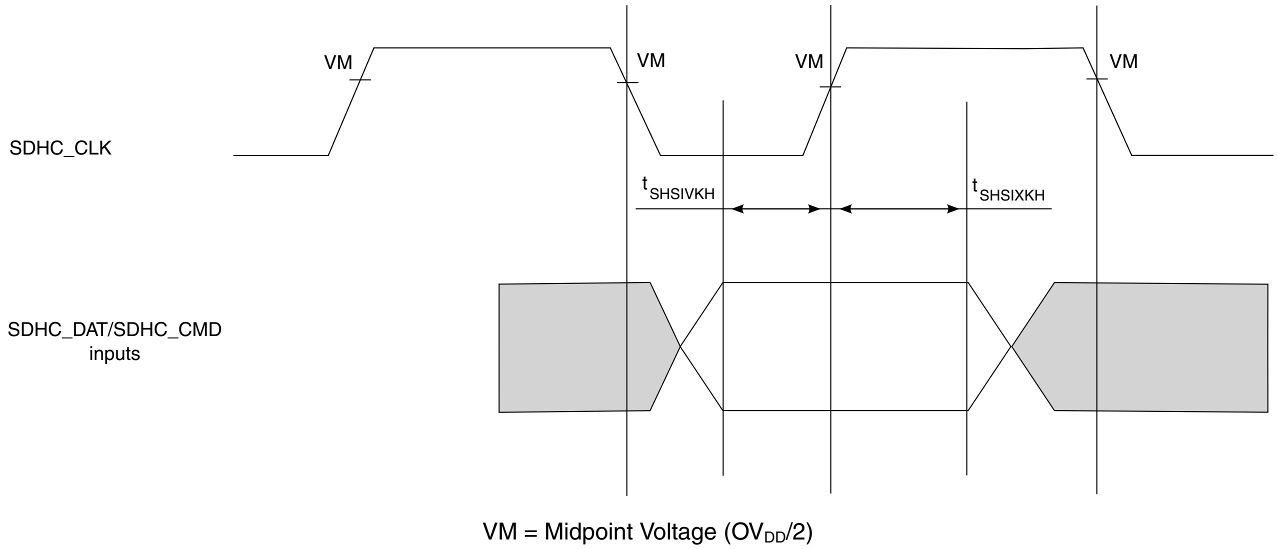


Figure 72. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.

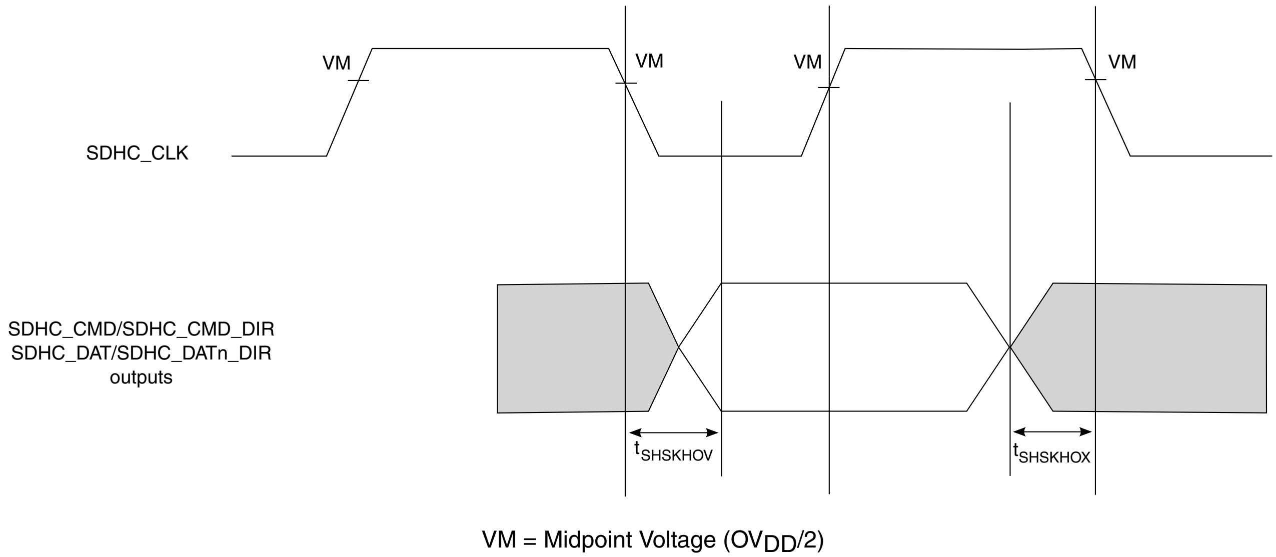


Figure 73. eSDHC high-speed mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR50 mode.

Table 109. eSDHC AC timing specifications (SDR50)[2]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	-	80	MHz	-
SDHC_CLK duty cycle	-	40	60	%	-
SDHC_CLK clock rise and fall times	$t_{SHCKR/}$	-	1	ns	1

Table continues on the next page...

Table 109. eSDHC AC timing specifications (SDR50)[2] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
	t_{SHCKF}				
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	-	-0.1	0.1	ns	-
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	t_{SHIVKH}	3.1	-	ns	-
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	t_{SHIXKH}	1.0	-	ns	-
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{SHKHOX}	2.85	-	ns	-
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{SHKHOV}	-	8.05	ns	-

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.

2. At recommended operating conditions with OV_{DD}=1.8V.

This figure provides the eSDHC clock input timing diagram for SDR50 mode.

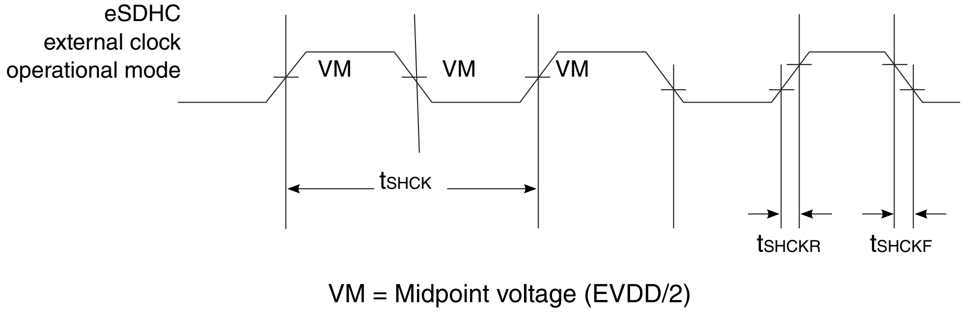


Figure 74. eSDHC SDR50 mode clock input timing diagram

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

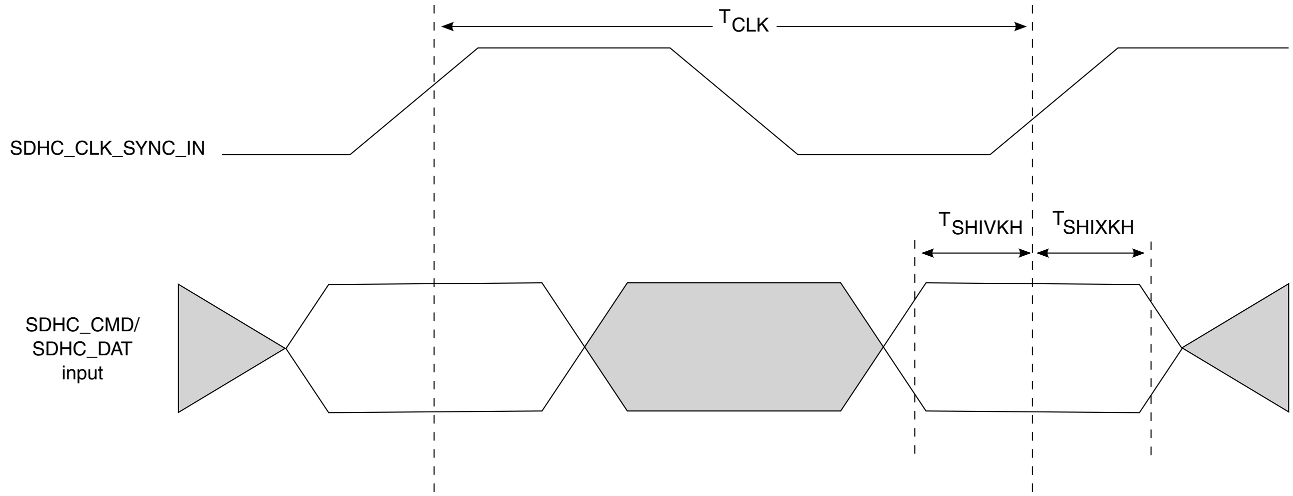


Figure 75. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

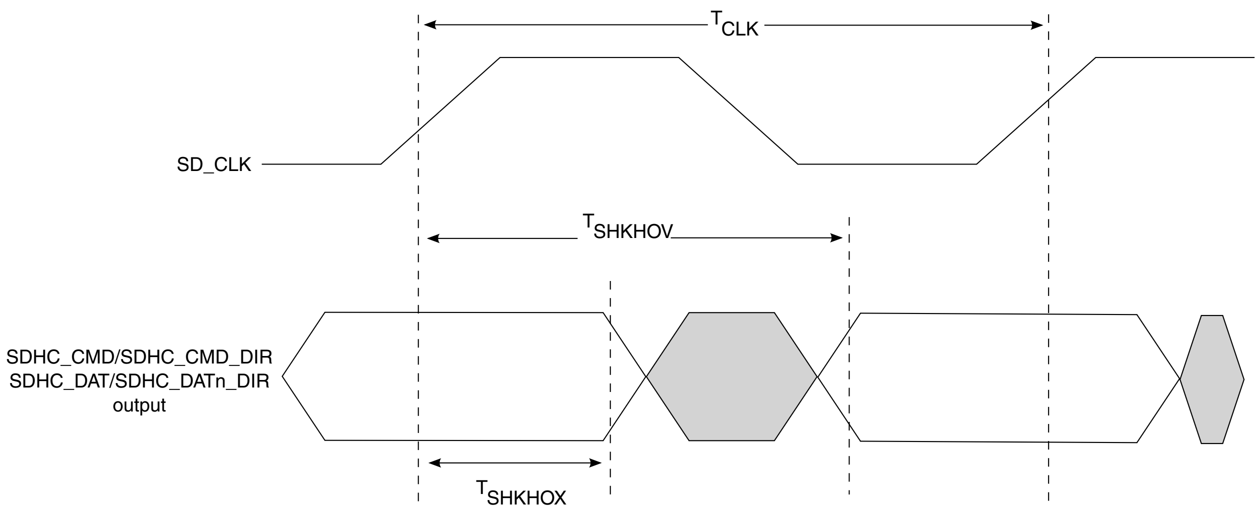


Figure 76. eSDHC SDR50 mode output timing diagram

This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 110. eSDHC AC timing specifications (DDR50/DDR)[3]

Parameter		Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO DDR50 mode	f_{SHCK}	-	37	MHz	-
	eMMC DDR mode			37		
SDHC_CLK duty cycle		-	47.0	53.0	%	-
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		-	-0.1	0.1	ns	-

Table continues on the next page...

Table 110. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter		Symbol	Min	Max	Unit	Notes
SDHC_CLK clock rise and fall times	SD/SDIO DDR50 mode	$t_{SHCKR/}$	-	5.4	ns	1
	eMMC DDR mode	t_{SHCKF}		2.0		2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIVKH}$	3.82	-	ns	-
	eMMC DDR mode		3.91			
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIXKH}$	- 1.0	-	ns	-
	eMMC DDR mode		0.98			
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOX}$	2.4	-	ns	-
	eMMC DDR mode		4.12			
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOV}$	-	9.01	ns	-
	eMMC DDR mode			9.61		
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIVKH}$	10.13	-	ns	-
	eMMC DDR mode		10.27			
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIXKH}$	1.0	-	ns	-
	eMMC DDR mode		0.98			
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOX}$	2.4	-	ns	-
	eMMC DDR mode		4.62			
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOV}$	-	19.02	ns	-
	eMMC DDR mode			22.17		

Notes:

1. $C_{CARD} \leq 10pF$, (1 card).

2. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 20pF$ for MMC, 40pF for SD.

3. At recommended operating conditions with OV_{DD}/EV_{DD}=1.8 or 3.3V for eMMC DDR mode, OV_{DD}=1.8 V for DDR50.

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

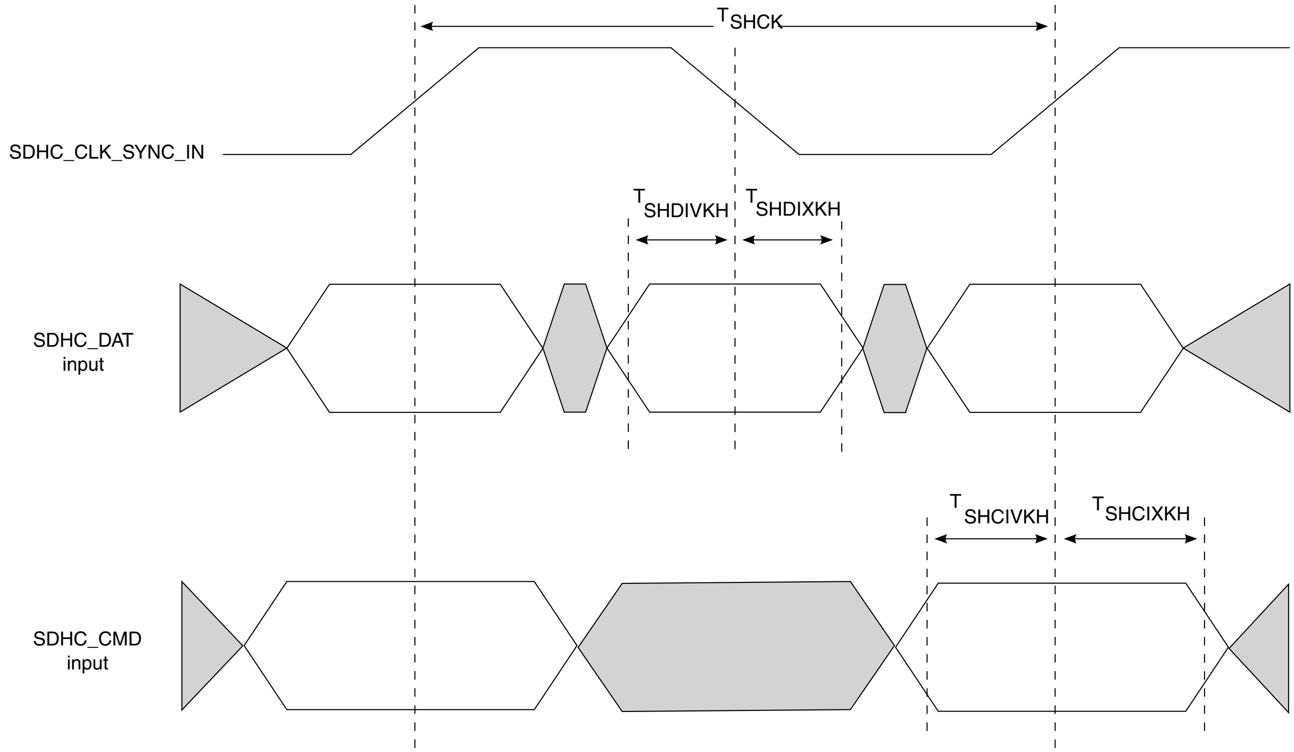


Figure 77. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

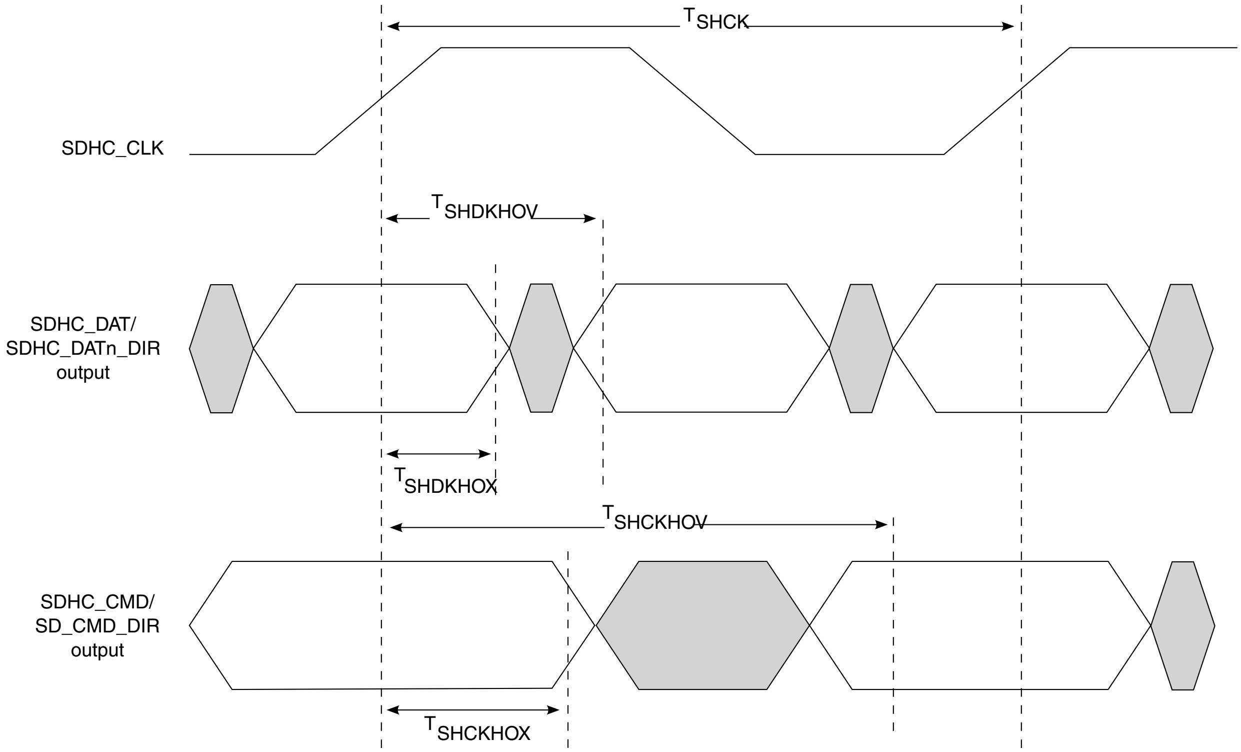


Figure 78. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 111. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	120	MHz	-
	eMMC HS200 mode			116.7		
SDHC_CLK duty cycle			40	60	%	-
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	- 1.93	-	ns	-
	eMMC HS200 mode		1.96			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	- 5.9 6.11	ns	-

Table continues on the next page...

Table 111. eSDHC AC timing specifications (SDR104/eMMC HS200) (continued)

Parameter		Symbol[1]	Min	Max	Unit	Notes
	eMMC HS200 mode					
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	-	-	Unit Interval	-
			0.5			
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \le 10pF$.
2. At recommended operating conditions with OV_{DD} =1.8 V.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

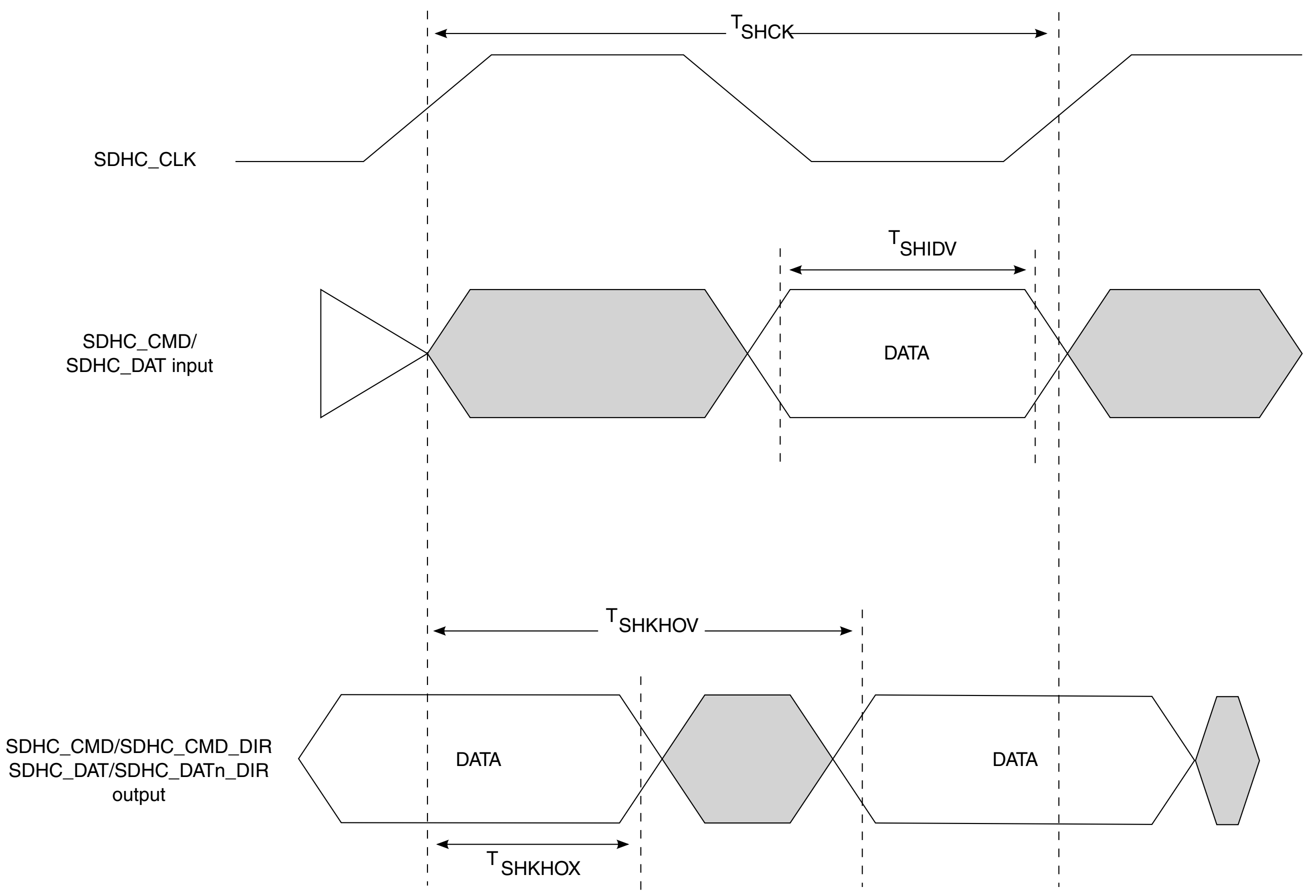


Figure 79. eSDHC SDR104/HS200 mode timing diagram

3.21 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.21.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 112. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL}= 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 5.
3. For recommended operating conditions, see Table 5.

3.21.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 80, Figure 81, Figure 82, and Figure 83.

Table 113. JTAG AC timing specifications[4]

Parameter		Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation		f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time		t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V		t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times		t_{JTGR}/t_{JTGF}	0	2	ns	—
TRST_B assert time		t_{TRST}	25	—	ns	2
Input setup times		t_{JTDVKH}	4	—	ns	—
Input hold times		t_{JTDXKH}	10	—	ns	—
Output valid times	Boundary-scan data	t_{JTKLDV}	—	15	ns	3
	TDO		—	10		
Output hold times		t_{JTKLDX}	0	—	ns	3

Notes:

Table 113. JTAG AC timing specifications[4]

Parameter	Symbol[1]	Min	Max	Unit	Notes
1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).					
2.TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.					
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.					
4. For recommended operating conditions, see Table 5.					

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

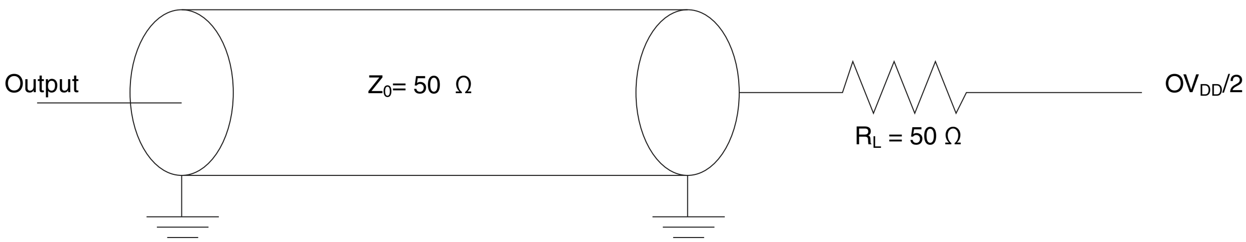


Figure 80. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

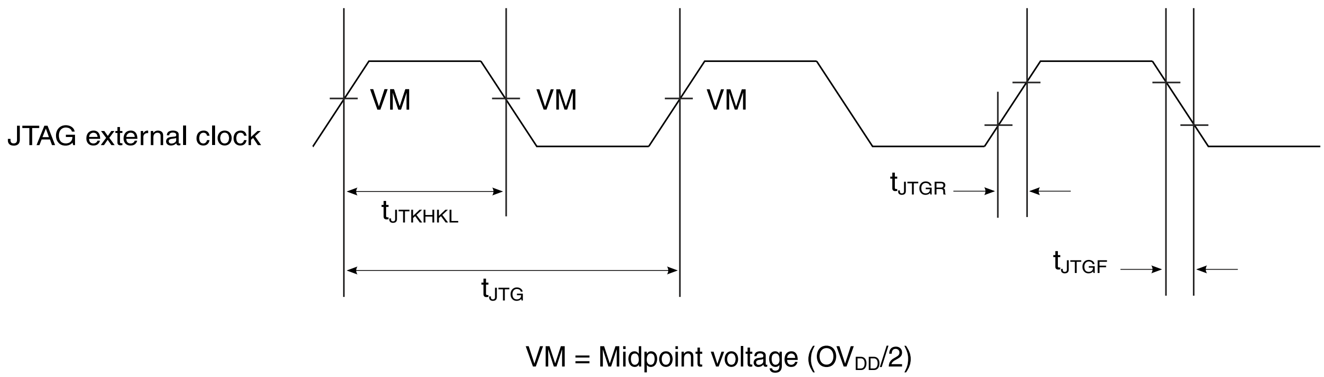


Figure 81. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

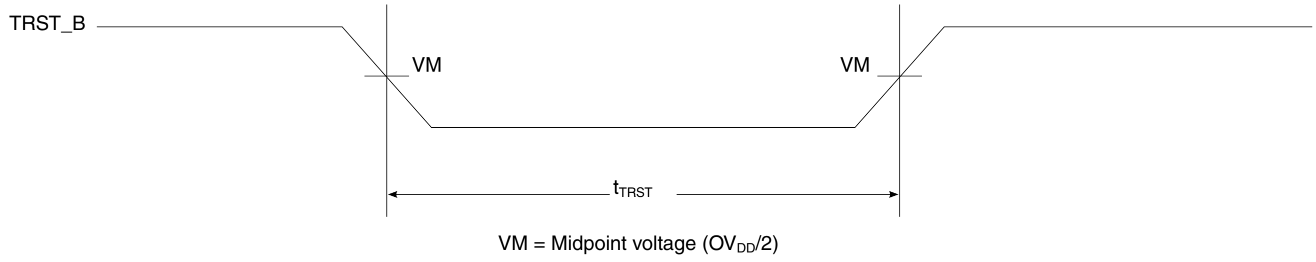


Figure 82. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

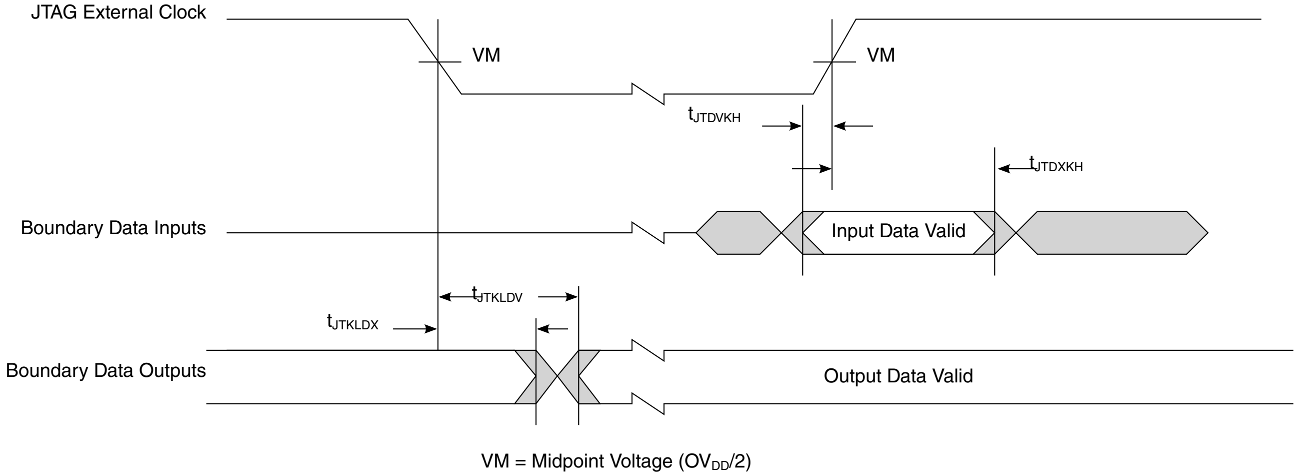


Figure 83. Boundary-scan timing diagram

3.22 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interfaces.

3.22.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1

Table continues on the next page...

Table 114. I^2C DC electrical characteristics (DV_{DD} = 3.3 V)[4] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	—	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	μA	-
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for the I^2C interfaces operating at DV_{DD} = 1.8 V.

Table 115. I^2C DC electrical characteristics (DV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	μA	-
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. For recommended operating conditions, see Table 5.

3.22.2 I^2C AC timing specifications

This table provides the AC timing specifications for the I^2C interfaces.

Table 116. I²C AC timing specifications[5]

Parameter		Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency		f_{I2C}	0	400	kHz	2
Low period of the SCL clock		t_{I2CL}	1.3	—	μs	—
High period of the SCL clock		t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition		t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		t_{I2SXKL}	0.6	—	μs	—
Data setup time		t_{I2DVKH}	100	—	ns	—
Data input hold time	CBUS compatible masters	t_{I2DXKL}	—	—	μs	3
	I²C bus devices		0	—		
Data output delay time		t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition		t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition		t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)		V_{NL}	0.1 x DV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)		V_{NH}	0.2 x DV_{DD}	—	V	—
Capacitive load for each bus line		Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 5.

This figure shows the AC test load for the I²C.

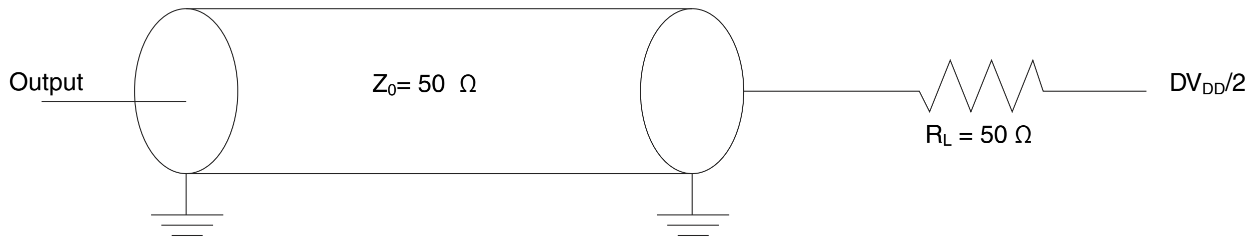


Figure 84. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

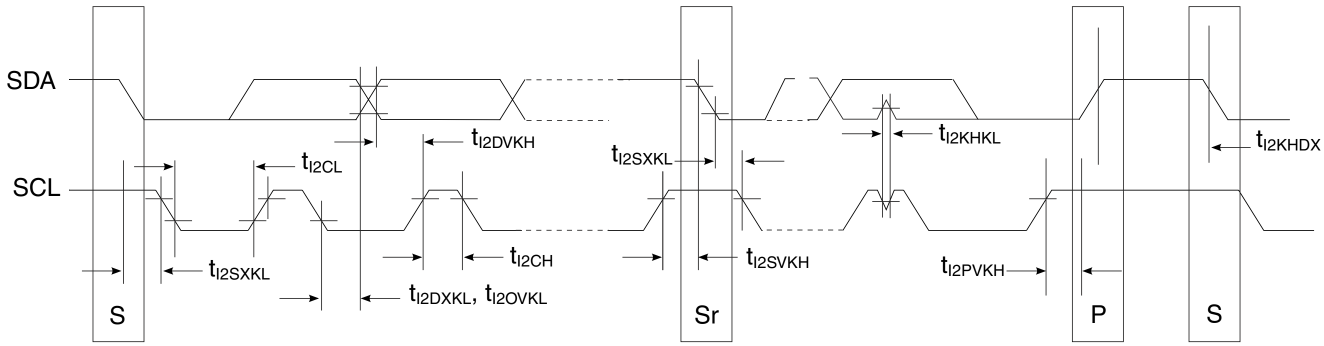


Figure 85. I²C bus AC timing diagram

3.23 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface. There are GPIO pins on various power supplies in this device.

3.23.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at D/ EV_{DD} = 3.3 V.

Table 117. GPIO DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= D/EV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage	V_{OH}	2.4	—	V	—

Table continues on the next page...

Table 117. GPIO DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
(D/EV_{DD} = min, I_{OH} = -2 mA)					
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the DV_{IN}/EV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD} = 2.5 V.

Table 118. GPIO DC electrical characteristics (TV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= TV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (TV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the TV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for GPIO pins operating at $DV_{DD}/EV_{DD}/TV_{DD}$ = 1.8 V.

Table 119. GPIO DC electrical characteristics ($DV_{DD}/EV_{DD}/TV_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/E/TV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.2 x $D/E/TV_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $D/E/TV_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($D/E/TV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($D/E/TV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Table continues on the next page...

Table 119. GPIO DC electrical characteristics ($DV_{DD}/EV_{DD}/TV_{DD}$ = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max $DV_{IN}/EV_{IN}/TV_{IN}$ values found in Table 5. 2. The symbol V_{IN}, in this case, represents the $DV_{IN}/EV_{IN}/TV_{IN}$ symbol referenced in Table 5. 3. For recommended operating conditions, see Table 5.					

This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD} = 1.2 V.

Table 120. GPIO DC electrical characteristics (TV_{DD} = 1.2 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 100uA)	V_{OL}	—	0.2	V	—
Input Capacitance	C_{IN}	—	10	pF	—
Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 5. 2. The symbol V_{IN}, in this case, represents the TV_{IN} symbol referenced in Table 5. 3. For recommended operating conditions, see Table 5.					

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 121. GPIO DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—
Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5. 2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5. 3. For recommended operating conditions, see Table 5.					

This table provides the DC electrical characteristics for GPIO pins operating at OV_{IN}/ LV_{IN} = = = 1.8 V.

Table 122. GPIO DC electrical characteristics (OV_{DD}/LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = O/LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN}/LV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the OV_{IN}/LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.23.2 GPIO AC timing specifications

Table below provides the GPIO input and output AC timing specifications.

Table 123. GPIO Input AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least tPIWID to ensure proper operation.
2. For recommended operating conditions, see Table 5

Figure below provides the AC test load for the GPIO.

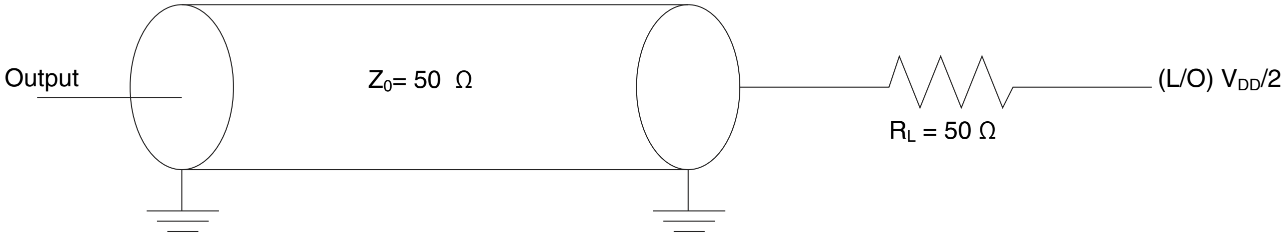


Figure 86. GPIO AC test load

3.24 GIC interface

This section describes the DC and AC electrical characteristics for the GIC interface.

3.24.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for GIC pins operating at DV_{DD} = 3.3 V.

Table 124. GIC DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for GIC pins operating at DV_{DD} = 1.8 V.

Table 125. GIC DC electrical characteristics (DV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for GIC pins operating at LV_{DD} = 2.5 V.

Table 126. GIC DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

This table provides the DC electrical characteristics for GIC pins operating at O/ LV_{DD} = 1.8 V.

Table 127. GIC DC electrical characteristics (O/LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = O/LV_{DD})	I_{IN}	—	±50	μA	2

Table continues on the next page...

Table 127. GIC DC electrical characteristics (O/LV_{DD} = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max O/LV_{IN} values found in Table 5.
2. The symbol V_{IN}, in this case, represents the O/LV_{IN} symbol referenced in Table 5.
3. For recommended operating conditions, see Table 5.

3.24.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications.

Table 128. GIC Input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 5.

3.25 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, QSGMII, XFI, 1000Base-KX and serial ATA (SATA) data transfers.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.25.1 Signal terms definitions

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

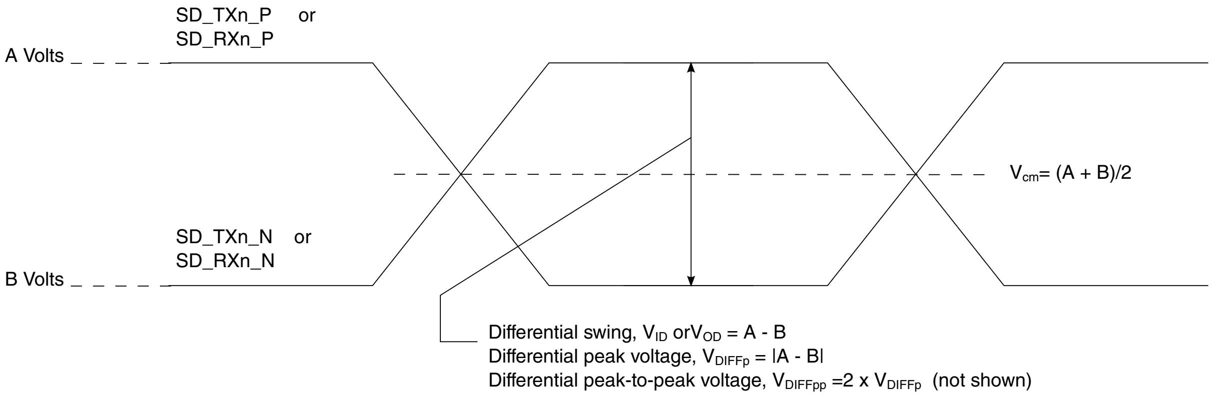


Figure 87. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P}$ - $V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 92 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

3.25.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP block based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbps or 3.125 Gbps), QSGMII (5 Gbps)
- XFI (10Gbps)
- PCIe (2.5 Gbps and 5 Gbps)
- SATA (1.5 Gbps, 3.0 Gbps and 6.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.25.2.1 SerDes spread-spectrum clock source recommendations

SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 129. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 129. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2
Notes: 1. At recommended operating conditions. See Table 5. 2. Only down-spreading is allowed.				

3.25.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

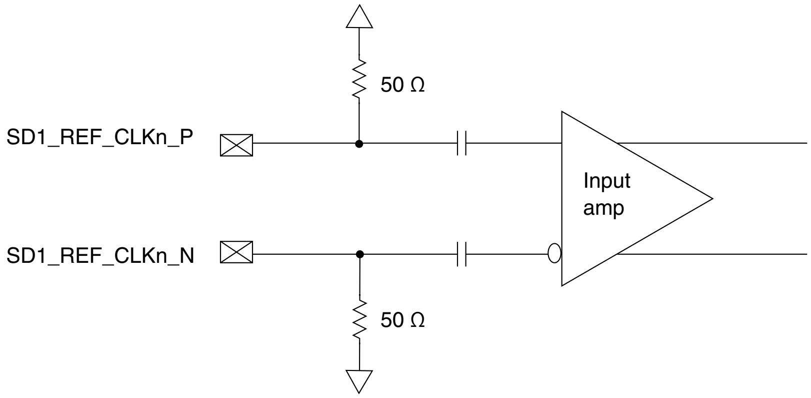


Figure 88. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceiver's core power supply voltage requirements ($S1V_{DD}$) are as specified in Table 5.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 88. Each differential clock input (SD1_REF_CLK*n*_P or SD1_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.25.2.3 DC-level requirements for SerDes reference clocks

The DC-level requirements for the SerDes reference clock inputs are different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Figure 88, the maximum average current requirements set the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.
  - This figure shows the SerDes reference clock input requirement for a DC-coupled connection scheme.

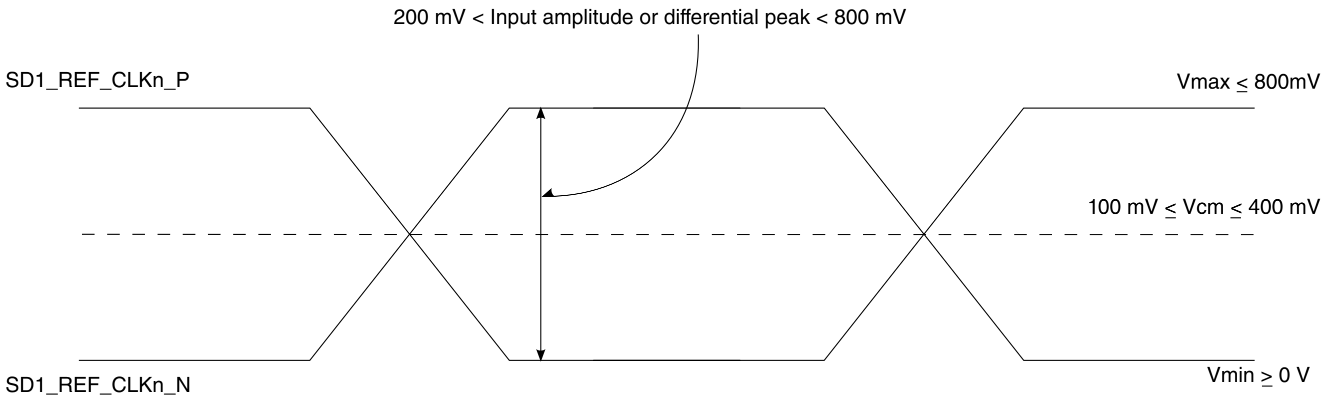


Figure 89. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*).
  - This figure shows the SerDes reference clock input requirement for an AC-coupled connection scheme.

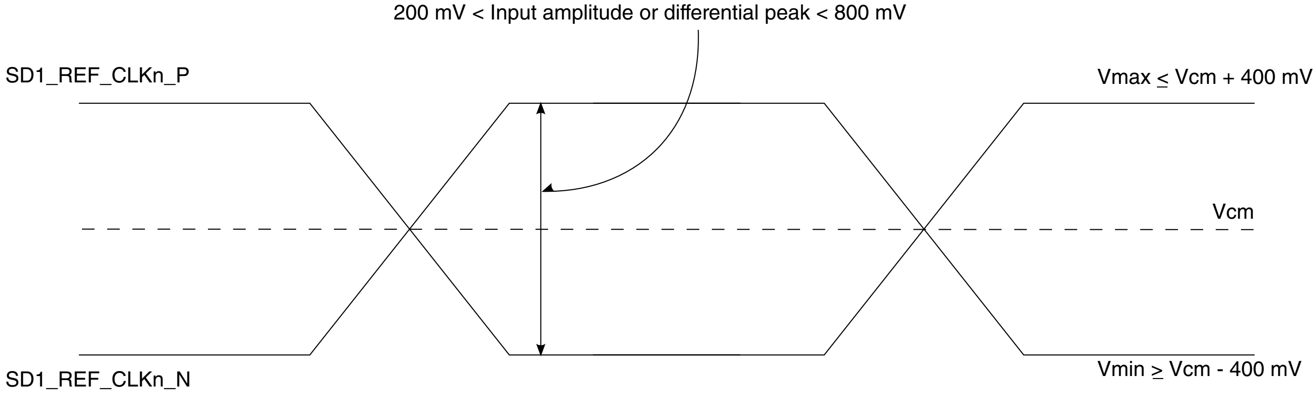


Figure 90. Differential reference clock input DC requirements (external AC-coupled)

- Single-ended mode
  - The reference clock can also be single-ended. The SD1_REF_CLK*n*_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD1_REF_CLK*n*_N either left unconnected or tied to ground.
  - To meet the input amplitude requirement, the reference clock inputs may need to be externally DC- or AC-coupled. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD1_REF_CLK*n*_N) through the same source impedance as the clock input (SD1_REF_CLK*n*_P) in use.
  - The SD1_REF_CLK*n*_P input average voltage must be between 200 and 400 mV.
  - This figure shows the SerDes reference clock input requirement for single-ended signaling mode.

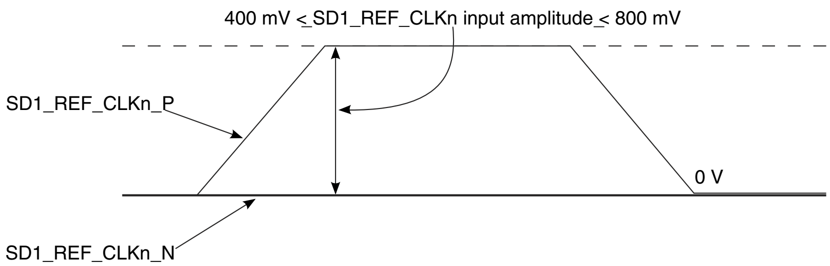


Figure 91. Single-ended reference clock input DC requirements

3.25.2.4 AC requirements for SerDes reference clocks

This table provides the AC requirements for SerDes reference clocks for PCI Express protocols running at data rates up to 5 Gb/s.

This includes PCI Express (2.5 and 5 GT/s), QSGMII (5Gbps), SGMII (1.25 Gbps and 3.125 Gbps), and SATA (1.5, 3.0 and 6.0 Gbps). SerDes reference clocks need to be verified by the customer's application design.

Table 130. SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N input clock requirements ($S1V_{DD}$) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	2
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	4
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	—	4	V/ns	9
Differential input high voltage	V_{IH}	150	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-150	mV	5
Rising edge rate (SD1_REF_CLK*n*_P) to falling edge rate (SD1_REF_CLK*n*_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 5.

2. **Caution:** Only 100, 125 and 156.25 MHz frequencies have been tested. In-between values do not work correctly with the rest of the system.

3. For PCI Express (2.5 and 5 GT/s).

4. For SGMII and QSGMII.

5. Measurement taken from differential waveform.

6. Limits from PCI Express CEM Rev 2.0.

7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.

9. Measured from -150 mV to +150 mV on the differential waveform (derived from SD1_REF_CLK*n*_P minus SD1_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 92.

10. Measurement taken from single-ended waveform.

11. Matching applies to rising edge for SD1_REF_CLK*n*_P and falling edge rate for SD1_REF_CLK*n*_N. It is measured using a +/-75 mV window centered on the median cross point where SD1_REF_CLK*n*_P rising meets SD1_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD1_REF_CLK*n*_P must be compared to the fall edge rate of SD1_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 93.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

Table 131. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements ($S1V_{DD}$)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-

Notes:

1. For recommended operating conditions, see Table 5.
2. **Caution:** Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.
3. Measurement taken from differential waveform.
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

This figure shows the differential measurement points for rise and fall time.

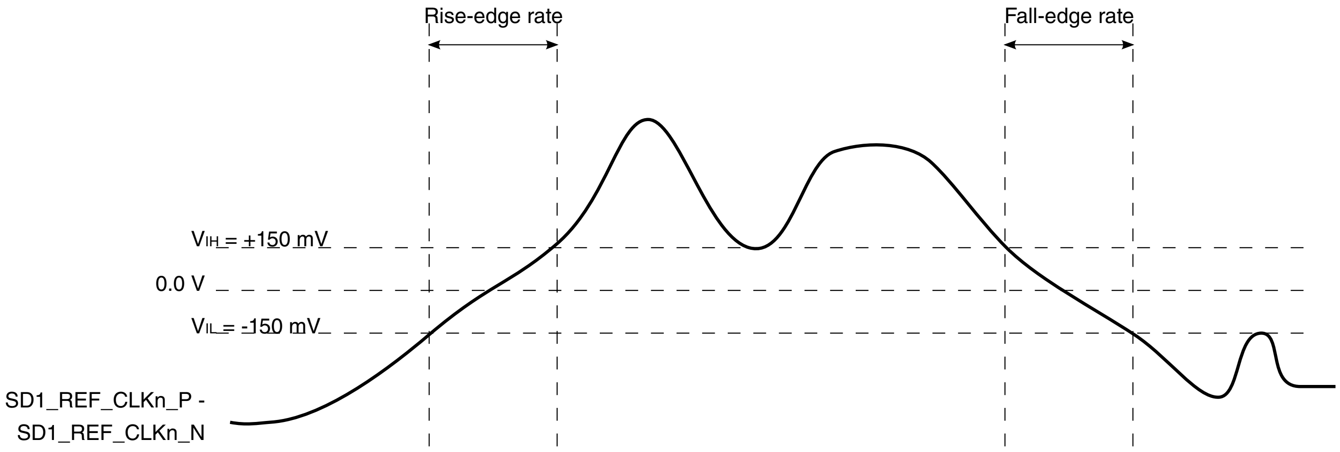


Figure 92. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

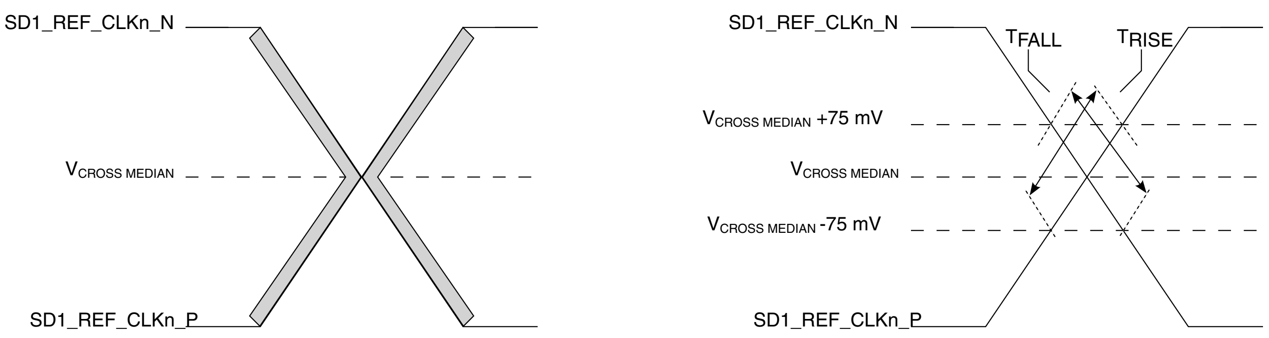


Figure 93. Single-ended measurement points for rise and fall time matching

3.25.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

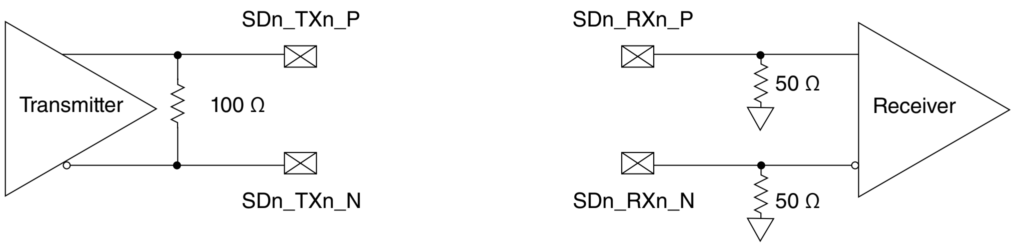


Figure 94. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.25.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.25.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.25.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.25.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 132. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

Table continues on the next page...

Table 132. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states
Notes: 1. For recommended operating conditions, see Table 5.						

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 133. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states
Notes: 1. For recommended operating conditions, see Table 5.						

3.25.4.2.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 134. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications ($S1V_{DD}$)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 5.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 135. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications ($S1V_{DD}$)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver

Table continues on the next page...

Table 135. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications ($S1V_{DD}$)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes:						
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.						
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.						
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.						
4. For recommended operating conditions, see Table 5 .						

3.25.4.3 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.25.4.3.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 136. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	$T_{TX\text{-}EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} =$ 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all

Table continues on the next page...

Table 136. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
						edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Test and measurement load and measured over any 250 consecutive transmitter UIs.

2. A $T_{TX\text{-}EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 5.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 137. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	$T_{TX\text{-}EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE}$ = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	-	-	0.15	UI	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX\text{-}LF\text{-}RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Test and measurement load and measured over any 250 consecutive transmitter UIs.

2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

3. For recommended operating conditions, see Table 5.

3.25.4.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 138. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Test and measurement load must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 5.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 139. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture
Note: 1. For recommended operating conditions, see Table 5.						

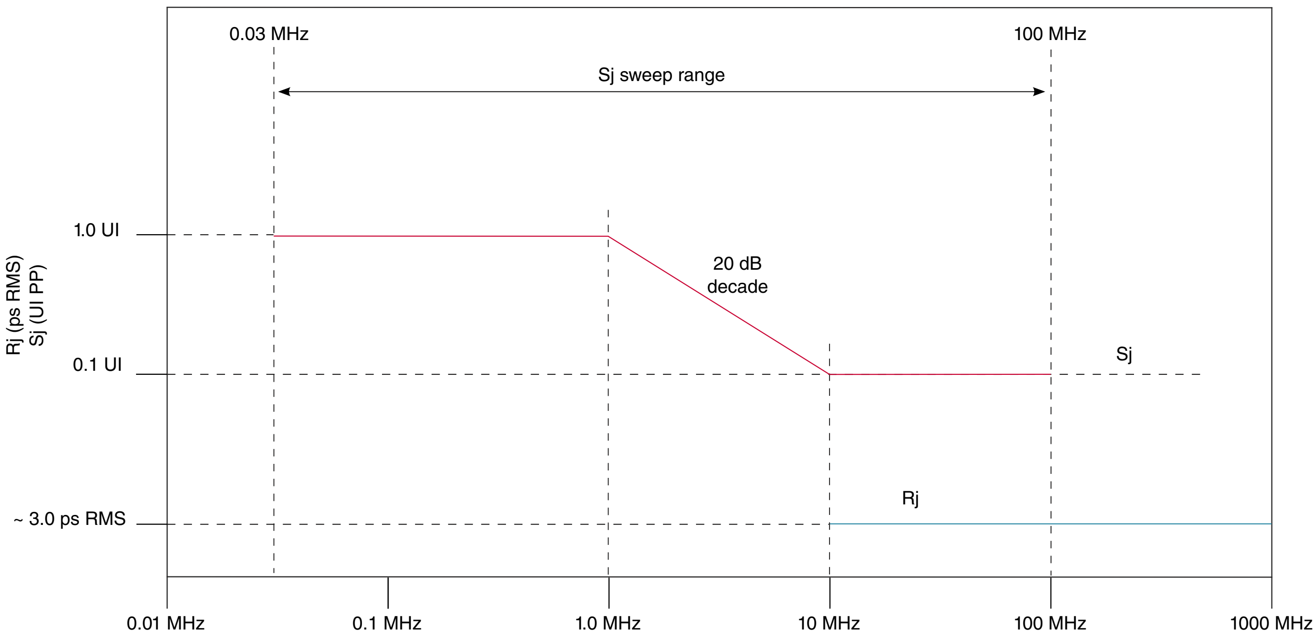


Figure 95. Swept sinusoidal jitter mask

3.25.4.4 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

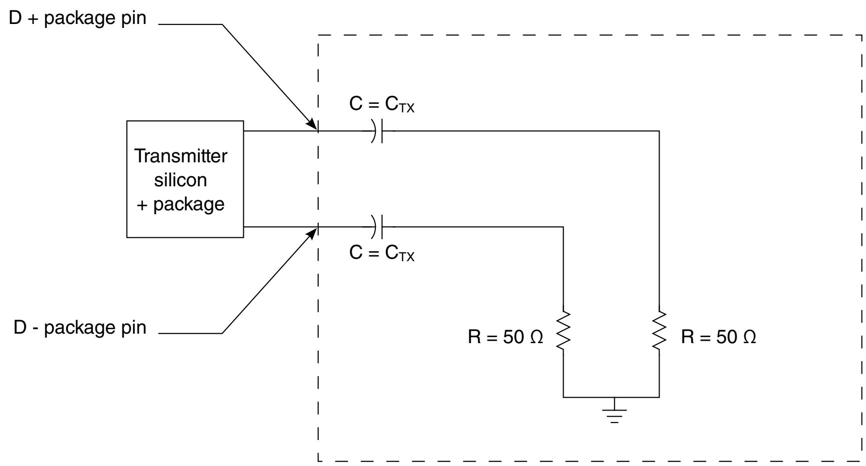


Figure 96. Test and measurement load

3.25.5 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the SATA interface.

3.25.5.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.25.5.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 140. Gen1i/1m 1.5 G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Table continues on the next page...

Table 140. Gen1i/1m 1.5 G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[3] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Terminated by 50 Ω load. 2. DC impedance. 3. For recommended operating conditions, see Table 5.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 141. Gen 2i/2m 3 G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—
Notes: 1. Terminated by 50 Ω load. 2. For recommended operating conditions, see Table 5.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 142. Gen 3i transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	240	—	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—
Notes: 1. Terminated by 50 Ω load. 2. For recommended operating conditions, see Table 5.						

3.25.5.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 143. Gen1i/1m 1.5 G receiver input DC specifications ($S1V_{DD}$)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2

Table continues on the next page...

Table 143. Gen1i/1m 1.5 G receiver input DC specifications ($S1V_{DD}$)[3] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 5.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 144. Gen2i/2m 3 G receiver input DC specifications ($S1V_{DD}$)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 5.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 145. Gen 3i receiver input DC specifications ($S1V_{DD}$)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	—	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 5.

3.25.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

3.25.5.2.1 AC requirements for SATA REF_CLK

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 146. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLK1_P/SD1_REF_CLK1_N frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD1_REF_CLK1_P/SD1_REF_CLK1_N clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD1_REF_CLK1_P/SD1_REF_CLK1_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLK1_P/SD1_REF_CLK1_N cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD1_REF_CLK1_P/SD1_REF_CLK1_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	—	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100 and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input.
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform.
6. For recommended operating conditions, see Table 5.

3.25.5.2.2 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 147. Gen 1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 5.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 148. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.

2. For recommended operating conditions, see Table 5.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 149. Gen 3i transmitter AC specifications

Parameter	Symbol	Min	Typ	Max	Units
Speed	—	—	6.0	—	Gb/s
Total jitter before and after compliance interconnect channel	J_T	—	—	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

3.25.5.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 150. Gen 1i/1m 1.5 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	—	—	0.25	UI p-p	1

Table continues on the next page...

Table 150. Gen 1i/1m 1.5 G receiver AC specifications[2] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.

2. For recommended operating conditions, see Table 5.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 151. Gen 2i/2m 3 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.

2. For recommended operating conditions, see Table 5.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 152. Gen 3i receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	—	—	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	—

Notes:

1. Measured at the receiver.

2. The AC specifications do not include RefClk jitter.

4 Hardware design considerations

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- Core cluster CGA PLL1 generates a clock for all the cores and/or FMAN, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- Core cluster CGA PLL2 generates a clock for all the cores and/or FMAN & eSDHC, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input.
- The 4 lane SerDes blocks has two PLLs which generate a clock from their respective externally supplied SD1_REF_CLK*n*_P/SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in Valid reference clocks and PLL configurations for SerDes protocols .

4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 153. Processor, platform, and memory clocking specifications (V_{DD} = 0.9 V)

Characteristic	Maximum processor core frequency				Unit	Notes
	1000 MHz		1200 MHz			
	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	MHz	1
Platform clock frequency	256	300	256	300	MHz	1
Memory Bus Clock Frequency (DDR3L)	500	650	500	650	MHz	1, 2, 3
Memory Bus Clock Frequency (DDR4)	650	650	650	650	MHz	1, 3
IFC clock frequency	-	100	-	100	MHz	4
FMan	350	500	350	500	MHz	-

Table continues on the next page...

Table 153. Processor, platform, and memory clocking specifications (V_{DD} = 0.9 V) (continued)

Characteristic	Maximum processor core frequency				Unit	Notes
	1000 MHz		1200 MHz			
	Min	Max	Min	Max		

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate. DDR3L memory bus clock frequency is limited to min = 1000 MT/s whereas DDR4 memory bus clock frequency is limited to min/max = 1300 MT/s.

3. The memory bus clock speed is dictated by its own PLL.

4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

6. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com

Table 154. Processor, platform, and memory clocking specifications (V_{DD} = 1.0 V)

Characteristic	Maximum processor core frequency								Unit	Notes
	1000 MHz		1200 MHz		1400 MHz		1600 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	1000	1400	1000	1600	MHz	1
Platform clock frequency	256	300	256	300	256	300	256	400	MHz	1
Memory Bus Clock Frequency (DDR3L)	500	800	500	800	500	800	500	800	MHz	1, 2, 3
Memory Bus Clock Frequency (DDR4)	650	800	650	800	650	800	650	800	MHz	1, 3
IFC clock frequency	-	100	-	100	-	100	-	100	MHz	4
FMan	350	500	350	500	350	500	350	500	MHz	

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate. DDR3L memory bus clock frequency is limited to min = 1000 MT/s whereas DDR4 memory bus clock frequency is limited to min = 1300 MT/s.

3. The memory bus clock speed is dictated by its own PLL.

4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

6. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com

4.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 155. Memory bus clocking specifications

Characteristic	Min Freq.(MHz)	Max Freq.(MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
Memory bus clock frequency and Data Rate for DDR3L	500	800	1000	1600	1, 2, 3
Memory bus clock frequency and Data Rate for DDR4	650	800	1300	1600	1, 2, 3

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings.

2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:3] and Dn_MCK[0:3]_B output clocks, running at half of the DDR data rate.

3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios.

4. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com

4.1.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock-frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 156. Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1

Table continues on the next page...

Table 156. Platform to SYSCLK PLL ratios (continued)

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0110	6:1
All Others	Reserved
Notes: 1. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.	

4.1.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CG*m*_PLL*n*_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CG*n*_PLL_CFG = 0b00.

This table below lists the supported asynchronous core cluster to SYSCLK ratios.

Table 157. Core cluster PLL to SYSCLK ratios

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0001	17:1
01_0010	18:1
01_0011	19:1
01_0100	20:1
01_0101	21:1
01_0110	22:1
01_0111	23:1
01_1000	24:1
01_1001	25:1
All others	Reserved
Notes: 1. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A multicore communications processors at www.nxp.com.	

4.1.5 Core complex PLL select

The clock frequency of each core is determined by the binary value of the RCW Configuration field C1_PLL_SEL. The tables describe the selections available for each core, where each individual core can select a frequency from their respective tables.

Table 158. Core PLL select

Binary Value of C*1*_PLL_SEL	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
0100	CGA PLL2 /1
0101	CGA PLL2 /2

4.1.6 DDR controller PLL ratios

DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 159. DDR clock ratio

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1010	10:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1011	11:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1100	12:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1101	13:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1110	14:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1111	15:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.

Table continues on the next page...

Table 159. DDR clock ratio (continued)

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
01_0000	16:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0001	17:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0010	18:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0011	19:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0100	20:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0101	21:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0110	22:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0111	23:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_1000	24:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
All Others	Reserved	-
Notes: 1. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.		

4.1.7 Valid reference clocks and PLL configurations for SerDes protocols

Each supported SerDes protocol allows for a finite set of valid SerDes-related RCW fields and reference clock frequencies.

The clock ratio between each SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs is determined by a set of RCW configuration fields, SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_PEX as shown in this table.

Table 160. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Valid setting for SRDS_PRTCL_S1	Valid setting for SRDS_PLL_REF_CLK_SEL_S1		Valid setting for SRDS_DIV_PEX
			PLL1	PLL2	
High Speed Serial interface					

Table continues on the next page...

Table 160. Valid SerDes RCW encodings and reference clocks (continued)

SerDes protocol (given lane)	Valid reference clock frequency	Valid setting for SRDS_PRTCL_S1	Valid setting for SRDS_PLL_REF _CLK_SEL_S1		Valid setting for SRDS_DIV_PEX
			PLL1	PLL2	
PCI Express 2.5 Gbit/s (doesn't negotiate upwards)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	10: 2.5 G
	125 MHz		1: 125 MHz	1: 125 MHz	
PCI Express 5 Gbit/s (can negotiate up to 5 Gbit/s)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	01: 5 G
	125 MHz		1: 125 MHz	1: 125 MHz	
SATA (1.5, 3, 6 Gbit/s)	100 MHz	Any SATA	0: 100 MHz	-	Don't Care
	125 MHz		1: 125 MHz	-	
Networking interfaces					
SGMII (1.25 Gbit/s)	100 MHz	SGMII @ 1.25 Gbit/s	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
2.5 G SGMII (3.125 Gbit/s)	125 Mhz	SGMII @ 3.125 Gbit/s	0: 125 MHz	-	Don't Care
	156.25 MHz		1: 156.25 MHz	-	
QSGMII (5 Gbit/s)	100 MHz	Any QSGMII	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
XFI (10.3125 Gbit/s)	156.25 Mhz		1: 156.25 MHz	-	-
				-	

Notes:

1) A spread-spectrum reference clock is permitted for PCI Express. However, if any other high speed interface such as SGMII, QSGMII, SATA, or Debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

2) SerDes lanes configured as SATA initially operate at 3.0 Gbit/s. 1.5 Gbit/s operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.

4.1.8 Frequency options

This section discusses interface frequency options.

4.1.8.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 161. SYSCLK and core cluster frequency[1]

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Core cluster Frequency - (MHz)[1]		
10:1			1000
11:1			1100
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1267	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1467	
23:1	1472	1533	
24:1	1536	1600	
25:1	1600		

Notes:

1. Core cluster output is the operating frequency of the core.
2. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
3. When using Single Source clocking only 100 MHz input is available.
4. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.

4.1.8.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 162. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Platform Frequency (MHz)[1]		
3:1			300
4:1	256	267	400
5:1	320	333	
6:1	384	400	

Notes:

Table 162. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Platform Frequency (MHz)[1]		
1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)			
2. When using Single source clocking, only 100 MHz options are valid			
3. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.			

4.1.8.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 163. DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)		
	64.00	66.67	100.00
	DDR Data Rate (MT/s)[1]		
10:1			1000
11:1			1100
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1266	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1466	
23:1	1472	1533	
24:1	1536	1600	
Notes:			
1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed)			
2. When using Single Source clocking, only 100 MHz options are available.			
3. Minimum Frequency supported by DDR4 is 1300 MT/s. DDR3 supports a minimum of 1000 MT/s.			
4. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.			

4.1.8.4 SYSCLK and eSDHC high speed modes frequency options

This table shows the frequency multiplier options for SYSCLK when eSDHC operates in High Speed modes (>=52 MHz). For low frequency options CGA PLL2 is bypassed and eSDHC receives platform clock directly.

Table 164. SYSCLK multiplier/frequency options when eSDHC operates in High Speed mode (clocked by CGA PLL2 / 1)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Resultant Frequency (MHz)[1]		
12:1			1200
18:1	1152	1200	

Notes:

1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. For Low speed operation, eSDHC is clocked from Platform PLL and does not use CGA PLL2.

4.1.8.5 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below:.For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 97. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 98. Gen 2 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

4.2 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, DV_{DD}, EV_{DD}, LV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$ as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, DV_{DD}, EV_{DD}, LV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$ and GND pins of the device.
- The chip has temperature diodes on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). If a temperature diode monitoring device is not connected, these pins must be connected to GND.

4.2.1 JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins, as demonstrated in Figure 100. Take care to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The ARM Cortex 10-pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals.

The Cortex Debug Connector has a standard header, as shown in Figure 99. The connector typically has pin 7 removed as a connector key.

The ARM Cortex 10-pin header adds many benefits, such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the ARM Cortex 10-pin header unpopulated until needed.

4.2.1.1 Termination of unused signals

If the JTAG interface and ARM Cortex 10-pin header are not used, no pull-up/pull-down is required for TDI, TMS, or TDO.

This figure shows the ARM Cortex 10-pin header physical pinout.

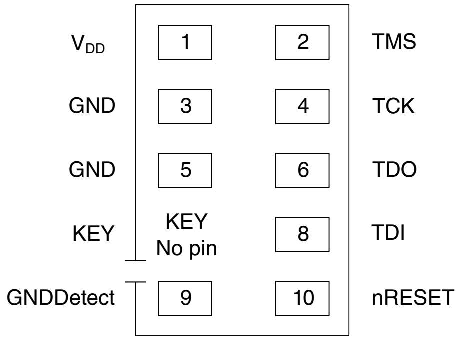
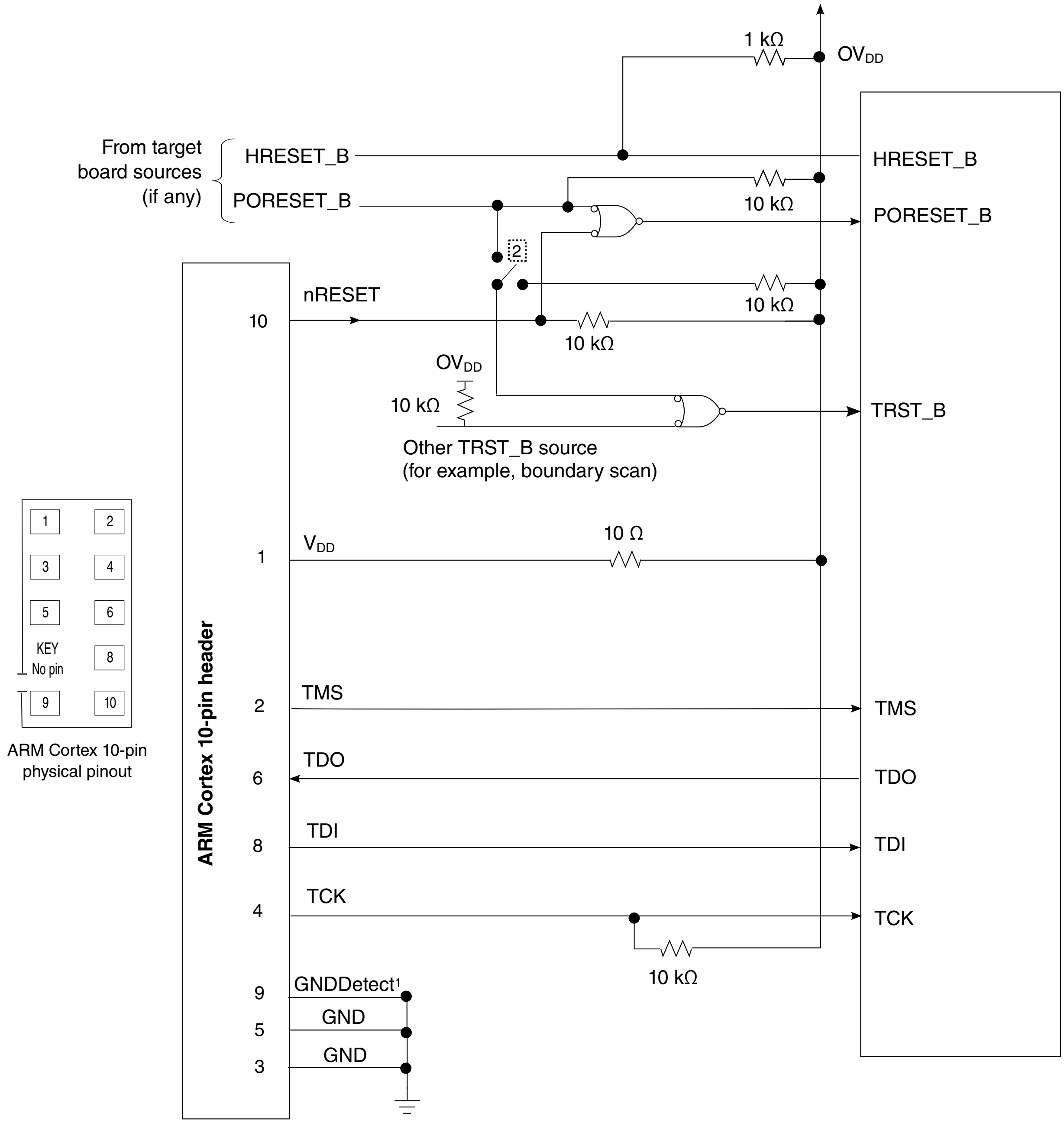


Figure 99. ARM Cortex 10-pin header physical pinout

This figure shows the JTAG interface connection.



Note:

1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, ensure this switch is closed.

Figure 100. JTAG interface connection

4.2.2 Guidelines for high-speed interface termination

4.2.2.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that $S1V_{DD}$, $X1V_{DD}$, AVDD_SD1_PLL1, and AVDD_SD1_PLL2 must remain powered.

AVDD_SD1_PLL1 must be connected to $X1V_{DD}$ through a 0-Ω resistor (instead of through a filter circuit, as shown in Figure 2).

The following pins must be left unconnected:

- SD1_TX[3:0]_P
- SD1_TX[3:0]_N
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to SD_GND:

- SD1_REF_CLK1_P, SD1_REF_CLK2_P
- SD1_REF_CLK1_N, SD1_REF_CLK2_N

It is recommended for the following pins to be connected to SD_GND:

- SD1_RX[3:0]_P
- SD1_RX[3:0]_N

It is possible to disable the SerDes module by disabling all PLLs associated with it. Use the following method to disable the SerDes module:

- SRDS_PLL_PD_S1 = 2’b11 (Both PLLs are configured as powered down; all data lanes selected by the protocols defined in SRDS_PRTCL_S1 associated to the PLLs are powered down, as well.)
- SRDS_PLL_REF_CLK_SEL_S1 = 2’b00
- SRDS_PRTCL_S1 = 2 (No other values are permitted when both PLLs are powered down.)

4.2.2.2 SerDes interface partly unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both $S1V_{DD}$ and $X1V_{DD}$ must remain powered.

If any of the PLLs are unused, the corresponding AVDD_SD1_PLL1 and AVDD_SD1_PLL2 must be connected to $X1V_{DD}$ through a 0-Ω resistor (instead of through a filter circuit, as shown in Figure 2).

The following unused pins must be left unconnected:

- SD1_TX0_P
- SD1_TX0_N

The following unused pins must be connected to SD_GND:

- SD1_REF_CLK*n*_P, SD1_REF_CLK*n*_N (If the entire SerDes is unused.)

It is recommended for the following unused pins to be connected to SD_GND:

- SD1_RX0_P
- SD1_RX0_N

In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

Unused lanes must be powered down through the SRDSx Lane m General Control 0 (LNmGCR0) register as follows:

- LNmGCR0[RRST] = 0
- LNmGCR0[TRST] = 0
- LNmGCR0[RX_PD] = 1
- LNmGCR0[TX_PD] = 1

Note that in the case where the SerDes pins are connected to slots, it is acceptable to have these pins unterminated when unused.

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 165. Package thermal characteristics[6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	33	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	24	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	27	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	20	°C/W	1, 2

Table continues on the next page...

Table 165. Package thermal characteristics[6] (continued)

Rating	Board	Symbol	Value	Unit	Notes
Junction to board	-	$R_{\Theta JB}$	14	°C/W	3
Junction to case (Top)	-	$R_{\Theta JCtop}$	<0.1	°C/W	4

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.

4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5. See Thermal management information, for additional details.

6. Package thermal characteristics are applicable for the 21x21mm and 23x23mm package.

Table 166. Thermal Resistance with Heat Sink in Open Flow, No Lid[4]

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance °C/W
Wakefield 53 x 53 x 25 mm Pin Fin	Natural Convection	6.9
	0.5 m/s	4.3
	1.0 m/s	3.3
	2.0 m/s	2.8
	4.0 m/s	2.5
Aavid 35 x 31 x 23 mm Pin Fin	Natural Convection	9.2
	0.5 m/s	5.5
	1.0 m/s	4.6
	2.0 m/s	4.0
	4.0 m/s	3.5
Aavid 30 x 30 x 9.4 mm Pin Fin	Natural Convection	12.9
	0.5 m/s	8.7
	1.0 m/s	6.9
	2.0 m/s	5.4
	4.0 m/s	4.5
Aavid 43 x 41 x 16.5 mm Pin Fin	Natural Convection	9.3
	0.5 m/s	5.9
	1.0 m/s	4.5
	2.0 m/s	3.6
	4.0 m/s	3.0

1. Simulations with heat sinks were done with package mounted on 2s2p thermal board.

2. Standard thermal interface was a typical thermal grease with thermal resistance 67 C-mm2/W.

Table 166. Thermal Resistance with Heat Sink in Open Flow, No Lid[4]

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance °C/W
3. See Thermal management information, for additional details.		
4. Thermal Resistance with Heat Sink in Open Flow (No Lid) are applicable for 21x21mm and 23x23mm package.		

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 - 230 μA

Ideality factor over 13.5 - 220 μA; Temperature range 80°C - 105°C: n = 1.004 ± 0.008

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 101. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 Newton).

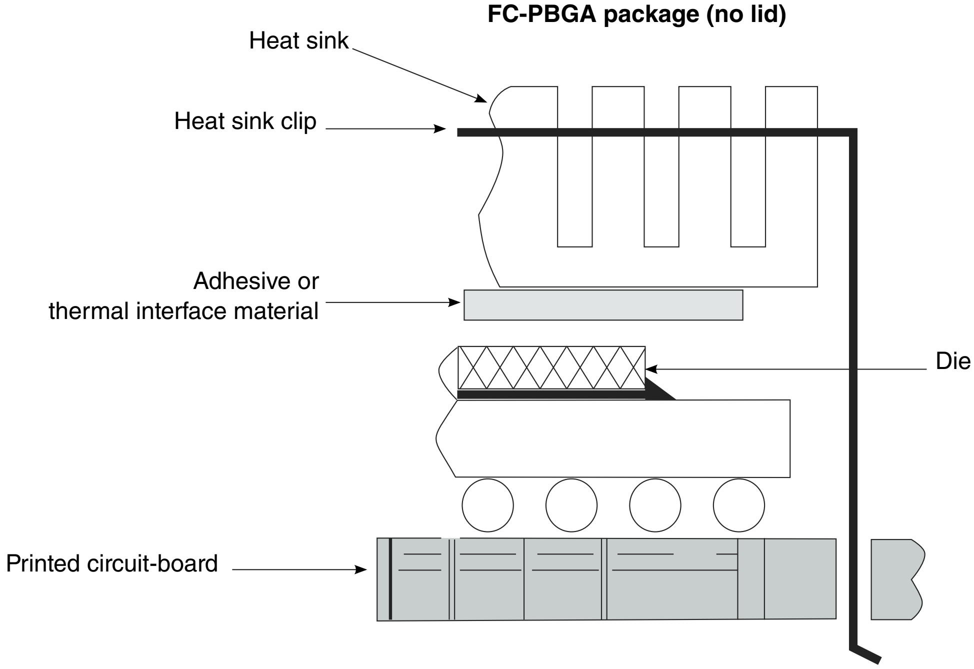


Figure 101. Package exploded, cross-sectional view-FC-PBGA (no lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

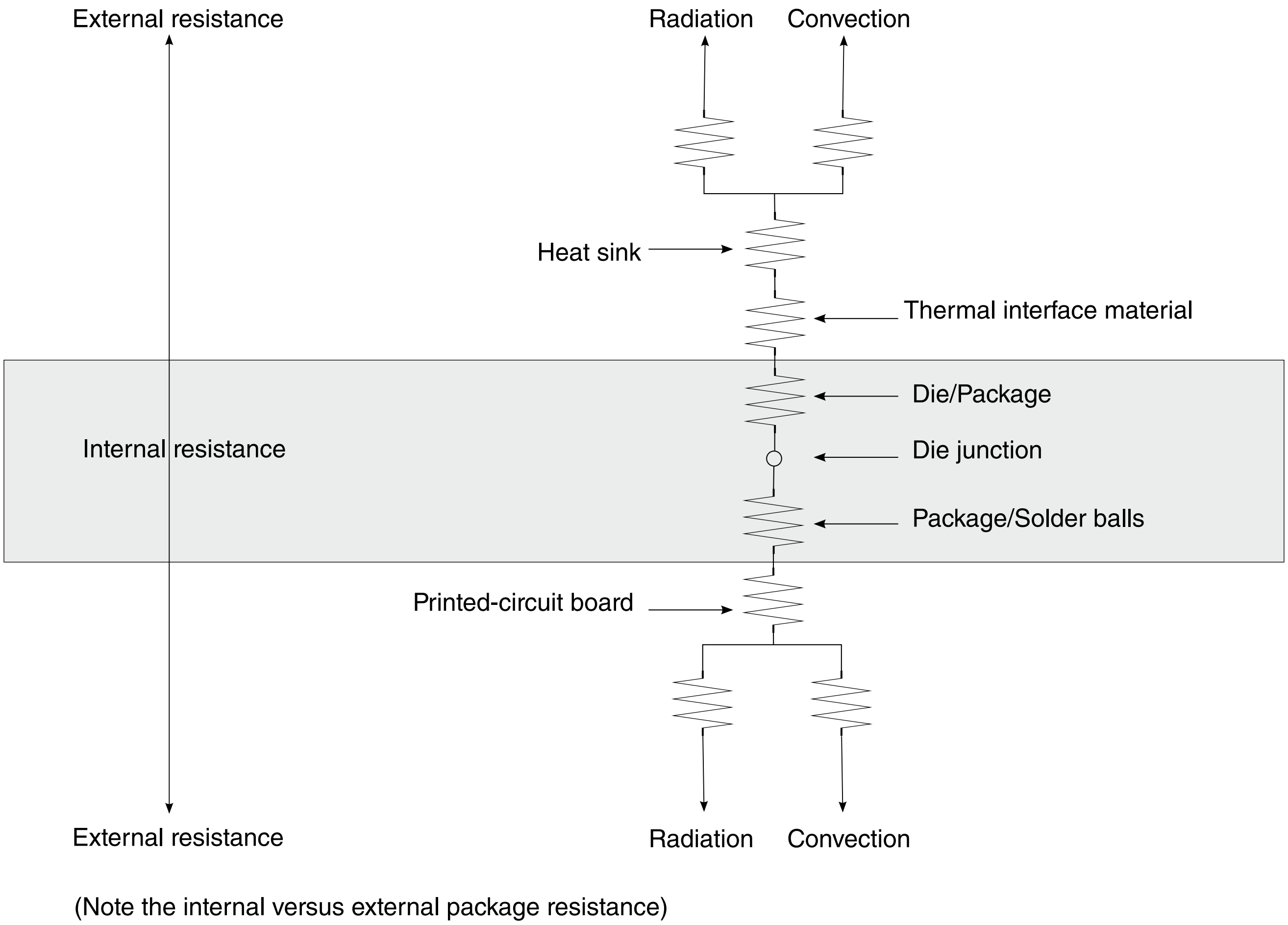


Figure 102. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

5.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 101).

The system board designer can choose among several types of commercially available thermal interface materials.

6 Package information

6.1 Package parameters for the FC-PBGA

The package type is 21 mm x 21 mm, 621 flip-chip, plastic ball grid array (FC-PBGA).

- Package outline - 21 mm x 21 mm
- Interconnects - 621
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - SAC305
- Module height (typical) - 1.77 mm (minimum), 1.92 mm (typical), 2.07 mm (maximum).

The package type is 23 mm x 23 mm, 780 flip-chip, plastic ball grid array (FC-PBGA).

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - SAC305
- Module height (typical) - 1.77 mm (minimum), 1.92 mm (typical), 2.07 mm (maximum).

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip in 21x21 mm (621 balls) pakage.

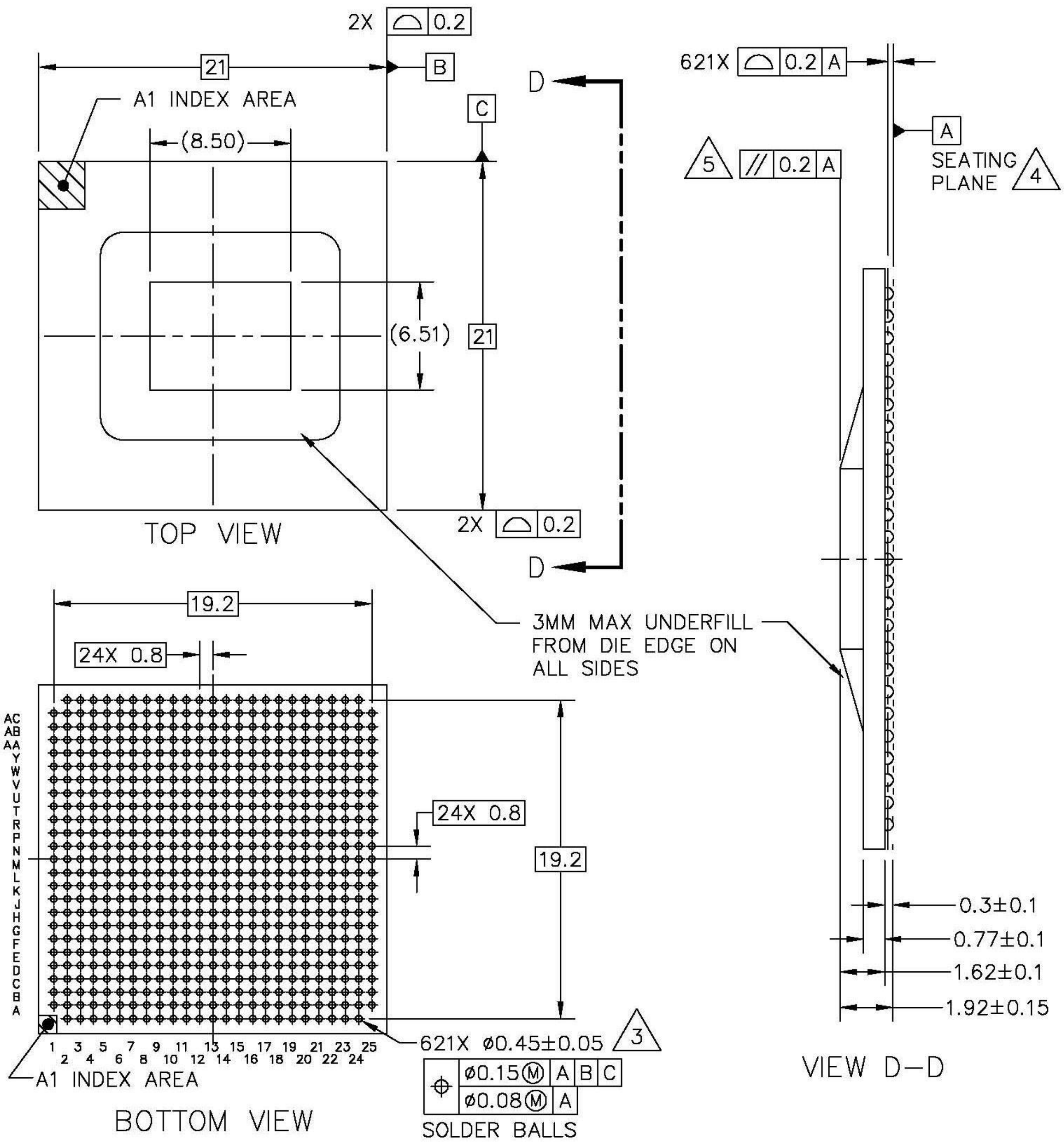


Figure 103. Mechanical dimensions of the FC-PBGA 21x21 mm (621 balls)

Notes:

1. ALL DIMESNSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip in 23x23 mm (780 balls) package.

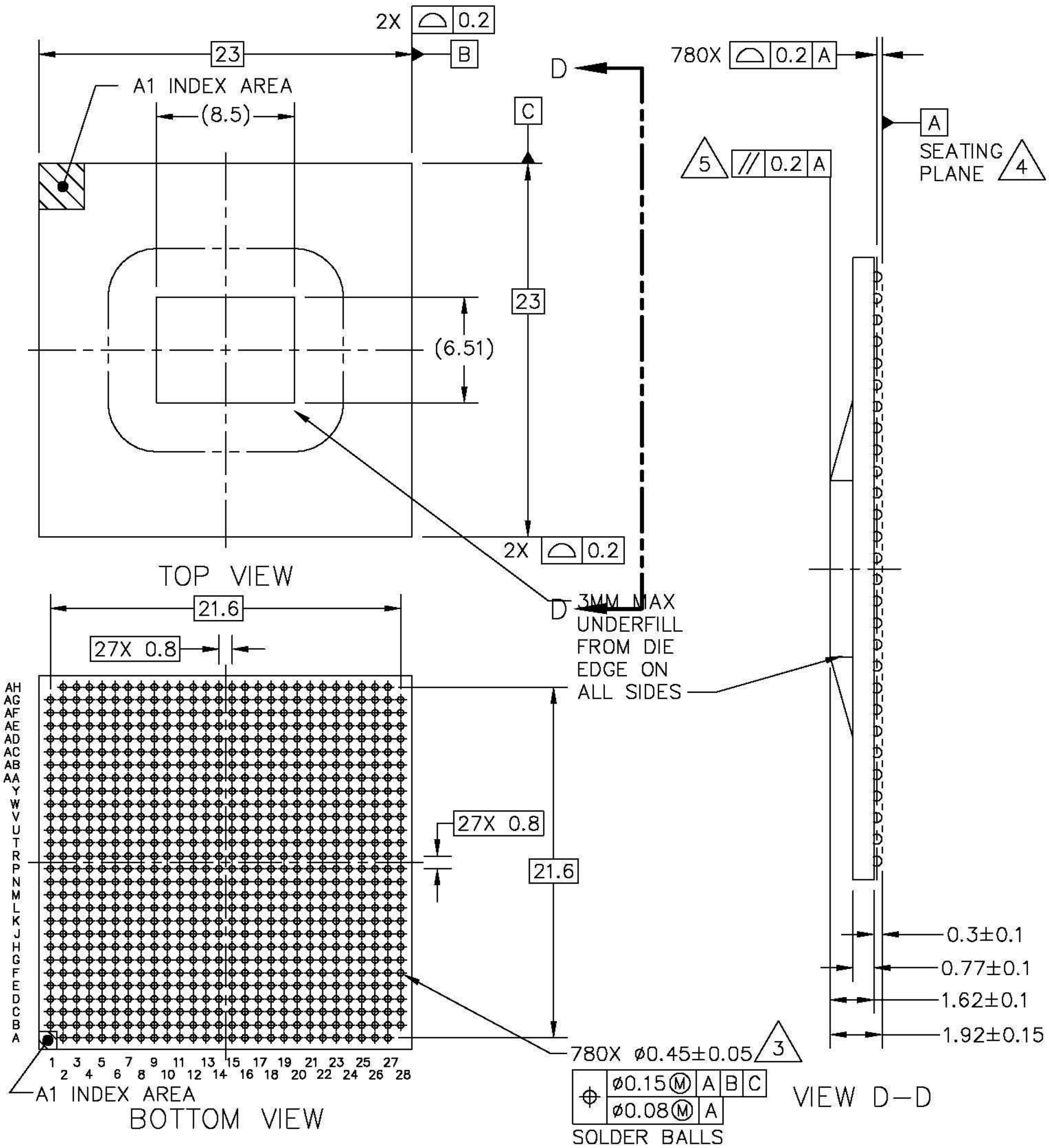


Figure 104. Mechanical dimensions of the FC-PBGA 23x23 mm (780 balls)

Notes:

1. ALL DIMENSIONS IN MILLIMETRES.

2. DIMESNSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALEL TO DATUM A
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

7 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of six fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 5.

NOTE

Users not implementing the QorIQ platform's Trust Architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

This table provides the NXP QorIQ platform part numbering nomenclature.

8.1 Part numbering nomenclature

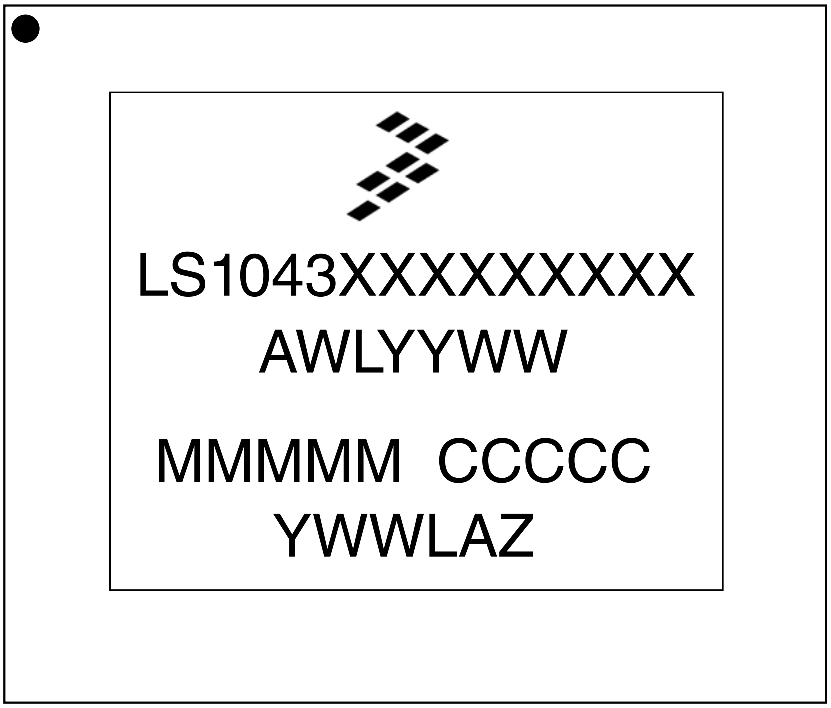
This table provides the NXP QorIQ platform part numbering nomenclature.

Table 167. Part numbering nomenclature

p	ls	n	nn	n	x	t	e	n	c	d	l	r
Qual status	Generation	Performance Level	Number of cores	Unique ID	Core Type	Temperature Range	Encryption	Package Type	CPU Speed	DDR Data Rate	Low Power	Die Revision
P="Sampling" Blank="Qual"	LS	1	04 = Four Cores 02 = Two Cores	3	A = ARM	S = Standard temp X = Extended temp	E = SEC N = SEC not present	7 = LCFC 621 balls 8 = LCFC 780 balls	K = 1000 MHz M = 1200 MHz P = 1400 MHz Q = 1600 MHz	N = 1300 MT/s Q = 1600 MT/s	L = Low Power	A = Rev 1.0 B = Rev 1.1
1. For the LS1043A family of devices, parts marked with "L" (before Die-Revision) require 0.9V operating voltage. All others require 1.0 V. 2. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com												

8.2 Part marking

Parts are marked as in the example shown in this figure.



Legend:
LS1043XXXXXXXXX is the orderable part number
AWLYYWW is the test traceability code
MMMMM is the mask number
CCCCC is the country code
YWWLAZ is the assembly traceability code

Figure 105. Part marking for FC-PBGA chip LS1043A

9 Revision history

This table summarizes revisions to this document.

Table 168. Revision history

Revision	Date	Description

2	01/2017	• Pinlist changes
		  • Updated Signal description for JTAG_BSR_VSEL and TBSCAN_EN_B, added notes
		  • Updated note 3 with minor changes for DDR
		  • Updated USB_VBUS voltage to 5.25 V
		  • Updated USB_ID voltage reference, added note in 23x23 package
		  • Updated voltage reference for GPIO1_31/IRQ11 in 23x23 package

Table continues on the next page...

Table 168. Revision history (continued)

Revision	Date	Description
		• Removed reference for Ganged sense-line implementation from note 4 in Absolute maximum ratings • Updated number of secure boot programming cycles to six in Power sequencing and Security fuse processor • Updated DDR data rate unit to MT/s in Part numbering nomenclature • Removed SDHC_CD constraints in eSDHC AC timing specifications • Updated table Low power mode saving estimation • Updated Die revision in Part numbering nomenclature

1	06/2016	• Pinlist changes
		  ◦ Updated TA_BB_RTC as "Reserved"
		  ◦ Updated CKSTP_OUT_B as "Reserved"
		  ◦ Removed reference to USB_REFCLK/USB_REFCLK_ALT
		  ◦ Updated description of TA_BB_VDD as "Battery Backed Security Monitor Power"
		  ◦ Removed cfg_soc_use
		  ◦ Updated headings for Pinout list for more clarity
		  ◦ Updated pinlist sub-section for QSPI, removed "Data Strobe"
		  ◦ Updated package in number for QSPI_A_DATA1 in sub-section for QSPI
		  ◦ Updated note 23 to personality selection between LS1023A/LS1043A
		  ◦ Added note for SD_GND
		• Added Core power dissipation @ 0.9V for 4 cores and 2 cores personalities; updated core and platform activity factors in Power characteristics
		• Updated low power mode nomenclature (PW20->PH20); deleted PH20 and LPM20 power numbers; Added Low power saving estimate table for 0.9V in Low power mode saving estimation. Removed PCL10. Corrected typo LMP20->LPM20
		• Removed AC specification for TA_BB_RTC; updated RTC spec in Real-time clock timing (RTC)
		• Added reference to USB 3.0 clock specification in SYSCLK AC timing specifications and Differential system clock AC timing specifications
		• Updated USB 3.0 clock specification in USB 3.0 AC timing specifications
		• Added note for "Trust Architecture Security Monitor battery backed features" and deleted SYSCLK/DIFF_SYSCLK in note section of Power sequencing
		• Added note 2 in Differential system clock DC timing characteristics to clarify differential swing.
		• Removed note depicting restriction between PLL cluster and platform in Core complex PLL select
		• Corrected typo in Guidelines for high-speed interface termination
		• Added 0.9 V support; updated note 3 in Recommended operating conditions
		• Updated IFC-NVDDR specification for 0.9V in IFC-NAND NVDDR AC Timing Specification
		• Added 10 MHz MDC/MDIO specification in EMI2 AC timing specifications
		• Added 23x23 780 ball package details; ball layout diagrams, pinout list Pinout list and mechanical drawing Mechanical dimensions of the FC-PBGA
		• Corrected typo in PCI Express AC physical layer transmitter specifications
		• Removed power supply filters to avoid duplication with Design-Checklist.
		• Updated PORESET_B text in RESET initialization
		• Updated IO interface power numbers in I/O power dissipation
		• Corrected recommendations for Temperature diodes terminals in Connection recommendations.
		• Replaced mechanical dimension with updated format; No change in dimensions in in Mechanical dimensions of the FC-PBGA
		• Added notes in Part numbering nomenclature.
		• Added foot note refering to orderable part list on NXP website in the following table
		  ◦ DDR clock ranges
		  ◦ Platform to SYSCLK PLL ratio
		  ◦ DDR controller PLL ratios
		  ◦ Core cluster to SYSCLK PLL ratio
		  ◦ SYSCLK and core cluster frequency options

Table continues on the next page...

Table 168. Revision history (continued)

Revision	Date	Description
		• SYSCLK and platform frequency options • DDRCLK and DDR data rate frequency options • Clock ranges
0	02/2016	Initial release

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number LS1043A
Revision 2, 01/2017