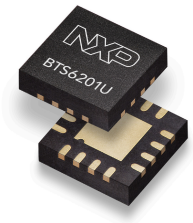


BTS6201U

Wideband high linearity pre-driver amplifier

Rev. 5 — 5 September 2022 Product data sheet

1 General description

The BTS6201U is a wideband, high linearity, pre-driver amplifier for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The amplifier is designed to operate between 2.3 GHz and 4.2 GHz. It is housed in a 3 mm x 3 mm x 0.85 mm 16-terminal HVQFN package. The amplifier is ESD protected on all terminals.

2 Features and benefits

- High saturated output power $P_{o(sat)}$ = 28 dBm
- High power-gain G_p = 30.5 dB
- High linearity performance ACLR = -46 dBc
- Unconditionally stable
- Programmable bias current (via external resistor)
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 78 mA
- Small 16-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1

3 Applications

- Wireless infrastructure 5G NR mMIMO
- High linearity pre-driver
- TDD systems

4 Quick reference data

Table 1. Quick reference data

f = 3.5 GHz; V_{CC} = 5 V; T_{case} = 25 °C; input and output 50 Ω; R_{SET} = 1.2 kΩ; unless otherwise specified. Values under Min/Max in boldface font are guaranteed by test; Values in lightface font are based on simulation or characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	95	115	mA
		ON state, quiescent	-	78	**90**	mA
		OFF state	-	1	**1.5**	mA
G_p	power gain	ON state	29.5	30.5	31.5	dB
		OFF state	-	-48	-	dB
$P_{o(sat)}$	saturated output power		27.5	28	-	dBm
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-46	-44.5	dBc

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
BTS6201U	BTS6201UJ	HVQFN16	3 mm x 3 mm x 0.85 mm, 16 terminals no leads	SOT758-1

6 Marking

Table 3. Marking

Type number	Marking code
BTS6201U	21U

7 Functional diagram

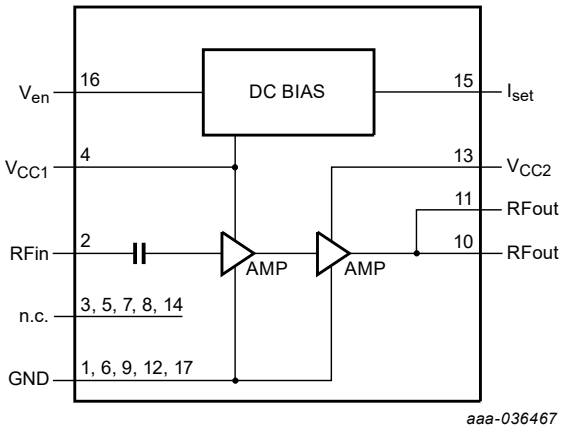


Figure 1. Functional diagram

8 Pinning information

8.1 Pinning

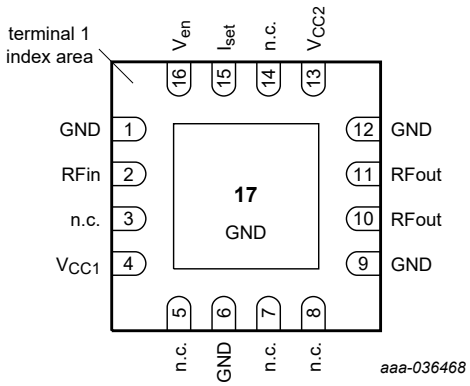


Figure 2. Pin configuration

8.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
GND	1, 6, 9, 12 and 17	PCB ground
RFin	2	RF input
n.c. [1]	3	PCB ground, or connect to RFin
n.c. [1]	5, 7, 8 and 14	PCB ground
RFout	10 and 11	RF output; connect both to the same track
V_{CC1}	4	supply voltage
V_{CC2}	13	supply voltage
I_{set}	15	current set; connect to external resistor
V_{en}	16	voltage enable; LOW = OFF state; HIGH = ON state

[1] n.c. means that pin is not connected inside package

9 Functional description

Table 5. Shutdown control

V_{en}	voltage applied at pin V_{en} [1]	State	Condition
LOW	$0 < V(V_{en}) < V_{IL(max)}$	OFF	bias active, amplifier not active
HIGH	$V_{IH(min)} < V(V_{en}) < V_{I(max)}$	ON	bias active, amplifier active

[1] V_{en} can only be made HIGH, after supply voltage has been applied to pin V_{CC1}

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	6	V
V_{en}	enable voltage		-0.3	4	V
$V_{I(set)}$	current set voltage		-0.3	4	V
$P_{i(RF)CW}$	continuous waveform RF input power	ON state, OFF state	-	10	dBm
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	175	°C
P	power dissipation	T_{case} ≤ 105 °C [1]	-	900	mW
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	+/-2	kV
		Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	-	+/-1	kV

[1] Case is ground solder pad.

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	4.75	5	5.25	V
V_{IL}	LOW-level input voltage		0	-	0.6	V
V_{IH}	HIGH-level input voltage		1.2	-	3.6	V
$V_{I(max)}$	maximum input voltage		-	-	3.6	V
Z_0	characteristic impedance		-	50	-	Ω
T_{case}	case temperature		-40	-	115	°C

[1] V_{CC} must be applied to pin V_{CC1} before, or at the same time as applying V_{CC} to pin V_{CC2}

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	junction to case thermal resistance	[1] [2]	50	K/W

[1] Case is ground solder pad.
[2] Thermal resistance determined with device mounted, and device bottom case kept at constant temperature.

13 Characteristics

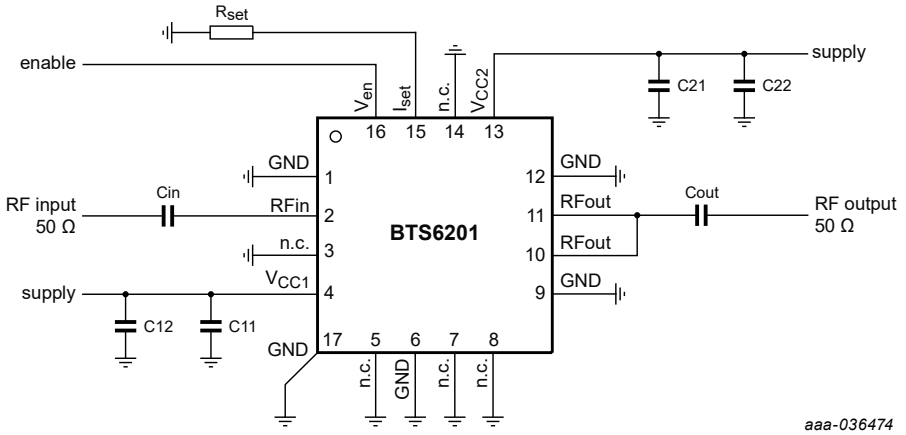
Table 9. Characteristics

f = 3.5 GHz; V_{CC} = 5 V; T_{case} = 25 °C; input and output 50 Ω; R_{bias} = 1.2 kΩ; unless otherwise specified. Values under Min/Max in boldface font are guaranteed by test; Values in lightface font are based on simulation or characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	95	115	mA
		ON state, quiescent	-	78	**90**	mA
		OFF state	-	1	**1.5**	mA
G_p	power gain	ON state	29.5	30.5	31.5	dB
		OFF state	-	-48	-	dB
G_{flat}	gain flatness	2.3 GHz to 2.7 GHz	-	0.7	-	dB
		3.3 GHz to 3.8 GHz	-	1	-	dB
$t_{d(grp)}$	group delay time	2.3 GHz to 2.7 GHz	-	0.3	-	ns
		3.3 GHz to 3.8 GHz	-	0.3	-	ns
$P_{o(sat)}$	saturated output power	3 dB gain compression [1]	27.5	28	-	dBm
$P_{L(1dB)}$	output power at1 dB gain compression		26.5	27	-	dBm
$IP3_o$	output third-order intercept point	2-tone; tone spacing = 100 MHz; P_o = 15 dBm	34	35	-	dBm
RL_i	input return loss		-	17	-	dB
RL_o	output return loss		-	12	-	dB
ISL_r	reverse isolation		-	45	-	dB
NF	noise figure	[1]	-	3.4	3.5	dB
$t_{s(pon)}$	power-on settling time	V_{en} from LOW to HIGH to output power reaching 90 % of final power	-	0.18	-	µs
$t_{s(poff)}$	power-off settling time	V_{en} from HIGH to LOW to output power reaching 10 % below initial power	-	0.1	-	µs
K	Rollett stability factor	1 MHz to 15 GHz	2	-	-	
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-46	-44.5	dBc

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded.

14 Application information



See Table 10 for a list of components.

Figure 3. Schematic of application board

Table 10. List of components

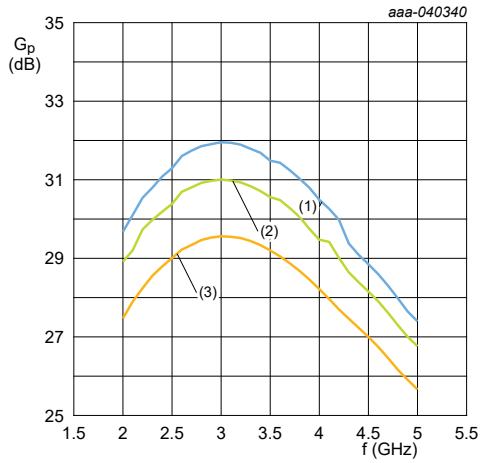
See figure 16 for schematics.

Component	Description	Value	Remarks
C_{in}	capacitor	18 pF	in a 50 Ω PCB track
C_{out}	capacitor	18 pF	in a 50 Ω PCB track
C11, and C21	capacitor	10 nF	
C12, and C22 [1]	capacitor	1 µF	
RSET	resistor	1.2 KΩ	default

[1] placement of C12, and C22 is optional

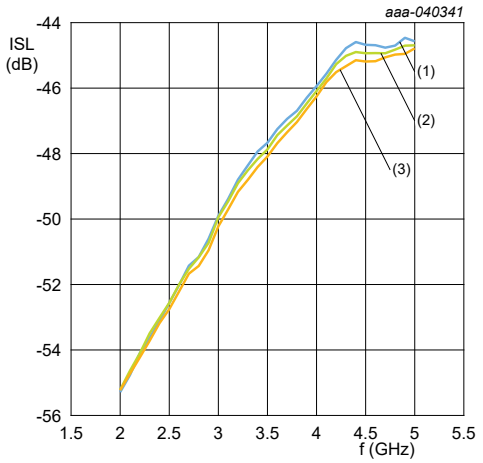
15 Graphics

Table 11.



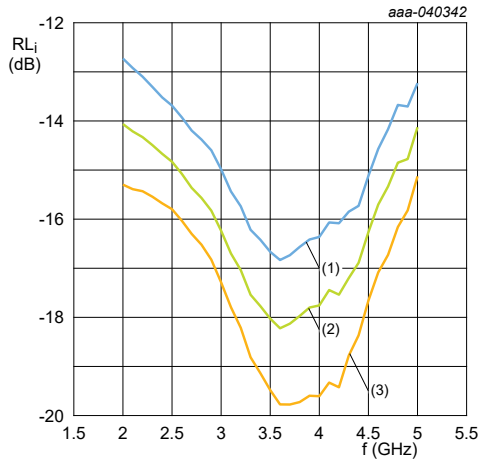
(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

Figure 4. G_p versus frequency over temperature



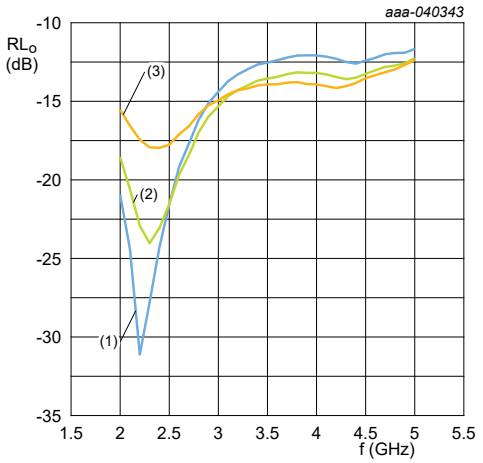
(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

Figure 5. ISL_r S12 versus frequency over temperature



(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

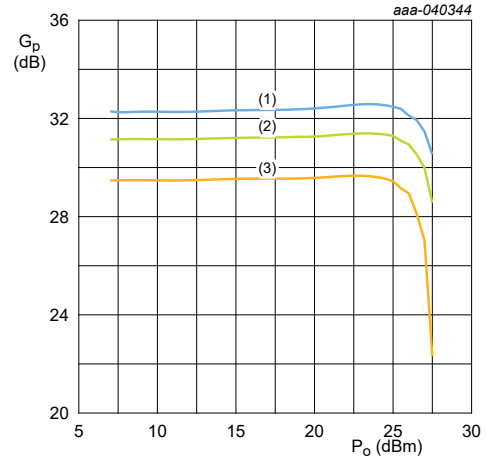
Figure 6. RL_i S11 versus frequency over temperature



(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

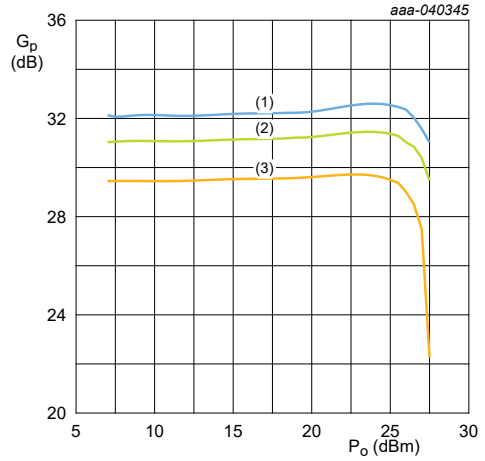
Figure 7. RL_o S22 versus frequency over temperature

Table 11. *...continued*



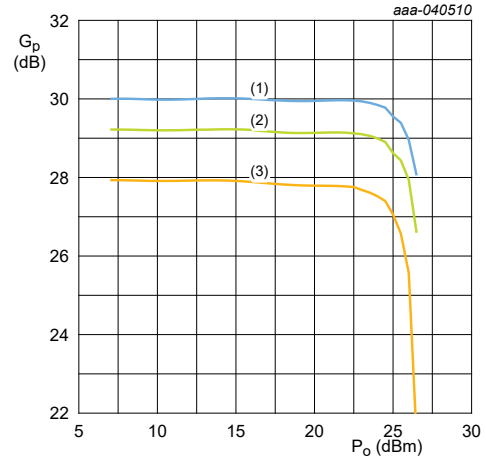
(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

Figure 8. G_p versus P_o at 2.6 GHz over temperature



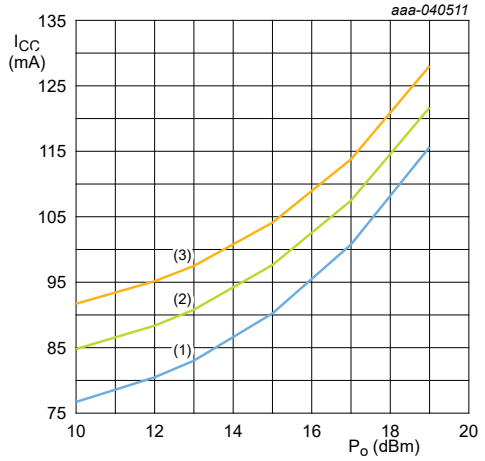
(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

Figure 9. G_p versus P_o at 3.5 GHz over temperature



(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

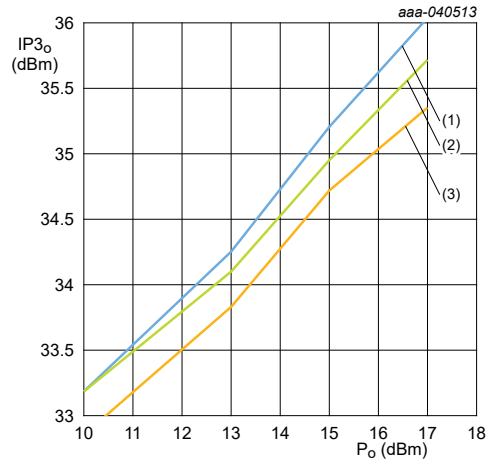
Figure 10. G_p versus P_o at 4.2 GHz over temperature



(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

Figure 11. I_{CC} versus P_o at 3.5 GHz over temperature

Table 11. *...continued*



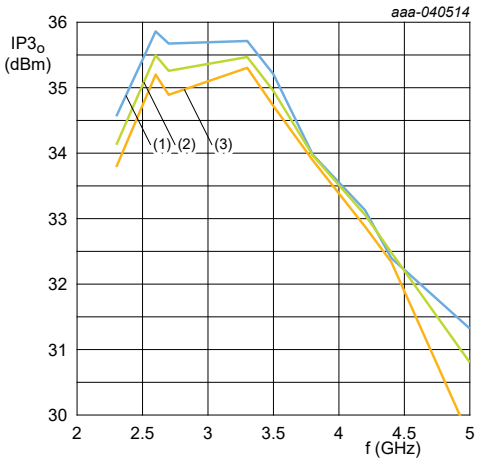
tone spacing = 100 MHz; V_{CC} = 5 V

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 105 °C

Figure 12. $IP3_o$ versus P_0 at 3.5 GHz over temperature



tone spacing = 100 MHz; P_o = 15 dBm;

V_{CC} = 5 V

(1) T_{case} = -40 °C

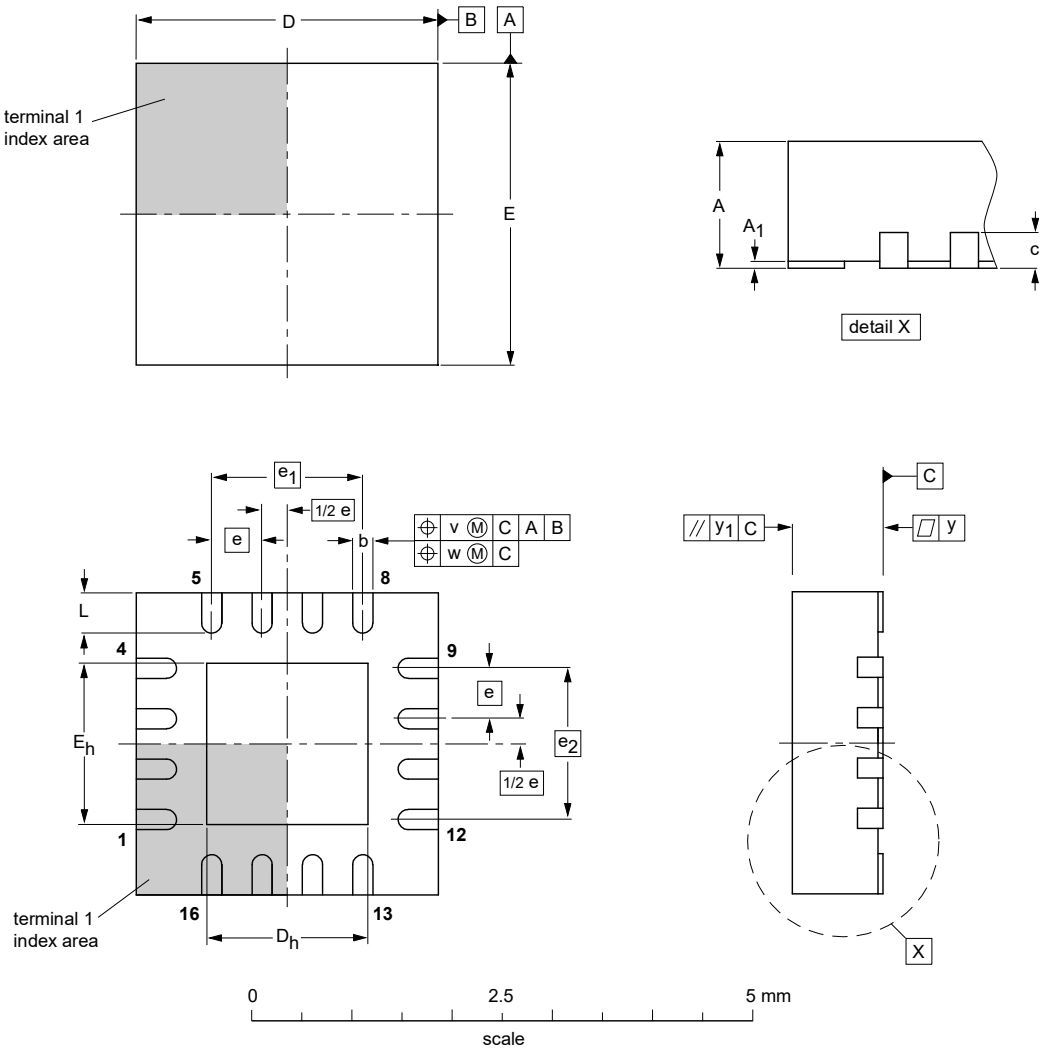
(2) T_{case} = 25 °C

(3) T_{case} = 105 °C

Figure 13. $IP3_o$ versus frequency over temperature

16 Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

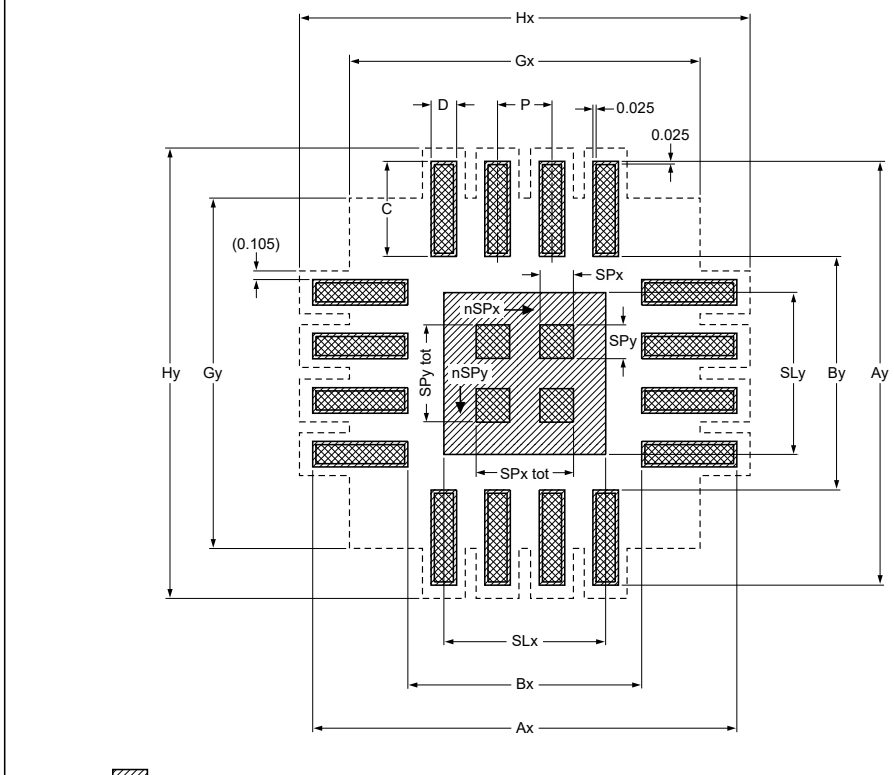
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Figure 14. Package outline SOT758-1 (HVQFN16)

16.1 Footprint and solder information

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

Figure 15. Footprint information

17 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 12. Abbreviations

Acronym	Description
5G NR	5th generation new radio
ACLR	adjacent channel leakage ratio
CP-OFDM	cyclic prefix orthogonal frequency division multiplexing
ESD	electrostatic discharge
mMIMO	massive multiple-input multiple-output
PA	power amplifier
RF	radio frequency
TDD	time-division duplexing

19 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BTS6201UV.5	20220905	Product data sheet	202209003I	BTS6201UV.4
modification	• changed the maximum value of T_J in the Limiting values table to 175 °C • changed the maximum value of T_{case} in the Recommended operating conditions table to 115 °C			
BTS6201U V.4	20210203	Product data sheet	-	BTS6201UV.3
modification	• changed security status to Public			
BTS6201U V.3	20210129	Product data sheet	-	BTS6201UV.2.1
modification	• changed Min, Typ, and Max values on some parameters • added remark: Values under Min/Max in boldface font are guaranteed by test; Values in lightface font are based on simulation or characterization. to the description at the tables on Quick reference, and characteristics • removed V_{RFin}, and V_{RFout} from Limiting values table • added graphics • changed remark, and footnote for C12, and C22 in list of components table • changed status to Product data sheet			
BTS6201UV.2.1	20201012	Preliminary data sheet	-	BTS6201UV.2
modification	• added marking			
BTS6201UV.2	20201002	Preliminary data sheet	-	BTS6201UV.1.1
modification	• changed status to Preliminary • added footprint and solder information			
BTS6201UV.1.1	20200716	Objective data sheet	-	BTS6201UV.1
modification	• updated some typical values to the latest validation results			
BTS6201UV.1	20200401	Objective data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

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