

# SCM-i.MX 6Dual/6Quad Datasheet for Industrial Products

## 1. Introduction

NXP Single Chip System Modules (SCMs) are a suite of highly integrated products in an ultra-small form factor. The first member of this portfolio, the NXP SCM-i.MX 6Dual/6Quad, drastically reduces time to market by providing a solution that minimizes design time. We've integrated and validated dual- and quad-core performance, the power management system, flash memory, and over a hundred passive system components all in the size of a dime. The SCM-i.MX 6Dual/6Quad is enabled with the standard i.MX 6Dual/6Quad multimedia, connectivity and security features including High Assurance Boot, cryptographic cipher engines, random number generator, and tamper detection. It is a scalable solution intended for use in a wide variety of consumer and industrial applications.

The SCM-i.MX 6Dual/6Quad speeds and eases development time by addressing technology challenges such as design of DDR and power management. Our single chip module i.MX 6Dual/6Quad consists of the i.MX 6Dual/6Quad applications processor, PF0100 (PMIC) for power management, 16 MB SPI NOR, over a hundred discrete components, and is enabled for LPDDR2 via PoP assembly.

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## 1.1. Ordering information

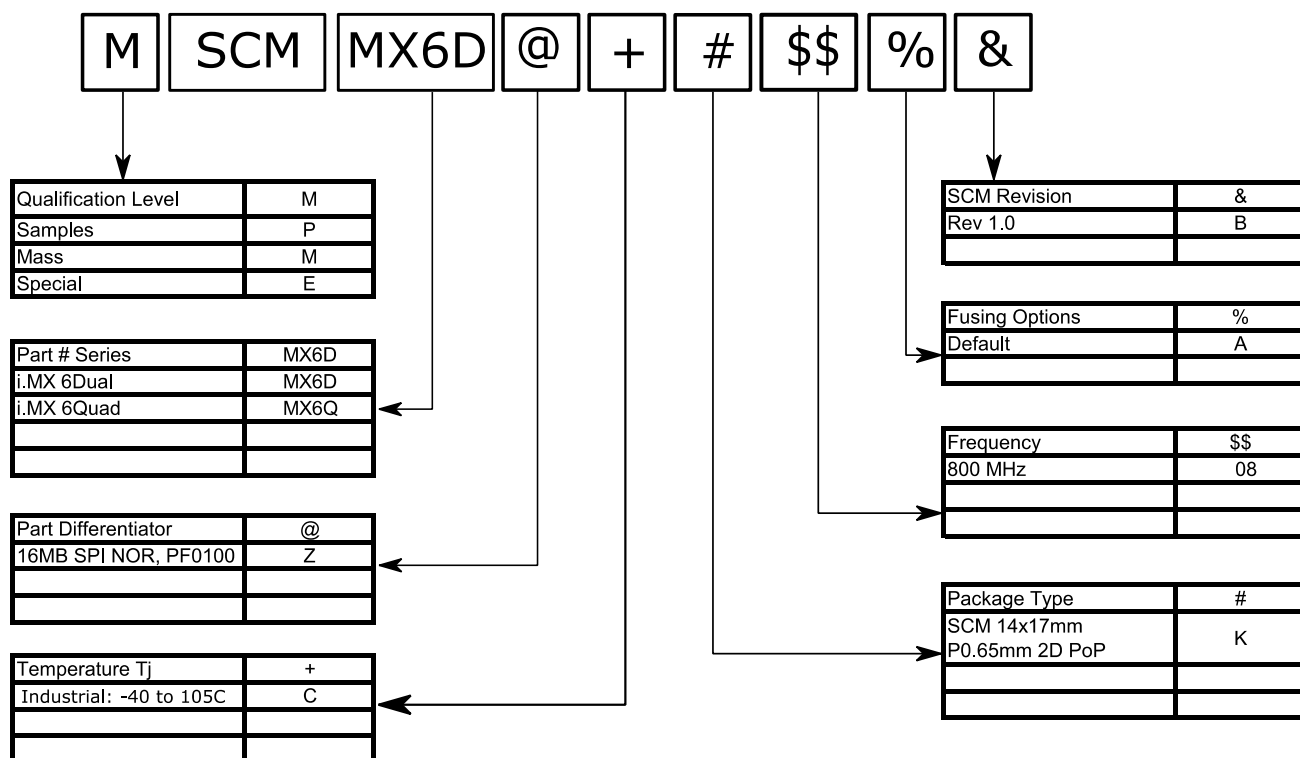


Figure 1. Part Number Nomenclature

The table below shows examples of orderable part numbers.

Table 1. Part Numbers

| Part Number     | CPU        | Part Differentiator  | Speed Grade | Temperature Grade       | Package                       |
|-----------------|------------|----------------------|-------------|-------------------------|-------------------------------|
| MSCMMX6DZCK08AB | i.MX 6Dual | 16MB SPI NOR, PF0100 | 800 MHz     | Industrial: -40 to 105C | SCM 14x17mm<br>P0.65mm 2D PoP |
| MSCMMX6QZCK08AB | i.MX 6Quad | 16MB SPI NOR, PF0100 | 800 MHz     | Industrial: -40 to 105C | SCM 14x17mm<br>P0.65mm 2D PoP |

## 1.2. Features

### 1.2.1. i.MX 6Dual/6Quad Features

The i.MX 6Dual/6Quad processors are based on ARM® Cortex®-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per [Table 5](#)
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
- Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 32-bit LPDDR2, supporting DDR interleaving mode, or fixed 2x32.
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bits.

- 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
- 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps
- Displays—Total of five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) PHY
- Expansion PCI Express port (PCIe) v2.0 one lane:
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I2S mode

- ESAI is capable of supporting audio sample frequencies up to 260kHz in I2S mode with 7.1 multi-channel outputs
- Five UARTs, up to 4.0 Mbps each:
  - Providing RS232 interface
  - Supporting 9-bit RS485 multidrop mode
  - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
- Five eCSPI (Enhanced CSPI)
- Three I2C, supporting 400 kbps
- Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000<sup>1</sup> Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

<sup>1</sup> The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document [IMX6DQCE](#).

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPU)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlit)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSES and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

### 1.2.2. PF0100Z Features

- Input voltage range to PMIC: 2.8 - 4.5 V
- Buck regulators
  - Four to six channel configurable
    - SW1A/B/C, 4.5 A (single); 0.3 to 1.875 V
    - SW1A/B, 2.5 A (single/dual); SW1C 2.0 A (independent); 0.3 to 1.875 V
    - SW2, 2.0 A; 0.4 to 3.3 V
    - SW3A/B, 2.5 A (single/dual); 0.4 to 3.3 V
    - SW3A, 1.25 A (independent); SW3B, 1.25 A (independent); 0.4 to 3.3 V
    - SW4, 1.0 A; 0.4 to 3.3 V
    - SW4, VTT mode provide DDR termination at 50% of SW3A
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS

- Programmable output voltage
- Programmable current limit
- Programmable soft start
- Programmable PWM switching frequency
- Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and Auto
  - OCP fault interrupt
- LDOs
  - Six user programmable LDO
    - VGEN1, 0.80 to 1.55 V, 100 mA
    - VGEN2, 0.80 to 1.55 V, 250 mA
    - VGEN3, 1.8 to 3.3 V, 100 mA
    - VGEN4, 1.8 to 3.3 V, 350 mA
    - VGEN5, 1.8 to 3.3 V, 100 mA

#### **NOTE**

VGEN5 power characteristics are modified from what is displayed in Table 106 of the MMPF0100 datasheet. SCM-specific tolerances are  $\pm 5\%$ , rather than  $\pm 3\%$  as presented in the table.

- VGEN6, 1.8 to 3.3 V, 200 mA
- Soft start
- LDO/Switch supply
  - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 400uA
- DDR memory reference voltage
  - VREFDDR, 0.6 to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP(One time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I2C interface
- User programmable Standby, Sleep, and Off modes

## 1.3. References

This document is intended to be a companion to the data sheets of the following integrated parts:

- a) NXP i.MX 6Dual/6Quad (Document Number: [IMX6DQIEC](#))
- b) NXP MMPF0100 (Document Number: [MMPF0100Z](#))
- c) SPI NOR ([N25Q128A13](#))

## 2. Architectural Overview

The following subsection provides an architectural overview of the SCM-i.MX 6Dual/6Quad.

### 2.1. Block Diagram

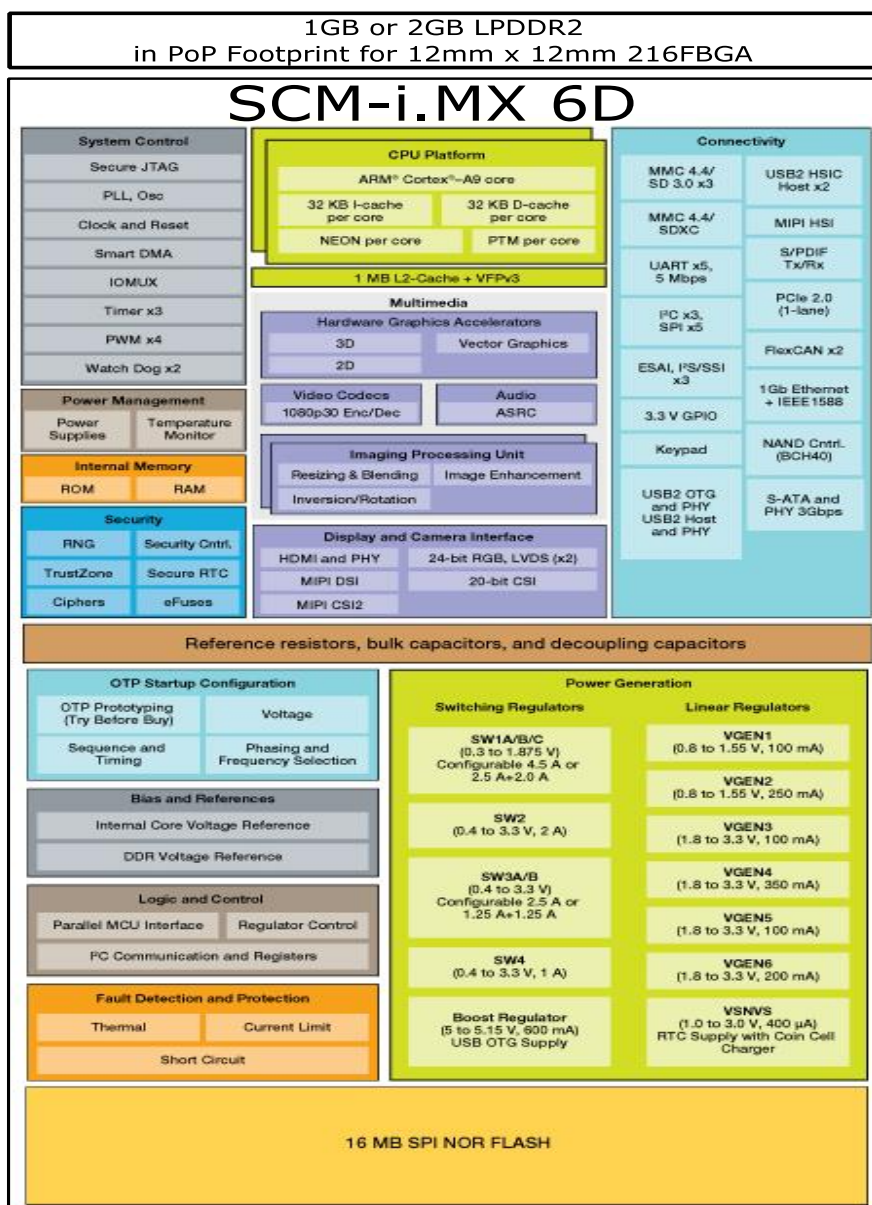


Figure 2. SCM-i.MX 6Dual/6Quad Block Diagram

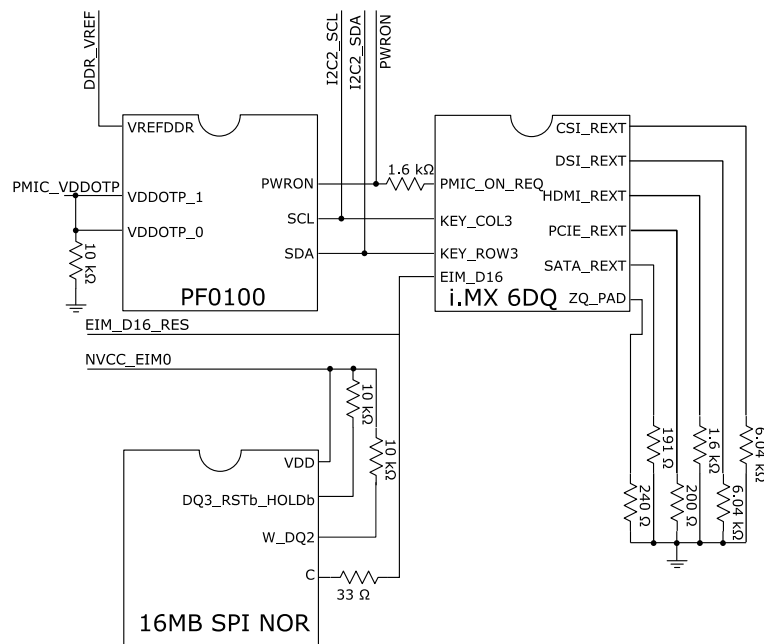
## 3. Modules List

**Table 2. Modules List**

| Block Name           | Description/Notes                                                                                                                                        |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| i.MX 6Dual/6Quad     | NXP i.MX 6Dual/6Quad Applications Processor. Fully functional as a normal i.MX 6Dual/6Quad except the MLB bus is disabled and not pinned out.            |
| MMPF0100             | Power management IC requires only a single supply and can provide power and voltage references to entire SCM. Refer to section 4 for electrical details. |
| SPI NOR              | 16 megabytes of SPI NOR which is fully available for user programming.                                                                                   |
| LPDDR2 PoP Interface | Interface to support LPDDR2 in PoP configuration using a 12mm x 12mm FBGA216 footprint.                                                                  |
| Discrete Components  | 109 passives for decoupling capacitors and reference resistors.                                                                                          |

### 3.1. Special Signal Considerations

The figure below shows critical internal connections, pull-ups and pulldowns.



**Figure 3. SCM-i.MX 6Dual/6Quad Critical Internal Connections**

#### Note

DDR\_VREF is connected internally to the LPDDR2 memory through one of the PoP landing pads.

## 4. Electrical Characteristics

### 4.1. Chip-Level Conditions

#### 4.1.1. Absolute Max Ratings

#### CAUTION

Stresses beyond those listed under Table 3, 4 and 5 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied."

**Table 3. Absolute Max Ratings**

| Parameter Description            | Symbol    | Min  | Max | Unit |
|----------------------------------|-----------|------|-----|------|
| PMIC System Supply Voltage Range | PMIC_VIN  | -0.3 | 4.8 | V    |
| Temperature range (storage)      | T_storage | -40  | 150 | C    |

#### 4.1.2. Thermal Resistance

Table 4 provides the FO-WLP thermal resistance data.

**Table 4. FO-WLP Thermal Resistance Data**

| Parameter Description                                       | Test Condition                                           | Symbol            | Value | Unit |
|-------------------------------------------------------------|----------------------------------------------------------|-------------------|-------|------|
| Junction to Ambient <sup>1,6</sup>                          | Single-layer board (1s); natural convection <sup>2</sup> | R <sub>θJA</sub>  | 36.5  | °C/W |
|                                                             | Four-layer board (2s2p); natural convection <sup>2</sup> | R <sub>θJA</sub>  | 19.9  | °C/W |
| Junction to Ambient <sup>1,6</sup>                          | Single-layer board (1s); air flow 200ft/min <sup>3</sup> | R <sub>θJMA</sub> | 27.7  | °C/W |
|                                                             | Four-layer board (2s2p); air flow 200ft/min <sup>3</sup> | R <sub>θJMA</sub> | 16.1  | °C/W |
| Junction to Board <sup>1,4,6</sup>                          | -                                                        | R <sub>θJB</sub>  | 6.6   | °C/W |
| Junction to top characterization parameter <sup>1,5,6</sup> | -                                                        | Ψ <sub>JT</sub>   | 2.9   | °C/W |

<sup>1</sup> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

<sup>6</sup> Values reported are modeled and based upon a summation of power dissipation of multiple die within the package. Junction temperatures will vary between die according to power ratios and use case.

### 4.1.3. Operating Ranges

Table 5. Operating Ranges

| Parameter Description                         | Symbol        | Min   | Max | Unit |
|-----------------------------------------------|---------------|-------|-----|------|
| PMIC System Supply Voltage Range              | PMIC_VIN      | 3.6   | 4.5 | V    |
| SPI NOR Flash Supply Voltage Range            | NVCC_EIM0_NOR | 2.775 | 3.6 | V    |
| Junction Temperature<br>(standard industrial) | Tj            | -40   | 105 | C    |

## 5. Power Supplies Requirements and Restrictions

SCM-specific power-up sequence requirements are shown in SCM-IMX6DQHUG.

### 5.1. Power-Up Sequences

Must follow the i.MX 6Dual/6Quad industrial datasheet (Document Number: [IMX6DQIEC](#)) recommendations for power up. The internal PMIC simplifies power sequence design.

### 5.2. Power-Down Sequences

Must follow the i.MX 6Dual/6Quad industrial datasheet (Document Number: [IMX6DQIEC](#)) recommendations for power down.

### 5.3. Power Supplies Usage

Must follow the i.MX 6Dual/6Quad industrial datasheet (Document Number: [IMX6DQIEC](#)) recommendations for power supply usage.

### 5.4. Power Supplies Restrictions

DDR\_1V2 and DDR\_1V2\_SW3AFB (switcher 3 feedback pin) are internally connected for dedicated LPDDR2 usage with SW3. SW3 cannot be used to supply anything else but the LPDDR2.

### 5.5. Boot Configuration

#### 5.5.1. OTP PMIC

Table 6. OTP Fuse Map

| Registers    | Default Configuration | Pre-programmed OTP Configuration | Program code (hex) | Intended Use |
|--------------|-----------------------|----------------------------------|--------------------|--------------|
| SW1AB_VOLT   | 1.375V                | 1.375V                           | 2B                 | VDDSOC       |
| SW1AB_SEQ    | 1                     | 2                                | 02                 |              |
| SW1AB CONFIG | Single Phase, 2.0 MHz | Single Phase, 2.0 MHz            | 05                 |              |

| Registers                    | Default Configuration        | Pre-programmed OTP Configuration | Program code (hex) | Intended Use |
|------------------------------|------------------------------|----------------------------------|--------------------|--------------|
| SW1C_VOLT                    | 1.375                        | 1.375V                           | 00                 | VDDARM       |
| SW1C_SEQ                     | 1                            | 2                                | 02                 |              |
| SW1C CONFIG                  | Independent, 2.0 MHz         | Independent, 2.0 MHz             | 00                 |              |
| SW2_VOLT                     | 3.0V                         | 3.15V                            | 6F                 | VDDHIGH_IN   |
| SW2_SEQ                      | 2                            | 1                                | 01                 |              |
| SW2 CONFIG                   | Single Phase, 2.0 MHz        | Single Phase, 2.0 MHz            | 01                 |              |
| SW3A_VOLT                    | 1.5V                         | 1.2V                             | 20                 | DDR 1.2V     |
| SW3A_SEQ                     | 3                            | 4                                | 04                 |              |
| SW3A CONFIG                  | Single Phase, 2.0 MHz        | Single Phase, 2.0 MHz            | 05                 |              |
| SW3B_VOLT                    | 1.5V                         | 1.2V                             | 20                 | DDR 1.2V     |
| SW3B_SEQ                     | 3                            | 4                                | 04                 |              |
| SW3B CONFIG                  | Single Phase, 2.0 MHz        | Single Phase, 2.0 MHz            | 01                 |              |
| SW4_VOLT                     | 1.8V                         | 1.8V                             | 54                 | DDR 1.8V     |
| SW4_SEQ                      | 3                            | 4                                | 04                 |              |
| SW4_CONFIG                   | No VTT, 2.0MHz               | No VTT, 2.0 MHz                  | 01                 |              |
| SWBST_VOLT                   | -                            | -                                | 00                 | Customer     |
| SWBST_SEQ                    | -                            | 4                                | 04                 |              |
| VSNVS_VOLT                   | 3.0V                         | 3.0V                             | 06                 | VDD_SNVS_IN  |
| VREFDDR_SEQ                  | 3                            | 4                                | 04                 |              |
| VGEN1_VOLT                   | -                            | -                                | 00                 | Customer     |
| VGEN1_SEQ                    | -                            | -                                | 00                 |              |
| VGEN2_VOLT                   | 1.5V                         | -                                | 00                 | Customer     |
| VGEN2_SEQ                    | 2                            | -                                | 00                 |              |
| VGEN3_VOLT                   | -                            | -                                | 00                 | Customer     |
| VGEN3_SEQ                    | -                            | -                                | 00                 |              |
| VGEN4_VOLT                   | 1.8V                         | -                                | 00                 | Customer     |
| VGEN4_SEQ                    | 3                            | -                                | 00                 |              |
| VGEN5_VOLT                   | 2.5V                         | -                                | 00                 | Customer     |
| VGEN5_SEQ                    | 3                            | -                                | 00                 |              |
| VGEN6_VOLT                   | 2.8V                         | -                                | 00                 | Customer     |
| VGEN6_SEQ                    | 3                            | -                                | 00                 |              |
| PU CONFIG1,<br>SEQ_CLK_SPEED | 1.0ms                        | 1.0ms                            | 01                 |              |
| PU CONFIG2,<br>SWDVS_CLK     | 6.25 mV/us                   | 12.5mV/us                        | 00                 |              |
| PU CONFIG3,<br>PWRON         | Level sensitive              | Level sensitive                  | 00                 |              |
| PG EN                        | RESETBMCU in<br>Default Mode | 00                               |                    |              |

### Note

1. Refer to application notes AN4714 (Features of Voltage Regulators in the MMPF0100) and AN4536 (MMPF0100 OTP Programming Instructions) for further usage instructions.
2. The OTP registers for regulators which default to (OFF) are free to be programmed according to customer needs.
3. The OTP Lock bit is not programmed from factory.
4. NXP not responsible for device issues caused by customer fuse programming.

## 6. Boot Mode Configuration

### 6.1. Boot Mode Configuration Pins

Refer to the i.MX 6Dual/6Quad industrial datasheet (Document Number: [IMX6DQIEC](#)).

### 6.2. Boot Devices Interfaces Allocation

Not limited to booting from internal SPI NOR.

Refer to the i.MX 6Dual/6Quad industrial datasheet (Document Number: [IMX6DQIEC](#)).

## 7. Package Information

### 7.1. Signal List

Table 7. Signal List

| Ball Name  | Ball | Power Group  | Comments |
|------------|------|--------------|----------|
| BOOT_MODE0 | U11  | VDD_SNVS_IN  |          |
| BOOT_MODE1 | V12  | VDD_SNVS_IN  |          |
| CLK1_N     | U18  | VDD_HIGH_CAP |          |
| CLK1_P     | U17  | VDD_HIGH_CAP |          |
| CLK2_N     | W19  | VDD_HIGH_CAP |          |
| CLK2_P     | W20  | VDD_HIGH_CAP |          |
| CSI_CLK0M  | N20  | NVCC_MIPI    |          |
| CSI_CLK0P  | N19  | NVCC_MIPI    |          |
| CSI_D0M    | R20  | NVCC_MIPI    |          |
| CSI_D0P    | R19  | NVCC_MIPI    |          |
| CSI_D1M    | P19  | NVCC_MIPI    |          |
| CSI_D1P    | P20  | NVCC_MIPI    |          |
| CSI_D2M    | M19  | NVCC_MIPI    |          |
| CSI_D2P    | M20  | NVCC_MIPI    |          |

| Ball Name    | Ball | Power Group | Comments |
|--------------|------|-------------|----------|
| CSI_D3M      | L20  | NVCC_MIPI   |          |
| CSI_D3P      | L19  | NVCC_MIPI   |          |
| CSIO_DAT10   | H17  | NVCC_CSI    |          |
| CSIO_DAT11   | H18  | NVCC_CSI    |          |
| CSIO_DAT12   | J17  | NVCC_CSI    |          |
| CSIO_DAT13   | J18  | NVCC_CSI    |          |
| CSIO_DAT14   | K17  | NVCC_CSI    |          |
| CSIO_DAT15   | K16  | NVCC_CSI    |          |
| CSIO_DAT16   | N16  | NVCC_CSI    |          |
| CSIO_DAT17   | M18  | NVCC_CSI    |          |
| CSIO_DAT18   | L17  | NVCC_CSI    |          |
| CSIO_DAT19   | M17  | NVCC_CSI    |          |
| CSIO_DAT4    | E17  | NVCC_CSI    |          |
| CSIO_DAT5    | E18  | NVCC_CSI    |          |
| CSIO_DAT6    | F17  | NVCC_CSI    |          |
| CSIO_DAT7    | F18  | NVCC_CSI    |          |
| CSIO_DAT8    | G17  | NVCC_CSI    |          |
| CSIO_DAT9    | G18  | NVCC_CSI    |          |
| CSIO_DATA_EN | D18  | NVCC_CSI    |          |
| CSIO_MCLK    | C18  | NVCC_CSI    |          |
| CSIO_PIXCLK  | C17  | NVCC_CSI    |          |
| CSIO_VSYNC   | D17  | NVCC_CSI    |          |
| DIO_DISP_CLK | A4   | NVCC_LCD    |          |
| DIO_PIN15    | A2   | NVCC_LCD    |          |
| DIO_PIN2     | B4   | NVCC_LCD    |          |
| DIO_PIN3     | B3   | NVCC_LCD    |          |
| DIO_PIN4     | A3   | NVCC_LCD    |          |
| DISPO_DAT0   | D5   | NVCC_LCD    |          |
| DISPO_DAT1   | C5   | NVCC_LCD    |          |
| DISPO_DAT10  | B7   | NVCC_LCD    |          |
| DISPO_DAT11  | A7   | NVCC_LCD    |          |
| DISPO_DAT12  | D8   | NVCC_LCD    |          |
| DISPO_DAT13  | C8   | NVCC_LCD    |          |
| DISPO_DAT14  | B8   | NVCC_LCD    |          |
| DISPO_DAT15  | A8   | NVCC_LCD    |          |
| DISPO_DAT16  | D9   | NVCC_LCD    |          |
| DISPO_DAT17  | C9   | NVCC_LCD    |          |
| DISPO_DAT18  | B9   | NVCC_LCD    |          |
| DISPO_DAT19  | A9   | NVCC_LCD    |          |
| DISPO_DAT2   | B5   | NVCC_LCD    |          |

| Ball Name   | Ball | Power Group   | Comments |
|-------------|------|---------------|----------|
| DISP0_DAT20 | D10  | NVCC_LCD      |          |
| DISP0_DAT21 | C10  | NVCC_LCD      |          |
| DISP0_DAT22 | B10  | NVCC_LCD      |          |
| DISP0_DAT23 | A10  | NVCC_LCD      |          |
| DISP0_DAT3  | A5   | NVCC_LCD      |          |
| DISP0_DAT4  | D6   | NVCC_LCD      |          |
| DISP0_DAT5  | C6   | NVCC_LCD      |          |
| DISP0_DAT6  | B6   | NVCC_LCD      |          |
| DISP0_DAT7  | A6   | NVCC_LCD      |          |
| DISP0_DAT8  | D7   | NVCC_LCD      |          |
| DISP0_DAT9  | C7   | NVCC_LCD      |          |
| DSI_CLK0M   | P18  | NVCC_MIPI     |          |
| DSI_CLK0P   | P17  | NVCC_MIPI     |          |
| DSI_D0M     | R17  | NVCC_MIPI     |          |
| DSI_D0P     | R18  | NVCC_MIPI     |          |
| DSI_D1M     | N17  | NVCC_MIPI     |          |
| DSI_D1P     | N18  | NVCC_MIPI     |          |
| EIM_A16     | H1   | NVCC_EIM1     |          |
| EIM_A17     | H4   | NVCC_EIM1     |          |
| EIM_A18     | J2   | NVCC_EIM1     |          |
| EIM_A19     | J3   | NVCC_EIM1     |          |
| EIM_A20     | J4   | NVCC_EIM1     |          |
| EIM_A21     | K1   | NVCC_EIM1     |          |
| EIM_A22     | K2   | NVCC_EIM1     |          |
| EIM_A23     | K3   | NVCC_EIM1     |          |
| EIM_A24     | K4   | NVCC_EIM1     |          |
| EIM_A25     | R5   | NVCC_EIM0     |          |
| EIM_BCLK    | B1   | NVCC_EIM2     |          |
| EIM_CS0     | H3   | NVCC_EIM1     |          |
| EIM_CS1     | H2   | NVCC_EIM1     |          |
| EIM_D16_NOR | V3   | NVCC_EIM0_NOR |          |
| EIM_D17_NOR | U4   | NVCC_EIM0_NOR |          |
| EIM_D18_NOR | U3   | NVCC_EIM0_NOR |          |
| EIM_D19     | T4   | NVCC_EIM0_NOR |          |
| EIM_D20     | T3   | NVCC_EIM0_NOR |          |
| EIM_D21     | R4   | NVCC_EIM0_NOR |          |
| EIM_D22     | P3   | NVCC_EIM0_NOR |          |
| EIM_D23     | P4   | NVCC_EIM0_NOR |          |
| EIM_D24     | T5   | NVCC_EIM0_NOR |          |
| EIM_D25     | N3   | NVCC_EIM0_NOR |          |

| Ball Name    | Ball | Power Group   | Comments |
|--------------|------|---------------|----------|
| EIM_D26      | M4   | NVCC_EIM0_NOR |          |
| EIM_D27      | M3   | NVCC_EIM0_NOR |          |
| EIM_D28      | L4   | NVCC_EIM0_NOR |          |
| EIM_D29      | L3   | NVCC_EIM0_NOR |          |
| EIM_D30      | L2   | NVCC_EIM0_NOR |          |
| EIM_D31      | L1   | NVCC_EIM0_NOR |          |
| EIM_DA0      | E1   | NVCC_EIM2     |          |
| EIM_DA1      | F4   | NVCC_EIM2     |          |
| EIM_DA10     | D2   | NVCC_EIM2     |          |
| EIM_DA11     | D4   | NVCC_EIM2     |          |
| EIM_DA12     | C4   | NVCC_EIM2     |          |
| EIM_DA13     | B2   | NVCC_EIM2     |          |
| EIM_DA14     | C2   | NVCC_EIM2     |          |
| EIM_DA15     | C3   | NVCC_EIM2     |          |
| EIM_DA2      | F2   | NVCC_EIM2     |          |
| EIM_DA3      | F3   | NVCC_EIM2     |          |
| EIM_DA4      | E2   | NVCC_EIM2     |          |
| EIM_DA5      | D1   | NVCC_EIM2     |          |
| EIM_DA6      | E4   | NVCC_EIM2     |          |
| EIM_DA7      | E3   | NVCC_EIM2     |          |
| EIM_DA8      | C1   | NVCC_EIM2     |          |
| EIM_DA9      | D3   | NVCC_EIM2     |          |
| EIM_EB0      | G3   | NVCC_EIM2     |          |
| EIM_EB1      | G2   | NVCC_EIM2     |          |
| EIM_EB2_NOR  | V4   | NVCC_EIM0_NOR |          |
| EIM_EB3      | N4   | NVCC_EIM0_NOR |          |
| EIM_LBA      | F1   | NVCC_EIM1     |          |
| EIM_OE       | G1   | NVCC_EIM1     |          |
| EIM_RW       | G4   | NVCC_EIM1     |          |
| EIM_WAIT     | F5   | NVCC_EIM2     |          |
| ENET_CRS_DV  | D11  | NVCC_ENET     |          |
| ENET_MDC     | D12  | NVCC_ENET     |          |
| ENET_MDIO    | C12  | NVCC_ENET     |          |
| ENET_REF_CLK | C13  | NVCC_ENET     |          |
| ENET_RX_ER   | C11  | NVCC_ENET     |          |
| ENET_RXD0    | A11  | NVCC_ENET     |          |
| ENET_RXD1    | B11  | NVCC_ENET     |          |
| ENET_TX_EN   | D13  | NVCC_ENET     |          |
| ENET_TXD0    | A12  | NVCC_ENET     |          |
| ENET_TXD1    | B12  | NVCC_ENET     |          |

| Ball Name         | Ball | Power Group   | Comments |
|-------------------|------|---------------|----------|
| GPIO_0            | E16  | NVCC_GPIO     |          |
| GPIO_1            | E15  | NVCC_GPIO     |          |
| GPIO_16           | M15  | NVCC_GPIO     |          |
| GPIO_17           | R16  | NVCC_GPIO     |          |
| GPIO_18_PMIC_INTB | AD12 | NVCC_GPIO     |          |
| GPIO_19           | P16  | NVCC_GPIO     |          |
| GPIO_2            | D16  | NVCC_GPIO     |          |
| GPIO_3            | A19  | NVCC_GPIO     |          |
| GPIO_4            | F16  | NVCC_GPIO     |          |
| GPIO_5            | G16  | NVCC_GPIO     |          |
| GPIO_6            | H16  | NVCC_GPIO     |          |
| GPIO_7            | J16  | NVCC_GPIO     |          |
| GPIO_8            | L16  | NVCC_GPIO     |          |
| GPIO_9            | M16  | NVCC_GPIO     |          |
| HDMI_CLKM         | K19  | HDMI_VPH      |          |
| HDMI_CLKP         | K20  | HDMI_VPH      |          |
| HDMI_D0M          | J19  | HDMI_VPH      |          |
| HDMI_D0P          | J20  | HDMI_VPH      |          |
| HDMI_D1M          | G19  | HDMI_VPH      |          |
| HDMI_D1P          | G20  | HDMI_VPH      |          |
| HDMI_D2M          | F19  | HDMI_VPH      |          |
| HDMI_D2P          | F20  | HDMI_VPH      |          |
| HDMI_HPD          | K18  | HDMI_VPH      |          |
| JTAG_MOD          | U19  | NVCC_JTAG     |          |
| JTAG_TCK          | T17  | NVCC_JTAG     |          |
| JTAG_TDI          | V18  | NVCC_JTAG     |          |
| JTAG_TDO          | V17  | NVCC_JTAG     |          |
| JTAG_TMS          | T18  | NVCC_JTAG     |          |
| JTAG_TRST_B       | T16  | NVCC_JTAG     |          |
| KEY_COL0          | E12  | NVCC_GPIO     |          |
| KEY_COL1          | E13  | NVCC_GPIO     |          |
| KEY_COL2          | C14  | NVCC_GPIO     |          |
| KEY_COL3_PMIC_SCL | W13  | NVCC_GPIO     |          |
| KEY_COL4          | C15  | NVCC_GPIO     |          |
| KEY_ROW0          | E11  | NVCC_GPIO     |          |
| KEY_ROW1          | F14  | NVCC_GPIO     |          |
| KEY_ROW2          | D14  | NVCC_GPIO     |          |
| KEY_ROW3_PMIC_SDA | W12  | NVCC_GPIO     |          |
| KEY_ROW4          | D15  | NVCC_GPIO     |          |
| LVDS0_CLK_N       | B19  | NVCC_LVDS_2P5 |          |

| Ball Name   | Ball | Power Group   | Comments |
|-------------|------|---------------|----------|
| LVDS0_CLK_P | B20  | NVCC_LVDS_2P5 |          |
| LVDS0_TX0_N | E19  | NVCC_LVDS_2P5 |          |
| LVDS0_TX0_P | E20  | NVCC_LVDS_2P5 |          |
| LVDS0_TX1_N | D19  | NVCC_LVDS_2P5 |          |
| LVDS0_TX1_P | D20  | NVCC_LVDS_2P5 |          |
| LVDS0_TX2_N | C19  | NVCC_LVDS_2P5 |          |
| LVDS0_TX2_P | C20  | NVCC_LVDS_2P5 |          |
| LVDS0_TX3_N | A18  | NVCC_LVDS_2P5 |          |
| LVDS0_TX3_P | B18  | NVCC_LVDS_2P5 |          |
| LVDS1_CLK_N | A16  | NVCC_LVDS_2P5 |          |
| LVDS1_CLK_P | B16  | NVCC_LVDS_2P5 |          |
| LVDS1_TX0_N | A17  | NVCC_LVDS_2P5 |          |
| LVDS1_TX0_P | B17  | NVCC_LVDS_2P5 |          |
| LVDS1_TX1_N | B15  | NVCC_LVDS_2P5 |          |
| LVDS1_TX1_P | A15  | NVCC_LVDS_2P5 |          |
| LVDS1_TX2_N | B14  | NVCC_LVDS_2P5 |          |
| LVDS1_TX2_P | A14  | NVCC_LVDS_2P5 |          |
| LVDS1_TX3_N | A13  | NVCC_LVDS_2P5 |          |
| LVDS1_TX3_P | B13  | NVCC_LVDS_2P5 |          |
| NANDF_ALE   | U15  | NVCC_NANDF    |          |
| NANDF_CLE   | T15  | NVCC_NANDF    |          |
| NANDF_CS0   | T14  | NVCC_NANDF    |          |
| NANDF_CS1   | Y16  | NVCC_NANDF    |          |
| NANDF_CS2   | W16  | NVCC_NANDF    |          |
| NANDF_CS3   | U16  | NVCC_NANDF    |          |
| NANDF_D0    | R13  | NVCC_NANDF    |          |
| NANDF_D1    | T13  | NVCC_NANDF    |          |
| NANDF_D2    | R12  | NVCC_NANDF    |          |
| NANDF_D3    | T12  | NVCC_NANDF    |          |
| NANDF_D4    | R11  | NVCC_NANDF    |          |
| NANDF_D5    | T11  | NVCC_NANDF    |          |
| NANDF_D6    | R10  | NVCC_NANDF    |          |
| NANDF_D7    | T10  | NVCC_NANDF    |          |
| NANDF_RB0   | U14  | NVCC_NANDF    |          |
| NANDF_WP_B  | V16  | NVCC_NANDF    |          |
| NOR_HOLD_B  | V13  | NVCC_EIM0     |          |
| NOR_W_B     | AA13 | NVCC_EIM0     |          |
| ONOFF       | AD13 | VDD_SNVS_IN   |          |
| PCIE_RXM    | Y20  | PCIE_VPH      |          |
| PCIE_RXP    | Y19  | PCIE_VPH      |          |

| Ball Name    | Ball | Power Group  | Comments |
|--------------|------|--------------|----------|
| PCIE_TXM     | AA19 | PCIE_VPH     |          |
| PCIE_TXP     | AA20 | PCIE_VPH     |          |
| RGMII_RD0    | N1   | NVCC_RGMII   |          |
| RGMII_RD1    | N2   | NVCC_RGMII   |          |
| RGMII_RD2    | M1   | NVCC_RGMII   |          |
| RGMII_RD3    | M2   | NVCC_RGMII   |          |
| RGMII_RX_CTL | P2   | NVCC_RGMII   |          |
| RGMII_RXC    | P1   | NVCC_RGMII   |          |
| RGMII_TD0    | T1   | NVCC_RGMII   |          |
| RGMII_TD1    | T2   | NVCC_RGMII   |          |
| RGMII_TD2    | R1   | NVCC_RGMII   |          |
| RGMII_TD3    | R2   | NVCC_RGMII   |          |
| RGMII_TX_CTL | U2   | NVCC_RGMII   |          |
| RGMII_TXC    | U1   | NVCC_RGMII   |          |
| RTC_XTALI    | V19  | VDD_SNVS_CAP |          |
| RTC_XTALO    | V20  | VDD_SNVS_CAP |          |
| SATA_RXM     | AE17 | SATA_VPH     |          |
| SATA_RXP     | AD17 | SATA_VPH     |          |
| SATA_TXM     | AE18 | SATA_VPH     |          |
| SATA_TXP     | AD18 | SATA_VPH     |          |
| SD1_CLK      | AE14 | NVCC_SD1     |          |
| SD1_CMD      | AD14 | NVCC_SD1     |          |
| SD1_DAT0     | AE16 | NVCC_SD1     |          |
| SD1_DAT1     | AD16 | NVCC_SD1     |          |
| SD1_DAT2     | AE15 | NVCC_SD1     |          |
| SD1_DAT3     | AD15 | NVCC_SD1     |          |
| SD2_CLK      | AB13 | NVCC_SD2     |          |
| SD2_CMD      | AC13 | NVCC_SD2     |          |
| SD2_DAT0     | AB14 | NVCC_SD2     |          |
| SD2_DAT1     | AB12 | NVCC_SD2     |          |
| SD2_DAT2     | AC12 | NVCC_SD2     |          |
| SD2_DAT3     | AC14 | NVCC_SD2     |          |
| SD3_CLK      | AC17 | NVCC_SD3     |          |
| SD3_CMD      | AC16 | NVCC_SD3     |          |
| SD3_DAT0     | AC18 | NVCC_SD3     |          |
| SD3_DAT1     | AB17 | NVCC_SD3     |          |
| SD3_DAT2     | AB18 | NVCC_SD3     |          |
| SD3_DAT3     | AA17 | NVCC_SD3     |          |
| SD3_DAT4     | Y17  | NVCC_SD3     |          |
| SD3_DAT5     | Y18  | NVCC_SD3     |          |

| Ball Name     | Ball | Power Group | Comments |
|---------------|------|-------------|----------|
| SD3_DAT6      | W17  | NVCC_SD3    |          |
| SD3_DAT7      | W18  | NVCC_SD3    |          |
| SD3_RST       | AB16 | NVCC_SD3    |          |
| SD4_CLK       | P9   | NVCC_NANDF  |          |
| SD4_CMD       | N9   | NVCC_NANDF  |          |
| SD4_DAT0      | N8   | NVCC_NANDF  |          |
| SD4_DAT1      | P8   | NVCC_NANDF  |          |
| SD4_DAT2      | N7   | NVCC_NANDF  |          |
| SD4_DAT3      | P7   | NVCC_NANDF  |          |
| SD4_DAT4      | N6   | NVCC_NANDF  |          |
| SD4_DAT5      | P6   | NVCC_NANDF  |          |
| SD4_DAT6      | N5   | NVCC_NANDF  |          |
| SD4_DAT7      | P5   | NVCC_NANDF  |          |
| SYS_POR_B     | AE12 | VDD_SNV5_IN |          |
| SYS_PWRON     | AE13 | VDD_SNV5_IN |          |
| SYS_STBY_REQ  | AB15 | VDD_SNV5_IN |          |
| TAMPER        | U13  | VDD_SNV5_IN |          |
| TEST_MODE     | R9   | VDD_SNV5_IN |          |
| USB_H1_DN     | AD20 | VDD_USB_CAP |          |
| USB_H1_DP     | AD19 | VDD_USB_CAP |          |
| USB_OTG_CHD_B | AB19 | VDD_USB_CAP |          |
| USB_OTG_DN    | AC19 | VDD_USB_CAP |          |
| USB_OTG_DP    | AC20 | VDD_USB_CAP |          |
| XTALI         | T19  | NVCC_PLL    |          |
| XTALO         | T20  | NVCC_PLL    |          |

## 7.2. Critical Signals

The table below shows the differences between the ball map of the i.MX6 Dual and the SCM-i.MX 6Dual/6Quad.

**Table 8. Signal Name differences from i.MX6 Dual**

| SCM-i.MX 6Dual/6Quad |      | i.MX6 Dual | Remarks                                             |
|----------------------|------|------------|-----------------------------------------------------|
| Ball Name            | Ball | Ball Name  |                                                     |
| EIM_D16_NOR          | V3   | EIM_D16    | connected to SPI NOR through a 330hm resistor       |
| EIM_D17_NOR          | U4   | EIM_D17    | Connected to SPI NOR                                |
| EIM_D18_NOR          | U3   | EIM_D18    | Connected to SPI NOR                                |
| EIM_EB2_NOR          | V4   | EIM_EB2    | Connected to SPI NOR                                |
| GPIO_18_PMIC_INTB    | AD12 | GPIO_18    | i.MX 6Dual/6QuadQ (GPIO18) connected to PMIC (INTB) |
| KEY_COL3_PMIC_SCL    | W13  | KEY_COL3   | i.MX6DQ (KEY_COL3) tied to PMIC (SCL)               |
| KEY_ROW3_PMIC_SDA    | W12  | KEY_ROW3   | i.MX6DQ (KEY_ROW3) tied to PMIC (SDA)               |

| SCM-i.MX 6Dual/6Quad |      | i.MX6 Dual    | Remarks                                             |
|----------------------|------|---------------|-----------------------------------------------------|
| Ball Name            | Ball | Ball Name     |                                                     |
| NOR_HOLD_B           | V13  |               | SPI NOR_HOLD_B                                      |
| NOR_W_B              | AA13 |               | SPI NOR_W_B                                         |
| PMIC_ICTEST          | Y8   |               | PMIC_ICTEST                                         |
| PMIC_SDWNB           | Y13  |               | PMIC_SDWNB                                          |
| SYS_POR_B            | AE12 | POR_B         | i.MX6DQ (POR_B) connected to PMIC (RESETBMCU)       |
| SYS_PWRON            | AE13 | PMIC_ON_REQ   | i.MX6DQ (PMIC_ON_REQ) connected to PMIC (PWRON)     |
| SYS_STBY_REQ         | AB15 | PMIC_STBY_REQ | i.MX6DQ (PMIC_STBY_REQ) connected to PMIC (STANDBY) |
| –                    | –    | CSI_REXT      | Grounded internally                                 |
| –                    | –    | DSI_REXT      | Grounded internally                                 |
| –                    | –    | FA_ANA        | Grounded internally                                 |
| –                    | –    | HDMI_REF      | Grounded internally                                 |
| –                    | –    | MLB_CN        | Not pinned out.                                     |
| –                    | –    | MLB_CP        | Not pinned out.                                     |
| –                    | –    | MLB_DN        | Not pinned out.                                     |
| –                    | –    | MLB_DP        | Not pinned out.                                     |
| –                    | –    | MLB_SN        | Not pinned out.                                     |
| –                    | –    | MLB_SP        | Not pinned out.                                     |
| –                    | –    | PCIE_REXT     | Grounded internally                                 |
| –                    | –    | SATA_REXT     | Grounded internally                                 |
| –                    | –    | ZQPAD         | Tied to ground through 240Ohm resistor.             |

The table below shows the device list for ground, power, sense, and reference contact signals

**Table 9. Supply Signal List for i.MX6 Dual**

| Supply Name    | Balls                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Remark                              |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| DDR_1V2        | E5, E9, E14, V15                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                     |
| DDR_1V2_SW3AFB | W8                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                     |
| DDR_1V8        | V5                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                     |
| GPANAIO        | U12                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Test signal. Should be unconnected. |
| GND            | A1, C16, U9, V6, W4, W9, Y4, Y5, E10, E6, E7, E8, F10, F11, F6, F7, F8, A20, F9, G10, G11, G12, G14, G6, G7, G9, H10, H11, AA12, H12, H14, H20, H9, J1, J10, J11, J12, J13, J14, AA14, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, AA15, L11, L12, L18, L7, L8, L9, R3, R6, R7, R8, AA16, U20, V10, V11, V14, V2, W11, W14, W15, Y12, Y14, AA18, Y15, AA3, AA4, AA5, AA6, AA7, AA8, AA9, AB11, AB3, AC15, AB4, AB5, AB6, AB7, AB8, AB9, AC4, AC5, AC6, AC7, |                                     |

| Supply Name   | Balls                                                                    | Remark                               |
|---------------|--------------------------------------------------------------------------|--------------------------------------|
|               | AE20, AC8, AC9, AE1, T6, T7, T8, T9, U6, U7, U8                          |                                      |
| HDMI_DDCCEC   | H19                                                                      |                                      |
| HDMI_VP       | L14                                                                      |                                      |
| HDMI_VPH      | K14                                                                      |                                      |
| LICELL        | Y11                                                                      | LICELL output from PMIC              |
| NVCC_CSI      | H15                                                                      |                                      |
| NVCC_EIM0_NOR | L5                                                                       | EIM0 domain shared with the SPI NOR. |
| NVCC_EIM1     | K5                                                                       |                                      |
| NVCC_EIM2     | J5                                                                       |                                      |
| NVCC_ENET     | G5                                                                       |                                      |
| NVCC_GPIO     | G15                                                                      |                                      |
| NVCC_JTAG     | P15                                                                      |                                      |
| NVCC_LCD      | H5                                                                       |                                      |
| NVCC_LVDS2P5  | F15                                                                      |                                      |
| NVCC_MIPI     | M14                                                                      |                                      |
| NVCC_NANDF    | P10                                                                      |                                      |
| NVCC_PLL_OUT  | R14                                                                      |                                      |
| NVCC_RGMII    | M5                                                                       |                                      |
| NVCC_SD1      | M6                                                                       |                                      |
| NVCC_SD2      | N10                                                                      |                                      |
| NVCC_SD3      | P11                                                                      |                                      |
| PCIE_VP       | N15                                                                      |                                      |
| PCIE_VPH      | N12                                                                      |                                      |
| PCIE_VPTX     | N14                                                                      |                                      |
| PMIC_VCOREREF | AD9                                                                      | PMIC V_core_ref                      |
| PMIC_VDDOTP   | Y9                                                                       | PMIC VDD OTP                         |
| PMIC_VIN      | AC10, AE11, AE2, AE3, V7, V8, AC11, AC2, AC3, AD10, AD11, AD2, AD3, AE10 | Main system supply.                  |
| SATA_VP       | N13                                                                      |                                      |
| SATA_VPH      | N11                                                                      |                                      |
| SW1ABFB       | AE9                                                                      |                                      |
| SW1ABLX       | AD7, AD8, AE6, AE7, AE8                                                  |                                      |
| SW1CFB        | AE5                                                                      |                                      |
| SW1CLX        | AD4, AD5, AD6, AE4                                                       |                                      |
| SW2LX         | W1, W2, W3, Y1, Y2, Y3                                                   |                                      |
| SW3ABLX       | W6, W7, Y6, Y7                                                           |                                      |
| SW4LX         | AA1, AA2, AB2                                                            |                                      |
| SWBSTFB       | Y10                                                                      |                                      |
| SWBSTIN       | AB10                                                                     |                                      |
| SWBSTLX       | AA10, AA11                                                               |                                      |

| Supply Name    | Balls              | Remark                                        |
|----------------|--------------------|-----------------------------------------------|
| SYS_SW2FB_VIN2 | V1                 |                                               |
| SYS_SW4FB_VIN1 | AB1                |                                               |
| SYS_VSNVS      | W10                | i.MX 6D/6Q (VDD_SNVS_IN) tied to PMIC (VSNVS) |
| USB_H1_VBUS    | AE19               |                                               |
| USB_OTG_VBUS   | AB20               |                                               |
| VDD_SNVS_CAP   | P12                |                                               |
| VDDARM_CAP     | M10, M11, M12      |                                               |
| VDDARM_IN      | M7, M8, M9         |                                               |
| VDDARM23_CAP   | K13, L13, M13      |                                               |
| VDDARM23_IN    | J15, K15, L15      |                                               |
| VDDHIGH_CAP    | P14                |                                               |
| VDDHIGH_IN     | R15                |                                               |
| VDDPU_CAP      | J6, K6, L6         |                                               |
| VDDSOC_CAP     | F12, F13, G13, H13 |                                               |
| VDDSOC_IN      | G8, H6, H7, H8     |                                               |
| VDDUSB_CAP     | P13                |                                               |
| VGEN1          | AD1                |                                               |
| VGEN2          | AC1                |                                               |
| VGEN3          | U5                 |                                               |
| VGEN4          | W5                 |                                               |
| VGEN5          | V9                 |                                               |
| VGEN6          | U10                |                                               |

## 7.3. Ball Map

Table 10. Ball Map

|   | 1        | 2         | 3        | 4            | 5          | 6          | 7           | 8           | 9           | 10          | 11          | 12        | 13           | 14          | 15          | 16          | 17          | 18           | 19          | 20          |
|---|----------|-----------|----------|--------------|------------|------------|-------------|-------------|-------------|-------------|-------------|-----------|--------------|-------------|-------------|-------------|-------------|--------------|-------------|-------------|
| A | GND      | DIO_PIN15 | DIO_PIN4 | DIO_DISP_CLK | DISPO_DAT3 | DISPO_DAT7 | DISPO_DAT11 | DISPO_DAT15 | DISPO_DAT19 | DISPO_DAT23 | ENET_RXD0   | ENET_TXD0 | LVDS1_TX3_N  | LVDS1_TX2_P | LVDS1_TX1_P | LVDS1_CLK_N | LVDS1_TX0_N | LVDS0_TX3_N  | GPIO_3      | GND         |
| B | EIM_BCLK | EIM_DA13  | DIO_PIN3 | DIO_PIN2     | DISPO_DAT2 | DISPO_DAT6 | DISPO_DAT10 | DISPO_DAT14 | DISPO_DAT18 | DISPO_DAT22 | ENET_RXD1   | ENET_TXD1 | LVDS1_TX3_P  | LVDS1_TX2_N | LVDS1_TX1_N | LVDS1_CLK_P | LVDS1_TX0_P | LVDS0_TX3_P  | LVDS0_CLK_N | LVDS0_CLK_P |
| C | EIM_DA8  | EIM_DA14  | EIM_DA15 | EIM_DA12     | DISPO_DAT1 | DISPO_DAT5 | DISPO_DAT9  | DISPO_DAT13 | DISPO_DAT17 | DISPO_DAT21 | ENET_RX_ER  | ENET_MDIO | ENET_REF_CLK | KEY_COL2    | KEY_COL4    | GND         | CSIO_PIXCLK | CSIO_MCLK    | LVDS0_TX2_N | LVDS0_TX2_P |
| D | EIM_DA5  | EIM_DA10  | EIM_DA9  | EIM_DA11     | DISPO_DAT0 | DISPO_DAT4 | DISPO_DAT8  | DISPO_DAT12 | DISPO_DAT16 | DISPO_DAT20 | ENET_CRS_DV | ENET_MDC  | ENET_TX_EN   | KEY_ROW2    | KEY_ROW4    | GPIO_2      | CSIO_VSYNC  | CSIO_DATA_EN | LVDS0_TX1_N | LVDS0_TX1_P |

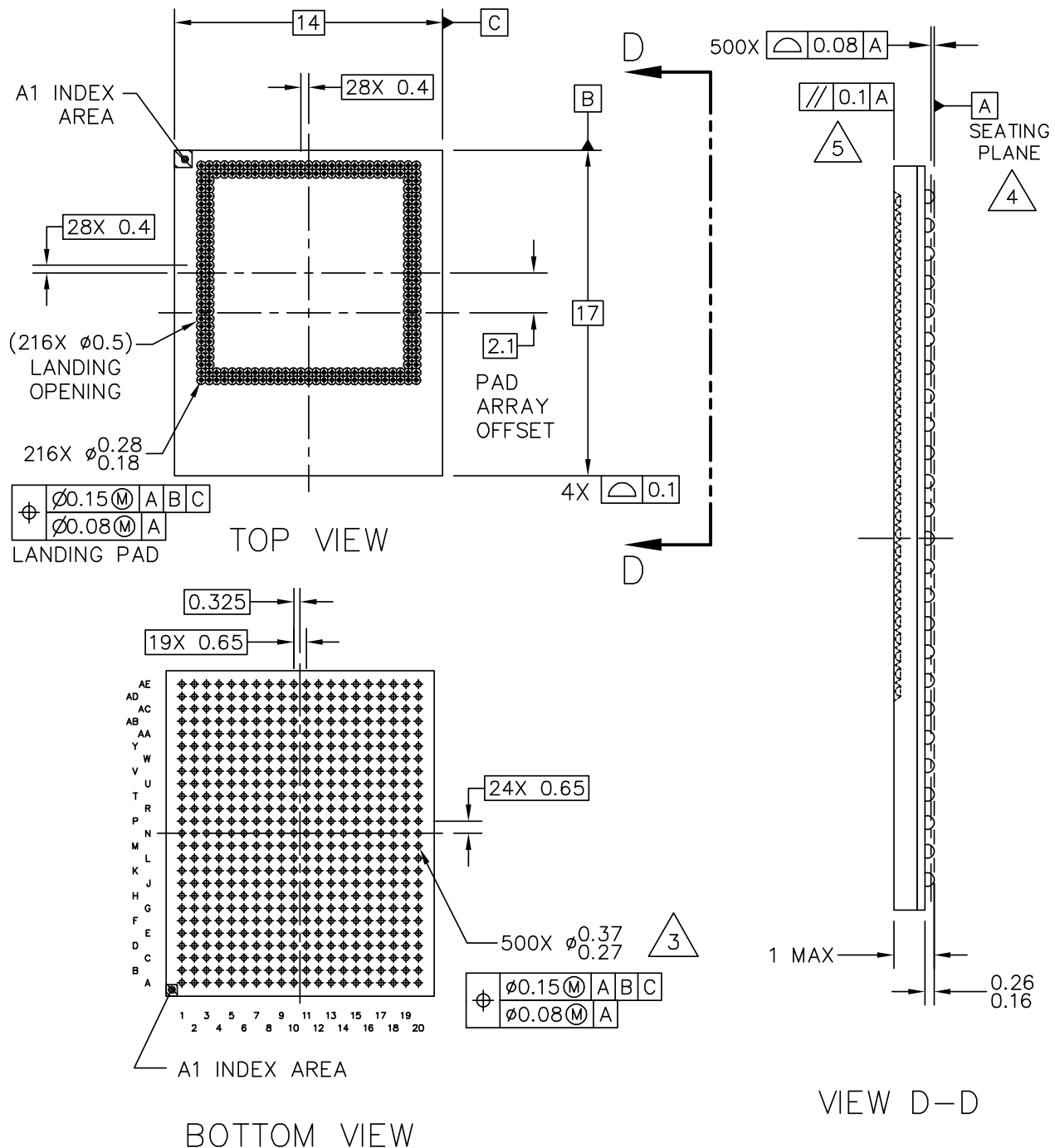
| U            | T           | R            | P            | N          | M            | L             | K            | J          | H            | G          | F             | E           |
|--------------|-------------|--------------|--------------|------------|--------------|---------------|--------------|------------|--------------|------------|---------------|-------------|
| RGMII_TXC    | RGMII_TD0   | RGMII_TD2    | RGMII_RXC    | RGMII_RD0  | RGMII_RD2    | EIM_D31       | EIM_A21      | GND        | EIM_A16      | EIM_OE     | EIM_LBA       | EIM_DAO     |
| RGMII_TX_CTL | RGMII_TD1   | RGMII_TD3    | RGMII_RX_CTL | RGMII_RD1  | RGMII_RD3    | EIM_D30       | EIM_A22      | EIM_A18    | EIM_CS1      | EIM_FB1    | EIM_DA2       | EIM_DA4     |
| EIM_D18_NO_R | EIM_D20     | GND          | EIM_D22      | EIM_D25    | EIM_D27      | EIM_D29       | EIM_A23      | EIM_A19    | EIM_CS0      | EIM_EB0    | EIM_DA3       | EIM_DA7     |
| EIM_D17_NO_R | EIM_D19     | EIM_D21      | EIM_D23      | EIM_EB3    | EIM_D26      | EIM_D28       | EIM_A24      | EIM_A20    | EIM_A17      | EIM_RW     | EIM_DA1       | EIM_DA6     |
| VGEN3        | EIM_D24     | EIM_A25      | SD4_DAT7     | SD4_DAT6   | NVCC_RGMII   | NVCC_EIM0_NOR | NVCC_EIM1    | NVCC_EIM2  | NVCC_LCD     | NVCC_ENET  | EIM_WAIT      | DDR_1V2     |
| GND          | GND         | GND          | SD4_DAT5     | SD4_DAT4   | NVCC_SD1     | VDDPU_CAP     | VDDPU_CAP    | VDDPU_CAP  | VDDSOC_IN    | GND        | GND           | GND         |
| GND          | GND         | GND          | SD4_DAT3     | SD4_DAT2   | VDDARM_IN    | GND           | GND          | GND        | VDDSOC_IN    | GND        | GND           | GND         |
| GND          | GND         | GND          | SD4_DAT1     | SD4_DAT0   | VDDARM_IN    | GND           | GND          | GND        | VDDSOC_IN    | VDDSOC_IN  | GND           | GND         |
| GND          | GND         | TEST_MODE    | SD4_CLK      | SD4_CMD    | VDDARM_IN    | GND           | GND          | GND        | GND          | GND        | GND           | DDR_1V2     |
| VGEN6        | NANDF_D7    | NANDF_D6     | NVCC_NAND_F  | NVCC_SD2   | VDDARM_CAP   | GND           | GND          | GND        | GND          | GND        | GND           | GND         |
| BOOT_MODE_0  | NANDF_D5    | NANDF_D4     | NVCC_SD3     | SATA_VPH   | VDDARM_CAP   | GND           | GND          | GND        | GND          | GND        | GND           | KEY_ROW0    |
| GPANAIO      | NANDF_D3    | NANDF_D2     | VDD_SNVS_CAP | PCIE_VPH   | VDDARM_CAP   | GND           | GND          | GND        | GND          | GND        | VDDSOC_CAP    | KEY_COL0    |
| TAMPER       | NANDF_D1    | NANDF_D0     | VDDUSB_CAP   | SATA_VP    | VDDARM23_CAP | VDDARM23_CAP  | VDDARM23_CAP | GND        | VDDSOC_CAP   | VDDSOC_CAP | VDDSOC_CAP    | KEY_COL1    |
| NANDF_RB0    | NANDF_CS0   | NVCC_PLL_OUT | VDDHIGH_CAP  | PCIE_VPTX  | NVCC_MIPI    | HDMI_VP       | HDMI_VPH     | GND        | GND          | GND        | KEY_ROW1      | DDR_1V2     |
| NANDF_ALE    | NANDF_CLE   | VDDHIGH_IN   | NVCC_JTAG    | PCIE_VP    | GPIO_16      | VDDARM23_N    | VDDARM23_N   | VDDARM23_N | NVCC_CSI     | NVCC_GPIO  | NVCC_LVDS2_P5 | GPIO_1      |
| NANDF_CS3    | JTAG_TRST_B | GPIO_17      | GPIO_19      | CSIO_DAT16 | GPIO_9       | GPIO_8        | CSIO_DAT15   | GPIO_7     | GPIO_6       | GPIO_5     | GPIO_4        | GPIO_0      |
| CLK1_P       | JTAG_TCK    | DSI_D0M      | DSI_CLK0P    | DSI_D1M    | CSIO_DAT19   | CSIO_DAT18    | CSIO_DAT14   | CSIO_DAT12 | CSIO_DAT10   | CSIO_DAT8  | CSIO_DAT6     | CSIO_DAT4   |
| CLK1_N       | JTAG_TMS    | DSI_D0P      | DSI_CLK0M    | DSI_D1P    | CSIO_DAT17   | GND           | HDMI_HPD     | CSIO_DAT13 | CSIO_DAT11   | CSIO_DAT9  | CSIO_DAT7     | CSIO_DAT5   |
| JTAG_MOD     | XTALI       | CSIO_D0P     | CSIO_D1M     | CSIO_CLK0P | CSIO_D2M     | CSIO_D3P      | HDMI_CLKM    | HDMI_D0M   | HDMI_DDCC_EC | HDMI_D1M   | HDMI_D2M      | LVDS0_TX0_N |
| GND          | XTALO       | CSIO_D0M     | CSIO_D1P     | CSIO_CLK0M | CSIO_D2P     | CSIO_D3M      | HDMI_CLKP    | HDMI_D0P   | GND          | HDMI_D1P   | HDMI_D2P      | LVDS0_TX0_P |

|  | AE          | AD                | AC         | AB             | AA       | Y            | W                 | V              |    |
|--|-------------|-------------------|------------|----------------|----------|--------------|-------------------|----------------|----|
|  | GND         | VGEN1             | VGEN2      | SYS_SW4FB_VIN1 | SW4LX    | SW2LX        | SW2LX             | SYS_SW2FB_VIN2 | 1  |
|  | PMIC_VIN    | PMIC_VIN          | PMIC_VIN   | SW4LX          | SW4LX    | SW2LX        | SW2LX             | GND            | 2  |
|  | PMIC_VIN    | PMIC_VIN          | PMIC_VIN   | GND            | GND      | SW2LX        | SW2LX             | EIM_D16_NO_R   | 3  |
|  | SW1CLX      | SW1CLX            | GND        | GND            | GND      | GND          | GND               | EIM_EB2_NO_R   | 4  |
|  | SW1CFB      | SW1CLX            | GND        | GND            | GND      | GND          | VGEN4             | DDR_1V8        | 5  |
|  | SW1ABLX     | SW1CLX            | GND        | GND            | GND      | SW3ABLX      | SW3ABLX           | GND            | 6  |
|  | SW1ABLX     | SW1ABLX           | GND        | GND            | GND      | SW3ABLX      | SW3ABLX           | PMIC_VIN       | 7  |
|  | SW1ABLX     | SW1ABLX           | GND        | GND            | GND      | PMIC_ICTEST  | DDR_1V2_SW3AFB    | PMIC_VIN       | 8  |
|  | SW1ABFB     | PMIC_VCORE_REF    | GND        | GND            | GND      | PMIC_VDDOT_P | GND               | VGEN5          | 9  |
|  | PMIC_VIN    | PMIC_VIN          | PMIC_VIN   | SWBSTIN        | SWBSTLX  | SWBSTFB      | SYS_V5NV5         | GND            | 10 |
|  | PMIC_VIN    | PMIC_VIN          | PMIC_VIN   | GND            | SWBSTLX  | LICELL       | GND               | GND            | 11 |
|  | SYS_POR_B   | GPIO_18_PMIC_INTB | SD2_DAT2   | SD2_DAT1       | GND      | GND          | KEY_ROW3_PMIC_SDA | BOOT_MODE1     | 12 |
|  | SYS_PWRON   | ONOFF             | SD2_CMD    | SD2_CLK        | NOR_W_B  | PMIC_SDWNB   | KEY_COL3_PMIC_SCL | NOR_HOLD_B     | 13 |
|  | SD1_CLK     | SD1_CMD           | SD2_DAT3   | SD2_DAT0       | GND      | GND          | GND               | GND            | 14 |
|  | SD1_DAT2    | SD1_DAT3          | GND        | SYS_STBY_REQ   | GND      | GND          | GND               | DDR_1V2        | 15 |
|  | SD1_DAT0    | SD1_DAT1          | SD3_CMD    | SD3_RST        | GND      | NANDF_CS1    | NANDF_CS2         | NANDF_WP_B     | 16 |
|  | SATA_RXM    | SATA_RXP          | SD3_CLK    | SD3_DAT1       | SD3_DAT3 | SD3_DAT4     | SD3_DAT6          | JTAG_TDO       | 17 |
|  | SATA_TXM    | SATA_TXP          | SD3_DAT0   | SD3_DAT2       | GND      | SD3_DAT5     | SD3_DAT7          | JTAG_TDI       | 18 |
|  | USB_H1_VBUS | USB_H1_DP         | USB_OTG_DN | USB_OTG_CHD_B  | PCIE_TXM | PCIE_RXP     | CLK2_N            | RTC_XTALI      | 19 |
|  | GND         | USB_H1_DN         | USB_OTG_DP | USB_OTG_VBUS   | PCIE_TXP | PCIE_RXM     | CLK2_P            | RTC_XTALO      | 20 |

## 7.4. Package Drawings

Figure 4. SCM-i.MX 6Dual/6Quad without Memory

MECHANICAL OUTLINE  
DO NOT SCALE THIS DRAWING



RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES.  
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TITLE: FLIP CHIP SIP STACKABLE,  
14 X 17 X 0.92 PKG,  
0.65 MM PITCH, 500 I/O

DOCUMENT NO: 98ASA00965D

REV: 0

STANDARD: NON-JEDEC

SOT1690-2

SHEET: 1 OF 3



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## MECHANICAL OUTLINE

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### NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3.  MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4.  DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5.  PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. SCORING OR GROOVES ON TOP SURFACE OF PACKAGE IS NOT PERMITTED.
7. NO VOIDS IN ENCAPSULATION PERMITTED.

TITLE: FLIP CHIP SIP STACKABLE,  
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## REVISION HISTORY

| LTR | ORIGINATOR  | REVISIONS                                | DRAFTER | DATE        |
|-----|-------------|------------------------------------------|---------|-------------|
| 0   | AKHIL SINGH | RELEASED FOR PRODUCTION.<br>(DAR #25395) | S. ZANG | 09 APR 2016 |

TITLE: FLIP CHIP SIP STACKABLE,  
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0.65 MM PITCH, 500 I/O

DOCUMENT NO: 98ASA00965D REV: 0

STANDARD: NON-JEDEC

SOT1690-2 SHEET: 3

## 8. Revision History

| Revision | Date    | Change description   |
|----------|---------|----------------------|
| 0        | 01/2017 | Technical Data Sheet |



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Document Number: SCMIMX6DQIEC  
Rev. 0  
01/2017

