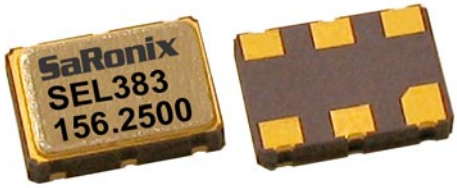
SaRonix™
A PERICOM® COMPANY

SEL383 Series

3.3V PECL Low Jitter Crystal Clock Oscillator (XO)



Actual Size = 7 x 5mm

Product Features

- Thicker crystal than conventional overtone for improved reliablity
- Less than 1 ps RMS jitter with advanced non-PLL, patented XP Technology (U.S. Patent #7002423)
- Tight stability over a broad range of operating conditions
- 3.3V PECL (LVPECL) compatible logic levels
- Low power stand-by mode up to 50 MHz
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow & washing techniques
- IBIS models available
- RoHS compliant **

  **per #7, Annex of Directive 2002/OS/EC

Product Description

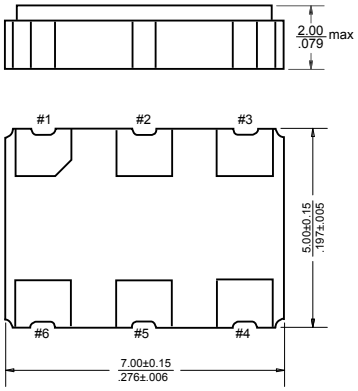
The SEL383 Series is a 3.3V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a patented oscillator design, is compatible with LVPECL logic levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The SEL383 Series is an ideal reference clock for high-speed applications requiring low jitter, including:

- 1/10 Gigabit Ethernet
- 2/4/10G FibreChannel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- Passive Optical Network (PON) devices
- HD Video Systems

Packaging Outline



Pin Functions

Pin	Function
1	OE or NC
2	OE or NC
3	V_{EE}
4	Q Output
5	$\overline{Q}$ Output
6	V_{CC}

Common Frequencies

Contact SaRonix for additional frequencies

38.8800 MHz	100.0000 MHz	156.2500 MHz
50.0000 MHz	106.2500 MHz	159.3750 MHz
62.5000 MHz	125.0000 MHz	160.0000 MHz
66.0000 MHz	133.0000 MHz	161.1328 MHz*
66.6667 MHz	148.3516 MHz	187.5000 MHz
74.1758 MHz	148.5000 MHz	200.0000 MHz
75.0000 MHz	150.0000 MHz	212.5000 MHz
77.7600 MHz	155.5200 MHz	

Ordering Information

S EL383 3 B - 212.5000 (T)

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Product Series

Output Enable/Disable Function
0 = N/C pin 1, and pin 2
3 = OE pin 1, N/C pin 2
4 = N/C pin 1, OE pin 2

Frequency Stability
A = ±25 ppm (-10 to +70°C)
B = ±50 ppm (-10 to +70°C)
E = ±50 ppm (-40 to +85°C)
Note: Others available, please inquire

Output Frequency (MHz)

Packaging
(T) = Tape & Reel
full reel increment
Blank = Bulk packagec

Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency	38.88		212.50	MHz	As specified
Supply voltage	2.97	3.3	3.63	V	
Supply current		55	85	mA	≤ 50 MHz (enabled)
Supply current			0.03	mA	≤ 50 MHz (disabled)
Supply current		50	60	mA	> 50 MHz (enabled)
Supply current			15	mA	> 50 MHz (disabled)
Frequency stability			±25 to ±50	ppM	See Note 1 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, V_{OL}			V_{CC} – 1.620	V	0 to +85°C
Output logic 0, V_{OL}			V_{CC} – 1.555	V	-40 to 0°C
Output logic 1, V_{OH}	V_{CC} – 1.025			V	0 to +85°C
Output logic 1, V_{OH}	V_{CC} – 1.085			V	-40 to 0°C
Output load	50Ω to V_{CC} – 2V				output requires termination
Duty cycle	45		55	%	measured 50% of waveform
Rise and fall time		500	850	ps	measured 20/80% of waveform
Jitter, phase			1	ps RMS (1-σ)	12kHz to 40MHz frequency band
Jitter, total			40	ps pk-pk	100,000 random periods

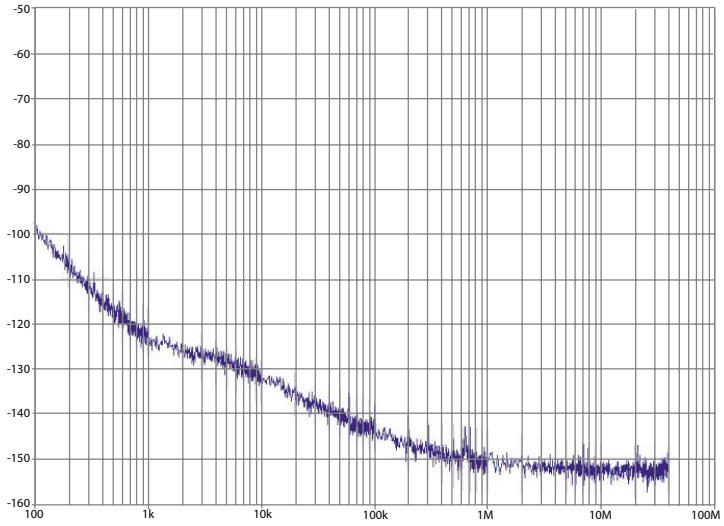
Notes:

1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 years at 40°C average effective ambient temperature), shock and vibration.

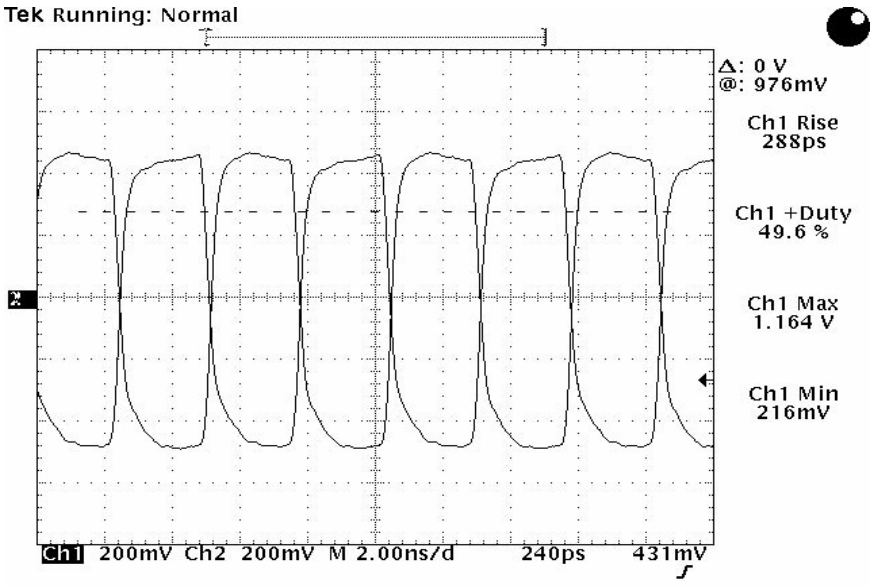
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (OE pin), Output Enable	2.2			V	or open
Input voltage (OE pin), Output Disable			0.8	V	Outputs disabled to Hi-Z
Internal Pull-up Resistance	50			kΩ	
Output disable delay			200	ns	
Output enable delay			10	ms	

Typical Phase Noise



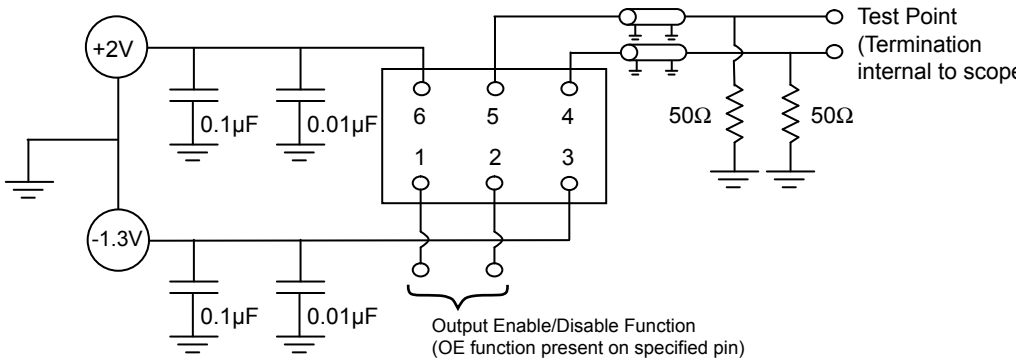
Typical Output Waveform



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

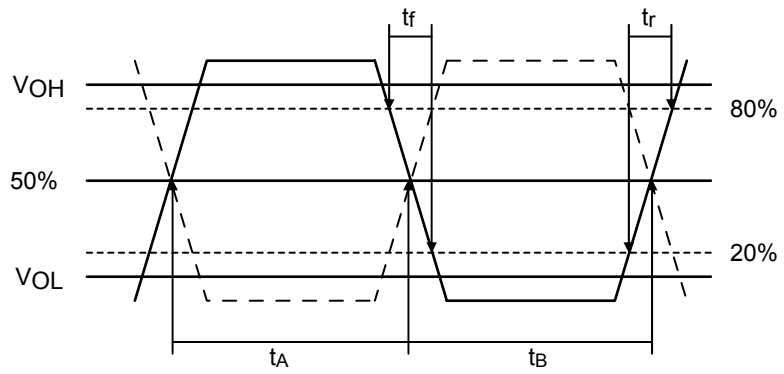


Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

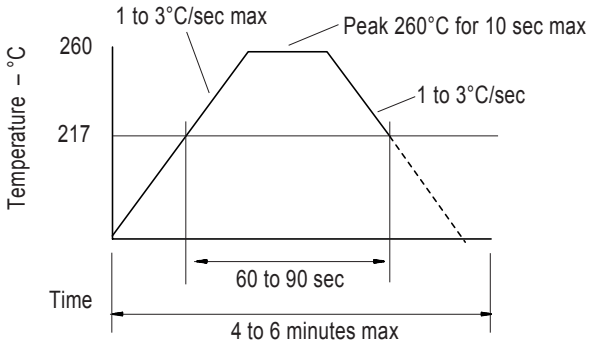
Output Waveform



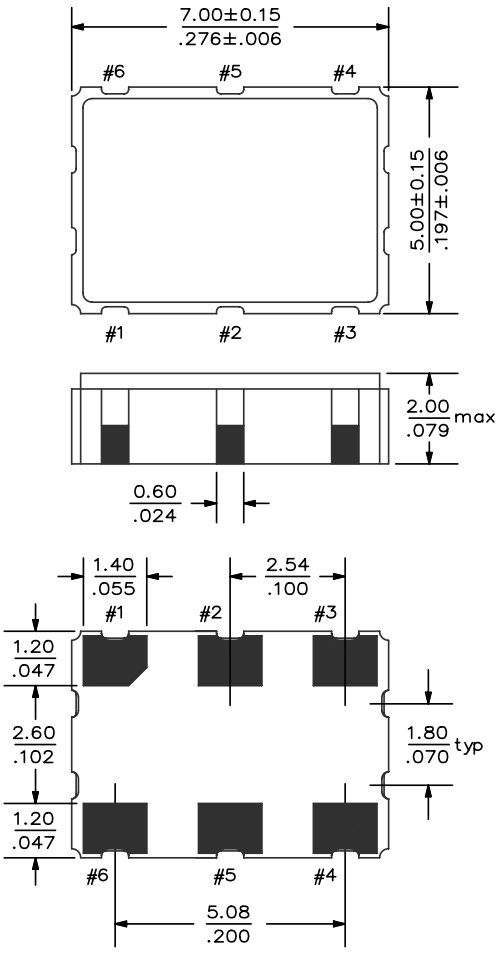
Duty cycle = 100% × (t_A) / (t_A + t_B)

Reflow Soldering Profile

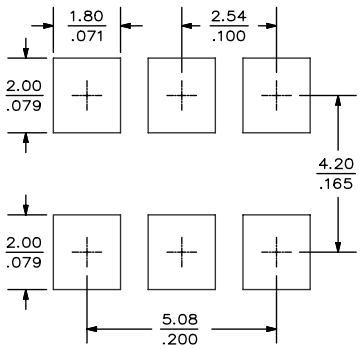
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1:	**SEL383 X**	**(SaRonix, Model, Stability code)**
Marking LINE 2:	**Frequency**	**(Frequency code)**
Marking LINE 3:	**● YY WW X**	**(Pin 1, Year, Week, Origin)**

**** Exact location of markings may vary**