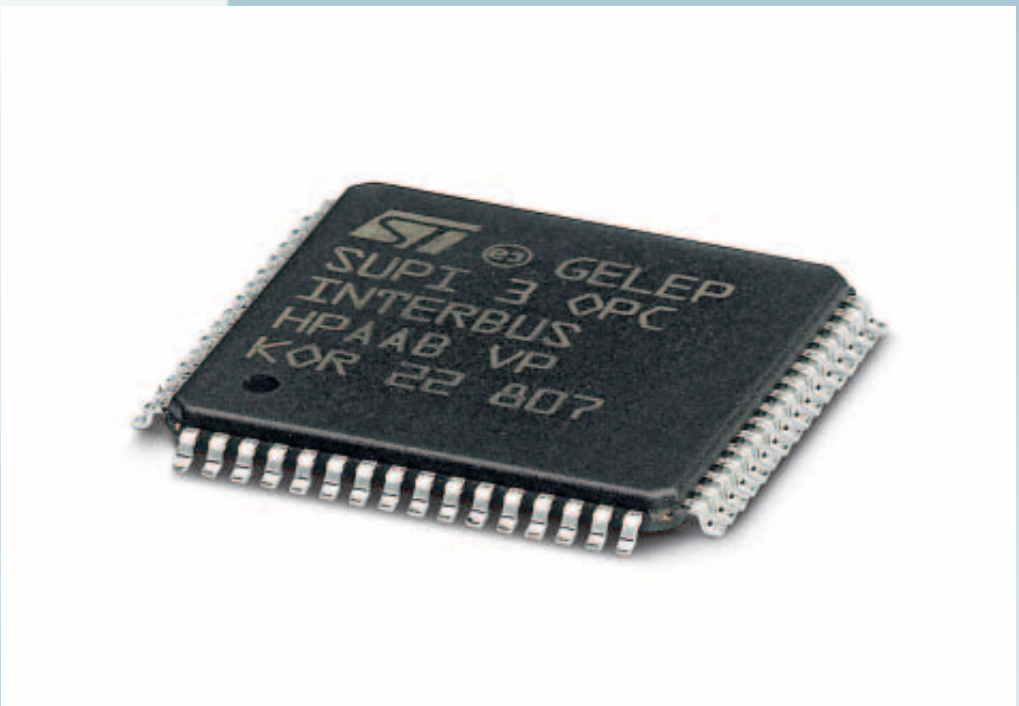
AUTOMATION



User manual

IBS SUPI 3 OPC UM E

Order No.: —

INTERBUS IBS SUPI 3 OPC protocol chip

PHOENIX CONTACT
INSPIRING INNOVATIONS

AUTOMATION

User manual
IBS SUPI 3 OPC INTERBUS protocol chip

04/2009

Designation: IBS SUPI 3 OPC UM E

Revision: 05

Order No.: —

This user manual is valid for:

Designation	Order No.
IBS SUPI 3 LS	2746977
IBS SUPI 3 OPC	2746980
IBS SUPI 3 OPC T&R	2746964

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In order to ensure the safe use of the product described, you have to read and understand this manual. The following notes provide information on how to use this manual.

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This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

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This indicates a hazardous situation which, if not avoided, will result in death or serious injury.

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This indicates a hazardous situation which, if not avoided, could result in death or serious injury.

CAUTION
This indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.

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Table of contents

1 General functions

1.1 Introduction

The SUPI 3 OPC/SUPI 3 OPC (T&R) (referred to in the following as: SUPI 3 OPC; OPC = **O**ptical **P**rotocol **C**hip) is another INTERBUS slave protocol chip of the SUPI 3 family. It can be used to develop all device classes such as digital modules, bus terminal modules (BK), and intelligent I/O devices.

This user manual describes the SUPI 3 OPC in detail and illustrates its most common applications.

The SUPI 3 OPC offers a high level of operational safety and diagnostic capability for optical signal transmission. The control systems and procedures required are described in this user manual.

On the basis of this description you may implement your own INTERBUS devices within a very short time. With the end user in mind, subject the devices to the INTERBUS conformance test.

In addition to this document you will find the INTERBUS Club guideline "Conformity Test and Certification" as a reference work on the Internet at www.interbusclub.com.

Current hardware and software information for the device manufacturer as well as further product documents from Phoenix Contact can be found on the Internet at www.phoenixcontact.net/download.

1.2 SUPI 3 OPC protocol chip

The SUPI 3 OPC protocol chip is an ASIC in 0.6 µm CMOS technology with approximately 15,000 gate equivalents. It can be used to implement 2-wire remote bus and 2-wire local bus devices.

The SUPI 3 OPC differs from the IBS SUPI 3 in particular through its support of optical transmission methods. These include:

– Optical power regulation for fiber optic transmitters
– Optical transmission diagnostics
– Automatic bus connector recognition (RBST/LBST[1]) for copper and fiber optic transmission
– Automatic recognition of the control function on other units or devices

[1] Signal, which indicates that another device follows.

The SUPI 3 OPC can be used for I/O applications, bus terminal modules, and intelligent slave devices. It has a parallel I/O interface (similar to the multi-function pins (MFPs) on SUPI 3), a voltage monitor, an SPI master and slave interface, and device-oriented local bus diagnostics for devices with and without data return.

Table 1-1 Housing versions

Order designation	Order No.	Housing
IBS SUPI 3 LS	2746977	TQFP44
IBS SUPI 3 OPC	2746980	TQFP64
IBS SUPI 3 OPC T&R	2746964	TQFP64

The SUPI 3 LS (TQFP 44) is a version of the SUPI 3 OPC with a smaller housing. Therefore it has less pins. This means that the SUPI 3 LS **cannot** be extended by additional data registers and is only suitable for copper interfaces. Therefore, SUPI 3 LS does **not** support optical signal transmission.

1.3 Basic structure

The device processes layer 2 of the ISO/OSI reference model independently according to IEC 61158.

All interfaces are designed for the **2-wire protocol only**. The following block diagram shows the chip structure.

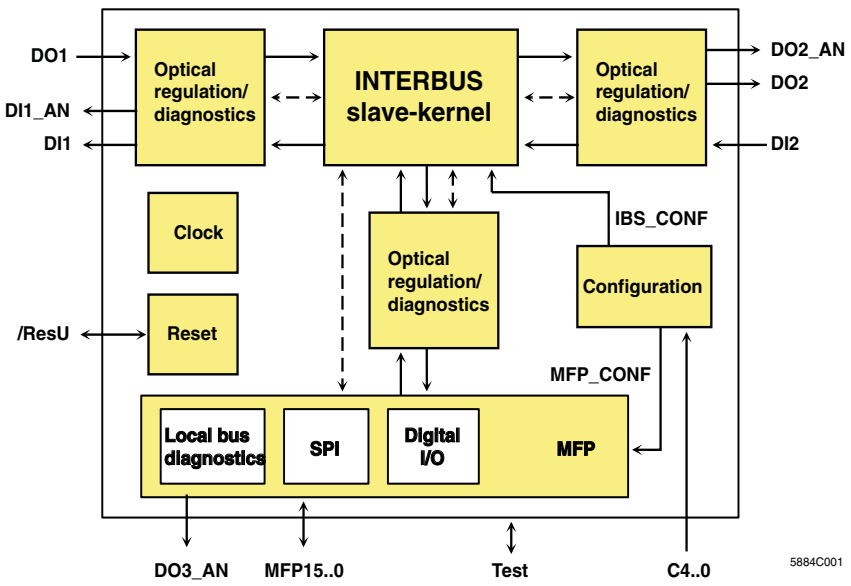


Figure 1-1 Block diagram of the SUPI 3 OPC

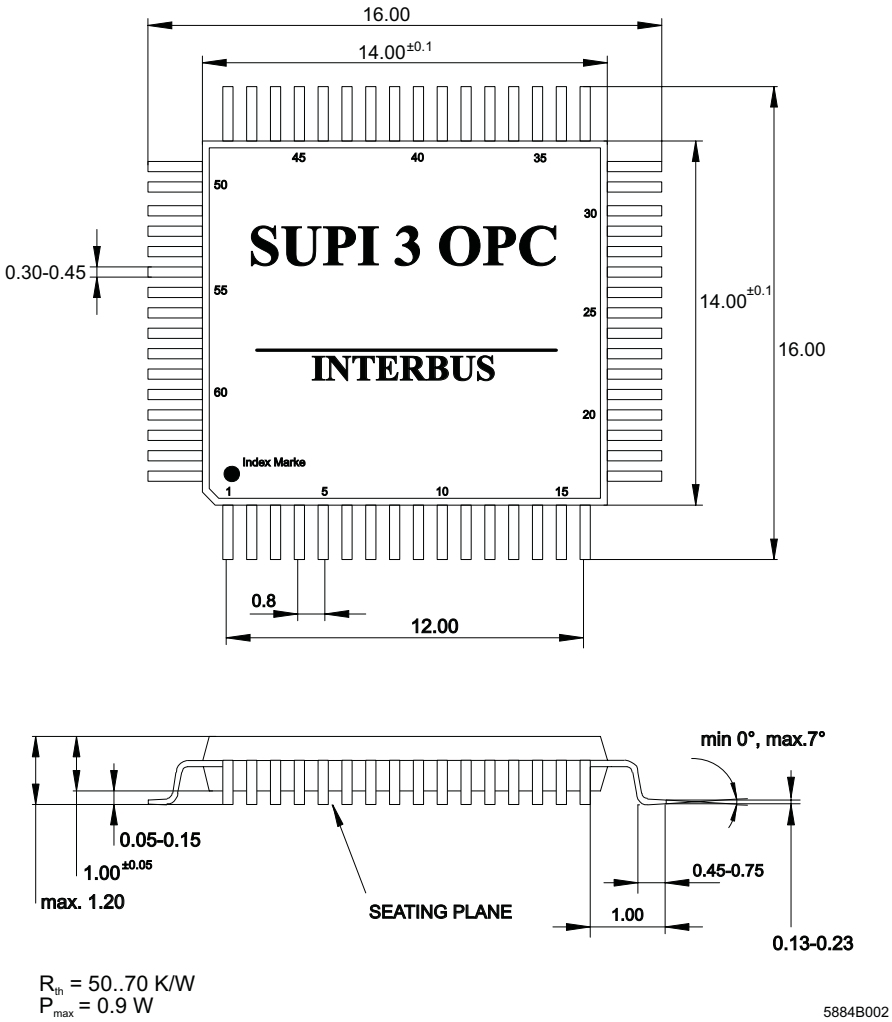
1.4 Housing type

The SUPI 3 OPC is available in housing versions TQFP 64 and TQFP 44.

For optical power regulation, SUPI 3 OPC/SUPI 3 OPC T&R (both housing type TQFP 64 (with slug)) must be used, because the power drivers for optical regulation are integrated into this housing. Because the SUPI 3 LS (housing type TQFP 44) has a reduced number of pins it **cannot** be expanded with additional data registers and is **only** suitable for copper interfaces.

The TQFP 64 housing should be connected to the printed circuit board for the removal of heat. Layout notes can be found in Section 1.4.2 "Cooling surface (slug)".

1.4.1 TQFP 64 housing (Thin Quad Flat Pack)



R_{th} = 50..70 K/W
P_{max} = 0.9 W

5884B002

Figure 1-2 TQFP 64 housing (all dimensions in mm)

1.4.2 Cooling surface (slug)

The TQFP 64 housing has a metal cooling surface on the back to improve its thermal properties. To ensure the optimum removal of heat, the cooling surface must be connected to a grounding surface. The contacts should be made according to the diagrams below.

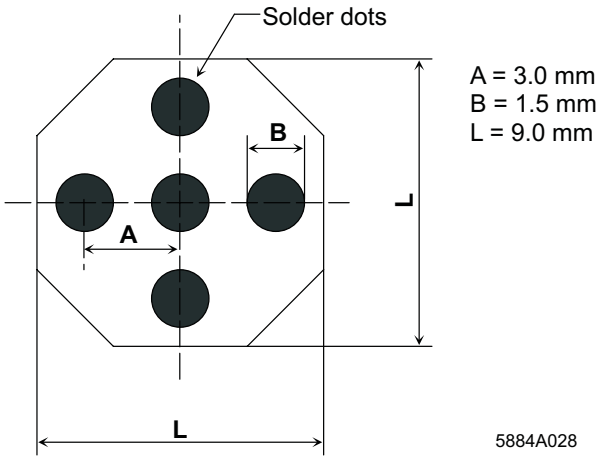


Figure 1-3 Contacts for the cooling surface

If a printed circuit board with grounding layer is used, it is recommended to provide approximately 15-20 through-contacts on the copper surface. An example is given in Figure 1-4.

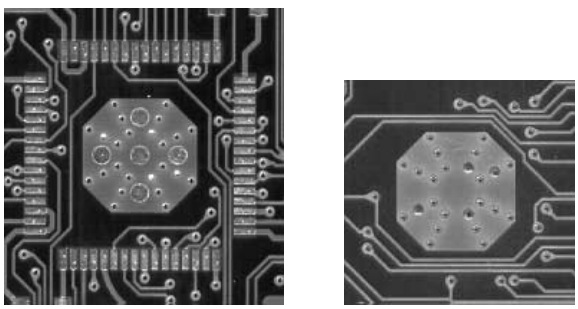


Figure 1-4 Layout example for TQFP 64 with cooling surface

1.4.3 TQFP 44 housing (Thin Quad Flat Pack)

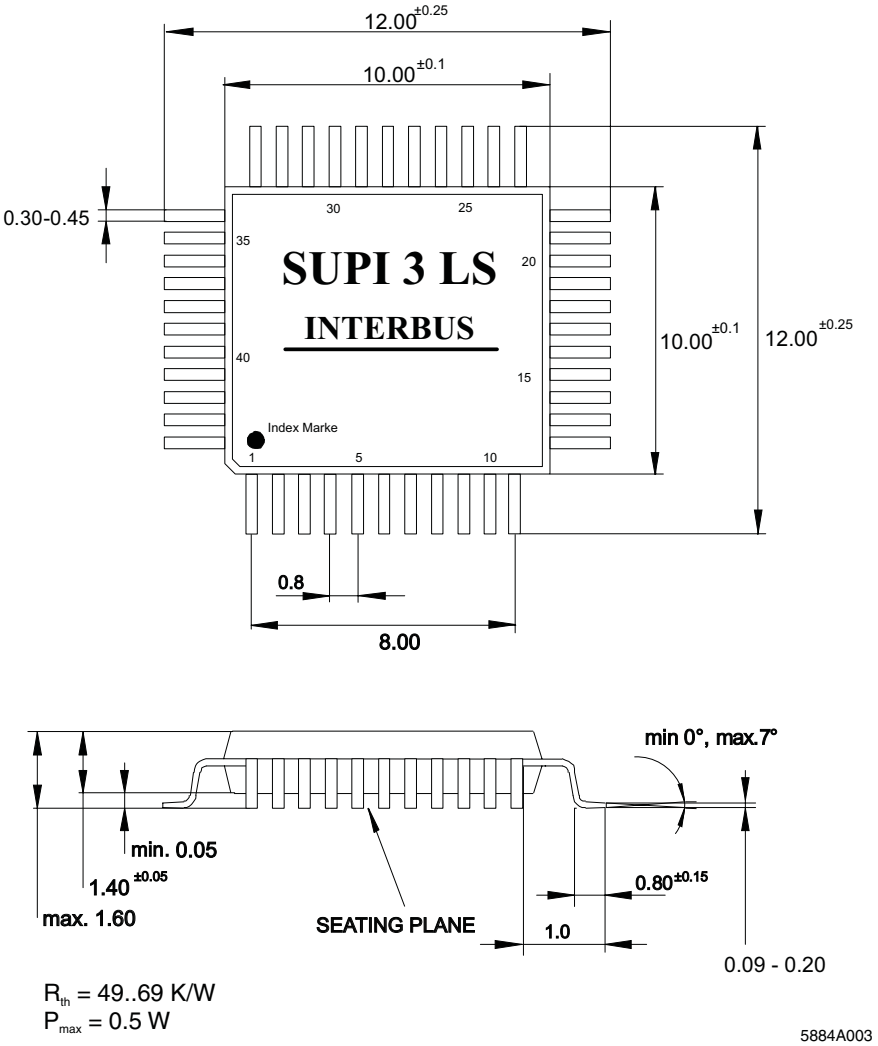


Figure 1-5 TQFP 44 housing (all dimensions in mm)

1.4.4 Pin boards

TQFP 64 pin board

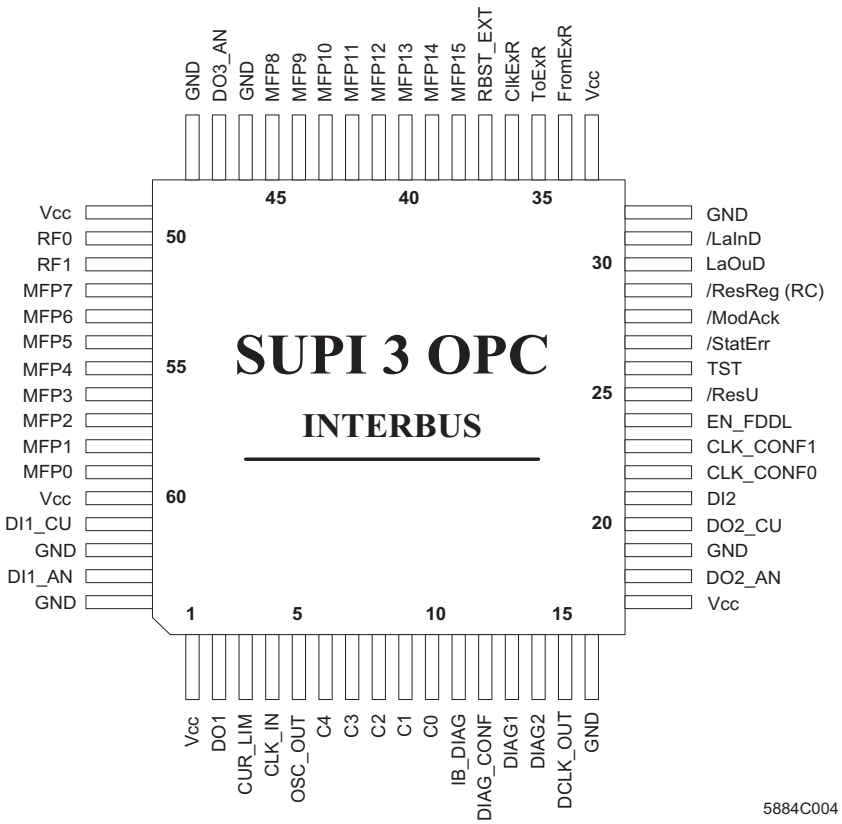


Figure 1-6 TQFP 64 housing with pin assignment (SUPI 3 OPC/SUPI 3 OPC T&R)

Table 1-2 TQFP 64 pin table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{cc}	23	CLK_CONF1	45	MFP8
2	DO1	24	EN_FDDL	46	GND
3	CUR_LIM	25	/ResU	47	DO3_AN
4	CLK_IN	26	TST	48	GND
5	OSC_OUT	27	/StatErr	49	V_{cc}
6	C4	28	/ModAck	50	RF0
7	C3	29	/ResReg (RC)	51	RF1
8	C2	30	LaOuD	52	MFP7
9	C1	31	/LaInD	53	MFP6
10	C0	32	GND	54	MFP5
11	IB_DIAG	33	V_{cc}	55	MFP4

Table 1-2 TQFP 64 pin table (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
12	DIAG_CONF	34	FromExR	56	MFP3
13	DIAG1	35	ToExR	57	MFP2
14	DIAG2	36	ClkExR	58	MFP1
15	DCLK_OUT	37	RBST_EXT	59	MFP0
16	GND	38	MFP15	60	V_{cc}
17	V_{cc}	39	MFP14	61	DI1_CU
18	DO2_AN	40	MFP13	62	GND
19	GND	41	MFP12	63	DI1_AN
20	DO2_CU	42	MFP11	64	GND
21	DI2	43	MFP10		
22	CLK_CONF0	44	MFP9		

TQFP 44 pin board

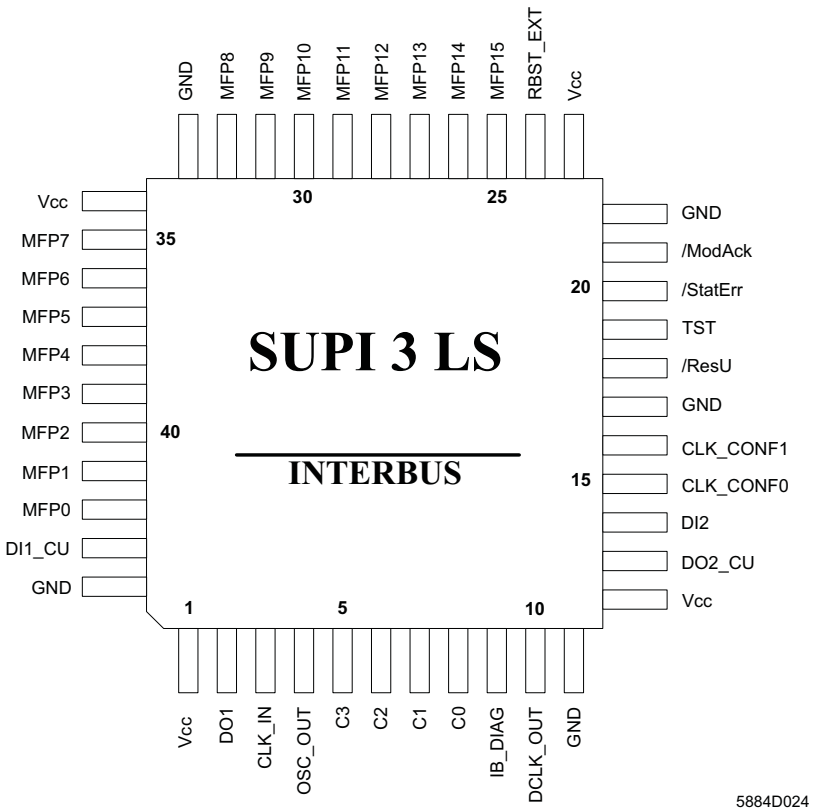


Figure 1-7 TQFP 44 housing with pin assignment (SUPI 3 LS)

Table 1-3 TQFP 44 pin table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{cc}	16	CLK_CONF1	31	MFP9
2	DO1	17	GND	32	MFP8
3	CLK_IN	18	/ResU	33	GND
4	OSC_OUT	19	TST	34	V_{cc}
5	C3	20	/StatErr	35	MFP7
6	C2	21	/ModAck	36	MFP6
7	C1	22	GND	37	MFP5
8	C0	23	V_{cc}	38	MFP4
9	IB_DIAG	24	RBST_EXT	39	MFP3
10	DCLK_OUT	25	MFP15	40	MFP2
11	GND	26	MFP14	41	MFP1
12	V_{cc}	27	MFP13	42	MFP0
13	DO2_CU	28	MFP12	43	DI1_CU
14	DI2	29	MFP11	44	GND
15	CLK_CONF0	30	MFP10		

1.5 Pin description

Table 1-4 Pin description (SUPI 3 OPC (T&R)/SUPI 3 LS)

Designation	Meaning	Type	TQFP 64	TQFP 44
CLK_IN	Oscillator input	CI	X	X
OSC_OUT	Oscillator output	OSC	X	X
DCLK_OUT	Data clock output (500 kbps/2 Mbps)	B8	X	X
CLK_CONF[1..0]	PLL/clock cell configuration	CI	X	X
C4	Operating mode configuration	CIp	X	–
C[3..0]	Operating mode configuration	CI	X	X
RF[1..0]	Optical regulation configuration	CIp	X	–
RBST_EXT	Optical regulation configuration (or alarm input if an outgoing interface is used)	STC	X	X
MFP[15..0]	Multi-function pins	BD4	X	X
	INTERBUS ring data line			
DO1	Input: Data line OUT forward	STC	X	X

Table 1-4 Pin description (SUPI 3 OPC (T&R)/SUPI 3 LS) (continued)

Designation	Meaning	Type	TQFP 64	TQFP 44
DI1_CU	Output: Data line OUT digital return for copper	B4	X	X
DI1_AN	Output: Data line OUT analog return for optical fiber	AN60	X	–
DI2	Input: Data line IN return	STC	X	X
DO2_CU	Output: Data line OUT digital forward for copper	B4	X	X
DO2_AN	Output: Data line OUT analog forward for optical fiber	AN60	X	–
DO3_AN	Output: Data line OUT analog forward branch for optical fiber	AN60	X	–
	Signals for external register expansion			
/LaInD	Latch signal for input data	B4	X	–
LaOuD	Latch signal for output data	B4	X	–
ClkExR	Clock for external data registers	B4	X	–
ToExR	Data output for external data registers **without** internal SUPI 3 OPC registers	B2	X	–
FromExR	Data input for external data registers	STC	X	–
	Diagnostics			
/StatErr	"Module error" alarm input	STCp	X	X
/ModAck	Acknowledgment output for detected module error	B2	X	X
/ResReg (RC)	Reset external register (or RC LED)	B4	X	–
DIAG_CONF	Configuration of diagnostic outputs	CIp	X	–
DIAG1	"BA" or "FO1 IN" alarm output	B4	X	–
DIAG2	"RBDA" or "FO2 OUT" alarm output	B4	X	–
IB_DIAG	Diagnostic output (limited)	B4	X	X
CUR_LIM	Control current setting	PAS	X	–
TST	Test input, hard-wire to GND	CI	X	X
EN_FDDL	Reserved, hard-wire to GND	CI	X	–
/ResU	Initialization reset (input **and** output)	OD8	X	X
V_{cc}	Voltage supply +5 V		X	X
GND	Ground		X	X

Cell types

CI: CMOS input
CIp: CMOS input with pull-up
STC: CMOS Schmitt trigger input
STCp: CMOS Schmitt trigger input with pull-up

B2:	Driver output 2 mA
B4:	Driver output 4 mA
B8:	Driver output 8 mA
BD4:	Bidirectional with TTL Schmitt trigger input without pull-up and 4 mA driver output
AN60:	DAC current output 60 mA
OD8:	8 mA open drain output
OSC:	Oscillator cell output
PAS:	Passive external components

1.6 Optical regulation (SUPI 3 OPC (T&R) only)

SUPI 3 LS does not support optical regulation.

The SUPI 3 OPC offers a high level of operational safety and diagnostic capability for optical signal transmission compared with the IBS SUPI 3. The control systems and procedures required are described in the following section.

The scope of functions for "optical regulation" includes automatic interface recognition, initialization, and online regulation.

Parameter variations in the fiber optic transmitters are automatically corrected in certain areas. This improves the performance of the system (longer distances) because it adapts to the actual (typical) and not the worst case component characteristics. To simplify configuration and diagnostics, the measured distances, the current power level and the enable status of the regulation can be transmitted to the master via the internal diagnostics and report manager in the SUPI 3 OPC.

Transmission power of the fiber optic components is adjusted to a set value by the device manufacturer to ensure compatibility with earlier SUPI 3 devices, and in no circumstances should the receiver be overcontrolled.

Online regulation

Online regulation adapts the transmission power to modifications in the transmission characteristics and ensures an adjustable system reserve of 3dB. The transmission characteristics may change during operation due to aging and temperature change in the transmission/reception element and fibers, and due to mechanical load (bending, tensile load) on the fibers.

Behavior on a reset

An INTERBUS reset it detected in the ASIC core. When a reset is detected, regulation is reset for the reset period. Once the INTERBUS reset has been canceled, automatic interface recognition is carried out. Initialization then starts in optical power regulation mode. During interface recognition and initialization the protocol core remains the reset state. Automatic interface recognition is always carried out at the end of an INTERBUS reset if *RF[1..0]* ≠ "10".

1.6.1 Initializing optical regulation

During initialization (6 ms, maximum), the transmission power of the optical interface is adapted to the characteristics of the transmission path present in the application (transmitter → fiber optic → receiver). In addition, the initialization determines whether the subsequent device also supports the optical regulation or diagnostic function. If the initialization sequence fails, the device is operated as a device without optical regulation, i.e., via an adjusted transmitter with maximum power for fiber optic transmission.

The following section details the mechanisms used to evaluate the signal received (which also apply for online regulation), and describes the initialization sequence. The path is only initialized if optical regulation operating mode is selected using *RF[1..0]* and the corresponding interface is a remote bus interface. The initialization result can be illustrated by a diagnostic LED for each interface if the diagnostic outputs are configured correspondingly (see Table 3-17 on page 3-34).

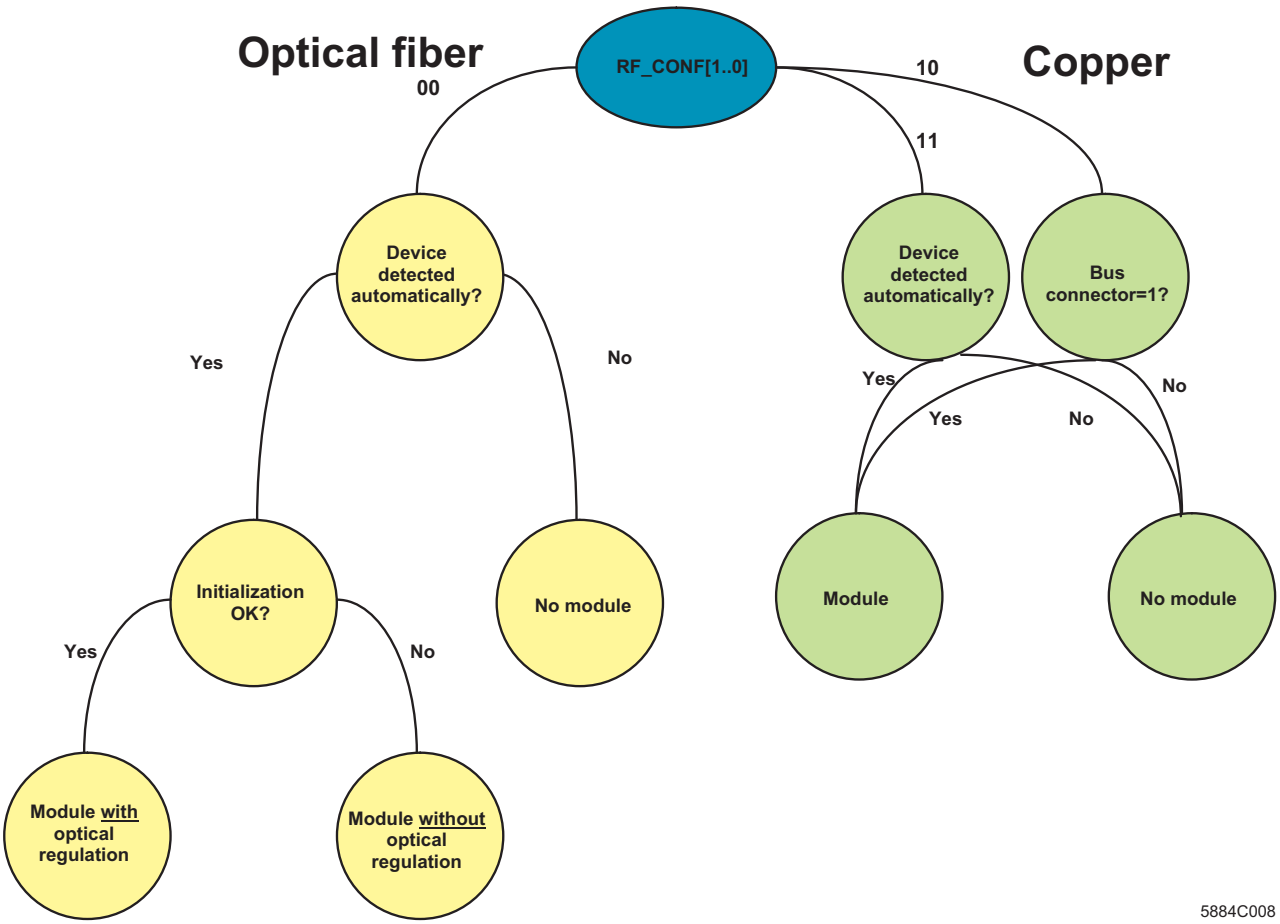


Figure 1-8 Interface recognition in optical regulation mode

The SUPI 3 OPC can correctly decode a bit using the signal distortion[1] shown in Figure 1-9. Clock deviation over 13 bits must be within the range 500 kbps ±0.1% or 2 Mbps ±0.1%.

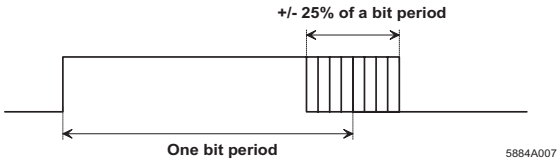


Figure 1-9 Time response of the MDS[2] sublayer

Initialization control

After a reset (power-up or INTERBUS reset) and automatic interface recognition, initialization automatically determines whether the corresponding interface is connected to a regulated or unregulated interface in the subsequent device (device detection without optical regulation).

If the interface is connected to a regulated interface, optical power of the interface is set to a power minimum with a defined reserve and distortion is checked. A regulation pattern is retransmitted, the regulation response from the other device is evaluated and, if necessary, transmission power is reduced.

Initialization is terminated:

– If the maximum number of regulation procedures is reached (13) or
– If the critical power level is only just ensured on a permissible distortion

The maximum possible number of regulations procedures is determined by the number of power levels. The maximum possible number of regulations procedures is determined by the precision of initialization. Initialization has 15 power levels.

After power-up or an INTERBUS reset, the transmitter for the incoming interface transmits the *"Light on"* signal and thus starts the initialization process in the outgoing interface of the previous device. Due to its location the outgoing interface is always the first transmitter. Transmission power for the outgoing interface is then reduced until the receiver for the outgoing interface receives the first negative regulation response. Transmission power is then increased by one and started up.

The *"Light off"* signal corresponds to the regulation response "Pattern detected", and the *"Light on"* signal corresponds to the regulation response "Pattern not detected". After successful initialization of the outgoing interface, the regulation direction changes, i.e. the transmitter for the incoming interface on the subsequent device is regulated in the same way.

Initialization starts once the end of the INTERBUS reset has been detected on the incoming interface. It leads to the cancellation of the INTERBUS reset on the outgoing interface or on the branch through telegrams. INTERBUS devices can only be switched off by the master after the maximum initialization period (6 ms) i.e., transmission power is adapted to the path characteristics.

[1] All amounts which are caused by sampling errors, distortions due to time recovery components, pulse width distortions due to optical components (transmitter, receiver, and fiber), distortions due to electronics, jitter, etc.

[2] **M**edium **D**ependent **S**ublayer

In addition, during initialization the length of the optical path is determined by a runtime measurement. This enables the detection of fiber optic cables, which are too long. During initialization, the time from the transmission of the first status telegram to the receipt of a positive response (logical 0 level) is measured using a timer. Using the clock frequency and the known runtime of the light in the medium, the distance can be calculated from the timer result using the following formula:

$$L = n \cdot \frac{1}{f \cdot t}$$

Where:

L: Length (forward and return)
n: Timer result
f: Clock at e.g., 500 kB (= 8 MHz)
t: 5 ns/m (runtime constant)

Table 1-5 Length of the transmission path

Path length	Resolution	Value range	INTERBUS
0 m to 400 m	24 m (...48 m), typical	0 to 62	500 kbaud
400 m to 20 km	–	63	500 kbaud
0 m to 400 m	6 m (...12 m), typical	0 to 62	2 Mbytes
400 m to 20 km	–	63	2 Mbytes

The typical resolution of the cable length for the fibers used at a transmission speed of 500 kbaud is 24 m (the worst case is 48 m) for fiber distances of up to 400 m (in each direction). For greater fiber distances (HCS and glass systems) the indicator is > 400 m. The worst case resolution of 48 m occurs in systems with a synchronous clock, where the clock system has no phase shift. The INTERBUS master can read the cable lengths from the chip.

If the interface cannot be initialized in optical regulation mode, all regulation mechanisms are deactivated.

1.6.2 Online regulation

After successful initialization (power set, distortion OK) online regulation is enabled. During initialization, the distance is determined for the outgoing interface or for the branch and this information is made available in the internal diagnostics and report manager. The enable status of the regulation function for each interface is also given in the chip for the master.

Optical fiber path regulation is used as the "optical power regulation" for the transmitter. Additional information for optical fiber path regulation is transmitted during data transmission within the INTERBUS protocol.

Optical power regulation

During data transmission, the path characteristics are monitored and, if necessary, the power is adapted to the modified path characteristics (online regulation).

If the system reserves are too low, this is signaled by an MAU warning, which prompts you to check the path or the cable **prior to** a system failure. Additional information can be found in Section 3.6, "Diagnostics". Errors are indicated centrally through the transmission of the error message to the INTERBUS protocol using the diagnostics and report manager and through diagnostic LEDs *FO1* and *FO2*.

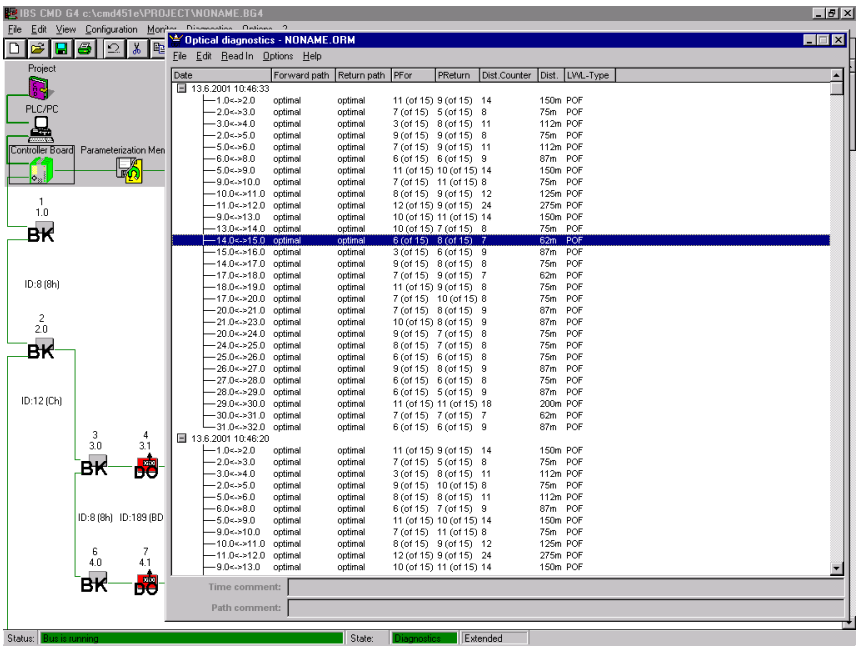


Figure 1-10 Optical path diagnostics (e.g., in CMD 4.50)

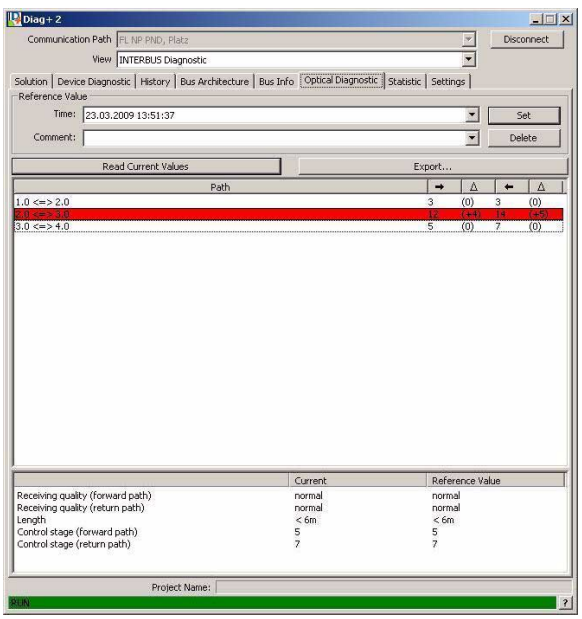


Figure 1-11 Optical path diagnostics (e.g., in Diag+)

The aim of online regulation is to set the power to a minimum value. At this value transmission with the defined system reserve is ensured. This also applies to short-term modifications in path characteristics with permissible distortions.

Online regulation has 15 power levels. The test over two levels can offer a higher level of system safety because it provides an additional reserve for short-term modifications. The reduction for the second test is one power level higher. The set reduction for the first test corresponds to the system reserve for online regulation.

Online regulation operates as 3-point regulation, i.e, when the minimum permissible transmission power is reached, it remains constant. Transmission power is increased as soon as a negative acknowledgment is received on a reduction of one power level. If a reduction by one power level is acknowledged positively and a reduction by two power levels is acknowledged negatively, the power remains unchanged. If the acknowledgment is positive for both reduction levels, the power is reduced by one level.

Operating behavior can be illustrated using two examples.

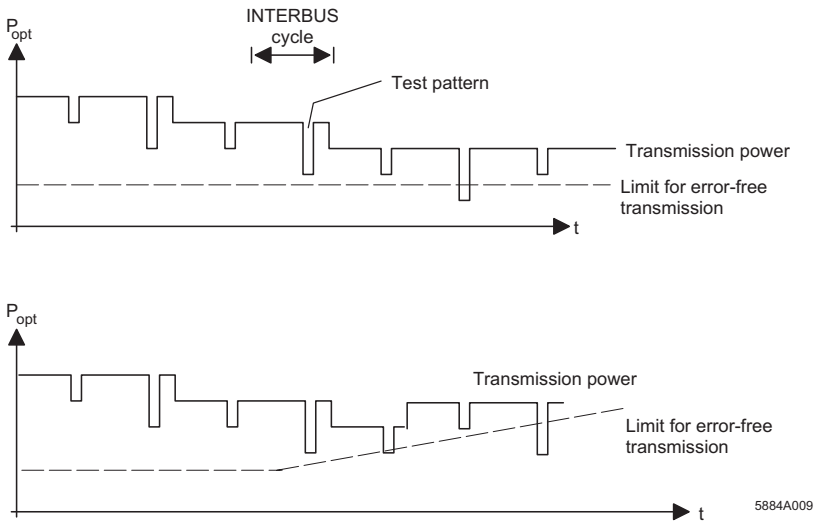


Figure 1-12 Example sequence for the transmission power

The upper diagram shows the transmission power sequence with a constant power limit. Once the power limit is reached, the power is constant.

The lower diagram shows the transmission power sequence with a modification to the power limit. The minimum rise time for the transmission power is given by the repeat frequency of the regulation. This largely depends on the number of devices on the bus and corresponds to twice the cycle time. Due to the repeat frequency, the regulation can only compensate for gradual modifications to the path characteristics, e.g., temperature drift and aging effects on the components.

It can be seen that a power increase when transmission quality deteriorates is faster than the power reduction when transmission quality improves.

Optical diagnostics

Alternatively, the SUPI 3 OPC can be operated with optical power diagnostics. With optical power diagnostics only the characteristics of the transmission medium are tested. The principle for power reduction is only used with a set transmission power to detect the point at which the power reserve falls below the limit. In this case an MAU warning is generated, which is assigned to the incoming interface of the corresponding device.

1.6.3 MAU warnings

There are three active high MAU[1] inputs, however, they are not available as pins to the user (automatic internal detection):

– MAUWH - Incoming INTERBUS interface
– MAUWR - Outgoing INTERBUS interface
– MAUWS - Branch interface (for bus terminal modules only)

The protocol chip can use these inputs to indicate to the master that the transmission quality of, for example, optical paths has fallen to a critical but still operational level. The SUPI 3 OPC is able to evaluate the reception quality of the MAU for the corresponding interface (incoming, outgoing or branch) and to make this available to the appropriate input as a digital signal. Setting this input generates an appropriate message at the bus master. This function is supported by firmware version 4.0.x or later.

During optical power regulation, a critical power reserve, at which transmission is still error-free but may be with damaged system reserves, is indicated in the MAU warning bits. Basically this means that transmission power cannot be increased any further. An appropriate hysteresis is implemented to ensure that the MAU warning bit does not change constantly at the threshold.

If only one reduced power reserve is available for the online regulation of the highest possible output power, i.e., at "MAX" power level the set reserve is not ensured, the diagnostic status MAU_WARNING is generated. An appropriate message is triggered on the INTERBUS master by the chip. When the MAU_WARNING status is activated on the transition of the transmission power MAX-1 → MAX and deactivated on the transition MAX-1 → MAX-2, a hysteresis occurs which prevents the repeated display of a MAU_WARNING without the return of the power to the saved operating range.

The current power value is made available by the chip in its registers. In optical power regulation mode the MAU_WARNING diagnostic status and the MAU_WARNING_EVENT diagnostic event are assigned to the transmitting interface. The MAU_WARNING state is reported to the INTERBUS master by the protocol chip.

[1] **M**edium **A**ttachment **U**nit

1.7 Basic wiring

1.7.1 Clock supply

The SUPI 3 OPC/SUPI 3 LS has an internal clock generator. It provides a simple means of implementing the required clock supply. All that is required is a 32 MHz quartz crystal for a quartz oscillator.

The clock signal is generated by the oscillator cell. The clock frequency depends on the frequency of the external quartz crystal. A quartz crystal or a quartz oscillator can be used, as shown in Figure 1-13. A quartz oscillator should be connected to *CLK_IN*, which acts as a CMOS input buffer. An alternative solution is to directly connect a 32 MHz quartz crystal, without additional external components, to *CLK_IN* and *OSC_OUT* (see Table 1-8). The Π filter network required for clock generation is already present in the ASIC.

With this clock no other components can be operated when a quartz crystal is used.

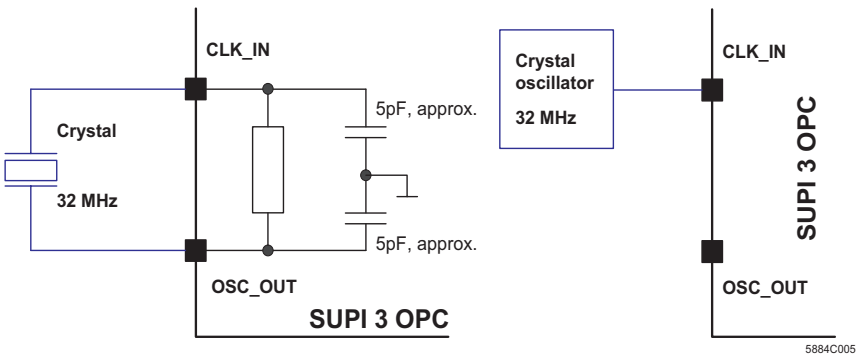


Figure 1-13 Clock supply for the SUPI 3 OPC/SUPI 3 LS

The tolerance of the quartz crystal or the oscillator must not exceed ***f = 32 MHz ±100 ppm***.

The following applies for the clock supply: Pulse duty factor: 50% ±10% duty cycles.

The permissible deviation applies to both the short-time as well as the long-time stability.

Pulse duty factor for the clock supply of INTERBUS protocol chips

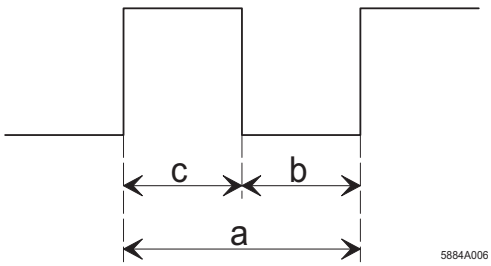


Figure 1-14 Pulse duty factor

Table 1-6 Clock timing

Designation	Name	Symbol	Min.	Type	Max.	Unit
a	Clock period	t_c	31.25 -3.125	31.25	31.25 +3.125	ns ps
b	Pulse width high	t_{pH}	12.5	15.625	18.75	ns
c	Pulse width low	t_{pL}	12.5	15.625	18.75	ns

The clock supply and INTERBUS transmission speed are configured using pins *CLK_CONF[1..0]*, as shown in the following table.

Table 1-7 Configuration of the transmission speed

CLK_CONF1	CLK_CONF0	Clock source	Data rate
0	1	Quartz, 32 MHz	500 kbps
1	1	Quartz, 32 MHz	2 Mbps
X	0	Reserved	

The following table lists suitable quartz crystals and quartz oscillators.

Table 1-8 Clock supply components

Manufacturer	Type	f	Temperature
Quartz			
Nippon	SXN-A	32 MHz	-40°C to +85°C
Hokuriku	SX-6B	32 MHz	-40°C to +85°C
Quartz oscillator			
Nippon	NMSOHR	32 MHz	-40°C to +85°C
Kinseki	FXO-31FH	32 MHz	-40°C to +85°C
	FXO-31FT	32 MHz	-40°C to +85°C
Hokuriku	KCO-765	32 MHz	-40°C to +85°C

1.7.2 Initializing the chip

The SUPI 3 OPC/SUPI 3 LS has an internal reset unit (Figure 1-15), which contains a voltage monitor and a clock monitor.

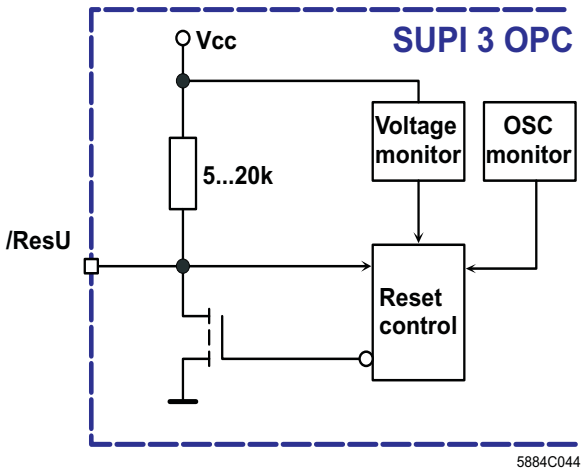


Figure 1-15 Structure of an internal reset cell (SUPI 3 OPC/SUPI 3 LS)

The voltage monitor is directly connected to the ASIC power supply. The internal voltage monitor generates a high signal if the voltage exceeds 4.5 V and a low signal if the voltage falls below 3.9 V. The reset time generated is at least 4 µs. If just the internal reset monitor is to be activated, only a 10 kΩ pull-up needs to be connected at */ResU*.

NOTE: The rise time for the supply voltage 0 through +5 V must be less than 100 µs, as this could otherwise damage the analog data outputs of the SUPI 3 OPC**.**

Externally, the active low bidirectional reset pin */ResU* is brought out. As long as the pin is at a low potential, the internal reset is active. The internal reset only becomes active if the lower voltage threshold is passed **and** the clock supply is stable. The */ResU* signal can also be used to reset other components with the same potential. The output has a current sink of up to a maximum of 8 mA. Internally, the pin has a pull-up resistor (5 to 20 kΩ) and filtering against malfunctions (spikes).

If the reset pin is used as an input, a current of 1 mA is required in the ASIC. In the SUPI 3 OPC/SUPI 3 LS it acts as an "open collector" output stage so that an external voltage monitor must either have an "open collector" output or a resistor for current limitation in the reset path. An application example is given in Figure 1-16.

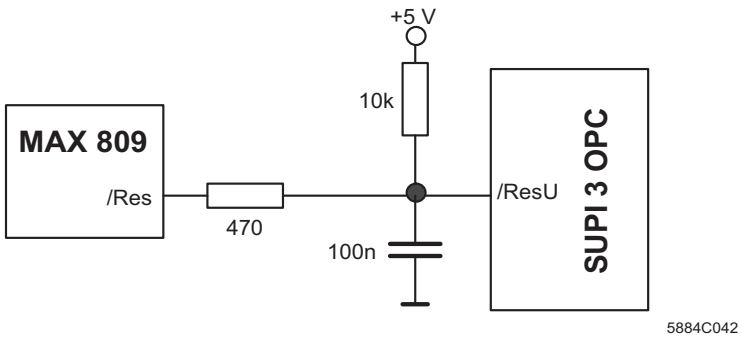


Figure 1-16 SUPI 3 OPC/SUPI 3 LS with external reset block

2 INTERBUS interfaces

2.1 Overview

The SUPI 3 OPC chip features three INTERBUS interfaces which can be used simultaneously. They are divided into one incoming and two outgoing interfaces. Each interface has a receive data line and a send data line. In the case of an outgoing interface there is also an alarm input, which indicates the assignment of this interface (RBST_EXT for the first, LBST (= MFP11) for the second interface).

The SUPI 3 LS chip features two INTERBUS interfaces which can be used simultaneously. They are divided into one incoming and one outgoing interface. Each interface has a receive data line and a send data line. In the case of an outgoing interface there is also an alarm input, which indicates the assignment of this interface (RBST_EXT).

The interfaces can be set using configuration pins *RF[1..0]* and *C[4..0]*. Further details on possible configurations can be found in this section.

INTERBUS interfaces and the application interface for the SUPI 3 OPC are configured using pins *C[4..0]* and *MFP[15..12]*. The following operating modes can be set:

Table 2-1 SUPI 3 OPC/SUPI 3 LS operating modes

INTERBUS interface
Remote bus (RB)
Local bus (LB) with return (MR)
Local bus (LB) without return (OR)
MFP interface
Bus terminal module
Digital I/O
Serial µP interface
Serial SPI interface
Serial register expansion

The **M**ulti-**F**unction **P**in interface *(MFP[15..0])* has 16 bidirectional I/O pins which are statically set to the IN or OUT direction depending on the MFP mode.

The MFP interface is the configurable user interface for the protocol chip. It is set using signals *C[4..0]*. A detailed overview of possible configurations is given in Section 3, "Application interface".

NOTE: MFP pins, which are not assigned any function (no signal) during configuration are connected as **inputs**. They should therefore be connected to GND.

In order to reduce the pins required for the ID code, configurations pins *C[4..0]* must be mapped internally to the complete 16-bit ID code (see also the SUPI 3 user manual IBS SUPI 3 UM E).

2.1.1 Bus connector recognition and regulation function

The SUPI 3 OPC/SUPI 3 LS supports automatic bus connector recognition (BST). Configuration pins *RF[1..0]* can be used to set various operating modes. The external input signals RBST (*RBST_EXT*) and LBST (*MPF11*) recognized by SUPI 3 are only required in *RF[1..0]=10* mode (copper, no automatic recognition). In all other operating modes the interfaces are recognized automatically by internal monitoring, i.e., the control signal required is automatically generated. The setting is made using the signals given in the table.

Table 2-2 Bus connector recognition and regulation function

RF1	RF0	RBST_EXT	Function
1	0	Controlled	Bus connector recognition via pin
1	1	0	Automatic bus connector recognition, only copper interface; bit distortion monitoring
0	0	0	Automatic bus connector recognition, regulation function with 3 dB power reserve, fiber optic interface only; bit distortion monitoring

Automatic bus connector recognition (*RF1*=1, *RF0*=1) should always be selected for new copper interface developments.

Automatic bus connector recognition works with all INTERBUS devices that have an INTERBUS protocol chip SUPI 2 or later, when they follow after the SUPI 3 OPC/SUPI 3 LS in the INTERBUS topology.

2.1.2 Setting the optical fiber transmitter current

Not supported by SUPI 3 LS.

The SUPI 3 OPC can be used to limit or preset all implemented fiber optic transmitters with a reference resistor at pin *CUR_LIM*. This means that the SUPI 3 OPC can counteract any fiber optic transmission modifications caused by aging and temperature fluctuations using its regulation functions.

The reference resistor can be designed in various forms: For example as a discrete potentiometer, a programmable resistor array, an individual resistor or a resistor network with solder bridges. The reference resistor must have a maximum resistor value of 2.4 KΩ and a minimum resistor value of 1.2 KΩ. The voltage at this pin is 1.2 V.

The value to be set is determined during transmitter compensation. The procedure for compensation is detailed in the document "Optical_Transmission_Technology_V2.pdf". This document can be found on the Internet at www.interbusclub.com.

A suitable increment is required when increasing or decreasing the light output. A compromise must be found between the lowest possible light output increment and low effort on the resistor network. Because the maximum resistor value of 2.4 kΩ must not be exceeded, 2.4 kΩ is hard-wired as the first resistor value. All additional resistors for reducing the value are connected in parallel using soldering bridges (LB 1..5).

One possible implementation provides a network with a total of six resistors and a maximum light output increment of 0.3 dB. The resistor values can be found in Table 2-3.

Table 2-3 Resistor values for the reference network to *CUR_LIM*

Resistor	Value
R1	**2.4 kΩ**
R2	**3.9 kΩ**
R3	**7.5 kΩ**
R4	**15 kΩ**
R5	**33 kΩ**
R6	**56 kΩ**

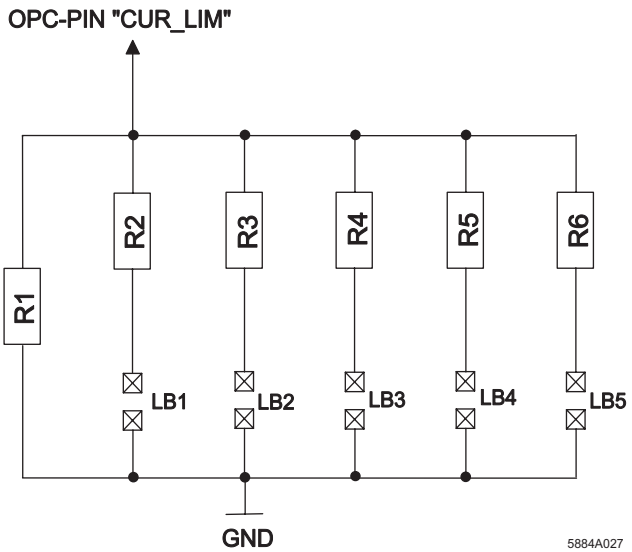


Figure 2-1 Reference network for the transmitter current

With copper applications, a resistor of 1**k**Ω after +5 V should be connected to *CUR_LIM*.

2.2 Local bus devices

Local bus devices are units within a limited space, which are often supplied with power centrally from a bus terminal module. Several local bus devices can be grouped together to form logical groups. These groups can only be isolated and disconnected from the remote bus as a unit. They differ from remote bus devices in their interface switching behavior. The SUPI 3 OPC/SUPI 3 LS chip divides the local bus operating modes into the number of active interfaces and support of device-oriented local bus diagnostics.

Local bus devices with SUPI 3 OPC or SUPI 3 LS include versions with/without device-oriented local bus diagnostics. Mixed operation is not permitted. A distinction is also made between devices with (MR; e.g., IBS Inline) and without return (OR; e.g., IBS Loop 2). In the event of an error, devices with device-orientated local bus diagnostics can send diagnostic information to the SUPI 3 OPC of the previous bus terminal module. The INTERBUS master can then retrieve this data.

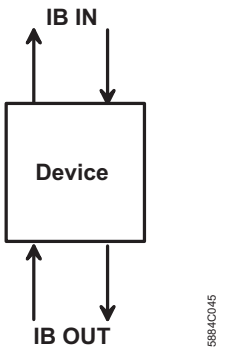


Figure 2-2 INTERBUS device with two interfaces (MR)

2.2.1 Local bus without device-oriented diagnostics

This operating mode corresponds to the function of the IBS SUPI 3. It is used to implement INTERBUS devices with return (MR). This mode should no longer be used for new developments.

Table 2-4 Local bus operating modes without device-oriented diagnostics

C4*	C3	C2	C1	C0	MFP				Data length†	ID code	Function
					15	14	13	12	(ID 12..8)	(Hex)	
0	1	0	0	0	See Table 3-2				0 1 0 0 1	BF	LB-MR, 8 IN/OUT
0	1	0	0	1	See Table 3-2				0 0 0 0 1	BE	LB-MR, 16 IN
0	1	0	1	0	See Table 3-2				0 0 0 0 1	BD	LB-MR, 16 OUT
0	1	0	1	1	0	0	0	0	0 1 1 0 1	BF	LB-MR, 2 IN/OUT
0	1	0	1	1	0	0	0	1	0 1 1 0 1	BE	LB-MR, 2 IN
0	1	0	1	1	0	0	1	0	0 1 1 0 1	BD	LB-MR, 2 OUT
0	1	0	1	1	0	0	1	1	0 1 0 0 0	BF	LB-MR, 4 IN/OUT
0	1	0	1	1	0	1	0	0	0 1 0 0 0	BE	LB-MR, 4 IN
0	1	0	1	1	0	1	0	1	0 1 0 0 0	BD	LB-MR, 4 OUT

Table 2-4 Local bus operating modes without device-oriented diagnostics (continued)

C4*	C3	C2	C1	C0	MFP				Data length†	ID code	Function
					15	14	13	12	(ID 12..8)	(Hex)	
0	1	0	1	1	0	1	1	0	0 1 0 0 1	BE	LB-MR, 8 IN
0	1	0	1	1	0	1	1	1	0 1 0 0 1	BD	LB-MR, 8 OUT
0	1	0	1	1	1	0	0	0	0 0 0 0 1	7F	LB-MR, SPI 16 IN/OUT
0	1	0	1	1	1	0	0	1	0 0 0 0 1	7D	LB-MR, SPI 16 OUT
0	1	0	1	1	1	0	1	0	0 0 0 0 1	7E	LB-MR, SPI 16 IN
0	1	0	1	1	1	0	1	1	0 0 0 1 0	7F	LB-MR, SPI 32 IN/OUT
0	1	0	1	1	1	1	0	0	0 0 0 1 0	7E	LB-MR, SPI 32 IN
0	1	0	1	1	1	1	0	1	0 0 0 1 0	7D	LB-MR, SPI 32 OUT
0	1	0	1	1	1	1	1	0	0 0 0 0 0	78	LB-MR, Init-µP

* Set to "1" for SUPI 3 LS and cannot be configured

† For decoding (actual data lengths) see Table 3-11

Abbreviations:

LB: Local bus without device-oriented local bus diagnostics
MR: With return
SPI: SPI master
Init-µP: SPI slave or synchronous serial Intel interface

2.2.2 Local bus with device-oriented diagnostics

This operating mode also offers device-oriented local bus diagnostics. It is used to implement 2-wire local bus devices, e.g., INTERBUS Inline.

The SUPI 3 OPC/SUPI 3 LS enables easy error localization on the local bus. Device-oriented local bus diagnostics detects the precise fault location of a physical interrupt in a local bus segment. A physical interrupt is, for instance, a cut through bus cable or the total failure of a device.

In local bus segments the ring system must not be implemented within a cable line. To locate an interrupt in this type of segment the number of devices behind the error location are detected. A counter is used which, with the aid of a telegram (the diagnostic telegram), moves round the data path behind the error location and is incremented in each device.

On the basis of this information, the INTERBUS master uses the stored configuration to determine and display the damaged transmission path. When local bus diagnostics are used in local bus segments with return line, the counter is incremented within one module on both the data forward line and the looped return line.

Table 2-5 Local bus operating modes with device-oriented diagnostics

C4*	C3	C2	C1	C0	MFP				Data length†	ID code	Function
					15	14	13	12	(ID12..8)	(Hex)	
1	1	0	0	0	See Table 3-2				0 1 0 0 1	BF	LBD-MR, 8 IN/8 OUT
1	1	0	0	1	See Table 3-2				0 0 0 0 1	BE	LBD-MR, 16 IN
1	1	0	1	0	See Table 3-2				0 0 0 0 1	BD	LBD-MR, 16 OUT
1	1	0	1	1	0	0	0	0	0 1 1 0 1	BF	LBD-MR, 2 IN/2 OUT
1	1	0	1	1	0	0	0	1	0 1 1 0 1	BE	LBD-MR, 2 IN
1	1	0	1	1	0	0	1	0	0 1 1 0 1	BD	LBD-MR, 2 OUT
1	1	0	1	1	0	0	1	1	0 1 0 0 0	BF	LBD-MR, 4 IN/4 OUT
1	1	0	1	1	0	1	0	0	0 1 0 0 0	BE	LBD-MR, 4 IN
1	1	0	1	1	0	1	0	1	0 1 0 0 0	BD	LBD-MR, 4 OUT
1	1	0	1	1	0	1	1	0	0 1 0 0 1	BE	LBD-MR, 8 IN
1	1	0	1	1	0	1	1	1	0 1 0 0 1	BD	LBD-MR, 8 OUT
1	1	0	1	1	1	0	0	0	0 0 0 0 1	7F	LBD-MR, SPI 16 IN/16 OUT
1	1	0	1	1	1	0	0	1	0 0 0 0 1	7D	LBD-MR, SPI 16 OUT
1	1	0	1	1	1	0	1	0	0 0 0 0 1	7E	LBD-MR, SPI 16 IN
1	1	0	1	1	1	0	1	1	0 0 0 1 0	7F	LBD-MR, SPI 32 IN/32 OUT
1	1	0	1	1	1	1	0	0	0 0 0 1 0	7E	LBD-MR, SPI 32 IN
1	1	0	1	1	1	1	0	1	0 0 0 1 0	7D	LBD-MR, SPI 32 OUT
1	1	0	1	1	1	1	1	0	0 0 0 0 0	78	LBD-MR, Init-µP
1	1	1	0	0	See Table 3-2				0 1 0 0 1	B3	LBD-OR, 8 IN/8 OUT
1	1	1	0	1	See Table 3-2				0 0 0 0 1	B2	LBD-OR, 16 IN

Table 2-5 Local bus operating modes with device-oriented diagnostics (continued)

C4*	C3	C2	C1	C0	MFP				Data length†	ID code	Function
					15	14	13	12	(ID12..8)	(Hex)	
1	1	1	1	0	See Table 3-2				0 0 0 0 1	B1	LBD-OR, 16 OUT
1	1	1	1	1	0	0	0	0	0 1 1 0 1	B3	LBD-OR, 2 IN/2 OUT
1	1	1	1	1	0	0	0	1	0 1 1 0 1	B2	LBD-OR, 2 IN
1	1	1	1	1	0	0	1	0	0 1 1 0 1	B1	LBD-OR, 2 OUT
1	1	1	1	1	0	0	1	1	0 1 0 0 0	B3	LBD-OR, 4 IN/4 OUT
1	1	1	1	1	0	1	0	0	0 1 0 0 0	B2	LBD-OR, 4 IN
1	1	1	1	1	0	1	0	1	0 1 0 0 0	B1	LBD-OR, 4 OUT
1	1	1	1	1	0	1	1	0	0 1 0 0 1	B2	LBD-OR, 8 IN
1	1	1	1	1	0	1	1	1	0 1 0 0 1	B1	LBD-OR, 8 OUT
1	1	1	1	1	1	0	0	0	0 0 0 0 1	73	LBD-OR, SPI 16 IN/16 OUT
1	1	1	1	1	1	0	0	1	0 0 0 0 1	72	LBD-OR, SPI 16 IN
1	1	1	1	1	1	0	1	0	0 0 0 0 1	71	LBD-OR, SPI 16 OUT
1	1	1	1	1	1	0	1	1	0 0 0 1 0	73	LBD-OR, SPI 32 IN/32 OUT
1	1	1	1	1	1	1	0	0	0 0 0 1 0	72	LBD-OR, SPI 32 IN
1	1	1	1	1	1	1	0	1	0 0 0 1 0	71	LBD-OR, SPI 32 OUT
1	1	1	1	1	1	1	1	0	0 0 0 0 0	68	LBD-OR, Init-µP

* Set to "1" for SUPI 3 LS and cannot be configured

† For decoding (actual data lengths) see Table 3-11

Abbreviations:

LBD: Local bus with device-oriented local bus diagnostics
MR: With return
OR: Without return
SPI: SPI master
Init-µP: SPI slave or synchronous serial Intel interface

2.3 Remote bus devices

This interface operating mode corresponds to the function of the IBS SUPI 3. INTERBUS devices for fiber optics and copper can be implemented with the SUPI 3 OPC (SUPI 3 LS: copper)

Table 2-6 Remote bus operating modes

C4	C3	C2	C1	C0	MFP				Data length*	ID code	Function
					15	14	13	12	(ID12..8)	(Hex)	
1	0	0	0	0	Table 3-2				0 1 0 0 1	03	RB, 8 IN/8 OUT
1	0	0	0	1	Table 3-2				0 0 0 0 1	02	RB, 16 IN
1	0	0	1	0	Table 3-2				0 0 0 0 1	01	RB, 16 OUT
1	0	0	1	1	0	0	0	0	0 1 1 0 1	03	RB, 2 IN/2 OUT
1	0	0	1	1	0	0	0	1	0 1 1 0 1	02	RB, 2 IN
1	0	0	1	1	0	0	1	0	0 1 1 0 1	01	RB, 2 OUT
1	0	0	1	1	0	0	1	1	0 1 0 0 0	03	RB, 4 IN/4 OUT
1	0	0	1	1	0	1	0	0	0 1 0 0 0	02	RB, 4 IN
1	0	0	1	1	0	1	0	1	0 1 0 0 0	01	RB, 4 OUT
1	0	0	1	1	0	1	1	0	0 1 0 0 1	02	RB, 8 IN
1	0	0	1	1	0	1	1	1	0 1 0 0 1	01	RB, 8 OUT
1	0	0	1	1	1	0	0	0	0 0 0 0 1	33	RB, SPI 16 IN/16 OUT
1	0	0	1	1	1	0	0	1	0 0 0 0 1	31	RB, SPI 16 OUT
1	0	0	1	1	1	0	1	0	0 0 0 0 1	32	RB, SPI 16 IN
1	0	0	1	1	1	0	1	1	0 0 0 1 0	33	RB, SPI 32 IN/32 OUT
1	0	0	1	1	1	1	0	0	0 0 0 1 0	32	RB, SPI 32 IN
1	0	0	1	1	1	1	0	1	0 0 0 1 0	31	RB, SPI 32 OUT
1	0	0	1	1	1	1	1	0	0 0 0 0 0	38	RB, Init-µP

* For decoding (actual data lengths) see Table 3-11

Abbreviations:

RB : Remote bus

SPI: SPI master

Init-µP: SPI slave or synchronous serial Intel interface

2.4 Bus terminal module

A bus terminal module connects the devices of the INTERBUS branch (remote bus or local bus) to the INTERBUS remote bus. In addition, the bus terminal module can connect or disconnect the branch to or from the rest of the network when requested by the master. Bus terminal modules can be implemented with the SUPI 3 OPC chip.

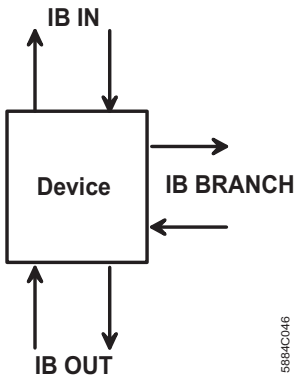


Figure 2-3 Bus terminal module with two outgoing interfaces

In bus terminal module operating modes, additional I/O functions can be implemented using serial register expansion and microprocessor connection with the SPI interface. In this case, ID code and data length must be specified using the microprocessor interface (Init-µP) for these configurations.

Table 2-7 Bus terminal operating modes

C4	C3	C2	C1	C0	Data length (ID12..8)	ID code (hex)	Function
0	0	0	0	0	0 0 0 0 0	0C	BK-RB (Remote bus)
0	0	0	0	1	0 0 0 0 0	08	BK-LB (Local bus)
0	0	0	1	0	0 0 0 0 0	04	BK-LBD (Local bus with diagnostics)
0	0	0	1	1	0 0 0 0 0	38	BK-RB, Init-µP
0	0	1	0	0	0 0 0 0 0	38	BK-LB, Init-µP

The *CONF* I/O signal is used for the "Distributed request for a bus configuration" management function. There is no separate pin as for the IBS SUPI 3. A positive edge triggers an acknowledged reconfiguration request for the system at the bus master.

When the SUPI 3 OPC is used as a bus terminal module, the MFP interface assignment is as follows:

Table 2-8 MFP interface (SUPI 3 OPC) - bus terminal module operating mode

MFP(n)	Assignment	Meaning	
15	ALARM	Alarm output*	OUT
14	LBDA	"LD" (Local bus Disabled) diagnostic LED	OUT
13	ERROR	"Error" diagnostic LED	OUT
12	CONF	"Reconfigure Request" control input	IN
11	LBST	Alarm input for local bus connector	IN
10	DI3	Branch data input	IN
9	DO3_CU	Branch data output (copper)	OUT
8	FO3	Initialization diagnostics, optical fiber interface in "READY" bus status or MAU warning in "RUN" bus status.	OUT
7..0	xx	µP interface, only Init-µP operating mode	xx

* The alarm output can be set by the master (Generation 4) using the firmware command 0714_{hex}.

If the "CONF" and "LBST" inputs are not used, 10 kΩ pull-down resistors should be connected.

Input "DI3" should be provided with a 10 kΩ pull-up resistor, if this interface is not used.

If the µP interface is not used, MFP[7..0] should be connected to GND (open inputs are not permitted).

The function of the LBST[1] signal (MFP11) depends on the configuration of the regulation function (see Section , "If the interface cannot be initialized in optical regulation mode, all regulation mechanisms are deactivated." and Table 2-2 on page 2-2). The following functions are available for *LBST*:

Table 2-9 LBST function

RF1	RF0	Function
1	0	LBST via external signal (as IBS SUPI 3)
0	0	Automatic bus connector recognition: Optical fiber interface, possible to switch on ... (LBST=1)*
1	1	Copper interface, possible to switch off ... (LBST=0) ... the power unit for the branch interface using LBST. When switched off, the current consumption of copper applications reduces.

* Not for SUPI 3 LS

[1] Signal, which indicates that another device follows.

Extended bus terminal module functions

Using a bus terminal module, implemented with the SUPI 3 OPC, the user can automatically isolate a segment from the higher-level bus line and provide diagnostic information to the master using local bus diagnostic functions. This function must be activated in advance by the INTERBUS master.

To detect an interrupt in the connected local bus segment, the local bus return line is monitored in the bus terminal module. If there are no telegrams present for a specified period, the bus terminal module automatically closes the branch interface. This behavior differs from that of a standard bus terminal module because then only the incoming remote bus line is monitored.

If the bus terminal module closes its faulty branch interface automatically, the data path is closed automatically. An error then occurs in the master due to the change in the data length of the remaining operational system, which triggers the diagnostic mechanisms. Depending on the configuration in the master, the "remaining" system can be stopped or continue to operate without adverse effects.

3 Application interface

The SUPI 3 OPC/SUPI 3 LS enables digital or analog I/Os to be connected directly to INTERBUS. This does not require the use of a microprocessor. The SUPI 3 OPC/SUPI 3 LS has a 32-bit data register for transferring user data using a microprocessor between the application and INTERBUS. For this, a configurable serial microprocessor interface is implemented. If the INTERBUS data registers are not large enough, they can be extended using the SUPI 3 OPC (see Section 3.5, "Serial register expansion"). A register expansion is not possible with the SUPI 3 LS.

3.1 Overview

On the SUPI 3 OPC/SUPI 3 LS, the application can access the INTERBUS network in several ways. Communication takes place via a Multi Function Pin interface (MFP for short). Three operating modes are distinguished:

– Binary input/output
– Serial input/output (SPI master mode)
– Serial access with the aid of a microcontroller (serial µP interface)

The MFP interface is configured using pins C[4..0]. In some operating modes these can be extended by MFP[15..12].

In addition to the operating mode, the device length (data length) and ID code (type), with which the device identifies itself to the master, are specified. The codes which are taken from the internally stored assignment tables are set by setting the configuration pins.

All MFP pins are connected as inputs after initialization as long as they were not assigned another function (output, µP interface, etc.) during configuration (C[4..0]). All open chip inputs should be connected to GND, otherwise the current consumption of the circuit may increase and the entire circuit may behavior in an unspecified manner.

3.2 Binary I/O operating mode

Data is exchanged in parallel with the application in this operating mode. INTERBUS I/O data is available at the MFP interface, and can be passed directly to the application. Data is updated synchronously with the INTERBUS cycle. Significance and functions of the MFP interface in the corresponding operating modes are displayed in the following table.

Table 3-1 MFP interface assignment for I/O applications with configuration expansion C[8..5]

MFP													Operating mode
15..12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
C[8..5]	–	–	–	–	–	–	–	–	–	–	In1	In0	2 IN
C[8..5]	–	–	–	–	–	–	–	–	–	–	Out1	Out0	2 OUT
C[8..5]	–	–	Out1	Out0	–	–	–	–	–	–	In1	In0	2 IN/2 OUT
C[8..5]	–	–	–	–	–	–	–	–	In3	In2	In1	In0	4 IN
C[8..5]	–	–	–	–	–	–	–	–	Out3	Out2	Out1	Out0	4 OUT
C[8..5]	Out3	Out2	Out1	Out0	–	–	–	–	In3	In2	In1	In0	4 IN/4 OUT
C[8..5]	–	–	–	–	In7	In6	In5	In4	In3	In2	In1	In0	8 IN
C[8..5]	–	–	–	–	Out7	Out6	Out5	Out4	Out3	Out2	Out1	Out0	8 OUT

Please note: Unused MFP pins ("-") are connected as inputs, however, they are not within the INTERBUS data area. These pins should be connected to GND. The configuration expansion C[8..5] assignment can be found in Section 2. The type of interface is configured in this section.

Table 3-2 MFP interface assignment for I/O applications without configuration expansion

MFP[15..8]	MFP[7..0]	Operating mode
Out7..0	In7..0	8 IN/8 OUT
In15..8	In7..0	16 IN
Out15..8	Out7..0	16 OUT

3.3 Serial I/O (SPI master mode) operating mode

3.3.1 General

In serial input/output operating mode the multi-function pins provide a synchronous serial SPI master interface via which the INTERBUS I/O data can be serially exchanged with the application. In this mode, the SUPI 3 OPC/SUPI 3 LS always transmits a complete byte. Depending on the configuration (16 or 32-bit device), 8 bits are transferred twice or four times. Data is updated synchronously with the INTERBUS cycle. The outputs are 4 mA CMOS drivers. The inputs are implemented as TTL Schmitt triggers.

The serial I/O interface of the SUPI 3 OPC/SUPI 3 LS is designed for direct connection of DACs (digital/analog converters) and ADCs (analog/digital converters) to INTERBUS. It is also possible to connect shift registers (e.g., 74HCT165 or 74HCT594) with a data length of up to 32 bits. 16 or 32 bits are always transmitted, regardless of the number of shift registers connected.

The SUPI 3 OPC/SUPI 3 LS is configured using pins C[4..0]. In master mode, only the SPI interface is available. The following tables gives the MFP pin assignment for the SPI master mode.

Table 3-3 Pin assignment for MFP as a serial user interface (master)

Pin	SPI master	Meaning
MFP0	GND	Does not serve any function
MFP1	GND	Does not serve any function
MFP2	GND	Does not serve any function
MFP3	/Conv	Latch (output)
MFP4	SCLK	Clock (output) 1 MHz at 500 kbaud, 4 MHz at 2 Mbaud
MFP5	/SS	Slave select (output)
MFP6	SerIn	Data (input)
MFP7	SerOut	Data (output)
MFP11..8	GND	Does not serve any function
MFP15..12	Configuration	See Table 2-4 on page 2-4, Table 2-5 on page 2-6 and Table 2-6 on page 2-8.

The serial interface of the chip behaves as follows in this configuration:

The SUPI 3 OPC/SUPI 3 LS generates a clock of f_{SCLK} =1 MHz / 4 MHz at the SCLK output. The /SS line is controlled by the SUPI 3 OPC/SUPI 3 LS in accordance with a 16-bit access. Read and write accesses are made separately.

In input mode (Figure 3-1) 16 or 32 data bits are read in at the SerIn input. The SerOut output is not used and remains open.

In output mode (Figure 3-2) 16 or 32 data bits are given out at the SerOut output.

The **SerIN** input is not used and should be connected to GND.

When data is transmitted from the SUPI 3 OPC/SUPI 3 LS to the I/O device, the /Conv signal is additionally generated, which DACs, for example, can use to begin a conversion (of a digital value into an analog value) or with which the acceptance of a control word can be triggered.

Input/output mode (Figure 3-3) is a combination of the two modes described above. Here the first step is for data to be read in serially by the SUPI 3 OPC/SUPI 3 LS, and data is output serially in the second step. The third step is the data exchange with the SUPI 3 OPC/SUPI 3 LS chip internal INTERBUS data registers. This ensures that information read in by the SUPI 3 OPC/SUPI 3 LS is always consistent with the information output previously.

NOTE: MFP pins 11..8, 2, 1, and 0 should be connected to GND.

3.3.2 Timing of the SPI interface

The SUPI 3 OPC/SUPI 3 LS timing for the serial I/O coupling is based on 16-bit or 32-bit access, depending on the configuration. The I/O devices are informed by the /SS (slave select) signal when 16/32-bit data transmission begins or ends.

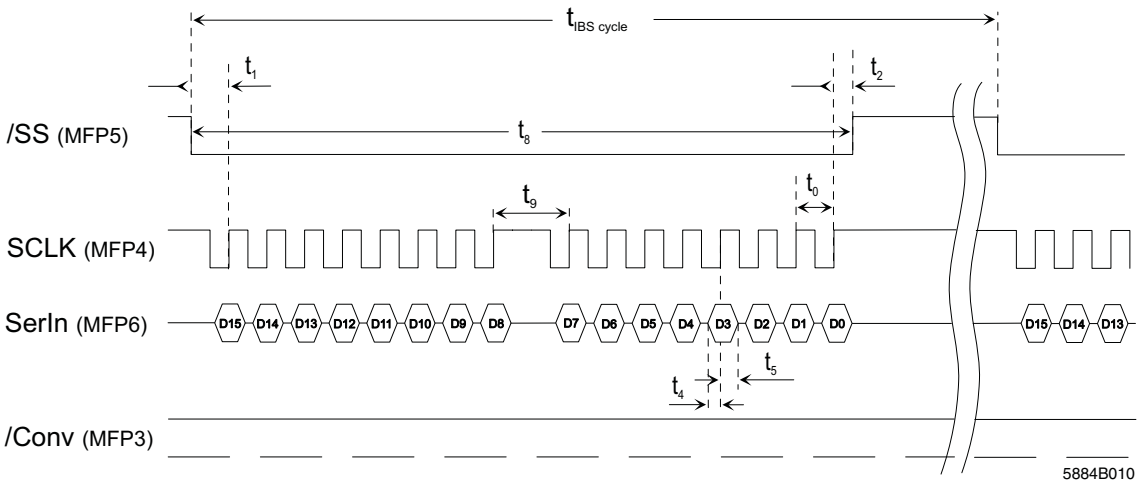


Figure 3-1 Serial input mode timing

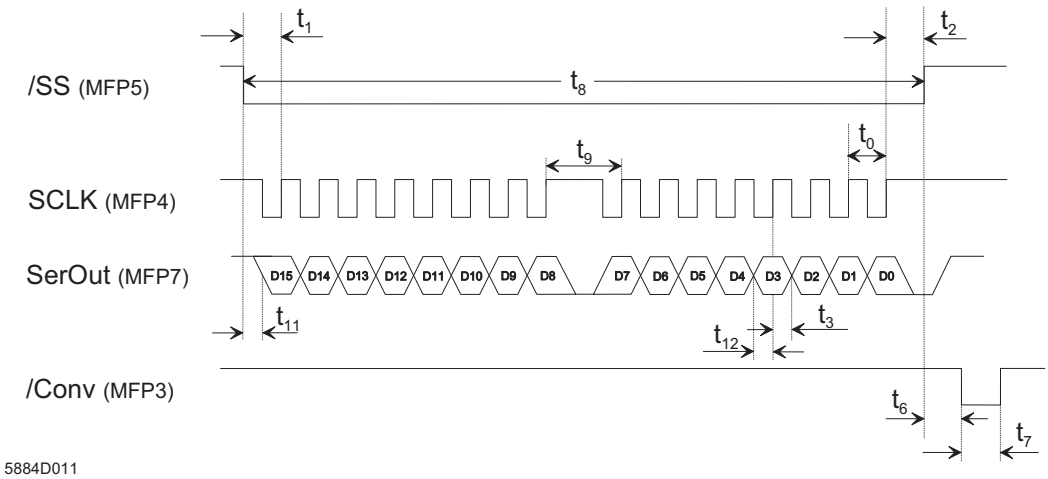


Figure 3-2 Serial output mode timing

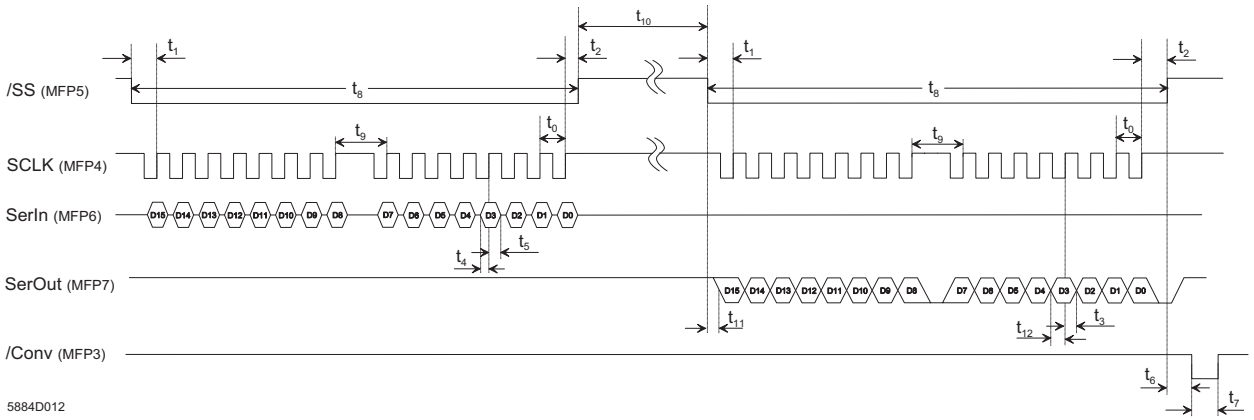


Figure 3-3 Serial input/output mode timing

Table 3-4 SPI master times

Symbol	Explanation	Time (minimum)	Time (maximum)
t_0	Clock period (t_{Bit_IBS} = 2 µs at 500 kbaud, = 0.5 µs at 2 Mbaud)	0.5 * t_{Bit_IBS}	
t_1	Negative edge of /SS before positive edge of SCLK	t_0	
t_2	Positive edge of /SS after positive edge of SCLK	t_0	
t_3	SerOUT data valid after positive edge of SCLK	0.5 * t_0	
t_4	SerIN data valid before positive edge of SCLK (setup)	100 ns	
t_5	SerIN data valid after positive edge of SCLK (hold)	50 ns	
t_6	Negative edge of /Conv after positive edge of /SS	t_0	
t_7	Duration of /Conv conversion signal	t_0	
t_8	Duration of /SS signal (n: number of bytes)	9 * n * t_0	
t_9	Pause between LOW byte and HIGH byte	2 * t_0	
t_{10}	Pause between Read /SS and Write /SS	50.5 * t_0	
t_{11}	SerOUT data item D15 valid before the first positive edge of SCLK	0.5 * t_0	
t_{12}	SerOUT data valid before positive edge of SCLK	0.5 * t_0	

3.4 Serial µP interface (SPI slave mode) operating mode

3.4.1 General

In this operating mode the multi-function pins provide a synchronous serial inteface. The protocol chip can communicate with a microprocessor and quickly exchange I/O data serially via this serial slave interface. The interface has been designed for direct connection of Motorola and Intel-compatible processors. In this operating mode, the SUPI 3 OPC/SUPI 3 LS is always a slave and does not itself initiate any access. Its data outputs remain in a high-impedance state as long as the slave-select signal /SS is inactive (=high).

The serial input/output interface can be configured in slave mode as an SPI or synchronous Intel interface.

An initialization byte, which must be sent to the SUPI 3 OPC/SUPI 3 LS from the microprocessor before communication starts is used to specify whether the interface operates in Intel or Motorola mode.

To simplify communication, the SUPI 3 OPC/SUPI 3 LS also provides the interrupt signal /IRQ and the status signal $\overline{C}/D$. These signals can be used to synchronize protocol chip and microprocessor easily.

The SUPI 3 OPC/SUPI 3 LS is configured using the internal SET register (relative address 13), which is written to by the microprocessor. As long as the SUPI 3 OPC/SUPI 3 LS has not been configured, the data length remains at 0, and the µP_Not_Ready ID code is present in the ID register. The actual ID code depends on the configuration of C[4..0]. If the INTERBUS master detects a µP_Not_Ready ID code it informs the user that the microprocessor has not yet configured the SUPI 3 OPC.

3.4.2 Serial interface timing

Table 3-5 MFP interface function in SPI slave mode

MFP	Signal	Function	
7	SerOUT	**Ser**ial output (MISO: Master In Slave **Out**)	OUT
6	SerIN	**Ser**ial output (MISO: Master Out Slave **In**)	IN
5	/SS	**S**lave **S**elect	IN
4	SCLK	Clock input for synchronous data transmission (1.5 MHz, maximum at 500 kbps, 6 MHz, maximum at 2 Mbps)	IN
3	/IRQ	**I**nterrupt **Req**uest	OUT
2	$\overline{C}$/D	$\overline{\textbf{C}}$ommand/**D**ata Status of the serial microprocessor interface. This signal indicates whether the next byte is expected to be a command ("0") or data ("1").	OUT
1	I/O	**I/O** access (polling) bit (corresponds to bit D7 in the interrupt event register (rel. addr. 14)	OUT
0	SAS_INIT	Initialization of the serial interface (active high)	IN

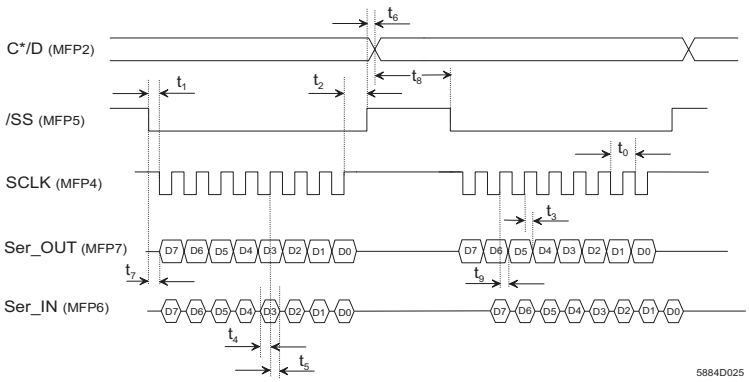


Figure 3-4 Timing of the synchronous serial interface (Motorola)

If the I/O access bit is not used, this output can be left open. MFPs 8 to 0.11 have no function unless "Bus terminal module Init-µP" operating mode is used. They should be connected to GND. For configuration, MFPs 12..15 are wired according to Tables 2-4 to 2-6 in Section 2.

Table 3-6 MFP interface function when connecting to an Intel microprocessor

MFP	Signal	Function	
7	S/$\overline{R}$	Control signal for data direction "1": The microprocessor sends data to the SUPI 3 OPC/SUPI 3 LS (**S**end) "0": The microprocessor expects data from the SUPI 3 OPC/SUPI 3 LS (**R**eceive)	IN
6	Ser_IN/OUT	Bidirectional data line	I/O
5	/SS	**S**lave **S**elect	IN
4	SCLK	Clock input for synchronous data transmission (1.5 MHz, maximum at 500 kbps, 6 MHz, maximum at 2 Mbps)	IN

Table 3-6 MFP interface function when connecting to an Intel microprocessor (continued)

MFP	Signal	Function	
3	/IRQ	**I**nterrupt **Req**uest	OUT
2	$\overline{C}$/D	**C**ommand/**D**ata Status of the serial microprocessor interface. This signal indicates whether the next byte from the SUPI 3 OPC/SUPI 3 LS is expected to be a command ("1") or data ("0").	OUT
1	I/O	**I/O** access (polling) bit (corresponds to bit D7 in the interrupt event register)	OUT
0	SAS_INIT	Initialization of the serial interface (active high)	IN

The user can see from the $\overline{C}$/D (MFP2) status signal whether the SPI interface requires a command or a data byte.

Status signal $\overline{C}$/D = 0 ⇒ Command byte
Status signal $\overline{C}$/D = 1 ⇒ Data byte

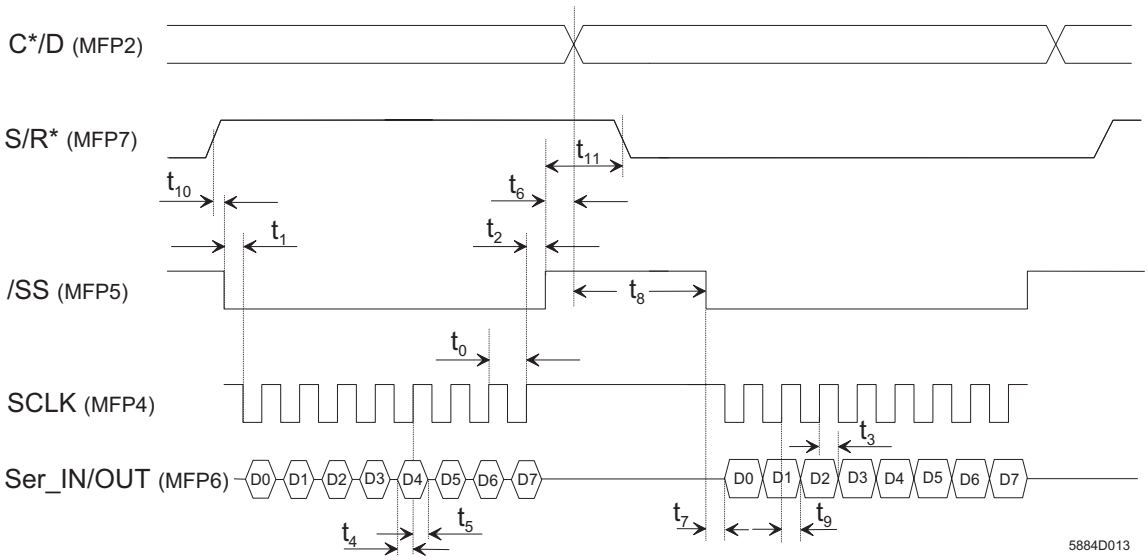


Figure 3-5 Timing of the synchronous serial interface (Intel)

The /SS signal cannot be set to "low" statically, because the change of signal is required internally for data transfer.

Table 3-7 Times for the synchronous serial interface (Intel and Motorola)

Symbol	Explanation	Time (minimum)	Time (maximum)
TCLK	Internal reference clock period (t_{Bit_IBS} = 2 µs at 500 kbps; t_{Bit_IBS} = 0.5 µs at 2 Mbps)	1/16 * t_{Bit_IBS}	
t_0	Clock period (1.5 MHz at 500 kbaud, 6 MHz at 2 Mbaud)	667/167 ns	
t_1	Negative edge of /SS before first negative edge of SCLK	1 * TCLK	
t_2	Positive edge of /SS after last positive edge of SCLK	3 * TCLK	
t_3	SerOUT data (n) valid after positive edge of SCLK (n)	2 * TCLK + 10 ns	

Table 3-7 Times for the synchronous serial interface (Intel and Motorola) (continued)

Symbol	Explanation	Time (minimum)	Time (maximum)
t_4	SerIN data valid before positive edge of SCLK (setup)	100 ns	
t_5	SerIN data valid after positive edge of SCLK (hold)	50 ns	
t_6	Change in the status signal after positive edge of /SS	2 * TCLK	3 * TCLK
t_7	SerOUT data valid after negative edge of /SS		3 * TCLK
t_8	Negative edge of /SS after change of C*/D	TCLK	
t_9	SerOUT data (n) valid after positive edge of SCLK (n-1)		3 * TCLK
t_{10}	S/R* valid before negative edge of /SS	0 ns	
t_{11}	Status change of S/R* after positive edge of /SS	0 ns	
t_{SAS_INIT}	High pulse to initialize the serial interface	250 ns	

3.4.3 Initializing the microprocessor interface

Since the function of the MFP interface differs between Intel and Motorola modes, MFP7 is preconfigured as input after each hardware reset in the “Microprocessor Interface“ operating mode.

The SUPI 3 OPC/SUPI 3 LS expects its initialization information first, **before** any other action. This determines wether, for all future access, the SUPI 3 OPC/ SUPI 3 LS is to behave according to Intel or Motorola notation.

The SUPI 3 OPC/SUPI 3 LS indicates with a low level at C/D* (MFP2) that it is ready for initialization. Once this access mode has been set it can only be changed by a hardware reset or SAS_INIT. Mode initialization is performed by writing an initialization byte. For this purpose the chip expects a clock on MFP4 (SCLK) and the serially transmitted data on MFP6. The $\overline{C}$/D output has a low level here. Since the significance of the bits is inverted between the Intel and Motorola format, the initialization byte is reflected along its length, so that the LSB has the same significance as the MSB. The contents of the mode bit determines the mode of the interface.

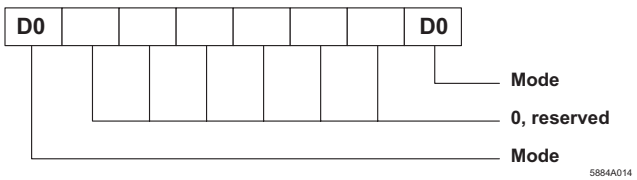


Figure 3-6 Contents of the initialization byte

Table 3-8 Mode bit of the initialization byte

Mode bit	Meaning	Value
0	SPI interface (Motorola)	00_{hex}
1	Asynchronous serial interface (Intel)	81_{hex}

Data transmission is started once initialization is complete. If a faulty initialization byte is received, it its ignored by the SUPI 3 OPC/SUPI 3 LS. Data transmission is disabled. Another initialization is only possible after a power-up reset or SAS_INIT.

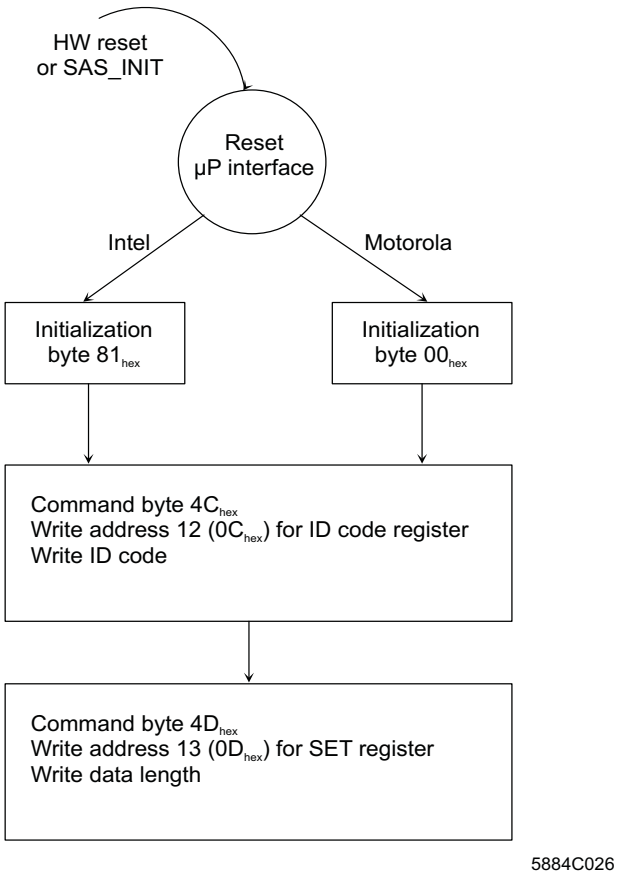


Figure 3-7 Initialization sequence

When the initialization byte has been correctly transmitted the interface mode setting is completed. The SUPI 3 OPC/SUPI 3 LS indicates with a low level at MFP2 ($\overline{C}$/D) that it is ready for data transmission, and is waiting for a command byte. The appearance of the "command" status twice at the SUPI 3 OPC/SUPI 3 LS $\overline{C}$/D pin is a characteristic of first initialization. This can, for example, be used by the connected microprocessor to determine after a microprocessor reset whether the SUPI 3 OPC/SUPI 3 LS was also affected by the reset and therefore whether it must be re-initialized.

SAS_INIT can be used to reset the serial user interface. All settings in the internal registers (e.g., SET and ID registers) are maintained. After a SAS_INIT the interface type (Motorola or Intel) must be specified again by an initialization byte.

After the power-up reset the ID code for the device in µP mode is µP_Not_Ready. The INTERBUS master knows from this ID code that this device has not yet been configured i.e., there is no valid configuration in the SET register (relative address 13). The device is configured by writing to the SET register. After the configuration, the user settings are applied.

NOTE: It is essential to ensure that this reconfiguration is only carried out during the SUPI 3 OPC/SUPI 3 LS initialization phase, i.e., **before** INTERBUS is started, and not during bus operation.

3.4.4 Data transmission to the SUPI 3 OPC/SUPI 3 LS

Complete data transmission to the SUPI 3 OPC/SUPI 3 LS requires two accesses to the interface (block transfer is an exception). The command byte is transmitted with the first access. The address for the following data access and the direction of data transfer are specified here. User data is transferred in the subsequent access. This is indicated by the SUPI 3 OPC/SUPI 3 LS through a high level on its $\overline{C}$/D output. Only a single byte access follows if the address bits in the command byte has selected a valid address in the range 0 to 14. The SUPI 3 OPC/SUPI 3 LS then expects a command byte.

If an invalid address (4 or 5) is entered in the command byte, the SUPI 3 OPC/SUPI 3 LS will ignore the following data access. Data written to the SUPI 3 OPC/SUPI 3 LS is rejected and data read from the SUPI 3 OPC/SUPI 3 LS is invalid. The command byte is read back in this case.

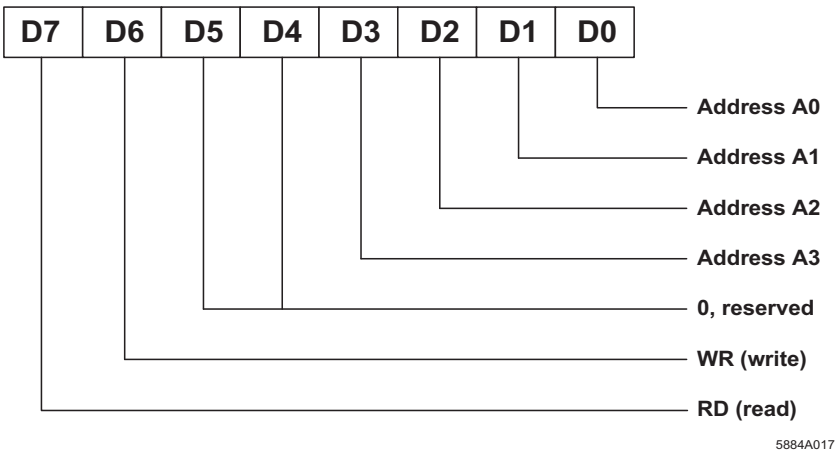


Figure 3-8 Contents of the command byte

RD/WR bits

The RD or WR bit determines the direction of the following data transfer. If data is only to be sent or received via this interface, the corresponding bit is to be set in the command register. The SPI interface enables data to be sent and received simultaneously. Both bits have to be set for this operating mode. Simultaneous transmission and reception is not possible on the Intel interface, since a changeover between the receive and transmit registers must be effected by hardware, using the S/$\overline{R}$ line.

This changeover is done with the S/$\overline{R}$ signal from the microprocessor and is implemented as follows:

Table 3-9 Meaning of S/$\overline{R}$ signal

S/$\overline{R}$	Signal meaning
0	The processor expects data from the SUPI 3 OPC/SUPI 3 LS, that is the SUPI 3 OPC/SUPI 3 LS sends data to the processor.
1	The processor send data to the SUPI 3 OPC/SUPI 3 LS.

Address bits

The address bits in the command byte define the binary coded address for the subsequent data access.

3.4.5 Initialization sequence - example

To illustrate the initialization procedure described in the previous section, access by an Intel processor to the SUPI 3 OPC/SUPI 3 LS using timings is explained again here in more detail.

First, the SUPI 3 OPC/SUPI 3 LS was changed to Init-µP via its configuration pins (C[4..0]) (see Section 2). The Intel processor does not permit a full duplex connection, i.e., read and write access must be carried out in succession because the processor must switch internally between its receive and send registers. Next, the SUPI 3 OPC/SUPI 3 LS must be informed whether the connected processor is an Intel or Motorola processor. This can be done using the initialization byte, which the OPC expects from the processor after every power-up. If the connected processor is an Intel, as in this example, the LSB and MSB must be set to "1" and transmitted via the serial interface (Figure 3-9 "Initialization byte timing (81_{hex})").

Afterwards, the desired protocol chip operating mode is set by writing the SET register (address 13) and entering the corresponding ID code in the ID register (address 12). Both are initiated by the processor and carried out via the serial processor interface. Data transmitted by the serial interface is shown in Figure 3-10 and Figure 3-11.

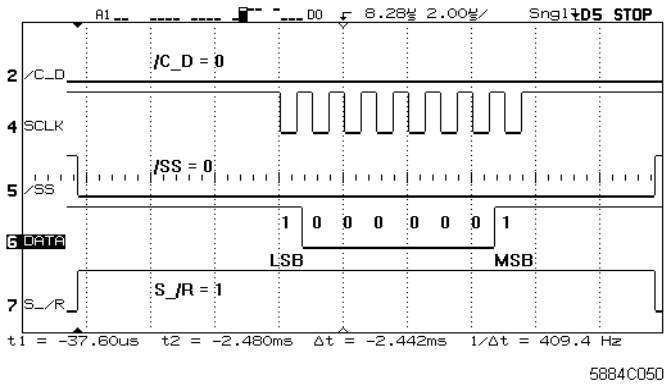


Figure 3-9 Initialization byte timing (81_{hex})

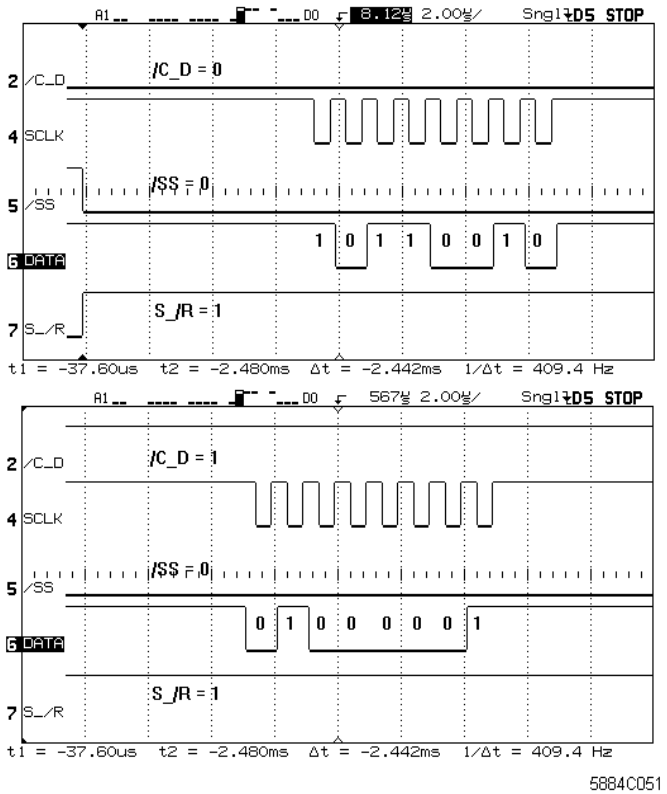


Figure 3-10 Timing access to the SET register (address and data)

First of all, the SET register is activated via $4D_{hex}$ to write to address 13. Next, 82_{hex} is set as the data item to set an I/O device using the decoded data length of a byte (see Table 3-12 "Encoded data length bit 2 to 0").

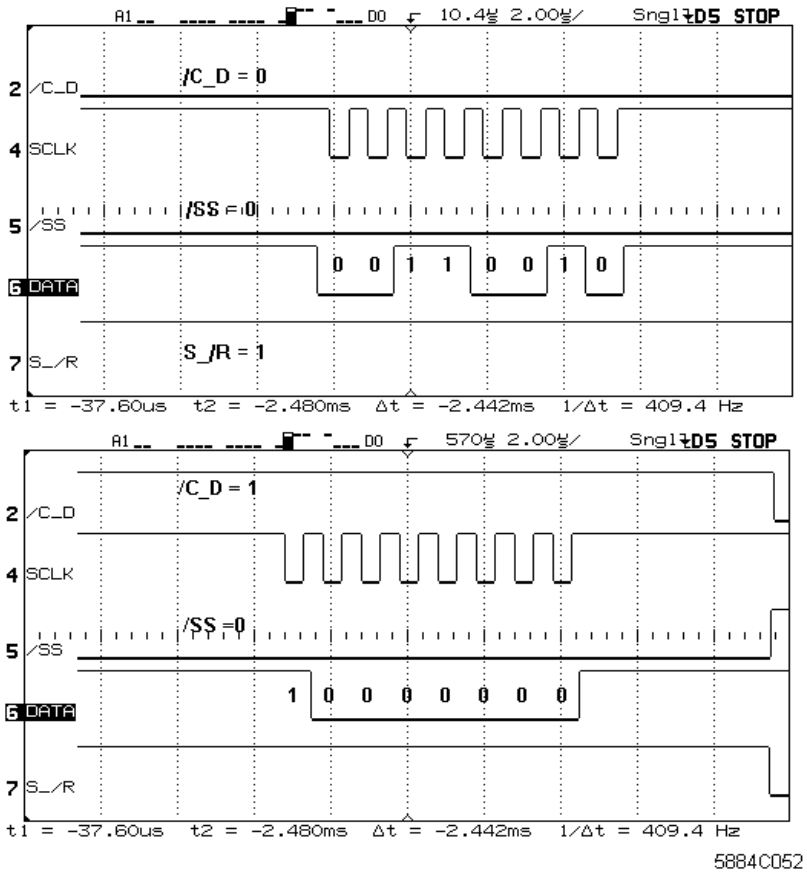


Figure 3-11 Timing access to the ID code register (address and data)

Programming of the write register 12 (ID code) is shown in Figure 3-11. First of all, the register 12 is prepared for write mode. Then, the ID code 01_{hex} (digital output device) is set.

3.4.6 Block transfer

If write access with CF_{hex} is made to address 15 of the SUPI 3 OPC/SUPI 3 LS, a special data transfer mode, the block transfer, is activated. In this operating mode the complete data exchange of all configured IN/OUT data is expected from the SUPI 3 OPC/SUPI 3 LS. After the appropriate access to address 15, all data bytes are transmitted one after another, without a command byte being needed for each. This speeds up access. Thus, for example, transmission in Intel mode with standard transmission of two words requires eight cycles, but only five cycles are required if block transfer is used.

If the SUPI 3 OPC/SUPI 3 LS has been initialized for the Intel mode, there is first read access and then write access when block transfer is used. In Motorola mode, read and write access occur simultaneously. The RD and WR bits in the command byte have no meaning for block transfer, i.e. both the IN bytes and the OUT bytes are always processed.

Block transfer is particularly helpful for exchanging larger amounts of data (such as in PCP communication). This means that block transfer mode can be used with all configurable data lengths ≥ 1 word.

Access to a 24-bit output device is shown in the following timing. The device only has to be accessed four times instead of the usual six (one command and one data item per byte).

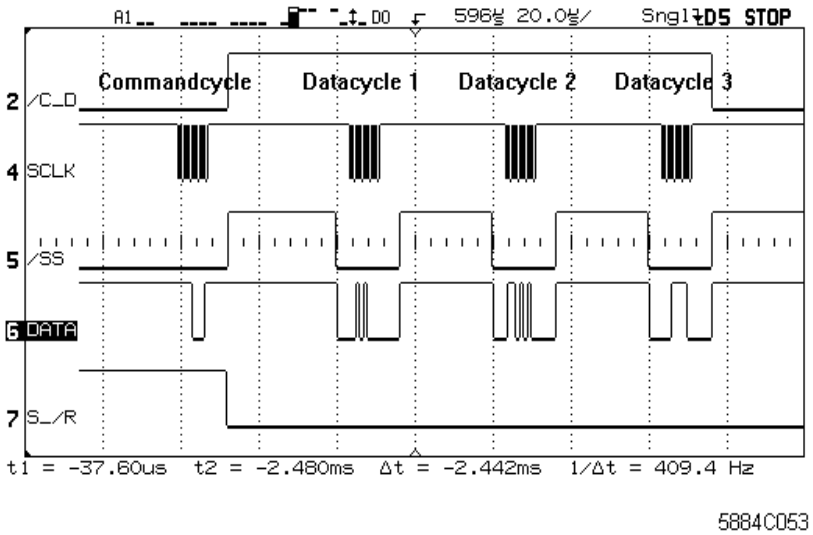


Figure 3-12 Command and data access during block transfer

In this example, $8F_{hex}$ is transmitted first as the command and then the three data bytes 14_{hex}, 56_{hex} and 78_{hex} are transmitted.

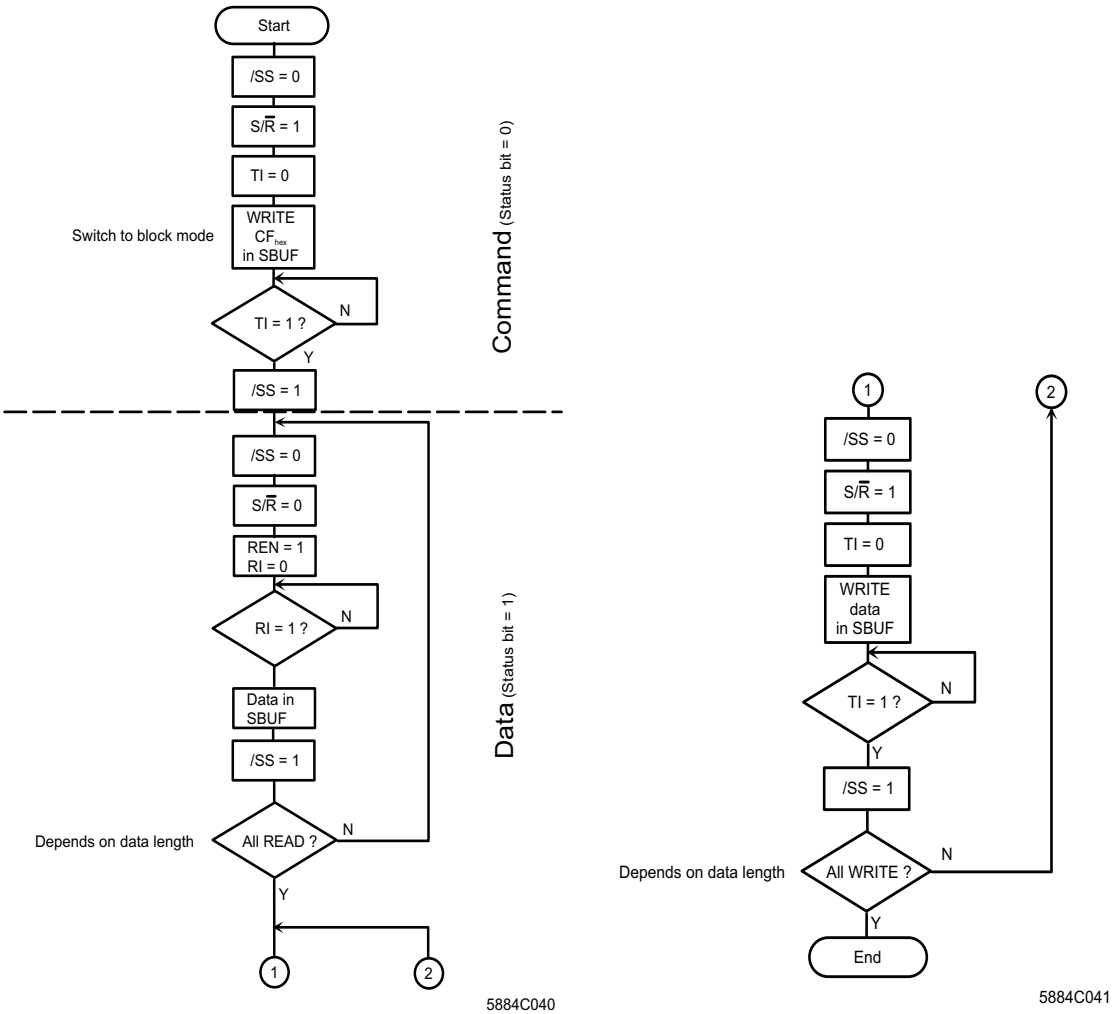


Figure 3-13 Flowchart for block transfer mode for Intel-µP

Block transfer mode should be controlled by interrupts for data lengths of more than one word because when the polling bit is used, the transfer of data may last longer than 60 µs (depending on the microprocessor).

3.4.7 Address area assignment

The SUPI 3 OPC/SUPI 3 LS has an address area of 16 bytes. Four address bits, A3..0, are available for addressing. A total area of 16 bytes can therefore be addressed. The user can access the areas given in the table. Data to be transmitted over INTERBUS is written into the INTERBUS IN byte registers. Data coming from INTERBUS is read from the INTERBUS OUT byte registers.

Table 3-10 Address area assignment for the SUPI 3 OPC/SUPI 3 LS

Relative address	WRITE register	READ register
0	INTERBUS IN byte 0	INTERBUS OUT byte 0
1	INTERBUS IN byte 1	INTERBUS OUT byte 1
2	INTERBUS IN byte 2	INTERBUS OUT byte 2
3	INTERBUS IN byte 3	INTERBUS OUT byte 3
4	Reserved	Reserved
5	Reserved	Reserved
6	–	Reserved
7	Processor alarm register	Processor command register
8	–	Length of the outgoing interface
9	–	Length of the bus branch
10	–	Power level of the incoming interface, enable
11	–	Power level of the branch and the outgoing interface
12	ID code	ID code
13	SET register	SET register
14	Interrupt enable	Interrupt event
15	Block transfer	Block transfer

All registers have the default value "0" after a reset. INTERBUS IN/OUT data registers are set to the default value either by a power-up reset or by an INTERBUS reset. All other registers are only set to 0 by a power-up reset.

Access to the reserved registers 4 and 5 is ignored by the SUPI 3 OPC/SUPI 3 LS. A command byte is expected after the discarded data access. Writing to addresses 6 and 8 to 11 as no effect.

3.4.8 INTERBUS data registers

Relative addresses 0..3

The INTERBUS data registers with relative addresses 0 to 3 are used for data exchange between the application and the INTERBUS master. If the command byte specifies read access, the registers are automatically interpreted as OUT bytes, and for a write command, correspondingly, as IN bytes. There is no provision for reading the IN bytes back after the data transmission. The significance of the data registers falls with rising addresses, i.e., for a device with a data length of four bytes, the contents of address 0 is the most significant byte (MSB), the contents of address 3 is the least significant byte (LSB).

If external data registers are required or used (e.g., IBS SRE 1), the internal SUPI 3 OPC/SUPI 3 LS data registers **cannot** be used. They are no longer in the data path.

3.4.9 Processor alarm register and processor command register

Relative address 7

The SUPI 3 OPC/SUPI 3 LS offers a management channel to the bus master. This function must be enabled by the bus master and is supported by firmware 4.0 or later. Management messages from the master to the slave are received in the processor command register and can trigger an interrupt. Management messages from slave to master are written to the processor alarm register. The management channel is reserved for future applications.

3.4.10 ID code register

Relative address 12

The ID code is determined in the INTERBUS Club ID Code Specification depending on the device functions. An extract from this code can be found in Appendix A 1 "ID code specification (extract)". As standard, this ID code is applied and decoded internally by the hardware via SUPI 3 OPC pins C4.0.. The SUPI 3 OPC/SUPI 3 LS offers the option of setting the ID code in the ID code register using software. This makes it possible to adapt the ID code to the application type without modifying the hardware (see Section 3.4.3, "Initializing the microprocessor interface"). The ID code is specified during the initialization phase of the device.

3.4.11 SET register

Relative address 13

The device data lengths and the type of the device (PCP or I/O) are set in the SET register. Like the ID code, these settings are made during the initialization phase of the device. Changing the register contents during bus operation is not permitted.

The following options are available:

– ExtReg = 1: The complete length code must be entered. PCP data is not transferred into the SUPI 3 OPC data registers. In this case, the /PCP bit is of no significance.
– ExtReg = 0: Abbreviated length code, which is decoded internally (see also Table 3-12 on page 3-22).

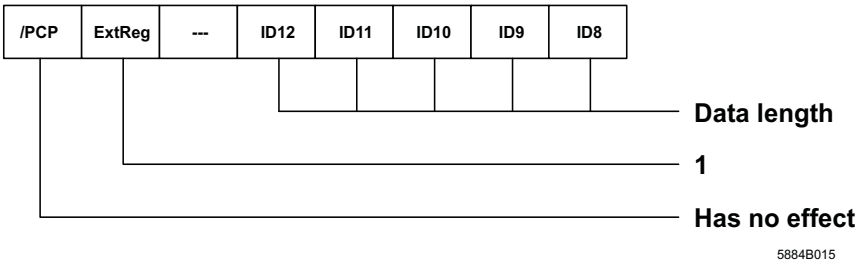


Figure 3-14 SET register with external data expansion

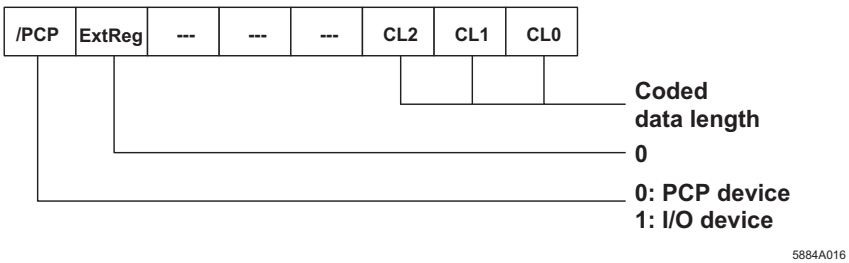


Figure 3-15 SET register without external data expansion

PCP communication

The SUPI 3 OPC/SUPI 3 LS can be configured as a PCP device using the PCP communication bit /PCP in the SET register. In order to support PCP communication, IN bytes 0 and 1, which constitute the communication channel for a PCP device must be erased after their contents have been transferred to INTERBUS. To use IN bytes 0 and 1 for dedicated I/O applications, the erase mechanism can be switched off by means of the PCP communication bit. If the bit is set, data contained in IN bytes 0 and 1 is transmitted with every data cycle (I/O operation). Then they behave like IN bytes 3 and 4.

All SUPI 3 OPC/SUPI 3 LS permissible data lengths can be used with a dedicated I/O device. In PCP operation without register expansion the data length is specified as ≥ 1 word.

If the data length of the SUPI 3 OPC/SUPI 3 LS is not sufficient because, e.g., 2 or 4 PCP words (additional I/O data) are to be used, the IBS SRE 1 can be used to expand the INTERBUS data registers. The erase mechanism should then be simulated in the IBS SRE 1 using software. If the entire device data length is entered directly via ID8..12, the setting should be selected from Table 3-11.

Table 3-11 Complete ID code for the data length

ID12	ID11	ID10	ID9	ID8	Data length	FW version[1]
0	0	0	0	0	0 words	
0	0	0	0	1	1 word	
0	0	0	1	0	2 words	
0	0	0	1	1	3 words	
0	0	1	0	0	4 words	
0	0	1	0	1	5 words	
0	0	1	1	0	8 words	

Table 3-11 Complete ID code for the data length (continued)

ID12	ID11	ID10	ID9	ID8	Data length	FW version[1]
0	0	1	1	1	9 words	
0	1	0	0	0	1 nibble	4.0
0	1	0	0	1	1 byte	4.0
0	1	0	1	0	Reserved	
0	1	0	1	1	3 bytes	4.0
0	1	1	0	0	Reserved	
0	1	1	0	1	2 bits	4.40
0	1	1	1	0	6 words	3.2
0	1	1	1	1	7 words	3.2
1	0	0	0	0	Reserved	
1	0	0	0	1	26 words	3.7
1	0	0	1	0	16 words	3.2
1	0	0	1	1	24 words	3.2
1	0	1	0	0	32 words	3.2
1	0	1	0	1	10 words	3.2
1	0	1	1	0	12 words	3.2
1	0	1	1	1	14 words	3.2
1	1	x	x	x	Reserved	

[1] The data length is supported by the INTERBUS master with the specified firmware version (FW) or later.

Table 3-12 Encoded data length bit 2 to 0

CL2	CL1	CL0	Data length	Bit 12..8
0	0	0	0 bits	0 0 0 0 0
0	0	1	4 bits (1 nibble)	0 1 0 0 0
0	1	0	1 byte	0 1 0 0 1
0	1	1	1 word	0 0 0 0 1
1	0	0	3 bytes	0 1 0 1 1
1	0	1	2 words	0 0 0 1 0

The master uses the above settings to determine the SUPI 3 OPC/SUPI 3 LS operating mode and the data length of the slave device. The ID code (bits 7..0) is entered by the microprocessor at relative address 12. All settings in the ID code register and in the SET register are mapped directly to the read registers and can thus be read back by the user.

3.4.12 Optical data register

Relative read addresses 8 and 9

In read registers 8 to 11, information on the cable lengths and the power levels of the SUPI 3 OPC can be read.

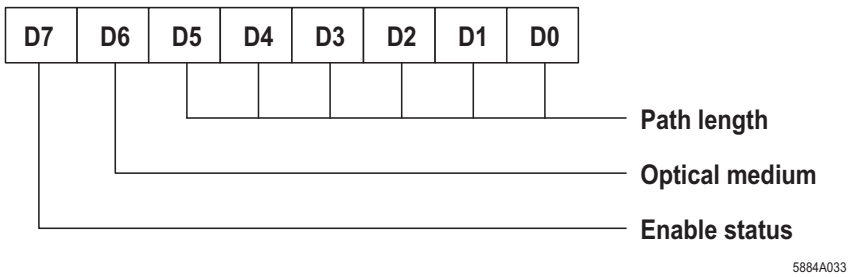


Figure 3-16 Length of the outgoing interface (READ register 8) and the bus branch (READ register 9)

Optical medium:

0 = Polymer fiber (length resolution: 12 m)

1 = Glass fiber (length resolution: 200 m)

Enable status:

0 = Optical initialization has not detected a regulated device or the interface is not in use.

1 = Optical initialization has detected a regulated device.

3.4.13 Optical status register

Relative read addresses 10 and 11

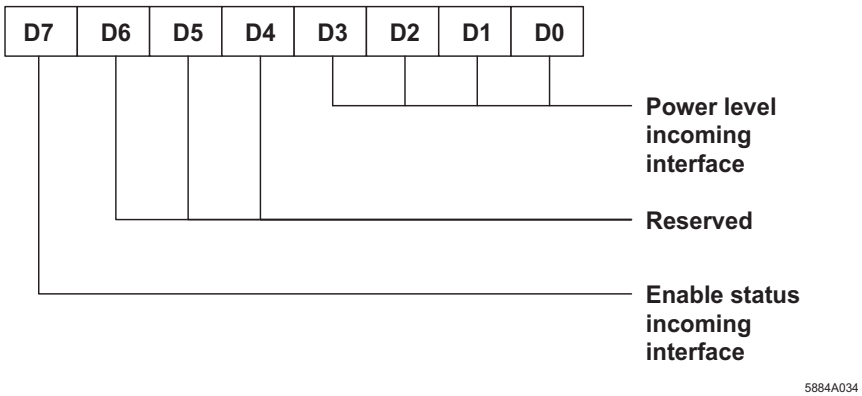


Figure 3-17 Incoming interface (READ register 10)

Enable status:

0 = Optical initialization has not detected a regulated device or the interface is not in use.

1 = Optical initialization has detected a regulated device.

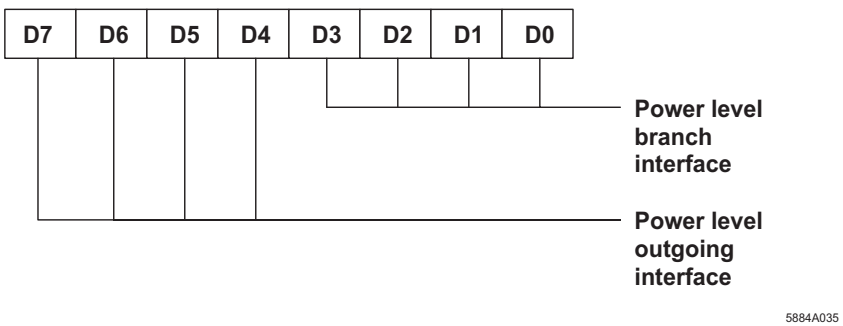


Figure 3-18 Outgoing interface and bus interface (READ register 11)

3.4.14 Synchronizing the application

The SUPI 3 OPC/SUPI 3 LS offers two methods for synchronizing the application with the protocol chip, therefore ensuring data consistency.

– Interrupt control
– Polling

Interrupt controlled access does not place such high demands on performance but does require that the processor is capable of handling interrupts. Another method is polling a bit in the SUPI 3 OPC/SUPI 3 LS. This places high demands on the performance of the connected microprocessor.

Interrupt enable register

The individual interrupt sources in the interrupt event register are selected in the interrupt enable register. The interrupt is enabled by setting the associated bit to high, while setting to low disables the associated interrupt. The default status of the interrupt enable register is "00_{hex}".

Relative write address 14

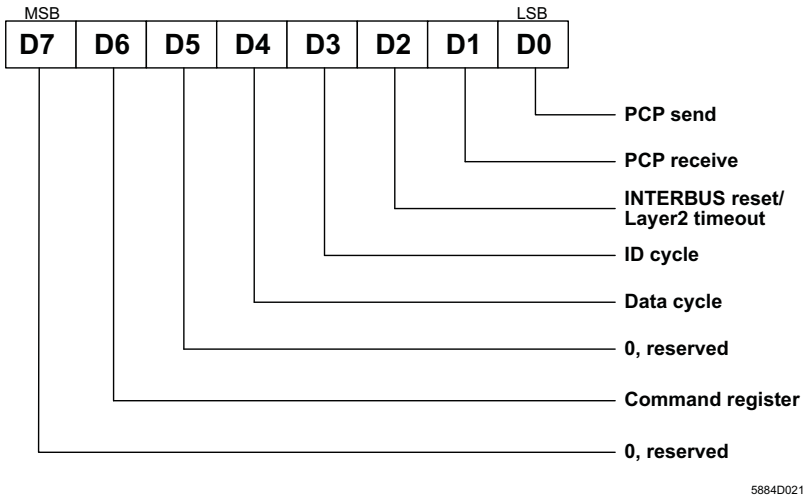


Figure 3-19 Interrupt enable register assignment

Interrupt event register

Interrupt events for the SUPI 3 OPC/SUPI 3 LS are stored in the interrupt event register. The microprocessor determines the source of an interrupt by reading the interrupt event register.

Relative read address 14

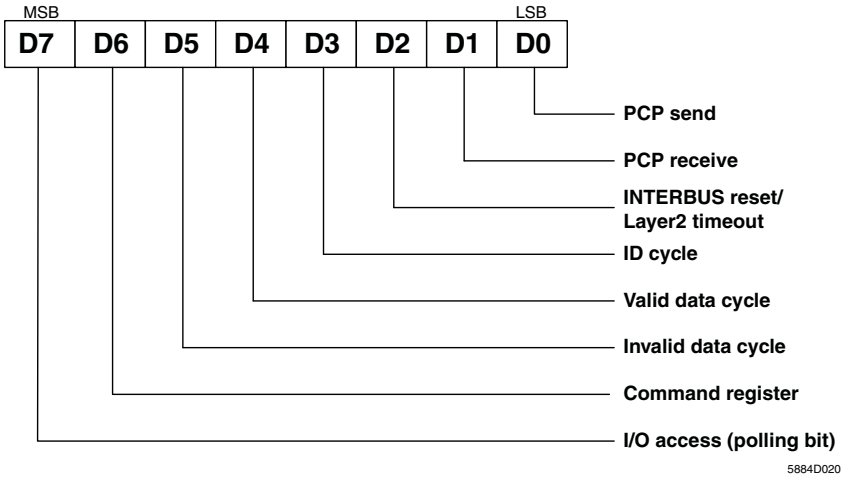


Figure 3-20 Interrupt event register assignment

The SUPI 3 OPC/SUPI 3 LS protocol chip provides the following interrupt sources:

Table 3-13 SUPI 3 OPC/SUPI 3 LS interrupt sources

Interrupt source	Cause
Invalid data cycle	After this interrupt event data is valid, but it originates from the last valid cycle, since the data cycle that has just ended is recognized as invalid. IN bytes should be rewritten from the CPU.
Valid data cycle	This interrupt indicates the end of a valid data cycle. Current OUT data can be accepted. This interrupt is suitable for synchronizing CPU accesses to the SUPI 3 OPC/SUPI 3 LS chip.
ID cycle	This interrupt indicates the end of an ID cycle. This event should be evaluated (write IN data), if current IN data is to be transmitted in the first data cycle.

Table 3-13 SUPI 3 OPC/SUPI 3 LS interrupt sources (continued)

Interrupt source	Cause
INTERBUS reset	This INTERBUS device has been switched to the reset state, either as a result of a fatal error or by the master using the INTERBUS reset ("Alarm Stop Request" command from the master). **This event should always be evaluated by the application.** The INTERBUS data registers (IN and OUT) are reset.
Layer2 timeout	Cyclic operation on the chip is monitored on the chip with a time base that is independent of the bus. Layer2 monitoring can only be set by the INTERBUS master (FW 4.0 or later). If no valid INTERBUS cycle is detected within the time preset by the master (50 ms, 200 ms, 1000 ms, off) process data will be reset. The /ResReg signal will be activated for connected external registers, if necessary. A single pulse of 375 ns is generated. The event is reported to the microprocessor of the device with an interrupt. (G4 firmware error message: $0C6B_{hex}$)
PCP receive	Interrupt source for PCP communication. If this interrupt is present, the CPU can read a new communication word from the SUPI 3 OPC/SUPI 3 LS chip. Interrupt receive identifies the end of a valid data cycle with idle bit = 1.
PCP send	Interrupt source for PCP communication. If this interrupt is present, the CPU can write a new communication word to the SUPI 3 OPC/SUPI 3 LS chip. The Send interrupt identifies the end of a data or ID cycle.

Interrupt operation

The connected microprocessor can read and write the SUPI 3 OPC/SUPI 3 LS INTERBUS data registers asynchronously to the INTERBUS cycle. Inconsistent data can therefore result if the access occurs during the latch updating phase of a bus cycle. The latch phase ends the check sequence of every INTERBUS cycle. In this phase stored OUT data is written to the OUT data registers. Data in the IN registers is transferred to INTERBUS.

The SUPI 3 OPC/SUPI 3 LS contains interrupt logic to synchronize the microprocessor access to the data registers. This logic provides a range of events, which are synchronized to the INTERBUS cycle. The various interrupt sources are enabled by means of the interrupt enable register (address 14). The associated bit should be set to high. When an interrupt event occurs, the associated bit in the interrupt event register is set, and the (/IRQ) MFP3 changes to low. By reading the interrupt event register, the microprocessor may then determine the exact interrupt event.

This read access clears the interrupt event register, and MFP3 (/IRQ) is reset.

Generation of interrupts is independent of the data length set, so that synchronization is also possible with a zero data length.

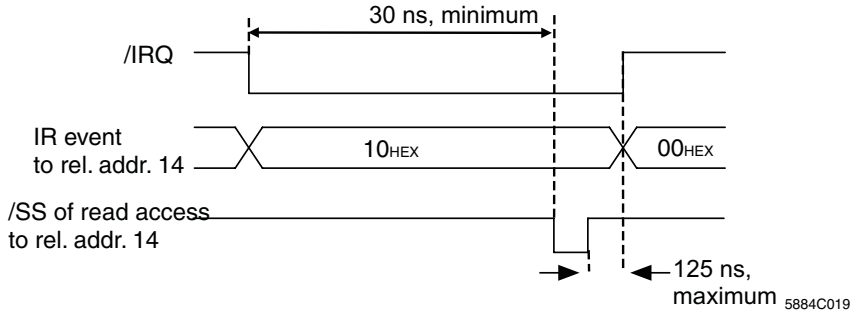


Figure 3-21 Timing using the example of a data cycle interrupt

Using interrupts

The example of the "valid data cycle" interrupt can be used to illustrate interrupt-controlled synchronization of data exchange between SUPI 3 OPC/SUPI 3 LS and microprocessor:

1. The interrupt is enabled by setting bit D4 in the interrupt enable register (relative address 14). This only needs to be done once when the SUPI 3 OPC/ SUPI 3 LS is initialized.
2. When an interrupt event occurs in the SUPI 3 OPC/SUPI 3 LS, the /IRQ line switches to low. This indicates to the microprocessor that an interrupt event has occurred.
3. The microprocessor now reads the interrupt status register.
4. If bit D4, "valid data cycle", is set in the interrupt event register, valid data is available in the OUT registers and can be fetched by the microprocessor.
5. After the interrupt request (/IRQ low) the microprocessor is available for reading the interrupt event register and the INTERBUS OUT data registers, and for writing the IN data registers for the following time in an ideal system:

$$\mathbf{T = 13 * (5 + n) * t_{Bit}}$$

t_{Bit}	Length of an INTERBUS bits (typical: 2 µs at 500 kbps)
n	Number of bytes in the entire network
T	Permissible access time for the CPU

The minimum time T occurs when the INTERBUS network comprises one device only. It should be noted that this is the theoretically determined maximum access time. Since the access time depends largely on the INTERBUS cycle time, the **typical** maximum access time in real systems is > 500 µs.

Example:

Implemented device: 2 words (32 bits). Input and output data will be used. The worst case time is therefore:

T = 234 µs

In the worst case the CPU has a maximum of 234 µs after an interrupt request to read the interrupt event register and the OUT data registers 0 to 3 as well as to write to the IN data registers 0 to 3.

After the interrupt event registers has been read its contents is cleared and the /IRQ line changes to the inactive state.

Using the polling bit

If it is not possible in the application to perform the synchronization using interrupts, the I/O access bit can be polled in the interrupt event register. The register with the relative address 14 is read for this purpose.

If the I/O access bit has the value "1", access to the INTERBUS data registers is not possible. If the bit is "0", the data registers can be accessed within the next 30 bit periods (= 60 µs at 500 kbps). After this time has elapsed, the latch phase can begin, in which data is transferred from the INTERBUS data registers into the internal registers of the SUPI 3 OPC/SUPI 3 LS. If an access occurs during the latch phase inconsistent data may result. This time does not depend on the device data lengths or the INTERBUS configuration. Synchronization by way of the polling bit places high demands on the performance of the microprocessor used.

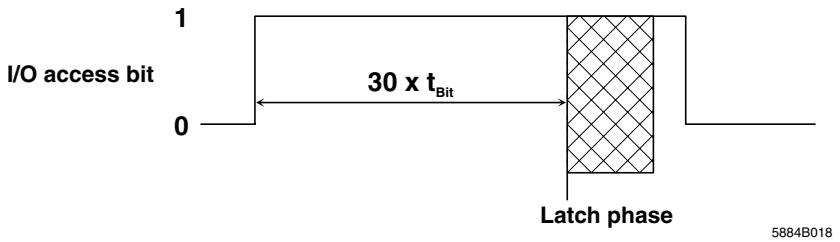


Figure 3-22 I/O access bit timing

3.5 Serial register expansion

The serial register expansion interface is a synchronous serial interface with additional parallel control signals. It is **only** suitable for the use of serial register expansion IBS SRE 1A (Order No. 2746595) in conjunction with a microprocessor incorporating connection via the serial user interface. If an external register expansion is connected to the SUPI 3 OPC, the internal registers **cannot** be used further.

The option to expand internal registers with the IBS SRE 1 should only be used for this. For EMC reasons it is not useful to implement an internal serial interface with remote shift registers. Extension ICs should be located as close as possible to the IBS SUPI 3 OPC.

Safe data transmission to and from these registers is controlled by the /LaInD and LaOuD control signals.

Table 3-14 Serial register expansion interface signals

Designation	Meaning
ClkExR	Clock line
ToExR	Serial data output (**before** internal data channel)
LaOuD	Request to transfer output data
/LaInD	Request to provide input data
FromExR	Serial data input
/ResReg (RC)	Reset data channel

/ResReg (RC) should be connected to the /ResReg input (pin 42) for external register expansions with the IBS SRE 1.

The ToExR output no longer needs to be connected with the FromExR input as with the IBS SUPI 3 to transmit the data correctly. The chip automatically connects the data interface internally if no data is detected at the FromExR input. However, it should be ensured that the FromExR input is connected to GND when not being used.

As shown in Figure 3-23, the request for or transmission of data is asynchronous to the clock for this interface (ClkExR).

The ClkExR clock depends on the INTERBUS transmission speed with which the SUPI 3 OPC/SUPI 3 LS is operated with. At 500 kbps the period length is 2 µs, at 2 Mbps it is 0.5 µs.

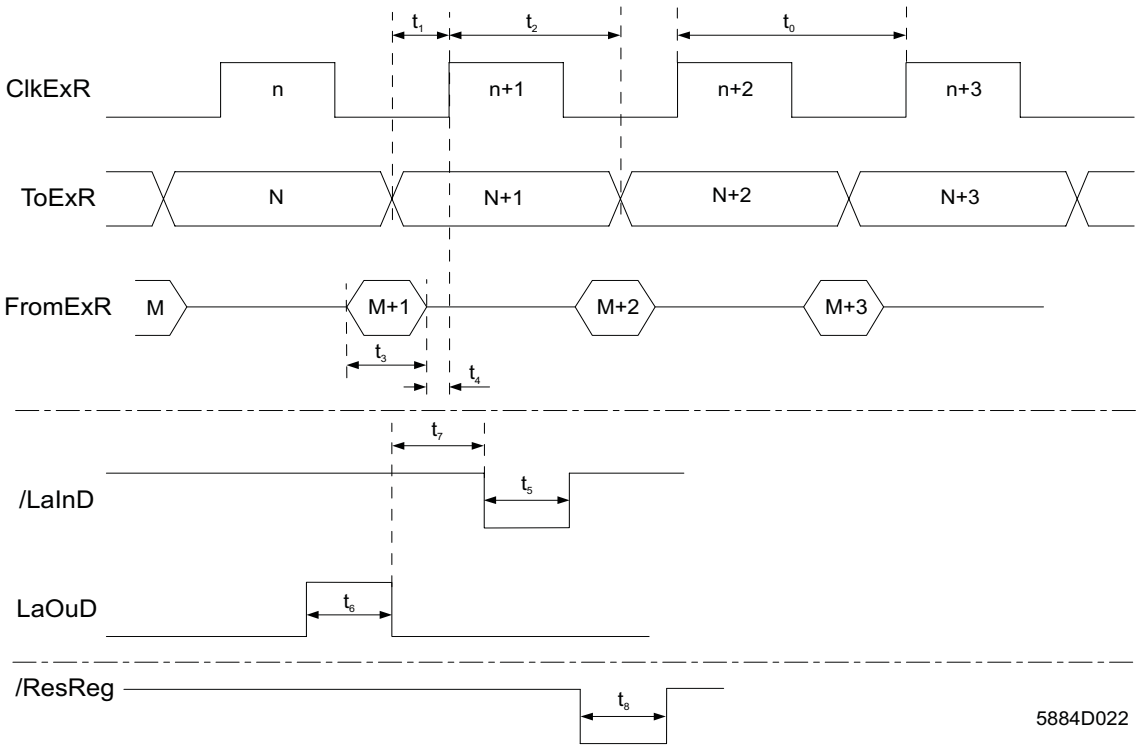


Figure 3-23 Serial register expansion interface timing

Table 3-15 Serial register expansion interface time periods

Symbol	Description	Time (minimum)
t_0	ClkExR period length (t_{Bit_IBS} = 2 µs at 500 kbps; t_{Bit_IBS} = 0.5 µs at 2 Mbps)	t_{Bit_IBS}
t_1	Data valid before positive edge of ClkExR[1]	0.25 * t_0
t_2	Data valid after positive edge of ClkExR[1]	0.75 * t_0
t_3	Data valid before positive edge of ClkExR (setup)	0.25 * t_0+100 ns
t_4	Data valid before positive edge of ClkExR (hold)	0.25 * t_0 - 50 ns (maximum)
t_5	**/LaInD pulse length**	4 * t_0
t_6	**LaOuD pulse length**	4 * t_0
t_7	/LaInD valid after negative edge of LaOuD	5 * t_0
t_8	**/ResReg (RC) pulse length**	4 * t_0
[1] Test condition: ClkExR is loaded with a fan-out of 4		

Accessing external registers:

This brief example illustrates the assignment of data bits during transmission to an external register. 3 bytes of data (78_{hex}, 56_{hex} and 14_{hex}) are sent via the ToExR output on the SUPI 3 OPC to the corresponding shift registers.

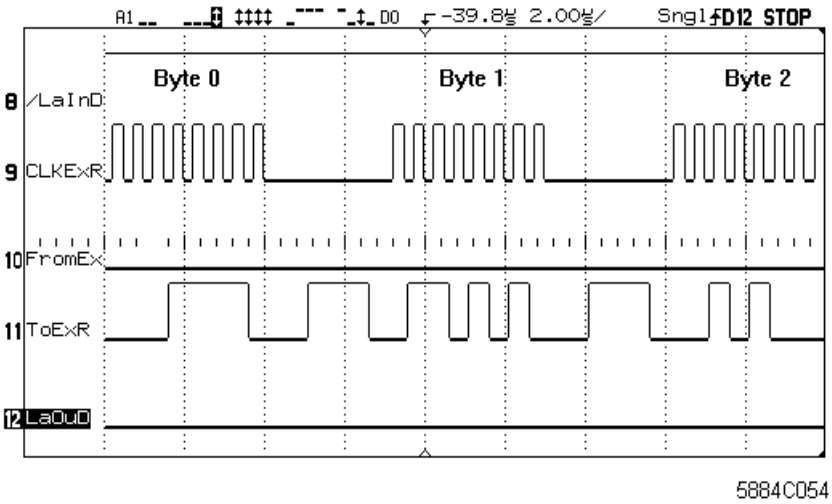


Figure 3-24 Assigning three data bytes with transmission via ToExR

The data bytes 0..2 sent via ToExR are moved in advance to the registers using the LSB. Data was transmitted in the INTERBUS data cycle in the order 14_{hex}. 56_{hex} and 78_{hex}.

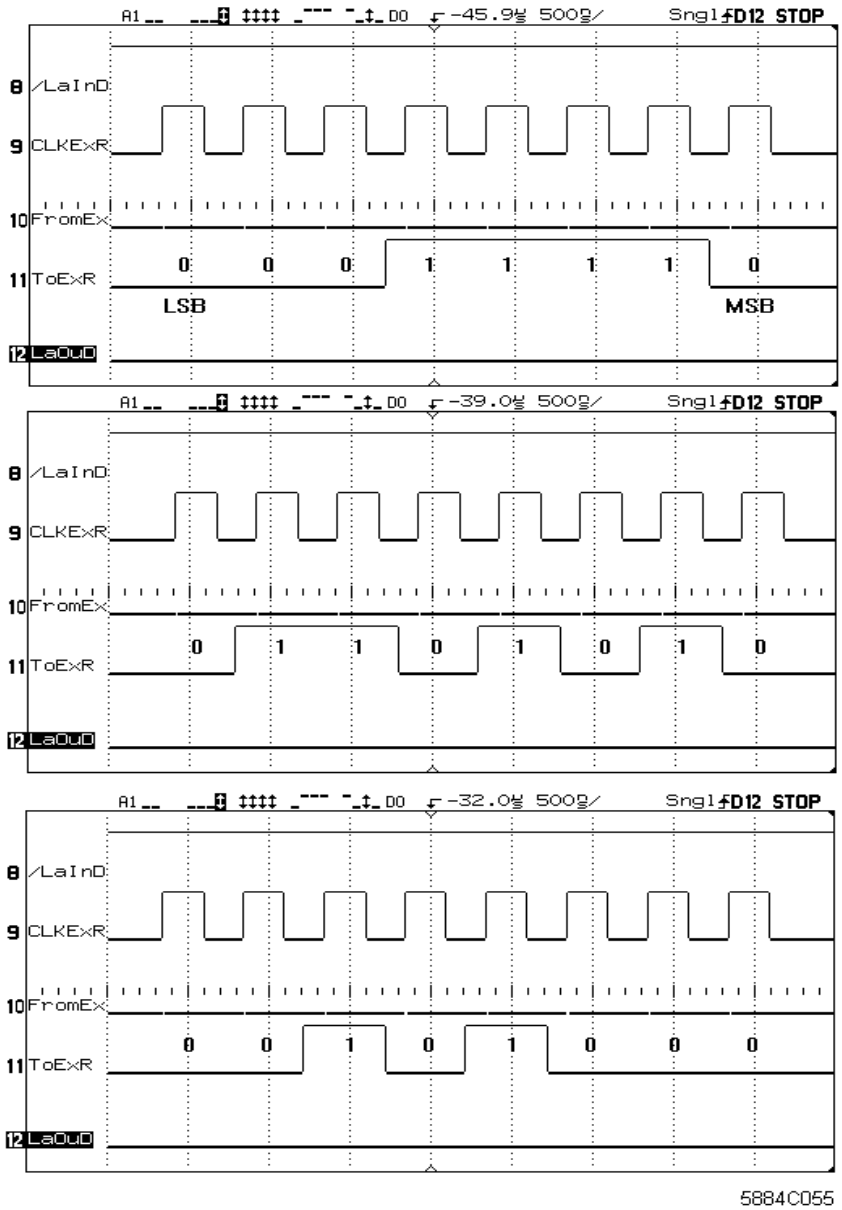


Figure 3-25 Detailed representation of the bytes

3.6 Diagnostics

The SUPI 3 OPC chip has various diagnostic outputs, which simplify error location within INTERBUS network.

3.6.1 Diagnostic inputs/outputs

On the SUPI 3 OPC, either the complete diagnostic display or the limited diagnostic display together with fiber optic diagnostics can be selected. It is selected using the DIAG_CONF input.

Table 3-16 Selecting the diagnostic display

DIAG_CONF	Type of diagnostics	DIAG1	DIAG2
0	Complete diagnostics	BA	RD
1	Limited diagnostics	FO1	FO2

Local bus devices with limited diagnostics

Local bus devices are often implemented using limited diagnostics. Remote bus devices can only be certified with complete diagnostics. If limited diagnostics is selected, **F**iber **O**ptic (FO) diagnostics is available at outputs **DIAG1** and **DIAG2** and on the bus terminal module at **FO3**:

Table 3-17 Fiber optic diagnostic display

Signal	Pin	Interface	State	Diagnostics
FO1	DIAG1	Incoming	0	Initialization OK No MAU warning[1]
			1	Initialization OK No MAU warning[2]
FO2	DIAG2	Outgoing	0	See above
			1	See above
FO3	MFP8 (BK only)	Branch	0	See above
			1	See above

[1] Master in READY state

[2] Master in RUN state

The "**FOx**" LEDs should be **yellow** to ensure system consistency. The following diagnostic states are mapped at the output of the **green** IB_DIAG LED:

Table 3-18 Limited diagnostic display

IB_DIAG pin (status)	Cause
No light	No supply
Steady light	Supply OK, module function error-free, bus active
Flashing slowly (0.5 Hz)	Supply OK, bus not active
Flashing quickly (2 Hz)	Supply OK, peripheral fault (/StatErr)
Flashing very quickly (4 Hz)	Supply OK, module has detected a line interrupt ahead on the local bus

If complete diagnostics is selected, the IB_DIAG output should remain open.

Complete diagnostic display

Complete diagnostic disply may be implemented with the following SUPI 3 OPC pins:

Table 3-19 Complete diagnostic display

Signal	Pin	Diagnostics	Color
U_L	/ResU	Voltage monitoring	Green
RC (CC)	/ResReg	**R**emote bus **C**heck (cable check)	Green
BA	DIAG1	**B**us **A**ctive	Green
RD	DIAG2	**R**emote bus **D**isabled	Yellow
LD	MFP14	Branch disabled (bus terminal module only)	Yellow
E	MFP13	Error in connected branch (bus terminal module only)	Red

For complete diagnostics, the state of the FOx LEDs should also be displayed for devices with fiber optic interfaces. This can be done using a switch-over option at the DIAG_CONF diagnostic configuration input. It is not permitted to use software to do this. The circuit suggestion given in Figure 3-26 can also be used.

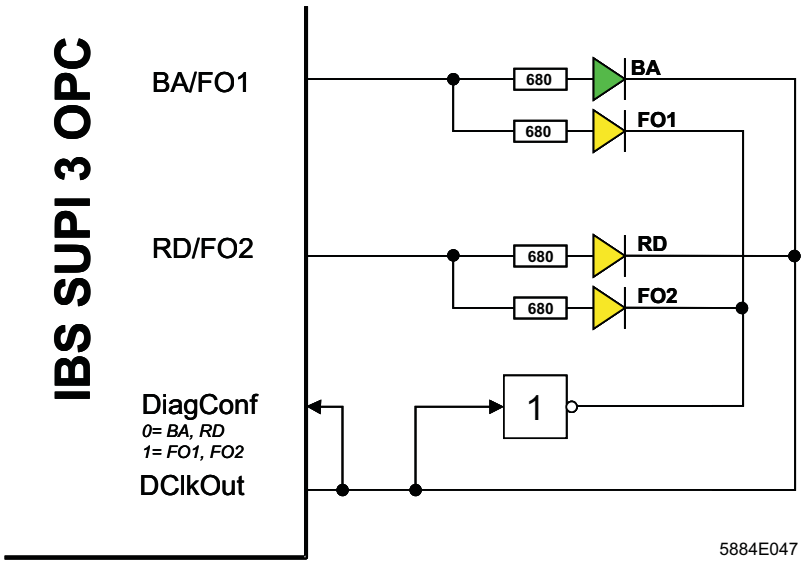


Figure 3-26 Possible implementation for complete diagnostics

TR LED

The PCP diagnostic output "TR" (green LED), which was found on the SUPI 3 cannot be implemented directly using the SUPI 3 OPC. "**TR**" (**T**ransmit/**R**eceive) indicates whether the device is operating PCP communication via INTERBUS. In µP operating modes with PCP communication, this diagnostic LED can be implemented via a port pin on the microprocessor. When sending and receiving PCP PDUs, the TR LED clearly lights up, i.e., if a send or receive interrupt occurs. When another event is reported and none of its sources are set, the LED must be switched off again (1 second afterwards at the very latest).

The status of the supply voltage is displayed by the "U_L" LED. The signal required for this can be taken from the /ResU pin. The /ResU pin is an open drain output with internal pull-up resistor. A driver should therefore be provided externally for the U_L LED.

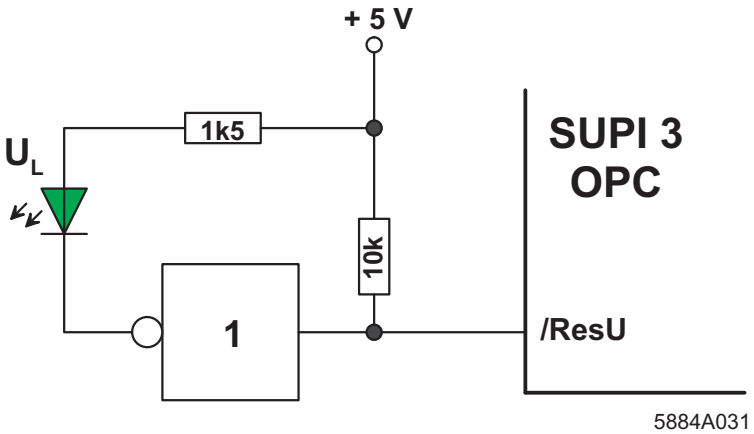


Figure 3-27 Connection of the U_L LED

Another possible implementation for the U_L LED is offered by the IB_DIAG output. The output is simply connected to the green LED. The LED then flashes during the various INTERBUS states (see Table 3-18 "Limited diagnostic display"). This option cannot be certified for remote bus devices.

3.6.2 Input/output module error

/StatErr

The active low input /StatErr is used, for example, to report an I/O error (e.g., I/O voltage error) to the INTERBUS master. An I/O error is triggered if a low level occurs at this input. If /StatErris not used, it should be statically set to high. The input is filtered. This input has a filter integrated into the circuit with the time t_3 = 200 ms ±31.5%. Setting this input generates the "I/O Device Error Indication $0BB1_{hex}$" message on a Generation 4 bus master.

/ModAck

The /ModAck output can be used to acknowledge a set module error. The acknowledgment is made in the bus master by an appropriate command ("Quit Peripheral Error"; 0714_{hex}).

A Technical appendix

Table A-1 Recommended operating conditions

Symbol	Parameters	Min.	Max.	Unit
V_{dd}	DC supply voltage	4.5	5.5	V
I_{maxSUP}	Current consumption[a]	–	40	mA
I_{addGND}	Additional current consumption for analog output	–	180	mA
T_A	Industrial operating temperature	-40	+85	°C

a. No DAC, reset cell, oscillator, bus operation (500 kbps), no I/O

Table A-2 Electrical I/O data

Symbol	Description	Parameters	Min.	Max.	Unit
	CMOS inputs CI, CIp				
V_{CIH}	CMOS input level high		–	3.5	V
V_{CIL}	CMOS input level low		1.5	–	V
	CMOS Schmitt trigger input STC, STCp				
V_{TH+}	Positive threshold		3.30	3.60	V
V_{TH-}	Negative threshold		1.35	1.70	V
V_H	Hystheresis		1.60	–	V
	TTL Schmitt trigger input BD4				
V_{TH+}	Positive threshold		1.80	2.05	V
V_{TH-}	Negative threshold		0.80	1.20	V
V_H	Hystheresis		0.6	–	V
	CMOS output B2				
V_{COH}	Output voltage high	I_{COmax}	4.0	–	V
V_{COL}	Output voltage low	$-I_{COmax}$	–	0.5	V
I_{COmax}	Minimum output current		2		mA
	Driver outputs B4, BD4				
V_{DOH}	Output voltage high	I_{DOmax}	3.8	–	V
V_{DOL}	Output voltage low	$-I_{DOmax}$	–	0.4	V
I_{DOmax}	Minimum output current		4	–	mA
	Driver outputs B8				
V_{DOH}	Output voltage high	I_{DOmax}	3.8	–	V
V_{DOL}	Output voltage low	$-I_{DOmax}$	–	0.4	V
I_{DOmax}	Minimum output current		8	–	mA
	Open drain outputs OD8				
V_{DOL}	Output voltage low	$-I_{DOmax}$	–	0.4	V

Table A-2 Electrical I/O data (continued)

Symbol	Description	Parameters	Min.	Max.	Unit
I_{DOmax}	Minimum output current		8	–	mA
	Pull-up resistor				
R_{pup}	Resistance		5	15	kΩ
	Output conditions				
C_L	Load capacitance		50	100	pF
t_{sw}	Switching frequency		–	1	MHz

A 1 ID code specification (extract)

Table A-3 Extract from the ID code specification

Description of module function		ID code (dec)	ID code (hex)
Bus terminal modules (BK)			
BK with 2-wire local bus branch	BK-LB	8	08
BK with 2-wire local bus branch and device-orientated diagnostics	BK-LBD	4	04
BK with 2-wire remote bus branch	BK-RB	12	0C
Remote bus device (digital)			
Digital output modules	DO	1	01
Digital input modules	DI	2	02
Digital input/output modules	DIO	3	03
Profile-compliant digital output modules	PROFILE DO	13	0D
Profile-compliant digital input modules	PROFILE DI	14	0E
Profile-compliant digital input/output modules	PROFILE DIO	47	2F
ISO valve manifolds	ISO valve manifolds	5	05
Remote bus device (analog)			
Analog output modules	AO	49	31
Analog input modules	AI	50	32
Analog input/output modules	AIO	51	33
Profile-compliant analog output modules	PROFILE AO	53	35
Profile-compliant analog input modules	PROFILE AI	58	3A
Profile-compliant analog input/output modules	PROFILE AIO	59	3B
ENCOM with input data	ENCOM	54	36
ENCOM with input and output data	ENCOM	55	37
Remote bus devices with parameter channel			
Modules with parameter channel (2 PCP words) *)	Parameter channel	240	F0

Table A-3 Extract from the ID code specification (continued)

Description of module function		ID code (dec)	ID code (hex)
Modules with parameter channel (4 PCP words) *)	Parameter channel	241	F1
Modules with parameter channel (1 PCP word)	Parameter channel	243	F3
DRIVECOM (2 PCP words) *)	DRIVECOM	224	E0
DRIVECOM (4 PCP words) *)	DRIVECOM	225	E1
DRIVECOM (1 PCP word)	DRIVECOM	227	E3
ENCOM (2 PCP words) *)	ENCOM	244	F4
ENCOM (4 PCP words) *)	ENCOM	245	F5
ENCOM (1 PCP word)	ENCOM	247	F7
Profile-compliant modules (2 PCP words) *)	Profile PA channel	228	E4
Profile-compliant modules (4 PCP words) *)	Profile PA channel	229	E5
Profile-compliant module (1 PCP word)	Profile PA channel	231	E7
"µP_Not_Ready" (with register latching) remote bus *)	Special	56	38
"µP_Not_Ready" (for re-initialization) remote bus *)	Special	60	3C
Local bus device (digital)			
Digital output modules	DO	189	BD
Digital input modules	DI	190	BE
Digital input/output modules	DIO	191	BF
Digital INTERBUS Loop output modules	IBS Loop DO	177	B1
Digital INTERBUS Loop input modules	IBS Loop DI	178	B2
Digital INTERBUS Loop input/output modules	IBS Loop DIO	179	B3
Profile-compliant digital output modules	PROFILE DO	181	B5
Profile-compliant digital input modules	PROFILE DI	182	B6
Profile-compliant digital input/output modules	PROFILE DIO	183	B7
Wrenching controllers	Wrench. contr.	187	BB
Local bus device (analog)			
Analog output modules	AO	125	7D
Analog output modules with alarm inputs **)	AIO^2	91	5B
Analog input modules	AI	126	7E
Analog input modules with configuration outputs **)	AI^2O	95	5F
Analog input/output modules	AIO	127	7F
Analog input and output modules with alarm inputs and configuration outputs **)	AI^2O^2	83	53
Analog INTERBUS Loop output modules	IBS Loop AO	113	71
Analog INTERBUS Loop output modules with alarm inputs **)	IBS Loop AIO^2	107	6B
Analog INTERBUS Loop input modules	IBS Loop AI	114	72
Analog INTERBUS Loop input modules with configuration outputs **)	IBS Loop AI^2O	111	6F

Table A-3 Extract from the ID code specification (continued)

Description of module function		ID code (dec)	ID code (hex)
Analog INTERBUS Loop input and output modules	IBS Loop AIO	115	73
Analog INTERBUS Loop input and Loop output modules with alarm inputs and configuration outputs **)	IBS Loop AI^2O^2	99	63
Profile-compliant analog output modules	PROFILE AO	121	79
Profile-compliant analog input modules	PROFILE AI	122	7A
Profile-compliant analog input/output modules	PROFILE AIO	123	7B
ENCOM with input data	ENCOM	102	66
ENCOM with input and output data	ENCOM	103	67
Local bus devices with parameter channel			
Modules with parameter channel (2 PCP words) *)	Parameter channel	220	DC
Modules with parameter channel (4 PCP words) *)	Parameter channel	221	DD
Modules with parameter channel (1 PCP word)	Parameter channel	223	DF
DRIVECOM (2 PCP words) *)	DRIVECOM	192	C0
DRIVECOM (4 PCP words) *)	DRIVECOM	193	C1
DRIVECOM (1 PCP word)	DRIVECOM	195	C3
ENCOM (2 PCP words) *)	ENCOM	212	D4
ENCOM (4 PCP words) *)	ENCOM	213	D5
ENCOM (1 PCP word)	ENCOM	215	D7
Profile-compliant modules (2 PCP words) *)	Profile PA channel	216	D8
Profile-compliant modules (4 PCP words) *)	Profile PA channel	217	D9
Profile-compliant module (1 PCP word)	Profile PA channel	219	DB
"µP_Not_Ready" (with register latching), local bus *)	Special	120	78
"µP_Not_Ready" (for re-initialization) local bus *)	Special	108	6C
"µP_Not_Ready" (for re-initialization), Loop *)	Special	104	68

*) This ID code is only supported by INTERBUS masters with firmware 4.0 or later.

**) This ID code is only supported by controller boards of Generation 4.5 or later.

A 2 General processing information

These guidelines do not necessarily specify extreme conditions which must be observed for safety reasons for the named surface-mounted components (IBS SUPI 3 OPC and IBS SUPI 3 LS) mentioned. In may cases, the housings withstand much higher temperatures than standard PCBs. These guidelines are intended to create soldering conditions permitting high-quality design and minimum improvement work.

A 2.1 Storage

Table A-4 Storage

Symbol	Parameters	Value	Unit
T_{stg}	Storage temperature	5 to 30	°C
RH_{stg}	Relative humidity for storage	30 to 60	%

A 2.2 Processing time

We recommend using the ASICs within two years of delivery. Proper storage of the components in an unopened package is required for good processing.

If the ASICs are packaged in dry packs and the moisture content is OK, according to HIC, the ASICs do not have to be dried before use. If this is not the case, the ASICs can be treated according to IPC/JEDEC J-STD-20....

A 2.3 Soldering

For information on soldering the surface-mounted component described in this manual (IBS SUPI 3 OPC and IBS SUPI 3 LS), please refer to the "**IPC/JEDEC J-STD-020...JOINT INDUSTRY STANDARD)**" document.

This document is available upon request. Please contact Phoenix Contact.

A 3 Length code specification

Table A-5 ID code data length

ID12	ID11	ID10	ID9	ID8	Data length	Firmware version*
0	0	0	0	0	0 words	
0	0	0	0	1	1 word	
0	0	0	1	0	2 words	
0	0	0	1	1	3 words	
0	0	1	0	0	4 words	
0	0	1	0	1	5 words	
0	0	1	1	0	8 words	
0	0	1	1	1	9 words	
0	1	0	0	0	1 nibble	4.0
0	1	0	0	1	1 byte	4.0
0	1	0	1	0	Reserved	
0	1	0	1	1	3 bytes	4.0
0	1	1	0	0	Reserved	
0	1	1	0	1	2 bits	4.40
0	1	1	1	0	6 words	3.2
0	1	1	1	1	7 words	3.2
1	0	0	0	0	Reserved	
1	0	0	0	1	26 words	3.7
1	0	0	1	0	16 words	3.2
1	0	0	1	1	24 words	3.2
1	0	1	0	0	32 words	3.2
1	0	1	0	1	10 words	3.2
1	0	1	1	0	12 words	3.2
1	0	1	1	1	14 words	3.2
1	1	x	x	x	Reserved	

* The data length is supported by the INTERBUS master with the specified firmware version or later.

The length entry determines the data register length of the entire INTERBUS device - that means the sum of the registers configured from the SUPI and possible external registers present. The physical data length of the SUPI to be set using C0-C3 and possibly used external register must match the logical data length to be set using ID8-ID12, even if the chip was reconfigured with software afterwards (see Section "SET register" on page 3-20).

B Wiring examples

The following applies for all wiring examples:

– All resistors have a tolerance of ±1%, maximum.
– All capacitors have a tolerance of ±20%, maximum.
– Electrical isolation has to be at least 500 VAC
– Only components from the "Conformity Test and Certification V2.0" of the INTERBUS Club are used.

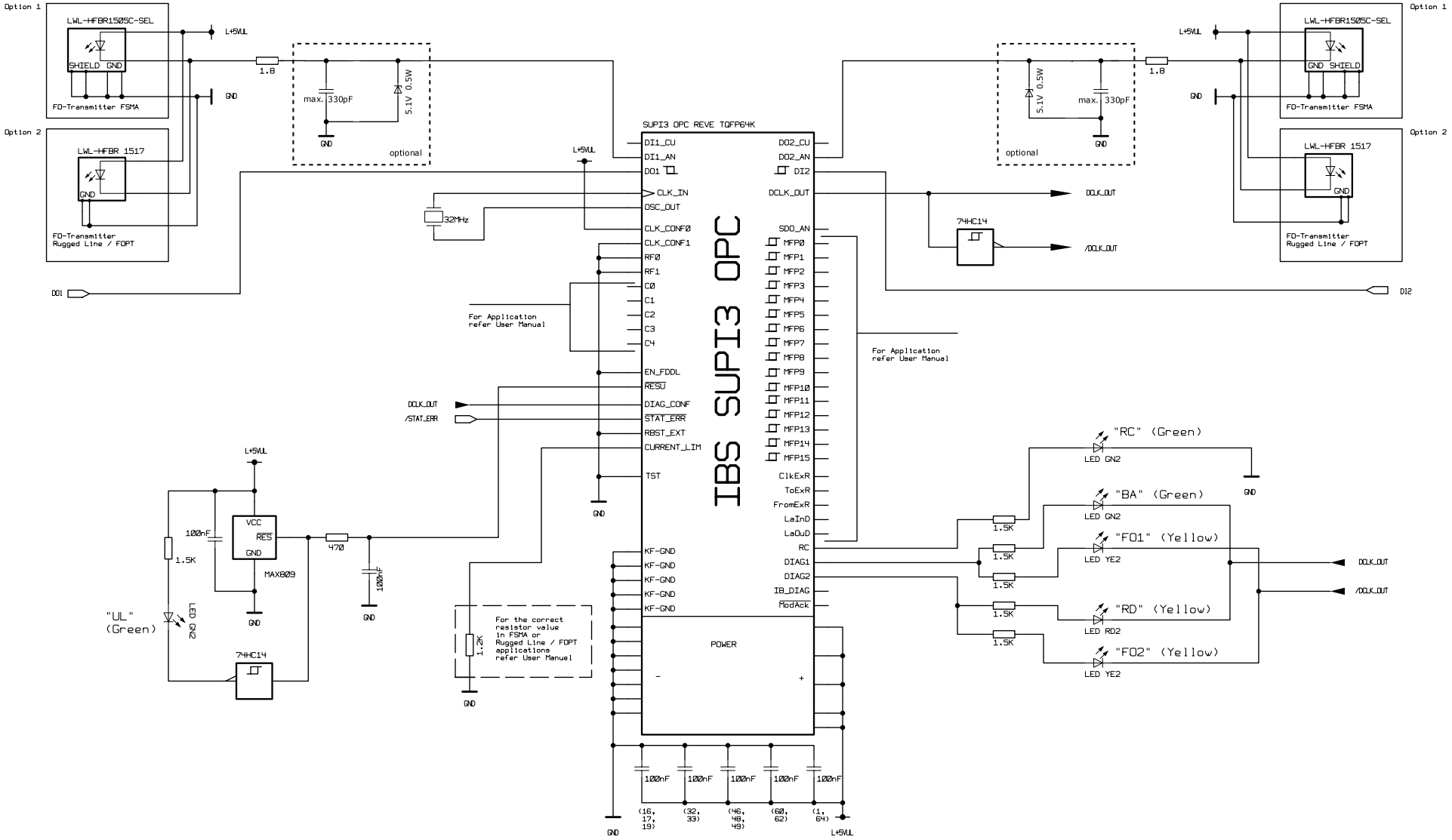
The circuit diagrams were prepared with the greatest possible care. Phoenix Contact does not guarantee the correctness of the circuit diagrams.

The capacitor (1 nF, ceramic) illustrated in the application circuit diagram "Application optical fiber remote bus" (see next page) is not required due to a redesign of fiber optic transmitter diodes. **It must no longer be installed in the INTERBUS interface. If, to optimize EMC, a capacitor has to be used instead, then its capacitance value must not exceed 330 pF.** Please refer to the application circuit diagram for the location of the critical capacitor.

application optical fibre remote bus

FO-Remotebus IN Transmitter Interface

FO-Remotebus OUT Transmitter Interface

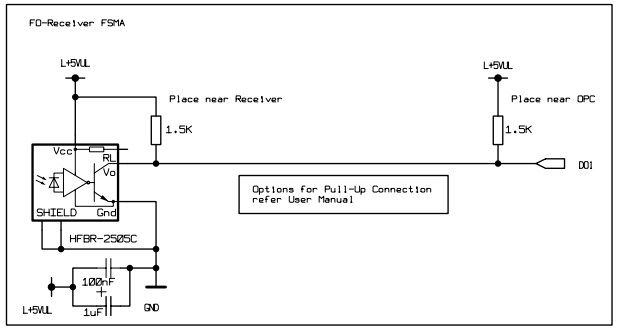


Sample Schematic				Masstab:									
Remotebus Application 500kBd with Fiber Optic Electrical Wiring SUPI3-OPC		Anzahl Blaetter: 2	Blatt Nr.: 1	gepr				Version 3.1	12.03.2009	V. Lutz			
PHOENIX CONTACT	1-2	Z.Nr.:		gezel				version 3.0	01.02.2002	H.Wieneke			
		Anzahl Kopien:	Kopie Nr.:		Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.	

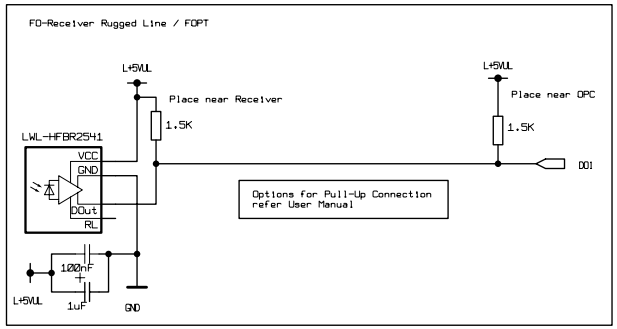
application optical fibre remote bus

FO-Remotebus IN
Receiver-Interface

Option 1

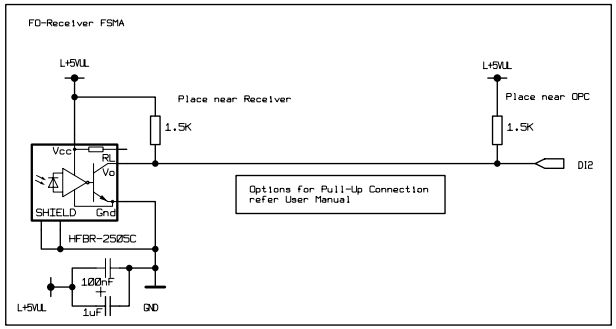


Option 2

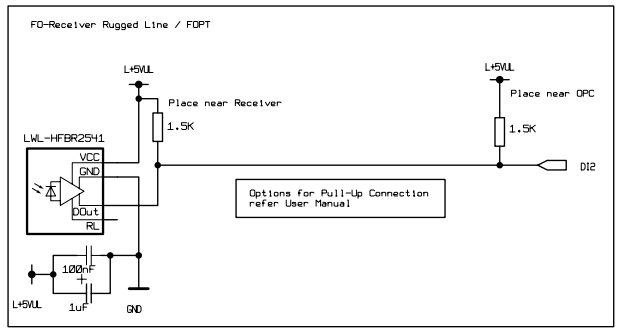


FO-Remotebus OUT
Receiver-Interface

Option 1

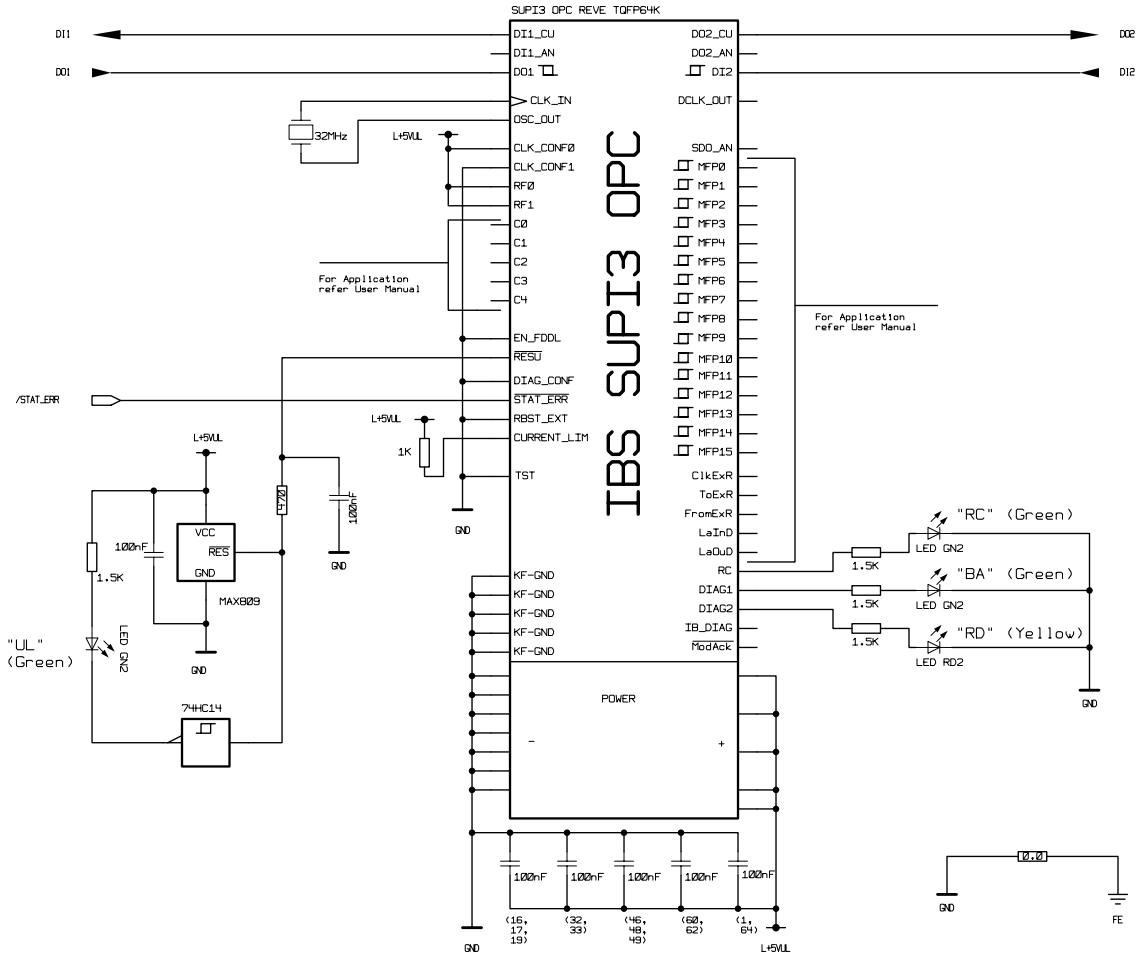


Option 2



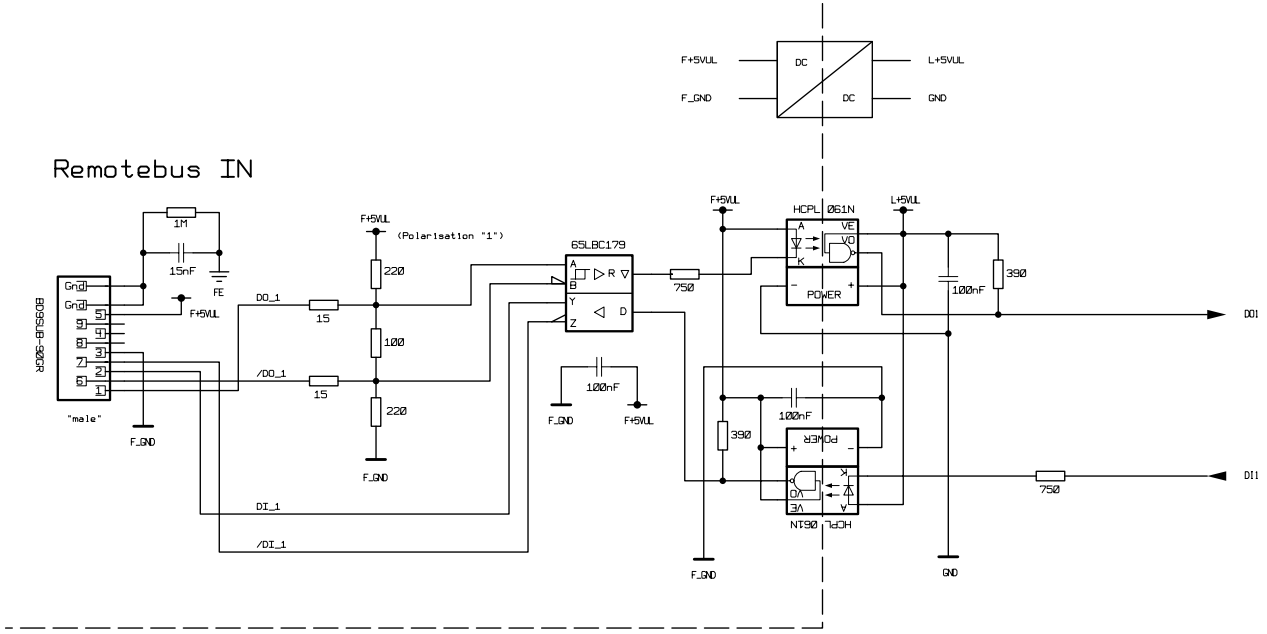
Sample Schematic					Masstab:								
Remotebus Application 500kBd with Fiber Optic Eectrical Wiring FO-Receiver-Interface			Anzahl Blaetter: 2	Blatt Nr.: 2	gepr								
PHOENIX CONTACT	2-2	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezel				version 3.0	01.02.2002	H.Wieneke		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

application remote bus with optical isolation type 1



Sample Schematic				Masstab:									
Remotebus Application 500kBd with optical isolation Electrical Wiring SUPI3-OPC		Anzahl Blaetter: 2	Blatt Nr.: 1	gepr									
PHOENIX CONTACT	1-2	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei			version 3.0	01.02.2002	H.Wieneke			
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

application remote bus with optical isolation type 1



Sample Schematic					Masstab:							
Remotebus Application 500kBd with optical isolation Electrical Wiring RS485-Interface			Anzahl Blaetter: 2	Blatt Nr.: 2	gepr							
PHOENIX CONTACT	2-2	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei			version 3.0	01.02.2002	H.Wieneke		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

C Appendix

C 1 List of figures

Section 1

Section 2

Section 3

C 2 List of tables

Section 1

Section 2

Section 3

Appendix A