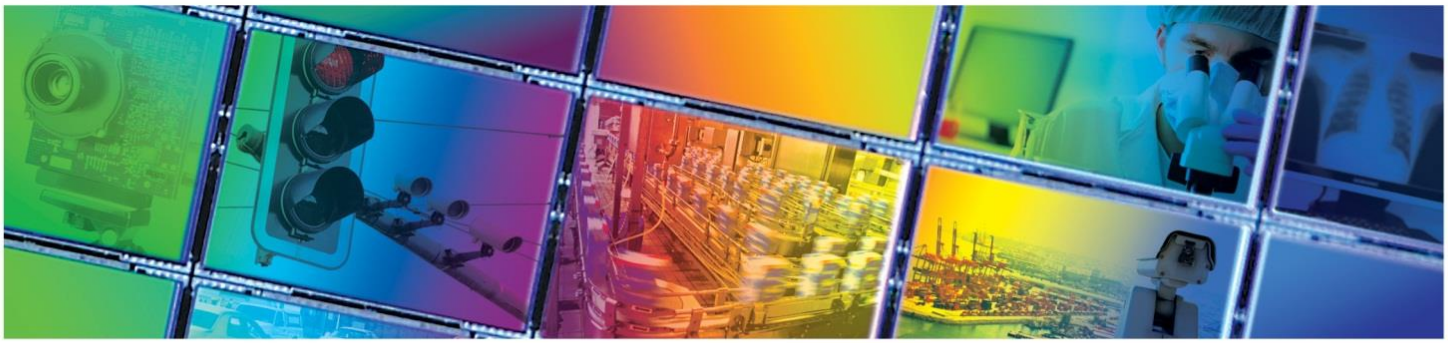
ON Semiconductor®

KAI-0330 IMAGE SENSOR

648 (H) X 484 (V) INTERLINE CCD IMAGE SENSOR



JUNE 9, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 2.1 PS-0023

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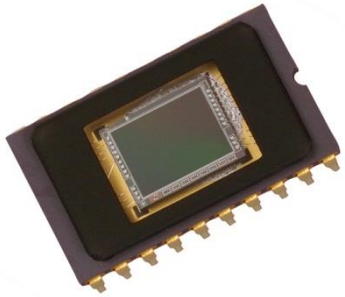
Summary Specification

KAI-0330 Image Sensor



Description

The KAI-0330 Image Sensor is a high performance, low cost, progressive scan 648(H) x 484(V) (1/2" optical format) Interline CCD Image Sensor designed specifically for demanding machine vision, surveillance, and computer input imaging applications.

Available in both single- and dual-output configurations, frame rates up to 120 Hz are available, providing the ability to design an image capture device that is up to 4X faster than traditional CCD image sensors. In addition, 9 µm square pixels with micolenses and anti-blooming structure provide high sensitivity and excellent specular reflection blooming control. Coupled with the additional benefits of electronic shutter, rapid clearing of horizontal lines for faster sub-region readout, and availability in color and monochrome configurations, this sensor is an ideal choice for challenging imaging applications.

Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	680 (H) x 496 (V)
Number of Effective Pixels	648 (H) x 484 (V)
Number of Active Pixels	648 (H) x 484 (V)
Pixel Size	9.0 µm (H) x 9.0 µm (V)
Active Image Size	5.832 mm (H) x 4.356 mm (V) 7.28 mm (diagonal) 1/2" format
Aspect Ratio	4:3
Number of Outputs	1 or 2
Saturation Signal	30,000 electrons
Output Sensitivity	11.5 µV/e^-
Quantum Efficiency -ABA (490 nm) -CBA (620 nm, 530 nm, 460 nm)	 36% 25%, 26%, 32%
Total Sensor Noise	0.5 mV rms
Dynamic Range	57 dB
Dark Current	<0.5 nA/cm^2
Dark Current Doubling Temperature	8 °C
Charge Transfer Efficiency	.99999
Blooming Suppression	>100X
Smear	.01%
Image Lag	Negligible
Maximum Data Rate	30 MHz
Package	20 pin cerDIP
Cover Glass	Clear Glass

Parameters above are specified at T = 40 °C unless otherwise noted.

Features

- Front Illuminated Interline Architecture
- Progressive Scan
- Electronic Shutter
- Integral RGB Color Filter Array (optional)
- On-Chip Dark Reference Pixels
- Low Dark Current
- Dual Output Shift Registers
- Antiblooming Protection
- Negligible Lag
- Low Smear

Applications

- Machine Vision

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0777	KAI- 0330-AAA-CP-AE-Dual Output	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Grade, Dual Output	KAI-0330D Serial Number
4H0776	KAI- 0330-AAA-CP-BA-Dual Output	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0330D Serial Number
4H0786	KAI- 0330-ABA-CB-AA-Single Output	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade, Single Output	KAI-0330SM Lot Number
4H0773	KAI- 0330-ABA-CB-AE-Dual Output	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade, Dual Output	KAI-0330DM Serial Number
4H0772	KAI- 0330-ABA-CB-BA-Dual Output	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade, Dual Output	KAI-0330DM Serial Number
4H0779	KAI- 0330-CBA-CB-AE-Dual Output	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade, Dual Output	KAI-0330DCM Serial Number
4H0778	KAI- 0330-CBA-CB-BA-Dual Output	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade, Dual Output	KAI-0330DCM Serial Number
4H0284	KEK-4H0284-KAI-0330-12-30	Evaluation Board (Complete Kit)	n/a

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

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Device Description

Architecture

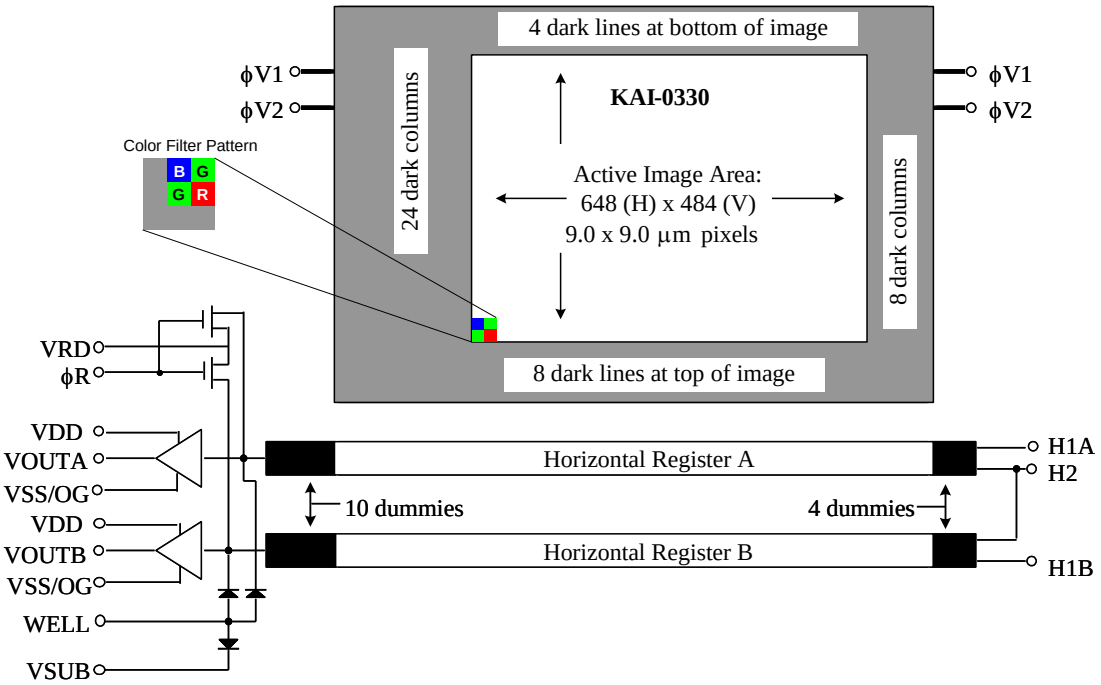

Figure 1: Functional Block Diagram

The KAI-0330 consists of 648 x 484 photodiodes, 680 vertical (parallel) CCD shift registers (VCCDs), and dual 496 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are surrounded by an additional 32 columns and 12 rows of light-shielded dark reference pixels.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (φV1). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, φH2, these charge packets are dumped over the output gate (OG, Figure 2) onto the floating diffusion (FDA and FDB, Figure 2).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when φV2 is clocked high and then low (while holding φH1A high) causing charge to be transferred from φV1 to φV2 and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this line is transferred into the B HCCD by clocking φH1A to a low state, and φH1B to a high state while holding φH2 low. After φH1A is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate.

OUTPUT STRUCTURE

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression $\Delta Vfd=\Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain.

The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of $\mu V/e^-$. After the signal has been sampled off-chip, the reset clock (φR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (VRD).

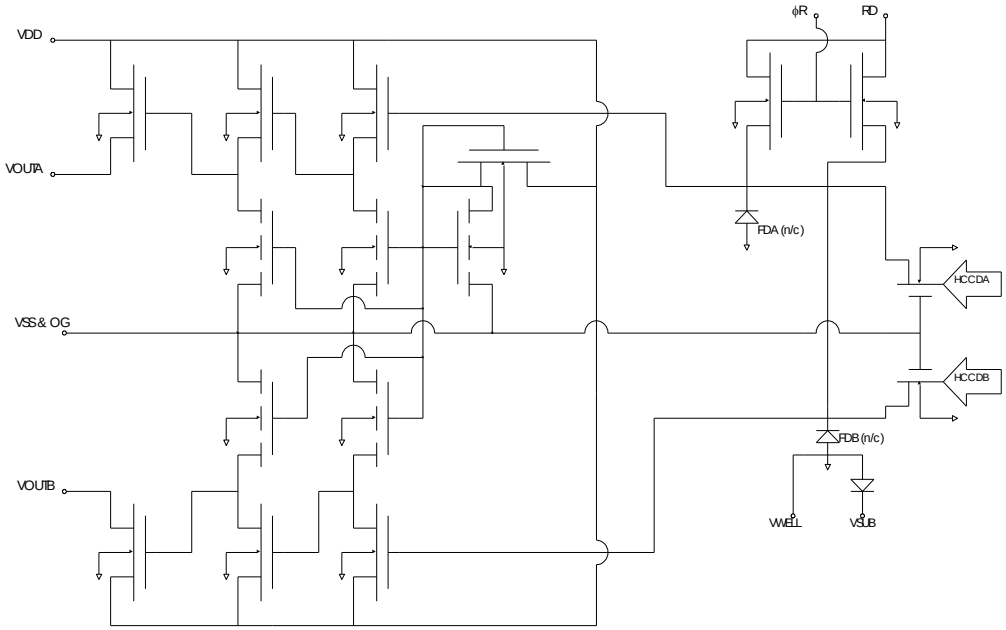

Figure 2: Output Structure

Note: For the single output version, VoutB is not active.

ELECTRONIC SHUTTER

The KAI-0330 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on φV1. The integration time is then the time between the falling edges of the substrate shutter pulse and φV1. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feed-through. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

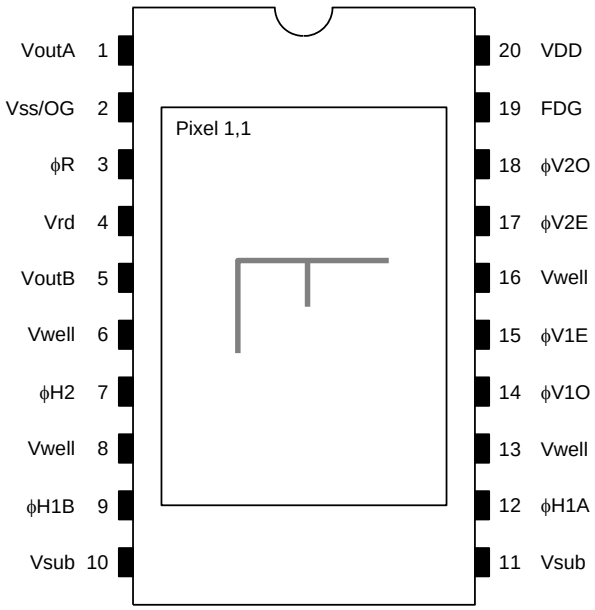

Figure 3: Pinout Diagram Top View

PIN NO.	SYMBOL	DESCRIPTION	Notes
1	VoutA	Video Output Channel A	
2	Vss/OG	Output Amplifier Return and OG	
3	φR	Reset Clock	
4	Vrd	Reset Drain	
5	VoutB	Video Output Channel B	1
6,8,13,16	Vwell	P-Well (Ground)	
7	φH2	A & B Horizontal CCD Clock - Phase 2	
9	φH1B	B Horizontal CCD Clock - Phase 1	
10,11	Vsub	Substrate	
12	φH1A	A Horizontal CCD Clock - Phase 1	
14	φV1O	Vertical CCD Clock - Phase 1, odd field	2
15	φV1E	Vertical CCD Clock - Phase 1, even field	2
17	φV2E	Vertical CCD Clock - Phase 2, even field	3
18	φV2O	Vertical CCD Clock - Phase 2, odd field	3
19	FDG	Fast Dump Gate	
20	VDD	Output Amplifier Supply	

Notes:
1. For the single output version, VoutB is not active.
2. Pins 14 and 15 must be connected together - only 1 Phase 1 clock driver is required.
3. Pins 17 and 18 must be connected together - only 1 Phase 2 clock driver is required.

Imaging Performance

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 40 ms, integration time = 40 ms and sensor temperature = 40 °C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.

Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

ELECTRO-OPTICAL FOR KAI-0330-CBA

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
F F	Optical Fill Factor		55.0		%	
E_{sat}	Saturation Exposure		0.046		$\mu J/cm^2$	1
QE_r	Red Peak Quantum Efficiency λ = 620nm		25		%	2
QE_g	Green Peak Quantum Efficiency λ = 530nm		26		%	2
QE_b	Blue Peak Quantum Efficiency λ = 460nm		32		%	2
R_{gs}	Green Photoresponse Shading		6		%	4
PRNU	Photoresponse Non-uniformity		5.0		p-p %	3
PRNL	Photoresponse Non-linearity		5.0		%	
ΔV/ΔN	Amplifier Sensitivity		11.5		$\mu V/e^-$	

Notes:
1. For λ = 530 nm wavelength, and Vsat = 350 mV.
2. Refer to typical values from Figure 4.
3. Under uniform illumination with output signal equal to 280 mV.
4. This is the global variation in chip output for green pixels across the entire chip.
5. It is recommended to use low pass filter with $\lambda_{cut\text{-}off}$ at ~ 680nm for high performance.

ELECTRO-OPTICAL FOR KAI-0330-ABA

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
F F	Optical Fill Factor		55.0		%	
Esat	Saturation Exposure		0.037		$\mu J/cm^2$	1
QE	Peak Quantum Efficiency		36		%	2
PRNU	Photoresponse Non-uniformity		5.0		p-p %	3
PRNL	Photoresponse Non-linearity		5.0		%	

Notes:
1. For λ = 550 nm wavelength, and Vsat = 350 mV.
2. Refer to typical values from Figure 5.
3. Under uniform illumination with output signal equal to 280 mV.

CCD Image Specifications

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vsat	Output Saturation Voltage		350		mV	1,2,8
I_d	Dark Current			0.5	nA	
DCDT	Dark Current Doubling Temp	7	8	10	°C	
CTE	Charge Transfer Efficiency		0.99999			2,3
f_H	Horizontal CCD Frequency			30	MHz	4
IL	Image Lag			100	e^-	5
Xab	Blooming Margin		100			6,8
Smr	Vertical Smear		0.01		%	7

Notes:
1. Vsat is the green pixel mean value at saturation as measured at the output of the device with Xab=1. Vsat can be varied by adjusting Vsub.
2. Measured at sensor output.
3. With stray output load capacitance of C_L = 10 pF between the output and AC ground.
4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
5. This is the first field decay lag measured by strobe illuminating the device at (Hsat, Vsat), and by then measuring the subsequent frame's average pixel output in the dark.
6. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that Vout rises above Vsat for irradiance levels above Hsat, as shown in Figure 7.
7. Measured under 10% (~ 100 lines) image height illumination with white light source and without electronic shutter operation and below Vsat.
8. It should be noted that there is tradeoff between Xab and Vsat.

Output Amplifier @ V_{DD} = 15V, V_{SS} = 0.0V

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vodc	Output DC Offset	——	7	——	V	1,2
Pd	Power Dissipation	——	55	——	mW	3
f_{-3db}	Output Amplifier Bandwidth	——	140	——	MHz	1,4
C_L	Off-Chip Load	——	——	10	pF	

Notes:
1. Measured at sensor output with constant current load of I_{out} = 5 mA per output.
2. Measured with VRD = 9 V during the floating-diffusion reset interval, (φR high), at the sensor output terminals.
3. Both channels.
4. With stray output load capacitance of C_L = 10 pF between the output and AC ground.

General

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vn - total	Total Sensor Noise		0.5		mV, rms	1
DR	Dynamic Range			58	dB	2

Notes:
1. Includes amplifier noise and dark current shot noise at data rates of 10 MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
2. Uses 20LOG(Vsat/Vn - total) where Vsat refers to the output saturation signal.

Typical Performance Curves

Color with Microlens Quantum Efficiency

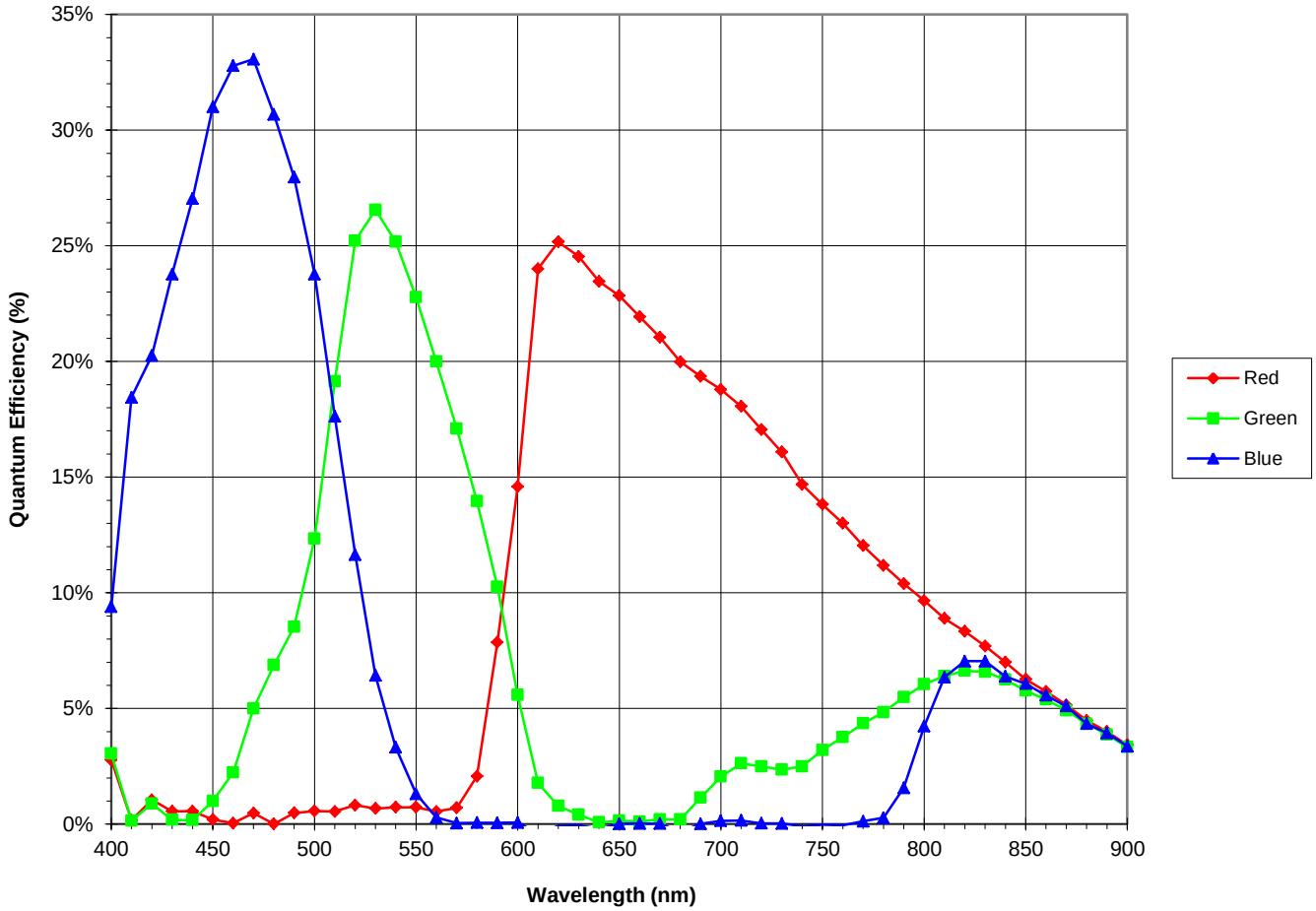

Figure 4: Nominal KAI-0330-CBA Spectral Response

MONOCHROME WITH MICROLENS QUANTUM EFFICIENCY

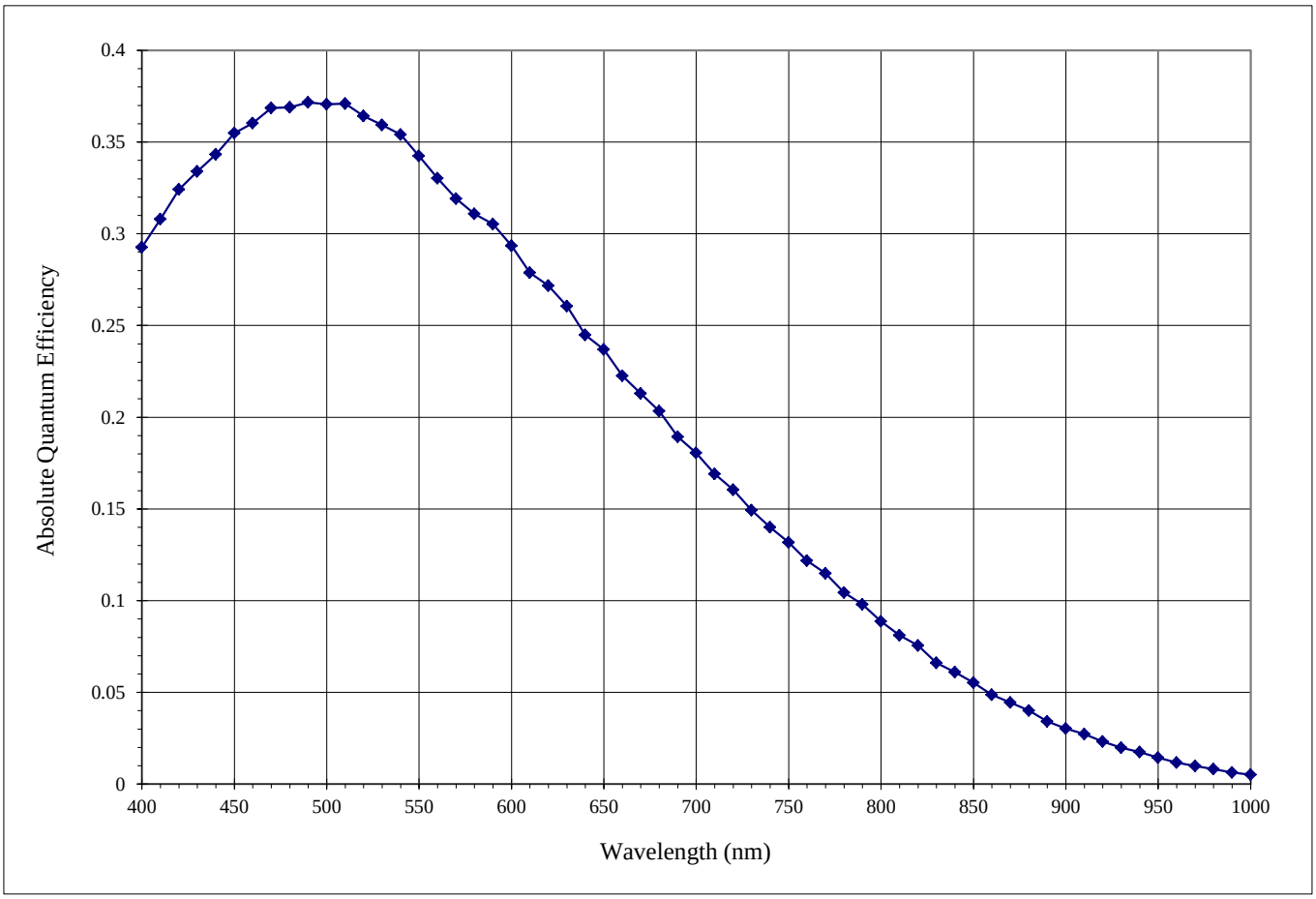

Figure 5: Nominal KAI-0330-ABA Spectral Response

Angular Quantum Efficiency

Monochrome with Microlens

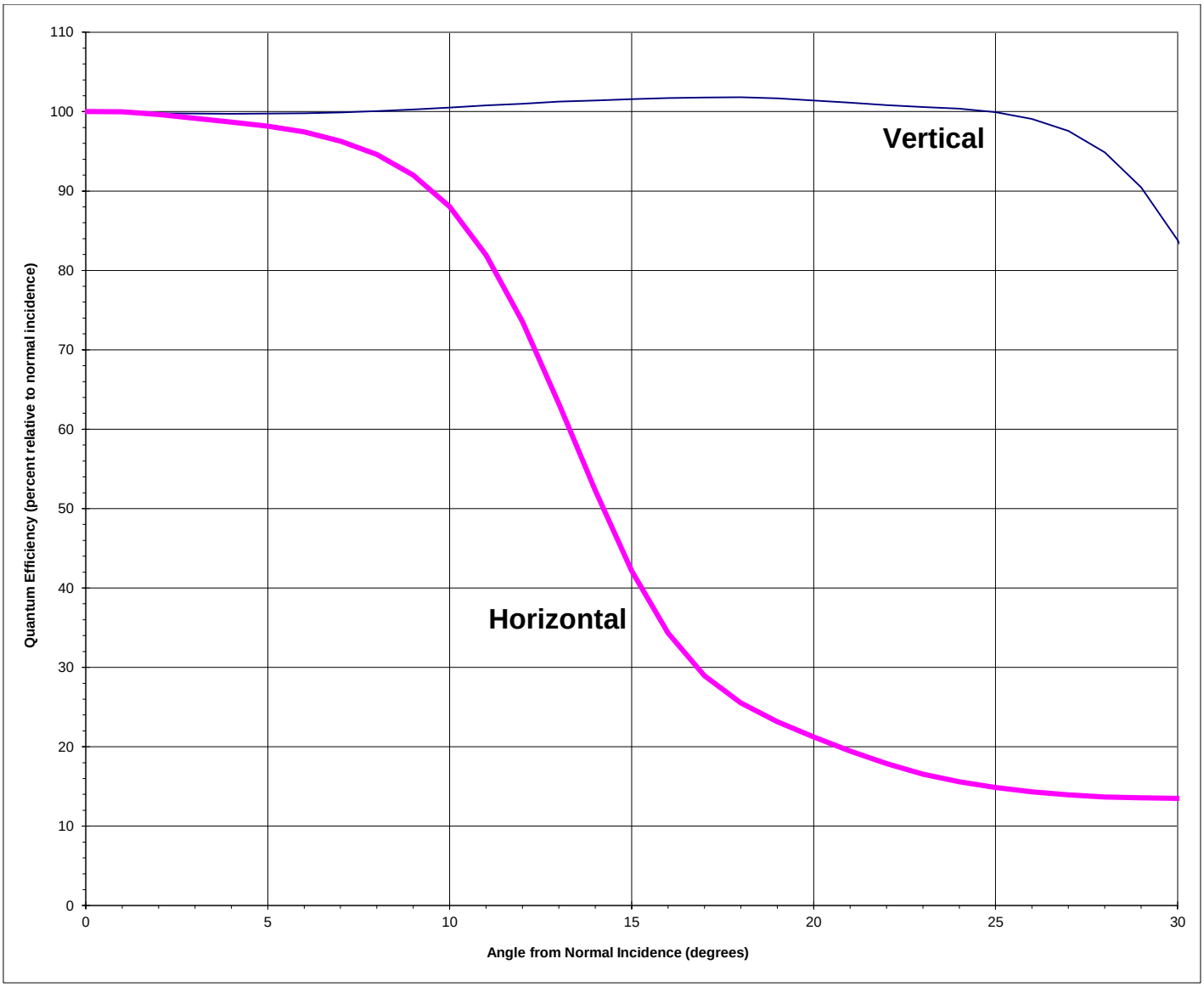

Figure 6: Angular Dependence on Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

TYPICAL PHOTORESPONSE

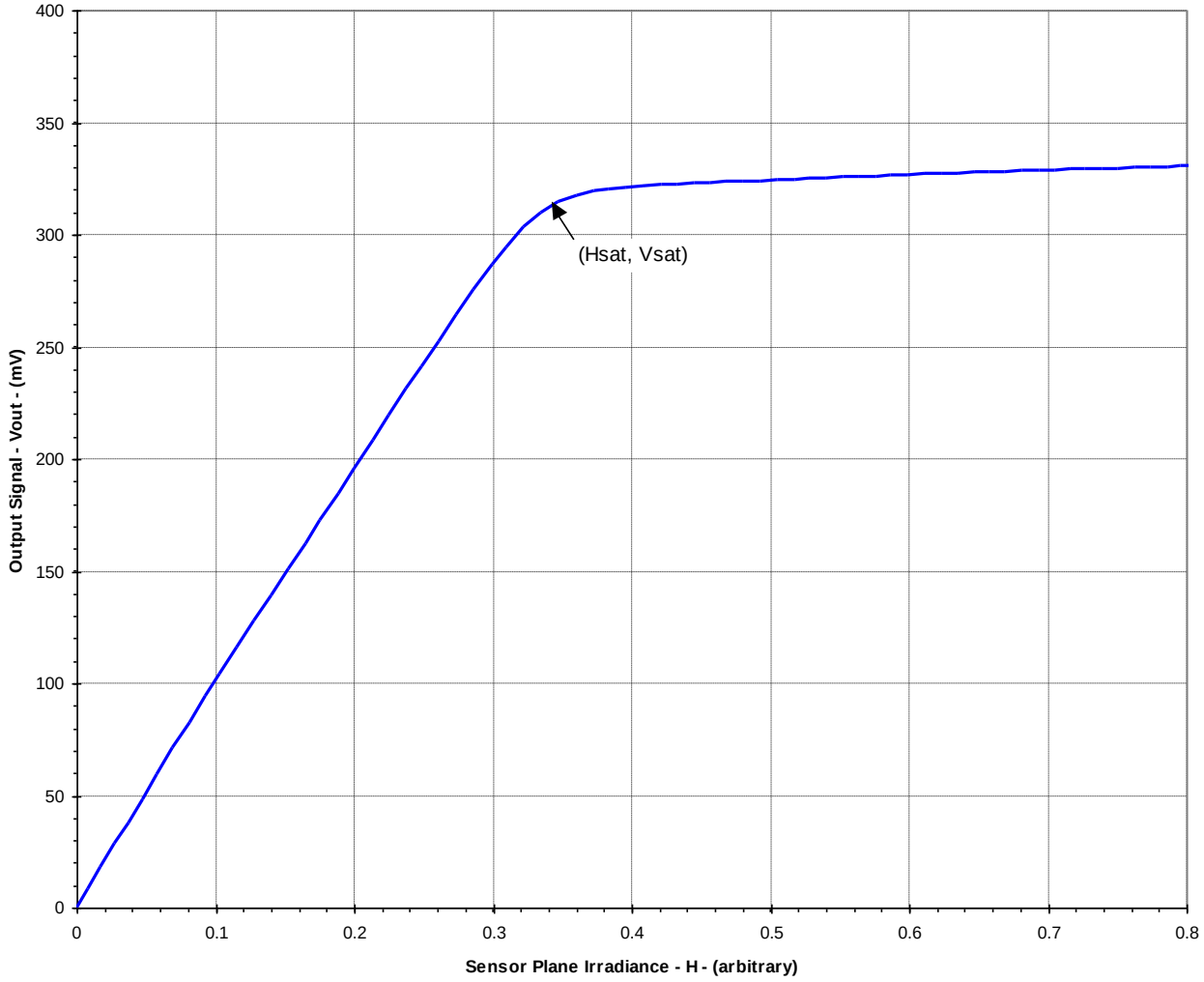

Figure 7: Typical KAI-0330 Photoresponse

Saturation Signal versus Substrate Voltage

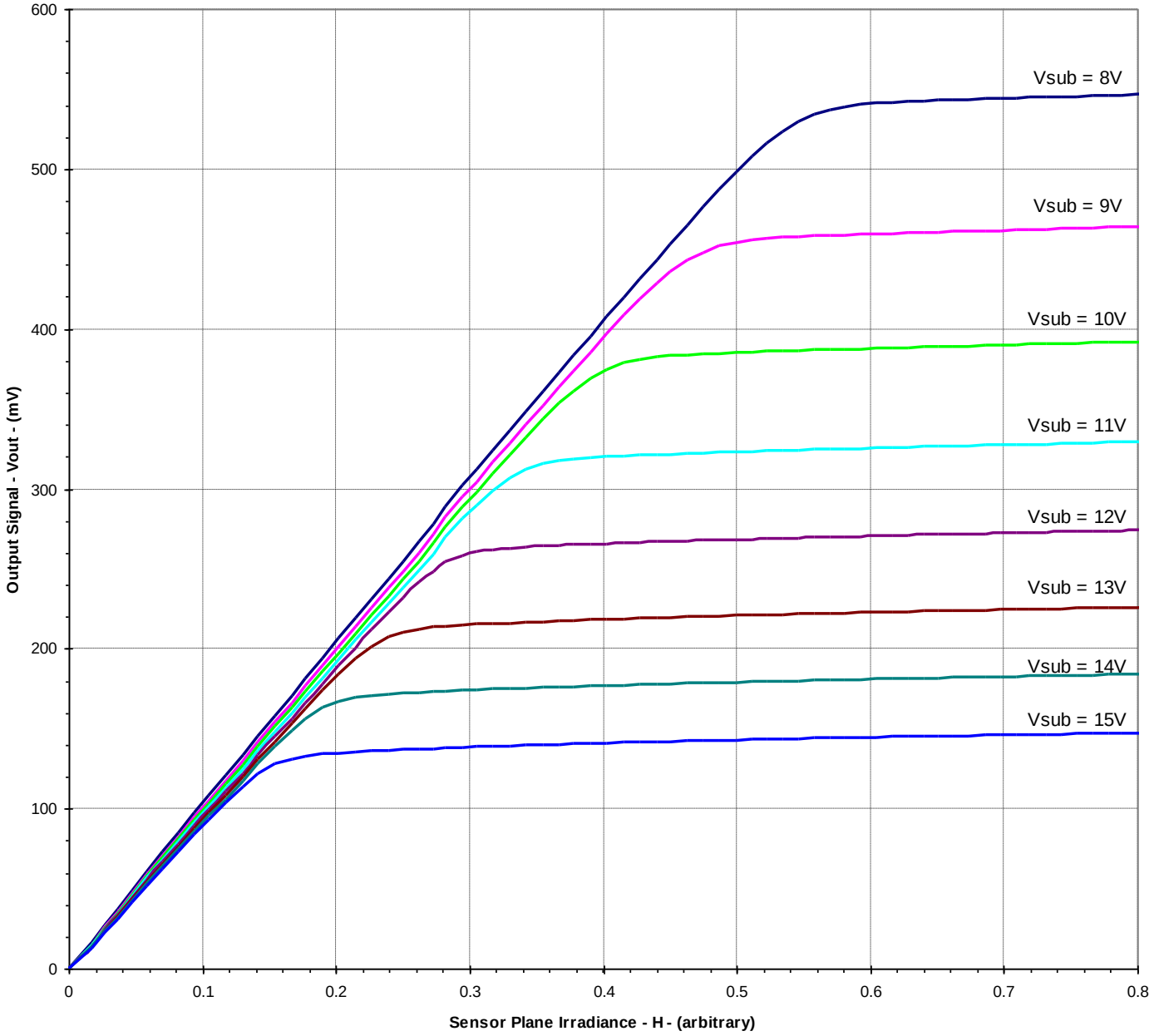

Figure 8: Example of Vsat versus Vsub

As Vsub is decreased, Vsat increases and anti-blooming protection decreases.

As Vsub is increased, Vsat decreases and anti-blooming protection increases.

Frame Rate

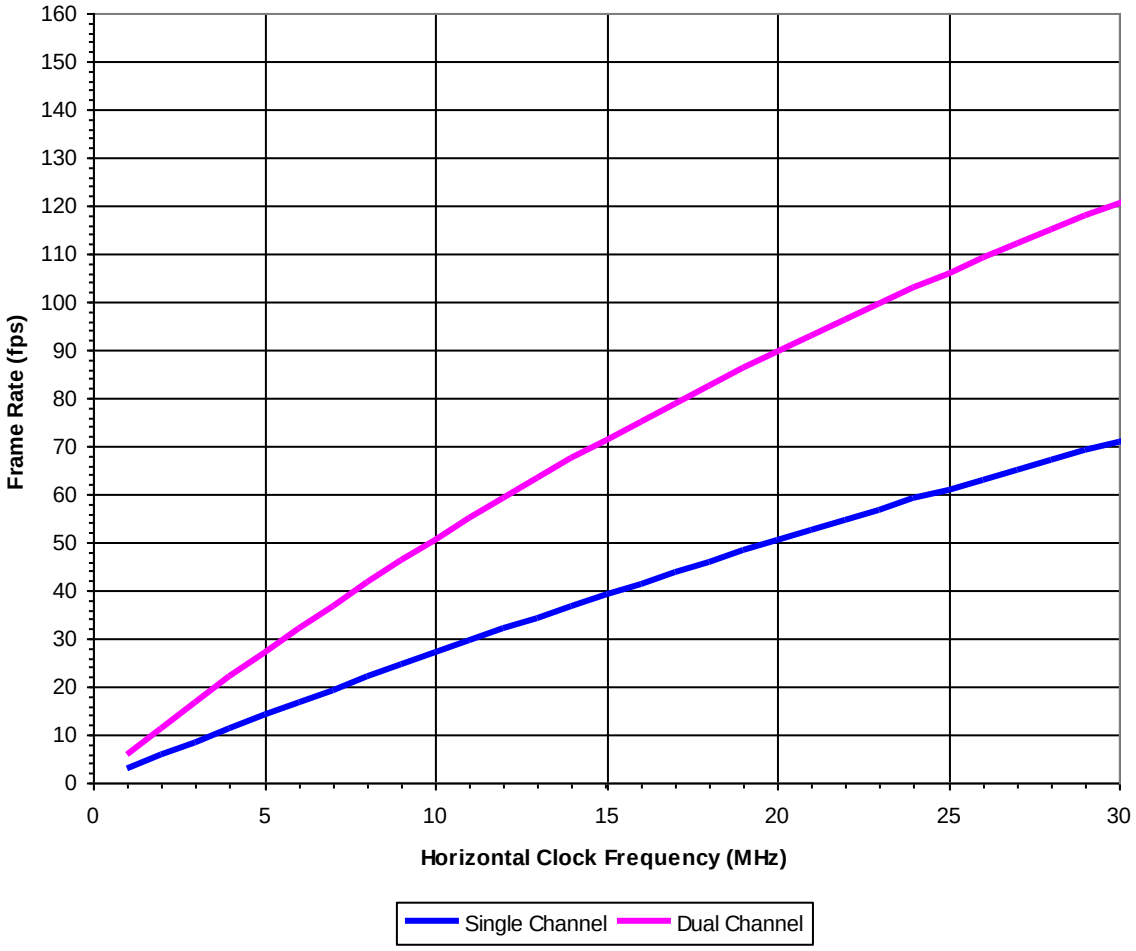

Figure 9: Frame Rate versus Horizontal Clock Frequency

Defect Definitions

Operational Conditions

Description	Symbol	Condition
Junction Temperature	T_j	40 °C
Integration Time	t_{int}	40 msec
Readout Rate	$t_{readout}$	40 msec

Specifications

Point Defects (Major)	Point Defects (Minor)	Cluster Defects	Column Defects
≤2	≤15	0	0

Defect Type	Defect Definition
Major Defective Pixel	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination at 80% of saturation.
Minor Defective Pixel	A pixel whose signal deviates by more than 6mV from the mean value of all active pixels under dark field condition.
Point Defect	An isolated defective pixel.
Cluster Defect	A group of 2 to 4 contiguous major defective pixels.
Column Defect	A group of more than 4 contiguous major defective pixels along a single column or row.

Note: No row defects are allowed.

Operation

Absolute Maximum Ratings

RATING	DESCRIPTION	MIN.	MAX.	UNITS	NOTES
Temperature (@ 10% ± 5% RH)	Operation Without Damage	-50	+70	°C	
Voltage (Between Pins)	SUB-WELL	0	+40	V	1, 5
	VRD,VDD,OG&VSS-WELL	0	+15	V	2
	VOUTA & VOUTB – WELL	0	+15	V	2
	φV1 - φV2	-12	+20	V	2
	φH1A, φH1B - φH2	-12	+15	V	2
	φH1A, φH1B, φH2, FDG - φV2	-12	+15	V	2
	φH2 - OG & VSS	-12	+15	V	2
	φR – SUB	-20	0	V	1,2,4
	All Clocks – WELL	-12	+15	V	2
Current	Output Bias Current (Iout)	----	10	mA	3

Notes:

1. Under normal operating conditions the substrate voltage should be above +7 V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Per Output, I_{out} affects the band-width of the outputs.
4. φR should never be more positive than VSUB.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

DC Operating Conditions

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	PIN IMPEDANCE5	NOTES
VRD	Reset Drain	8.5	9	9.5	V	5 pF, >1.2 MΩ	
IRD	Reset Drain Current		0.2		mA		
VSS	Output Amplifier Return & OG		0		V	30 pF, >1.2 MΩ	
ISS	Output Amplifier Return Current		5		mA		
VDD	Output Amplifier Supply	12	15.0	15.5	V	30 pF, >1.2 MΩ	
I_{out}	Output Bias Current		5	10	mA		4
WELL	P-well	——	0.0	——	V	Common	1
GND	Ground	——	0.0	——	V		1
FDG	Fast Dump Gate	-5.5	-5.0	-4.5	V	20 pF, >1.2 MΩ	2
SUB	Substrate	7	Vsub	15	V	1 nF, >1.2 MΩ	3, 7

Notes:
1. The WELL and GND pins should be connected to P-well ground.
2. The voltage level specified will disable the fast dump feature.
3. This pin may be pulsed to Ves = 40 V for electronic shuttering
4. Per output. Note also that I_{out} affects the bandwidth of the outputs.
5. Pins shown with impedances greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
6. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

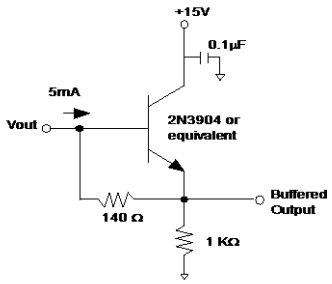

Figure 10: Recommended Output Structure Load Diagram

AC Clock Level Conditions

SYMBOL	DESCRIPTION	Level	Min.	NOM.	MAX.	UNITS	PIN IMPEDANCE
φV1	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25 nF, >1.2 MΩ
		Mid	0.0	0.2	0.4	V	
		High	8.5	9.0	9.5	V	
φV2	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25 nF, >1.2 MΩ
		High	0.0	0.2	0.4	V	
φH1A	φ1 Horizontal CCD A Clock	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φH1B[4]	φ1 Horizontal CCD B Clock (single register mode)	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
φH1B[4]	φ1 Horizontal CCD B Clock (dual register mode)	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φH2	φ2 Horizontal CCD Clock	Low	-7.5	-7.0	-6.5	V	125 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φR	Reset Clock	Low	-6.5	-6.0	-5.5	V	5 pF, > 1.2 MΩ
		High	-0.5	0.0	0.5	V	
φFDG[3]	Fast Dump Gate Clock	Low	-5.5	-5.0	-4.5	V	20 pF, > 1.2 MΩ
		High	4.5	5.0	5.5	V	

Notes:
1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
2. Pins shown with impedances greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
3. When not used, refer to DC operating condition.
4. For single register mode, set φH1B to -7.0 volts at all times rather than clocking it.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Truesense Imaging in those situations in which operating conditions meet or exceed minimum or maximum levels.

Timing

REQUIREMENT AND CHARACTERISTICS

For 30 MHz Operation

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS	NOTES	FIGURE
tφR	Reset Pulse Width		10		nsec		Figure 13
t es	Electronic Shutter Pulse Width	10	25		µsec		Figure 14
t int	Integration Time	0.1			msec	1	Figure 14
t φVh	Photodiode to VCCD Transfer Pulse Width	4	5		µsec	2	Figure 11
t cd	Clamp Delay		15		nsec		Figure 13
t cp	Clamp Pulse Width		15		nsec		Figure 13
t sd	Sample Delay		35		nsec		Figure 13
t sp	Sample Pulse Width		15		nsec		Figure 13
t rd	Vertical Readout Delay	10	——	——	µsec		Figure 11
t φV	φV1, φV2 Pulse Width	2	2.5		µsec		Figure 12
Clock Frequency t φH	φH1A, φH1B, φH2	——	——	30	MHz		Figure 13
t φAB	Line A to Line B Transfer Pulse Width	2	2.5		µsec		Figure 16
t φHd	Horizontal Delay	2	2.5		µsec		Figure 12
t φVd	Vertical Delay	25			nsec		Figure 12
t φHVES	Horizontal Delay with Electronic Shutter	1			µsec		Figure 14

Notes:

1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
2. Antiblooming function is off during photodiode to VCCD transfer.

FRAME TIMING - SINGLE REGISTER READOUT

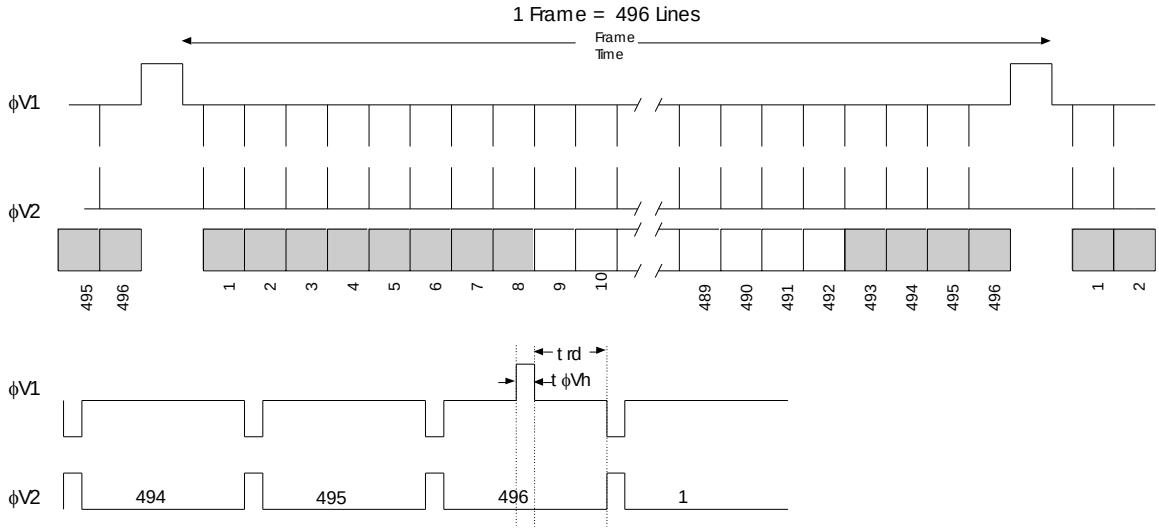

Figure 11: Frame Timing - Single Register Readout

Note: When no electronic shutter is used, the integration time is equal to the frame time.

Line Timing - Single Register Readout

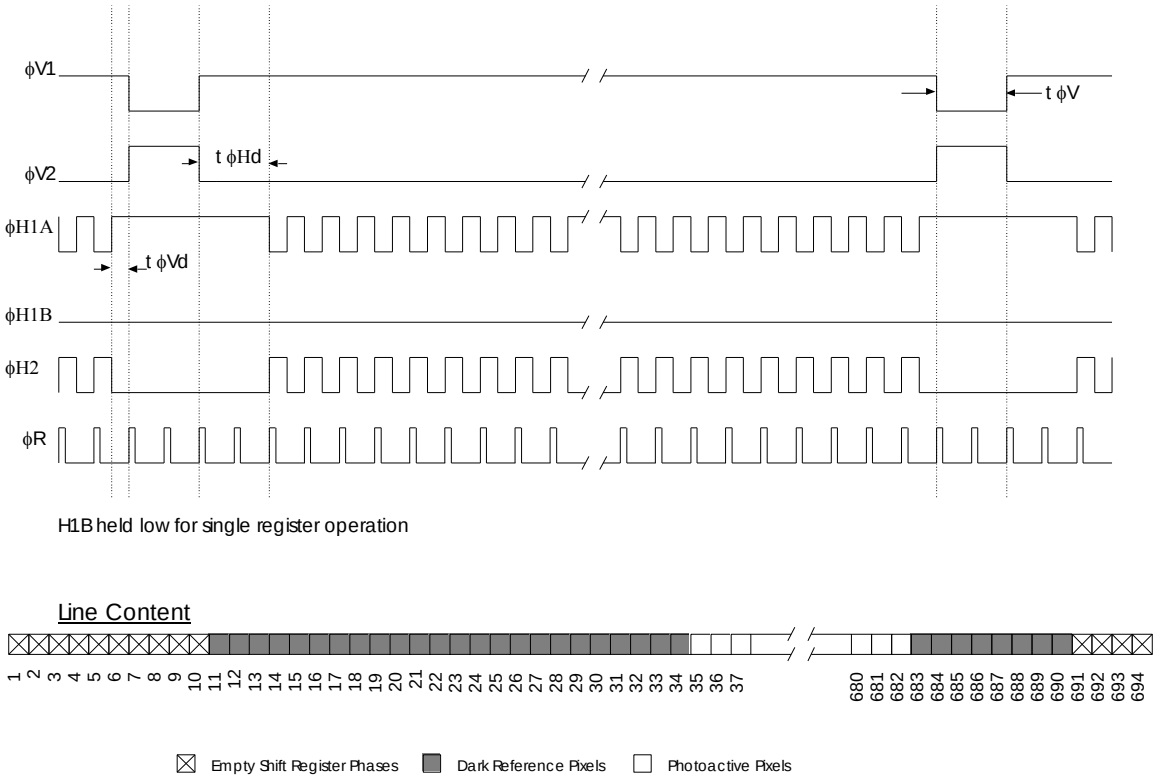

Figure 12: Line Timing - Single Register Output

Pixel Timing - Single Register Readout

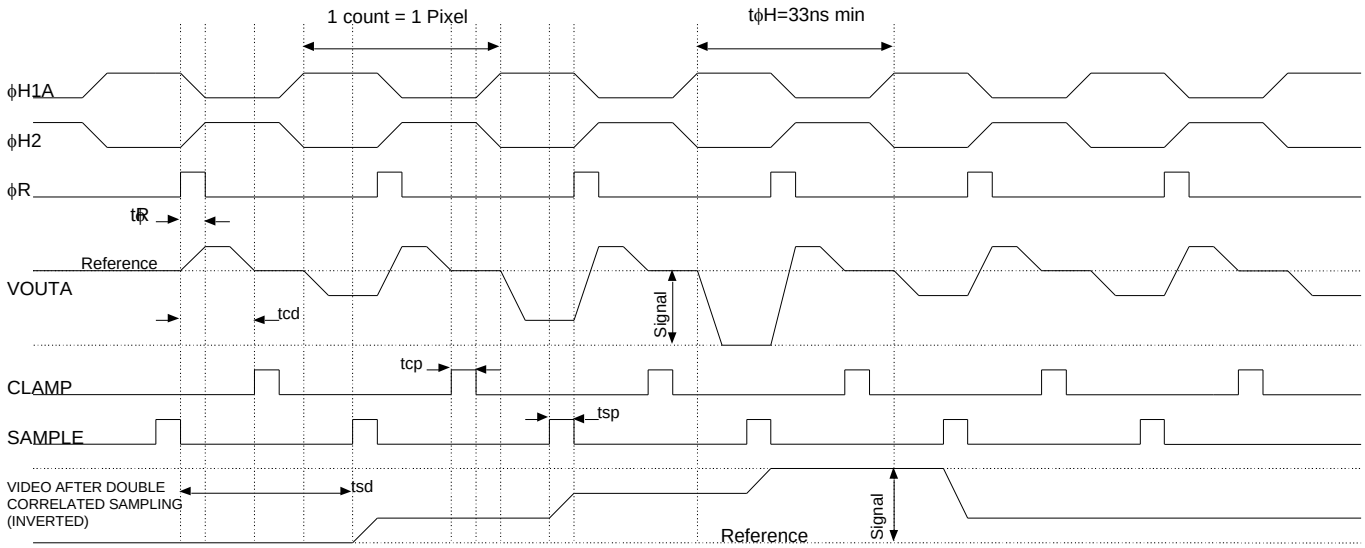

Figure 13: Pixel Timing Diagram - Single Register Readout

Electronic Shutter Timing - Single Register Readout

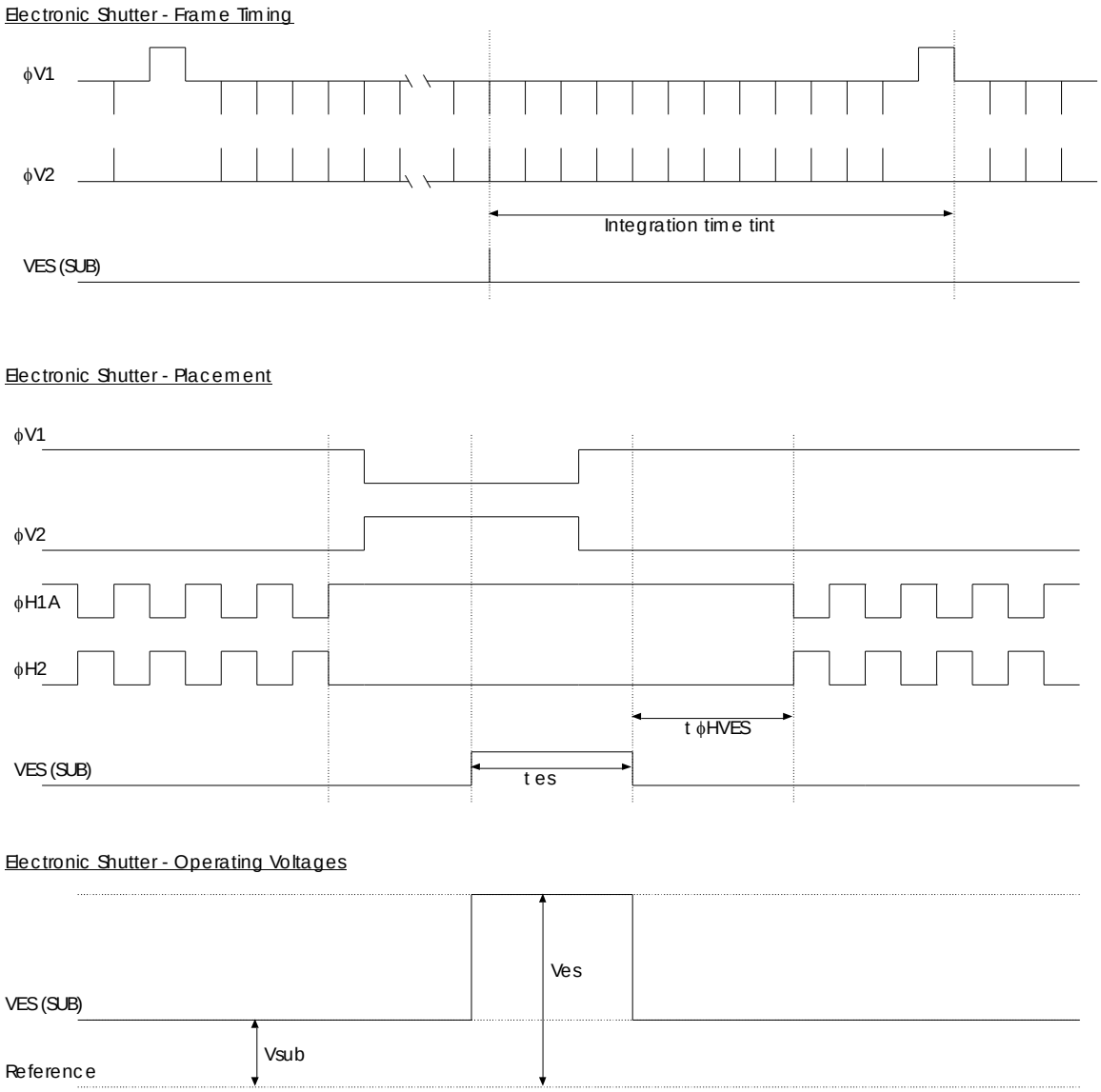

Figure 14: Electronic Shutter Timing Diagram - Single Register Readout

FRAME TIMING - DUAL REGISTER READOUT

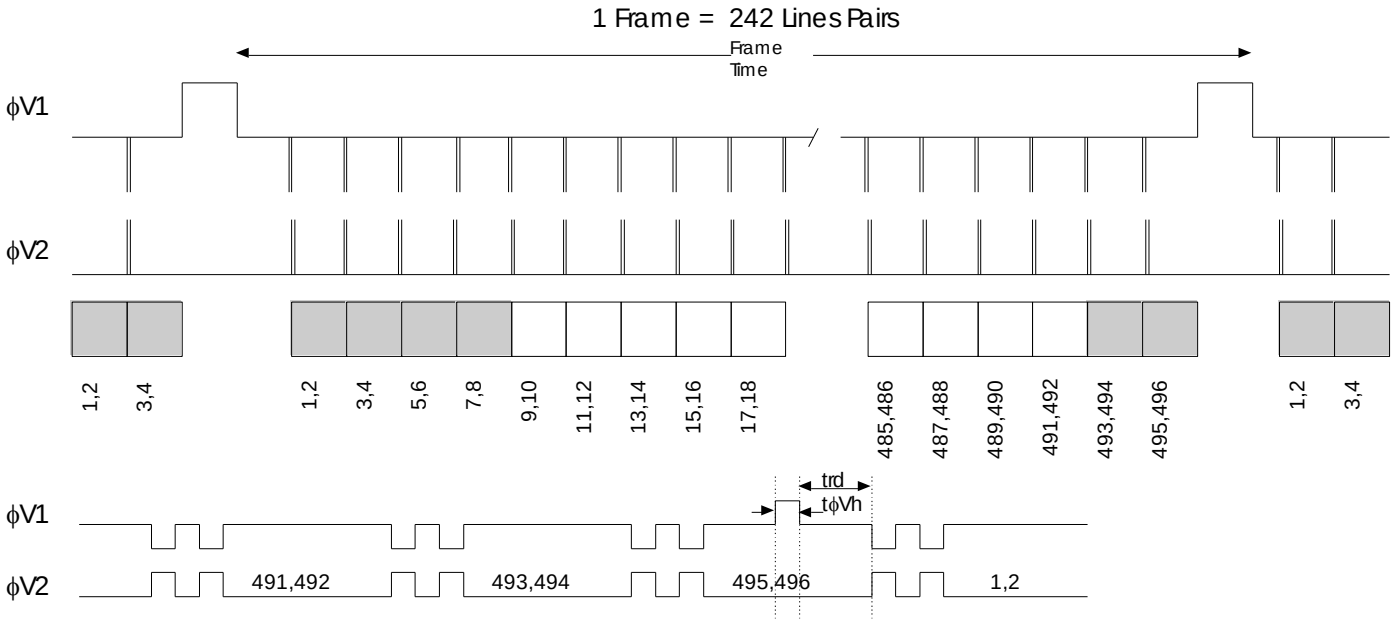

Figure 15: Frame Timing - Dual Register Readout

Note: When no electronic shutter is used, the integration time is equal to the frame time.

Line Timing - Dual Register Readout

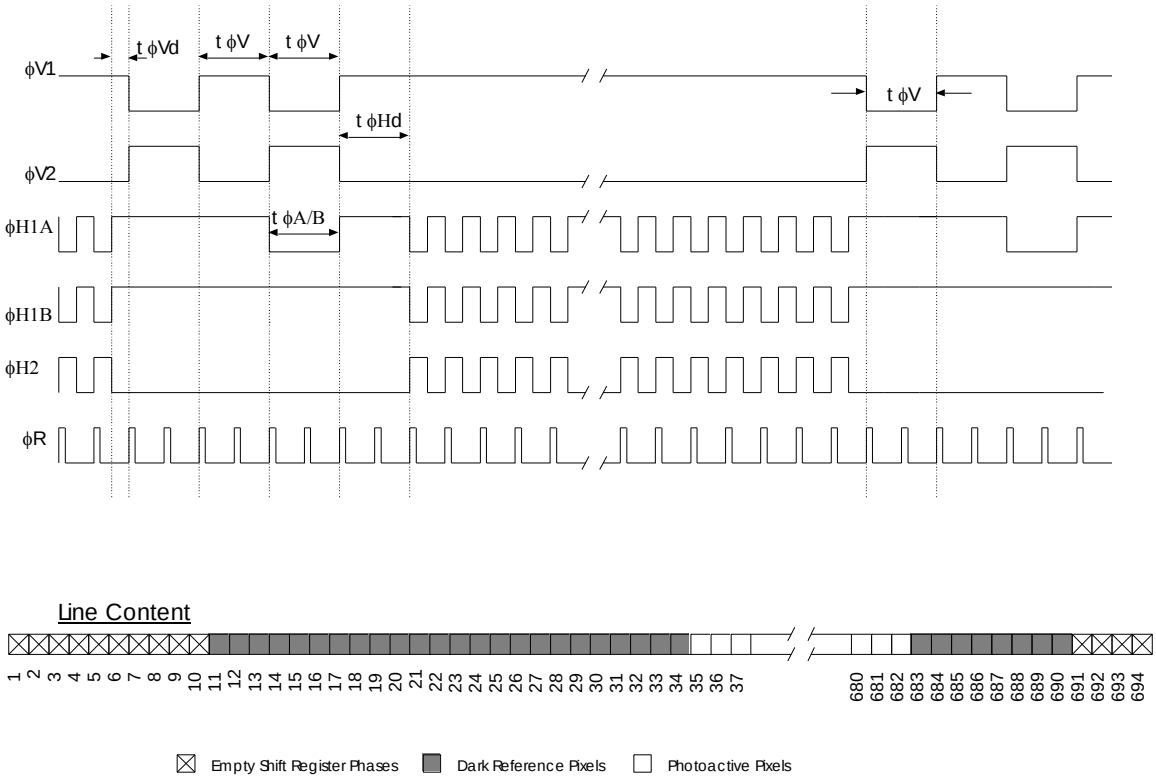

Figure 16: Line Timing - Dual Register Output

Pixel Timing - Dual Register Readout

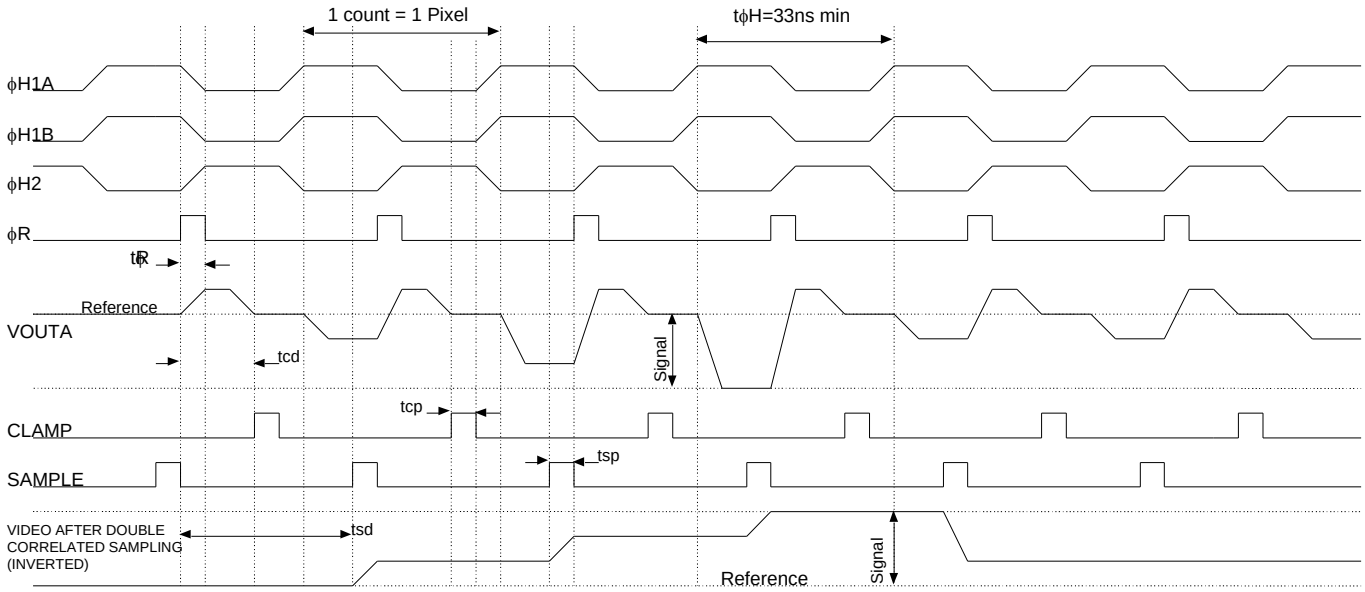

Figure 17: Pixel Timing Diagram - Dual Register Readout

Fast Dump Timing – Removing Four Lines

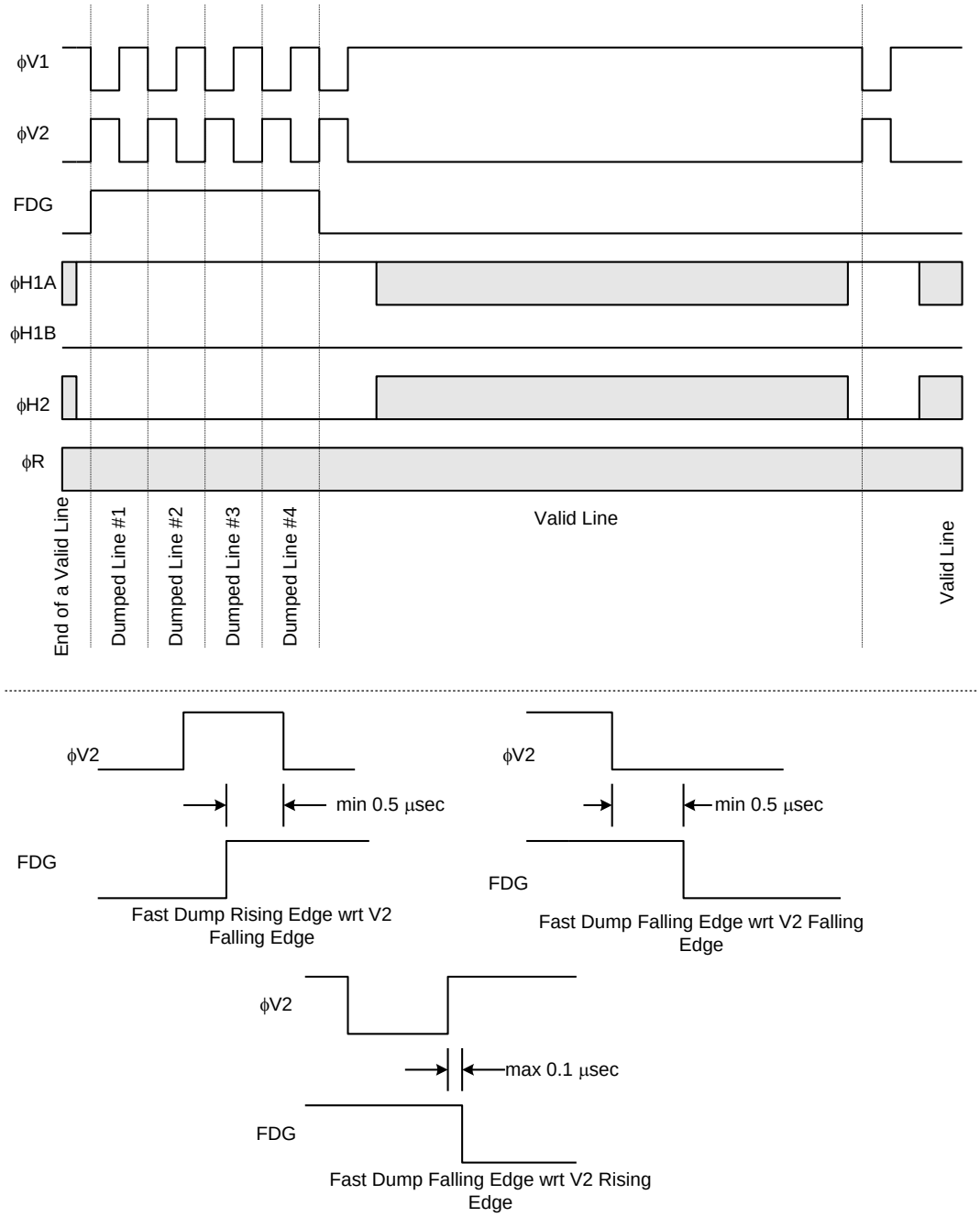

Figure 18: Fast Line Dump Timing - Removing Four Lines

Binning – Two to One Line Binning

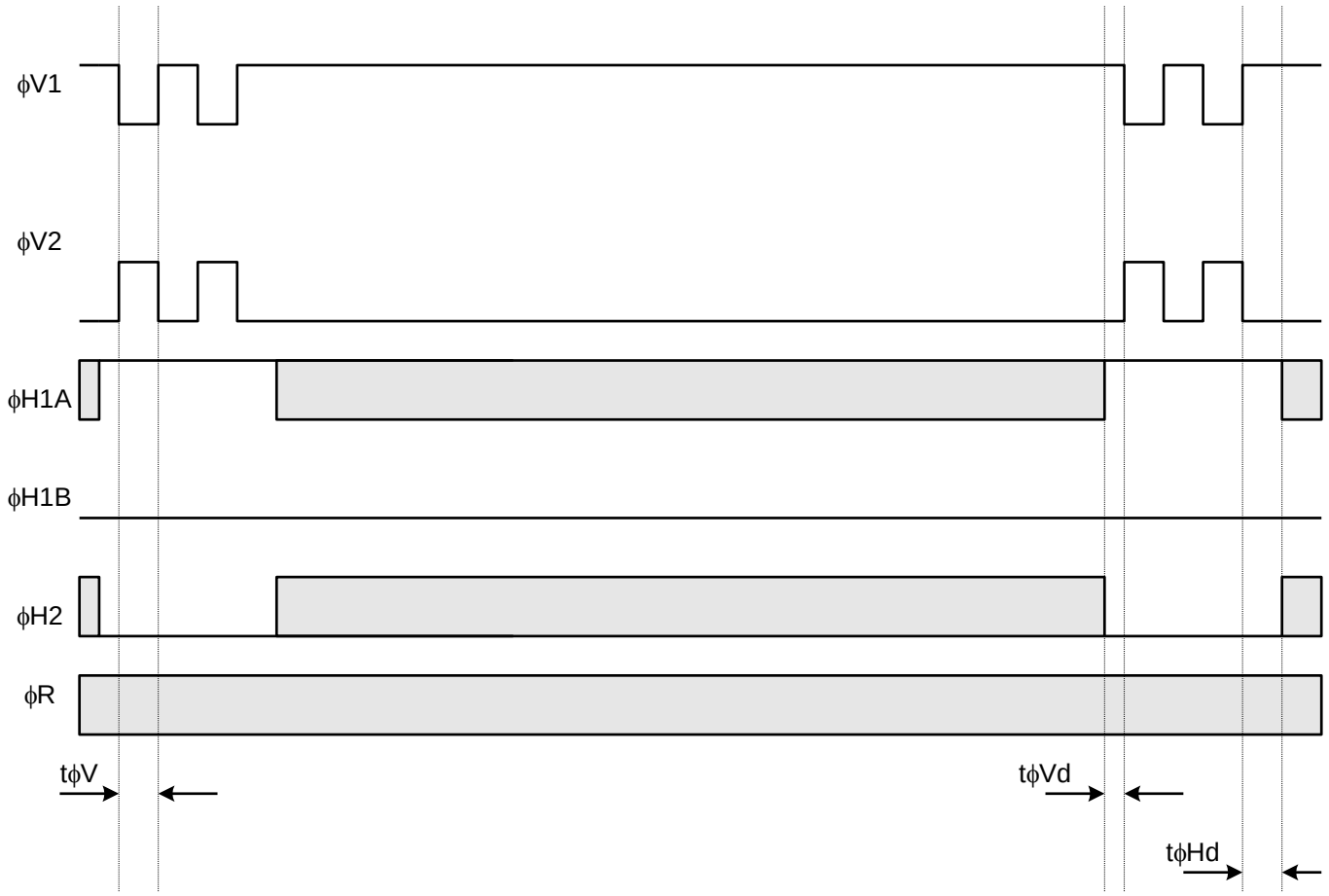

Figure 19: Binning - 2 to 1 Line Binning

TIMING – SAMPLE VIDEO WAVEFORM

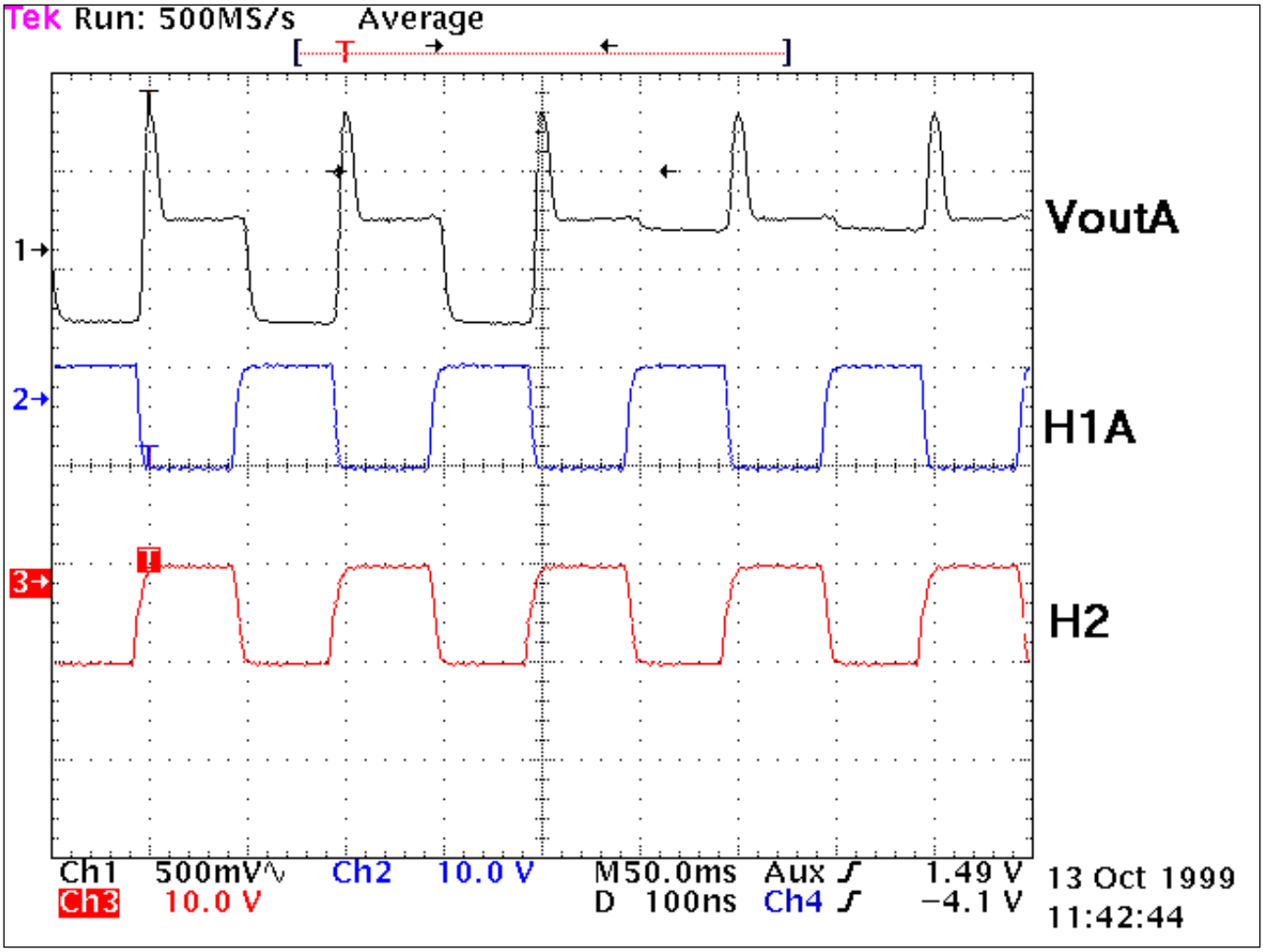

Figure 20: Sample Video Waveform at 5 MHz

Storage and Handling

Climatic Requirements

Item	Description	Min.	Max.	Units	Conditions	Notes
Operation to Specification	Temperature	-25	+40	°C	@ 10% ± 5% RH	1, 2
	Humidity	10 ± 5	86 ± 5	%RH	@ 36 ± 2 °C Temp.	1, 2
Storage	Temperature	-55	+70	°C	@ 10% ± 5% RH	2, 4
	Humidity	——	95 ± 5	%RH	@ 49 ± 2 °C Temp.	2, 4

Notes:
1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.

4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Drawings

Completed Assembly

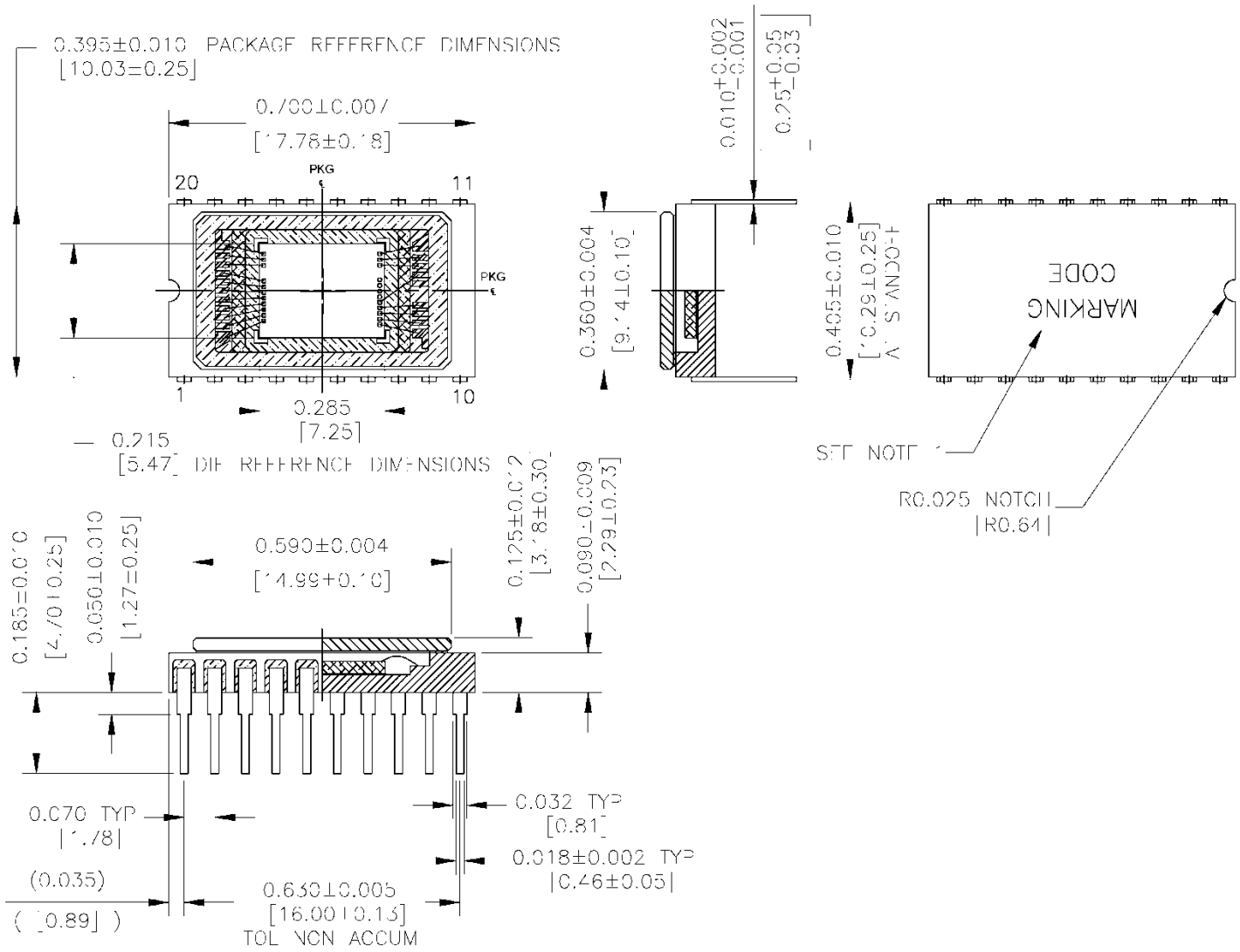

Figure 21: Completed Assembly (1 of 2)

Notes:
1. See Ordering Information for marking code.
2. Cover glass is visually aligned over die – no guarantee of location accuracy.

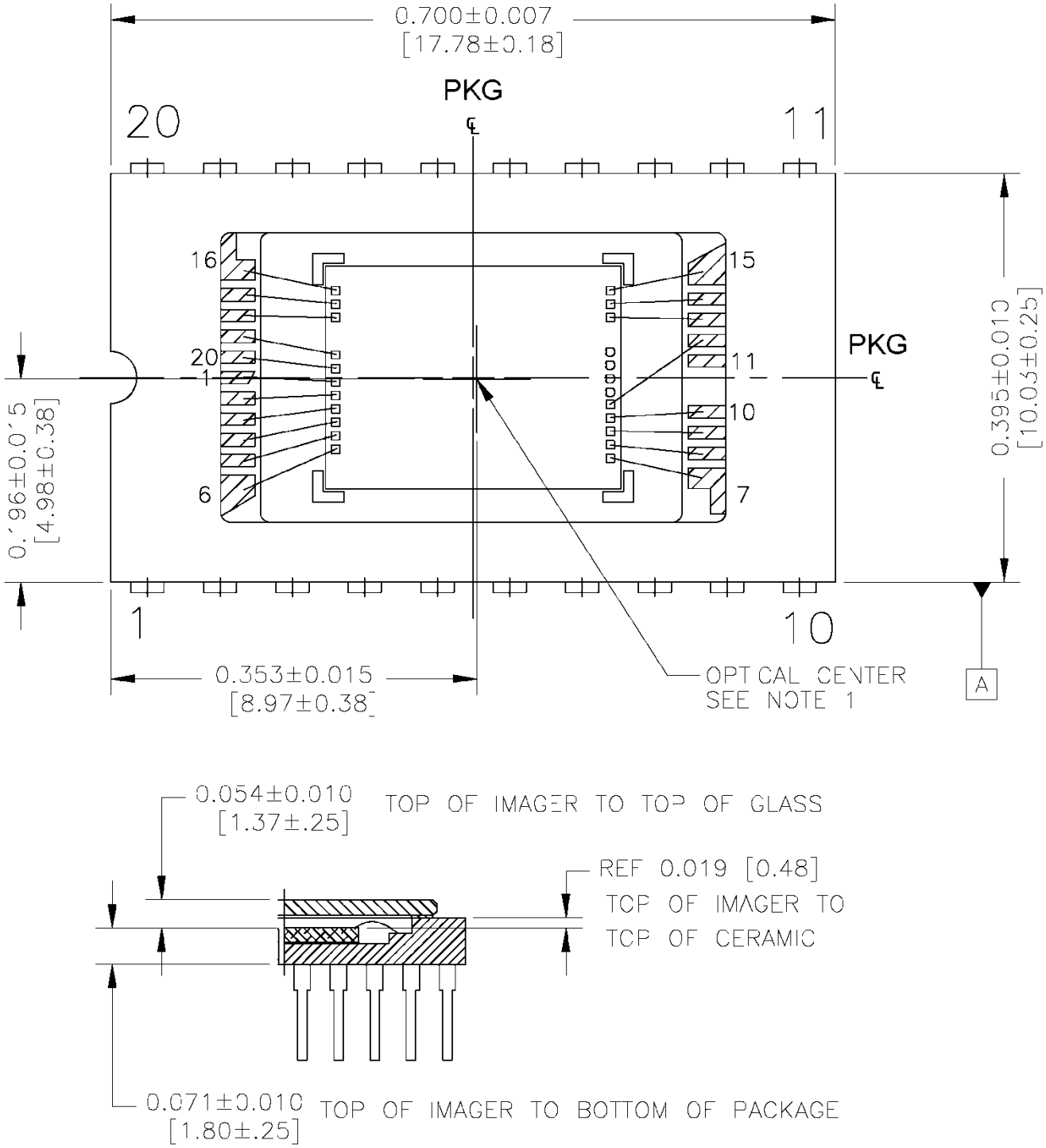

Figure 22: Completed Assembly (2 of 2)

Notes:

1. Center of image area is offset from center of package by (0.08, -0.04) mm nominal.
2. Die is visually aligned within ± 2° of datum A.

Cover Glass

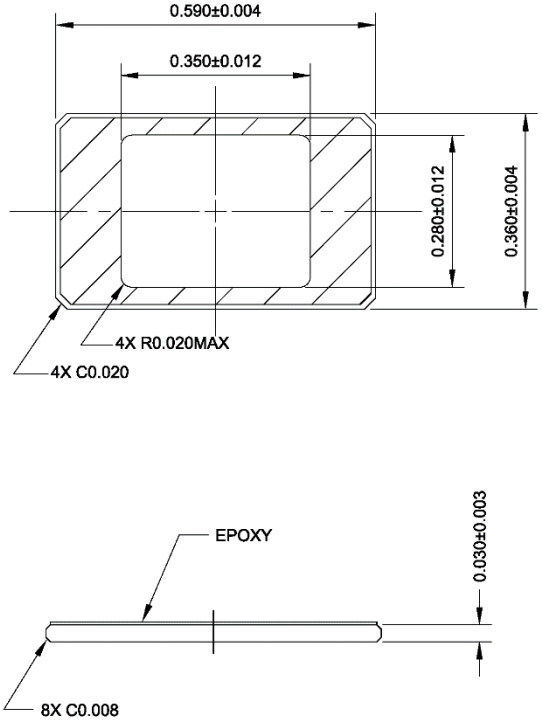

Figure 23: Cover Glass Drawing

Cover Glass Transmission

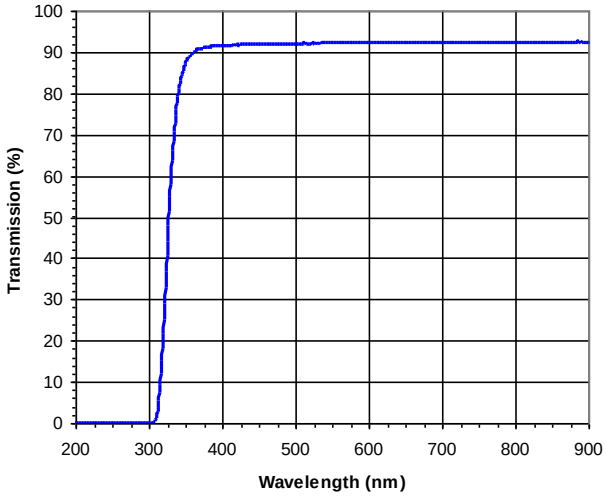

Figure 24: Cover Glass Transmission

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0484

Revision Number	Description
1.0	• Initial release

2.0	• Correction to Table 1 Package Pin Assignments. V2E and V2O were incorrectly labeled
	  ○ Pins were labeled:
	  ▪ Pin 17 V2O Vertical CCD Clock – Phase 2, odd field
	  ▪ Pin 18 V2E Vertical CCD Clock – Phase 2, even field
	  ○ Correct pin assignments:
	  ▪ Pin 17 V2E Vertical CCD Clock – Phase 2, even field
	  ▪ Pin 18 V2O Vertical CCD Clock – Phase 2, odd field
	• Corrected tφH in:
	  ○ Figure 9 - Single Register Readout and
	  ○ Figure 13- Dual Register Readout
	  ○ Incorrect tφH was 50 ns (20 MHz)
	  ○ Correct tφH value is 33 ns (30 MHz)

3.0	• Updated Format • Updated Storage and Handling section • Updated completed assembly drawings • Added cover glass drawing • Added cover glass transmission • Updated Quality Assurance and Reliability section
4.0	• Obsoleted the following part numbers: 4H0774, 4H0775, 4H0780, 4H0781, 4H0782, 4H0783, 4H0784, 4H0785, 4H0787, 4H0788

5.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections
	  ○ Electronic Shutter
	  ○ Absolute Maximum Ratings
	  ○ DC Operating Conditions
	  ○ Storage and Handling

PS-0023

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
2.0	• Updated Completed Assembly drawing. A scale factor error was corrected.
2.1	• Updated branding

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