PCS1P2192A

Product Preview

VDP Multiple Pixel Clock Generator

ON Semiconductor®

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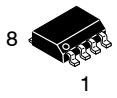


SOIC8−NB EP
CASE 751BU

Product Description

The PCS1P2192A is a clock generator that generates multiple selectable pixel clock outputs for Video Display Panel applications from an external 20 MHz reference clock. The PLL based clock generator is specifically designed to provide zero ppm frequency synthesis error on all clock outputs. Various pixel clock rates are selectable through frequency selection pins S[2:0] *(*Refer to *Frequency Selection Table)* The device provides a reference clock output additionally. Operating Supply Voltage for this device is 3.3 V ±0.3 V. The device is available in an 8−pin SOIC package.

Application

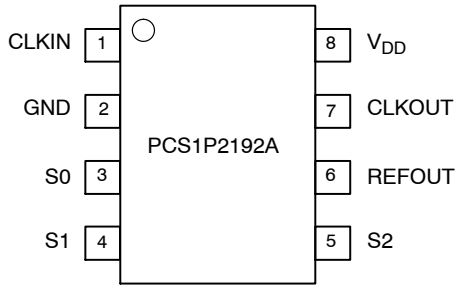
PCS1P2192A is targeted towards Video Display Panel (VDP) applications like VGA, SVGA, XGA, WXGA, UXGA.

Features

- Generates Multiple Clock Outputs from 20 MHz External Reference Clock
- Input Frequency: 20 MHz
- Output Frequencies:
  - Selectable CLKOUT: 108 MHz, 27 MHz, 33.2 MHz, 85 MHz, 65 MHz, 25 MHz, 45 MHz, and 40 MHz
  - REFOUT: 20 MHz
- Operating Supply Voltage: 3.3 V ± 0.3 V
- Zero ppm Frequency Synthesis Error on all Clock Outputs
- 8−pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

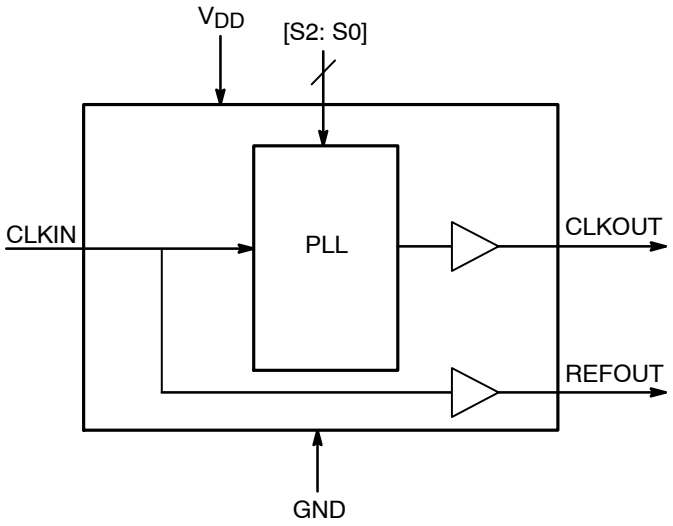


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN	Input	20 MHz external reference clock input.
2	GND	Power	Ground Connection.
3	S0	Input	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
4	S1	Input	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
5	S2	Input	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
6	REFOUT	Output	Reference clock output.
7	CLKOUT	Output	Clock output.
8	V_{DD}	Power	Device Power Supply.

Table 2. FREQUENCY SELECTION TABLE

S2	S1	S0	CLKOUT (MHz)
0	0	0	108
0	0	1	27
0	1	0	33.2
0	1	1	85
1	0	0	65
1	0	1	25
1	1	0	45
1	1	1	40

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
T_A	Operating Temperature	0		+85	°C
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance			7	pF

Table 5. DC ELECTRICAL CHARACTERISTICS

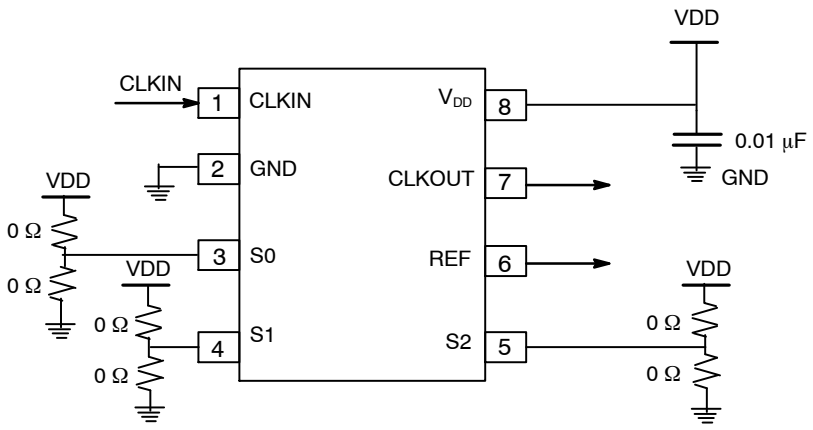
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage (for CLKIN)	GND − 0.3		0.8	V
V_{IH}	Input high voltage (for CLKIN)	2.0		VDD + 0.3	V
I_{IL}	Input low current			50	μA
I_{IH}	Input high current			−50	μA
V_{OL}	Output low voltage (VDD = 3.3 V, I_{OL} = 8 mA)			0.4	V
V_{OH}	Output high voltage (VDD = 3.3 V, I_{OH} = −8 mA)	2.4			V
I_{DD}	Static supply current (Note 1)			5	mA
I_{CC}	Dynamic supply current (3.3 V and no load)		9		mA
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power−up time (first locked cycle after power−up)		1		mS
Z_{OUT}	Output impedance		40		Ω

1. CLKIN pulled low.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency		20		MHz
f_{OUT}	Output frequency		108, 27, 33.2, 85, 65, 25, 45, 40		MHz
t_{LH} (Note 2)	Output rise time (Measured from 20% to 80%)	1.2		2.5	nS
t_{HL} (Note 2)	Output fall time (Measured from 80% to 20%)	0.8		1.6	nS
t_{JC}	Period Jitter		±150		pS
	Frequency Synthesis Error (All Outputs)		0		ppm
t_D	Output duty cycle	40	50	60	%

2. Measured with a capacitive load of 15 pF.



Use either pull−up or pull−down 0 Ω Resistor with [S2:S0] for selection of CLKOUT frequencies.

Figure 2. Typical Application Schematic

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.01 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the Figure 3.

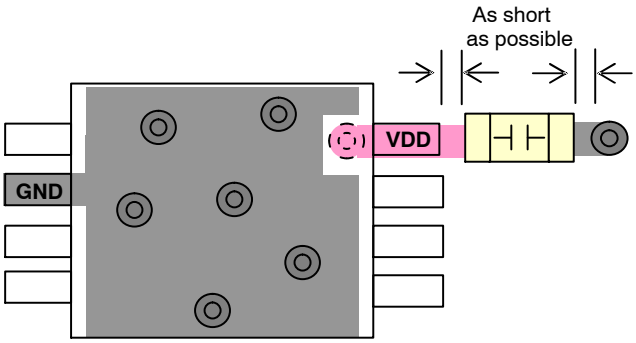
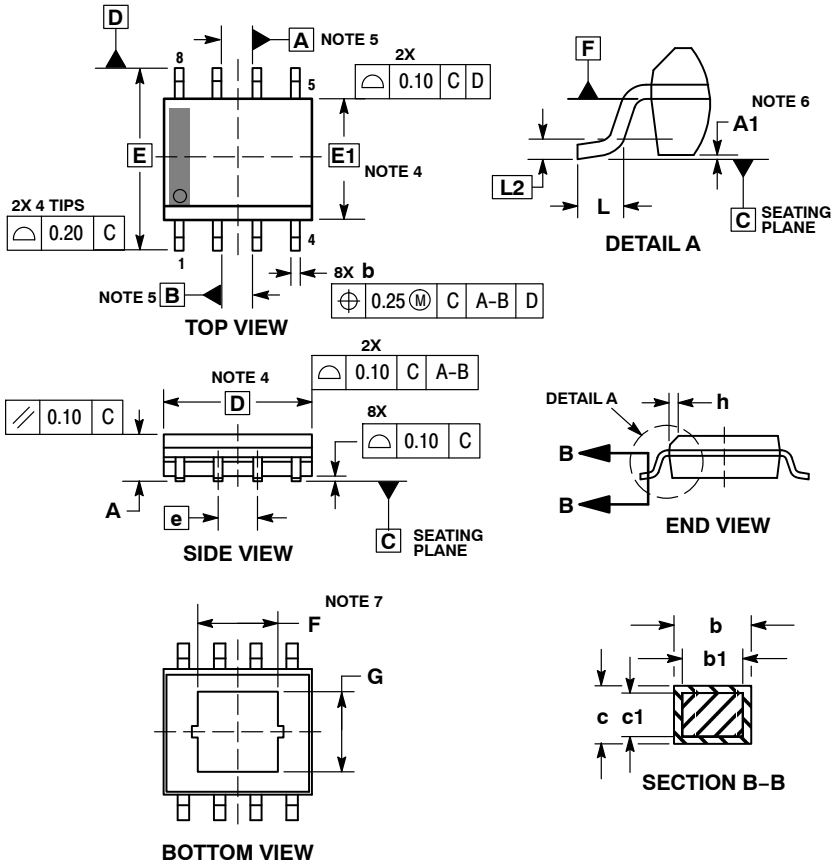


Figure 3. Typical Layout

PACKAGE DIMENSIONS

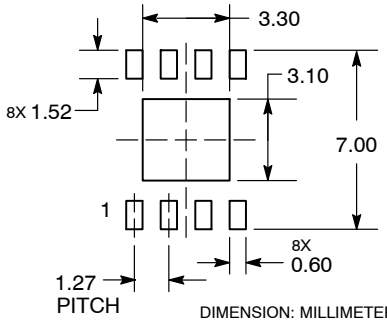
SOIC8−NB EP
CASE 751BU
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	−−−	0.10
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
F	1.55	3.07
G	1.55	3.07
h	0.25	0.50
L	0.40	1.27
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 7. ORDERING INFORMATION

Part Number	Top Marking	Package Type	Temperature
PCS1P2192AG−08SR	ACZ	8−Pin SOIC, TAPE & REEL, Green	0°C to +85°C

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−free.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

PCS1P2192A/D