## LV5219LG

Bi-CMOS IC
LED driver for cell phone
ON Semiconductor ${ }^{\text {® }}$
http://onsemi.com

## Overview

The LV5219LG is an LED driver IC for cellular phones. It incorporates 17 LED drivers (main, sub, tricolor $\times 2$, and flash) and a switching regulator circuit and supports the step-up through mode. Each LED current level can be adjusted over the $I^{2} \mathrm{C}$ serial bus. The LED driver IC also has functions to synchronize a ringing tone with a tricolor LED and to automatically control the brightness of white LEDs by brightness sensor.

## Functions

- PWM switching regulator control circuit
(Triangular wave oscillator, reference voltage, PWM comparator, driver, DTC, and short-circuit protection circuit incorporated)
(Timer-latch type output cut-off circuit in case of overload)
- LED driver

Main LCD backlight LED driver $\times 6$ with automatic brightness adjustment
LED current 5-bit changeover 0.0 mA to 18.6 mA
Fade in/out function
External brightness control function
Dim mode 3-bit changeover 0 mA to 1.4 mA
MLED4, MLED5, and MLED6 can be controlled independently
Sub LCD backlight LED driver $\times 2$
LED current 5 -bit changeover 0.0 mA to 18.6 mA
Fade in/out function
Independently controlled SLED2
Tricolor LED driver $\times 2$
LED current 5-bit changeover 0.0 mA to 18.6 mA
Gradation function
Ringing tone synchronization function (Forced to operate at SCTL : H)
Flash LED driver $\times 3$
LED current 5 -bit changeover 0.0 mA to 18.6 mA
Independent control

## Specifications

Maximum Ratings at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :--- | :--- | :--- | ---: | :---: |
| Maximum supply voltage | $\mathrm{V}_{\text {CC }} \max$ |  | 6 | V |
| Allowable power dissipation | Pd max | Mounted on a board ${ }^{*}$ | 1.2 | W |
| Operating temperature | Topr |  | -30 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg |  | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |

* Designated board : $40 \mathrm{~mm} \times 50 \mathrm{~mm} \times 0.8 \mathrm{~mm}$, glass epoxy 4-layter board (2S2P)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :--- | :--- | :--- | :--- | :---: |
| Supply voltage 1 | VBAT |  | 2.7 to 4.5 | V |
| Supply voltage 2 | $\mathrm{V}_{\mathrm{DD}}$ |  | 1.65 to 3 | V |
| Supply voltage 3 | $\mathrm{V}_{\mathrm{DD}^{2}}$ |  | 1.65 to 3 | V |

* Use the IC so that supply voltages 1,2 , and 3 have a magnitude relationship expressed as VBAT > VDD and VBAT > VDD 2 .
* Powers must be turned on so that VBAT brings up first.
* Powers must be turned off so that VBAT brings down last.

Electrical Characteristics $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VBAT}=3.7 \mathrm{~V}, \mathrm{VDD}_{\mathrm{D}}=\mathrm{V}_{\mathrm{DD}} 2=2.6 \mathrm{~V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| VBAT system (PVBAT, SVBAT) consumption current | ${ }^{\text {I CC }}{ }^{1}$ | RESET : L (standby mode) |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{1} \mathrm{Cc}{ }^{2}$ | RESET : H (sleep mode) |  | 0.3 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{1} \mathrm{CC}{ }^{3}$ | When the switching regulator is operated. |  | 1.5 | 2.5 | mA |
|  | ${ }^{1} \mathrm{CC} 4$ | Switching regulator operation LED : ON current set to 0 |  | 1.5 | 2.5 | mA |
| $\mathrm{V}_{\mathrm{DD}}$ system ( $\mathrm{V}_{\mathrm{DD}}$ ) consumption current | ${ }^{\text {I CC }}{ }^{5}$ | RESET : L (standby mode) |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{\text {I CC }}{ }^{1}$ | RESET : H (sleep mode) |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{\text {I CC }}{ }^{7}$ | When the switching regulator is operated. |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{\text {I CC }}{ }^{8}$ | Switching regulator operation LED : ON current set to 0 |  | 0 | 5 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{DD}}$ system ( $\left.\mathrm{V}_{\mathrm{DD}}{ }^{2}\right)$ consumption current | ${ }^{1} \mathrm{CC}{ }^{9}$ | RESET : L (standby mode) |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{1} \mathrm{CC}{ }^{10}$ | RESET : H (sleep mode) |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{1} \mathrm{CC}{ }^{11}$ | When the switching regulator is operated. |  | 0 | 5 | $\mu \mathrm{A}$ |
|  | ${ }^{1} \mathrm{CC}{ }^{12}$ | Switching regulator operation <br> LED : ON current set to 0 |  | 0 | 5 | $\mu \mathrm{A}$ |
| Switching regulator block |  |  |  |  |  |  |
| Output voltage 1 | $\mathrm{V}_{\mathrm{O}}{ }^{1}$ | $\mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}$, when output set to 5 V | 4.8 | 5.0 | 5.2 | V |
| LED pin voltage | $\mathrm{V}_{\mathrm{O}} 2$ | LED pin voltage Lowest voltage of feed back mode LED pin voltages MLED1, 2, 3, 4, 5, and 6 (except when MLED4, MLED5, and 6 are controlled independently) | 0.2 | 0.3 | 0.4 | V |
| Clock frequency | ${ }^{\text {fosc }}$ | External capacitance value connected to CT pin is 27pF | 0.8 | 1 | 1.2 | MHz |
| Changeover voltage | VD1 | Voltage for switching from through mode to LED pin fixed voltage mode when the LED pin voltage main current value is set to 18.6 mA |  | 0.2 |  | V |
| Changeover monitoring time | TVD1 | Time interval predetermined to detect error for the LED pin voltage when operation is switched over to stepping up with the detection of LED pin voltage. | 50 |  | 120 | $\mu \mathrm{s}$ |
| Soft start time | TST |  |  |  | 1000 | $\mu \mathrm{s}$ |
| Through SW ON resistance | RTH | Load $=100 \mathrm{~mA}$ |  | 1 |  | $\Omega$ |

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| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| LED driver block |  |  |  |  |  |  |
| Minimum output current | ${ }^{1} \mathrm{MIN}^{1}$ | Serial data $=$ \#00 | 0.2 | 0.6 | 1.7 | mA |
| Maximum output current | ${ }^{\text {MAX }}{ }^{1}$ | Serial data $=$ \#1E | 17.4 | 18.6 | 19.8 | mA |
| Nonlinearity error | LE | *1 | -2 |  | 2 | LSB |
| Differential linearity error | DLE | *2 | -2 |  | 2 | LSB |
| LED pin voltage Saturation characteristic 1 | VS1 | RGB1, RGB2, FLED1, 2 SLED1, 2 <br> MAX current set |  |  | 0.35 | V |
| LED pin voltage Saturation characteristic 2 | VS2 | MLED1, 2, 3, 4, 5, 6 set to MAX current |  |  | 0.2 | V |
| LED current pairing characteristic 1 | M1 | MLED1, 2, 3, 4, 5, 6 MAX current set |  |  | $\pm 5$ | \% |
| LED current pairing characteristic 2 | M2 | SLED1, 2 MAX current set |  |  | $\pm 5$ | \% |
| LED current pairing characteristic 3 | M3 | R1LED, R2LED MAX current set |  |  | $\pm 5$ | \% |
| LED current pairing characteristic 4 | M4 | G1LED, G2LED MAX current set |  |  | $\pm 5$ | \% |
| LED current pairing characteristic 5 | M5 | B1LED, B2LED MAX current set |  |  | $\pm 5$ | \% |
| Leakage current | ${ }_{\text {L }}$ | LED driver : OFF, $\mathrm{V}_{\mathrm{O}}=5 \mathrm{~V}$ |  |  | 1 | $\mu \mathrm{A}$ |
| KLED pin on resistance | RKE | KLED1, KLED2 50 mA drive mode |  | 5 |  | $\Omega$ |
| External CTL current 1 | VEM1 | MLED1, 2, 3 current values, MICTL pin voltage = $\mathrm{V}_{\mathrm{DD}}{ }^{2}, \mathrm{~V}_{\mathrm{DD}}{ }^{2}=2.6 \mathrm{~V}, \mathrm{RT} 2=120 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{DD}} 2=1.8 \mathrm{~V}$, RT2 $=82 \mathrm{k} \Omega$, difference current when serial MISW : OFF | -0.05 | 0 | +0.05 | mA |
| External CTL current 2 | VEM2 | MLED1, 2 , 3 current values, MICTL pin voltage $=$ $\mathrm{V}_{\mathrm{DD}} 2 \times 3 / 4, \mathrm{~V}_{\mathrm{DD}}{ }^{2}=2.6 \mathrm{~V}, \mathrm{RT} 2=120 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{DD}}{ }^{2}=$ $1.8 \mathrm{~V}, \mathrm{RT} 2=82 \mathrm{k} \Omega$, ratio to the current value when serial MISW : OFF | 69.6 | 74.6 | 79.6 | \% |
| External CTL current 3 | VEM3 | MLED1, 2, 3 current values, MICTL pin voltage $=$ $\mathrm{V}_{\mathrm{DD}} 2 \times 1 / 2, \mathrm{~V}_{\mathrm{DD}}{ }^{2}=2.6 \mathrm{~V}, \mathrm{RT} 2=120 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{DD}}{ }^{2}=$ $1.8 \mathrm{~V}, \mathrm{RT} 2=82 \mathrm{k} \Omega$, ratio to the current value when serial MISW : OFF | 42 | 47 | 52 | \% |
| External CTL current 4 | VEM4 | MLED1, 2,3 current values, MICTL pin voltage $=$ $\mathrm{V}_{\mathrm{DD}} 2 \times 1 / 4, \mathrm{~V}_{\mathrm{DD}}{ }^{2}=2.6 \mathrm{~V}, \mathrm{RT} 2=120 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{DD}}{ }^{2}=$ $1.8 \mathrm{~V}, \mathrm{RT} 2=82 \mathrm{k} \Omega$, ratio to the current value when serial MISW : OFF | 15.3 | 20.3 | 25.3 | \% |
| External CTL current 5 | VEM5 | MLED1, 2, 3 current values, MICTL pin voltage $=0$, $=\mathrm{V}_{\mathrm{DD}}{ }^{2}=2.6 \mathrm{~V}, \mathrm{RT} 2=120 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{DD}}{ }^{2}=1.8 \mathrm{~V}, \mathrm{RT} 2=$ $82 \mathrm{k} \Omega$, operation to turn off LED by applying 0 V to the MICTL pin is prohibited. |  | 0 | 0.5 | mA |
| SCTL response time | TSCTL | RGB1 and 2LED current delay time when switching SCTL on/off |  |  | 10 | $\mu \mathrm{s}$ |

*1 Nonlinearity error : Error from the ideal current value.
*2 Differential linearity error : Error from the ideal increment when increase by 1 bit is made.

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| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| Brightness sensor information input circuit |  |  |  |  |  |  |
| PTD pin threshold voltage 1 | VP1 | Brightness 1-2 switching PTD pin voltage | 0.197 | 0.247 | 0.297 | V |
| PTD pin threshold voltage 2 | VP2 | Brightness 2-3 switching PTD pin voltage | 0.241 | 0.291 | 0.341 | V |
| PTD pin threshold voltage 3 | VP3 | Brightness 3-4 switching PTD pin voltage | 0.283 | 0.333 | 0.838 | V |
| PTD pin threshold voltage 4 | VP4 | Brightness 4-5 switching PTD pin voltage | 0.325 | 0.375 | 0.425 | V |
| PTD pin threshold voltage 5 | VP5 | Brightness 5-6 switching PTD pin voltage | 0.369 | 0.419 | 0.469 | V |
| PTD pin threshold voltage 6 | VP6 | Brightness 6-7 switching PTD pin voltage | 0.411 | 0.461 | 0.511 | V |
| PTD pin threshold voltage 7 | VP7 | Brightness 7-8 switching PTD pin voltage | 0.453 | 0.503 | 0.553 | V |
| PTD pin threshold voltage 8 | VP8 | Brightness 8-9 switching PTD pin voltage | 0.492 | 0.547 | 0.602 | V |
| PTD pin threshold voltage 9 | VP9 | Brightness 9-10 switching PTD pin voltage | 0.530 | 0.589 | 0.648 | V |
| PTD pin threshold voltage 10 | VP10 | Brightness 10-11 switching PTD pin voltage | 0.563 | 0.631 | 0.694 | V |
| PTD pin threshold voltage 11 | VP11 | Brightness 11-12 switching PTD pin voltage | 0.605 | 0.672 | 0.739 | V |
| PTD pin threshold voltage 12 | VP12 | Brightness 12-13 switching PTD pin voltage | 0.645 | 0.717 | 0.789 | V |
| PTD pin threshold voltage 13 | VP13 | Brightness 13-14 switching PTD pin voltage | 0.683 | 0.759 | 0.835 | V |
| PTD pin threshold voltage 14 | VP14 | Brightness 14-15 switching PTD pin voltage | 0.721 | 0.801 | 0.881 | V |
| PTD pin threshold voltage 15 | VP15 | Brightness 15-16 switching PTD pin voltage | 0.752 | 0.843 | 0.920 | V |
| Control circuit block |  |  |  |  |  |  |
| High level 1 | $\mathrm{V}_{\text {IN }}{ }^{\mathrm{H}} 1$ | Input high level serial | $0.8 \mathrm{~V}_{\text {DD }}$ |  |  | V |
| Low level 1 | $\mathrm{V}_{\text {IN }} \mathrm{L} 1$ | Input low level serial | 0 |  | $0.2 \mathrm{~V}_{\text {DD }}$ | V |
| High level 2 | $\mathrm{V}_{\text {IN }} \mathrm{H}^{2}$ | Input high level RESET, SCTL | 1.5 |  |  | V |
| Low level 2 | $\mathrm{V}_{\text {IN }} \mathrm{V}^{\text {2 }}$ | Input low level RESET, SCTL | 0 |  | 0.3 | V |
| High output level 1 | $\mathrm{V}_{\mathrm{HO}}{ }^{1}$ | Output high level PTEN, $\mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ | $\mathrm{V}_{\text {DD }}{ }^{-0.3}$ |  |  | V |
| Low output level 1 | $\mathrm{V}_{\mathrm{LO}}{ }^{1}$ | Output low level PTEN, $\mathrm{I}_{\mathrm{L}}=-1 \mathrm{~mA}$ | 0 |  | 0.3 | V |
| High output level 2 | $\mathrm{V}_{\mathrm{HO}}{ }^{2}$ | Output high level $\mathrm{INT}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ | $\mathrm{V}_{\text {DD }}{ }^{-0.3}$ |  |  | V |
| Low output level 2 | $\mathrm{V}_{\mathrm{LO}}{ }^{2}$ | Output low level INT, I L $=-1 \mathrm{~mA}$ | 0 |  | 0.3 | V |
| High output level 3 | $\mathrm{V}_{\mathrm{HO}}{ }^{3}$ | Output high level GPO0, GPO1, GPO2, $\mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ Output setting: when set to buffer output setting | $\mathrm{V}_{\text {DD }}{ }^{-0.3}$ |  |  | V |
| Low output level 3 | $\mathrm{V}_{\mathrm{LO}}{ }^{3}$ | Output low level GPO0, GPO1, GPO2, $\mathrm{I}_{\mathrm{L}}=-1 \mathrm{~mA}$ Output setting: when set to buffer output setting | 0 |  | 0.3 | V |
| OPEN output leakage current 1 | ${ }^{1} \mathrm{OP}^{1}$ | Current flows in or or out when $\mathrm{V}_{\mathrm{DD}}$ is applied to output. When GPO0, GPO1, GPO2 output is set to OPEN output. | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| OPEN output leakage current 2 | ${ }^{\prime} \mathrm{OP}^{2}$ | Current flows in or out when OV is applied to output. When GPO0, GPO1, GPO2 output is set to OPEN output. | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| High input current 1 | ${ }^{1} \mathrm{HIN}{ }^{1}$ | Current flows in or out when VBAT voltage is applied to PTD pin | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| Low input current 1 | $\mathrm{ILIN}^{1}$ | Current flows in or out when OV is applied to PTD pin | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| High input current 2 | ${ }^{\text {H }} \mathrm{H} \mathrm{N}^{2}$ | Current flows in or out when $\mathrm{V}_{\mathrm{DD}}$ is applied to MICTL pin | -3 | 0 | 3 | $\mu \mathrm{A}$ |
| Low input current 2 | ${ }^{1} \mathrm{LIN}^{2}$ | Current flows in or out when OV is applied to MICTL pin | 5 | 6.5 | 8 | $\mu \mathrm{A}$ |
| High input current 3 | ${ }^{1} \mathrm{HIN} 3$ | Current flows in or out when VBAT voltage is applied to RESET pin | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| Low input current 3 | ${ }^{1} \mathrm{LIN}^{3}$ | Current flows in or out when OV is applied to RESET pin | -1 | 0 | 1 | $\mu \mathrm{A}$ |
| High input current 4 | ${ }^{1} \mathrm{HIN} 4$ | Current flows in or out when VDD is applied to SCTL pin | 28 | 40 | 52 | $\mu \mathrm{A}$ |
| Low input current 4 | ${ }^{1} \mathrm{LIN}^{4}$ | Current flows in or out when OV is applied to SCTL pin | -1 | 0 | 1 | $\mu \mathrm{A}$ |

## Package Dimensions

unit : mm (typ)
3359


## Pin Assignment

| G | F | E | D | C | B | A |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TEST3 | MLED3 | $\begin{aligned} & \text { LED } \\ & \text { GND1 } \end{aligned}$ | MLED2 | SGND | MLED_F | TEST |
| SLED2 | MLED4 | MLED5 | MLED6 | MLED1 | MICTL | CT |
| SLED1 | RLED1 | RT2 | GPO2 | GPO1 | SCL | SVBAT |
| $\begin{gathered} \text { LED } \\ \text { GND2 } \end{gathered}$ | RLED2 | SDA | PTD | SCTL | INT | IN |
| GLED1 | GLED2 | RESET | $V_{\text {DD }}$ | PTEN | GPOO | PVBAT |
| BLED2 | BLED1 | FLED3 | KLED1 | RT | $\mathrm{V}_{\mathrm{DD}}{ }^{2}$ | SWOUT |
| TEST1 | FLED2 | FLED1 | $\begin{aligned} & \text { LED } \\ & \text { GND3 } \end{aligned}$ | KLED2 | PGND | TEST2 |

Top View

## Block Diagram



Pin Functions

| Pin No. | Pin name | Pin Description | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| A1 | TEST | Test signal input pin. <br> Be sure to connect the pin to GND. |  |
| A2 | CT | Oscillator frequency setting capacitance connection pin. <br> Triangular wave output is generated by connecting an external capacitor across this pin and GND. The clock frequency of the switching regulator and the LED on/off fade time can be adjusted by changing the value of the external capacitor. |  |
| A3 | SVBAT | Power pin for analog circuit. |  |
| A4 | IN | DC/DC feedback voltage input pin. <br> Feedback is applied so that the input voltage becomes equal to the set voltage in the output voltage fixed mode. Overvoltage limiter is activated when the input voltage rises about 0.6 V higher than the fixed mode set voltage. When the input voltage falls, the switching regulator is stopped in about 10 ms . This condition is released by resetting the IC or setting the serial RGSW to OFF. |  |
| A5 | PVBAT | Power pin for DC/DC pulse output driver. |  |
| A6 | SWOUT | DC/DC PWM pulse output pin. <br> The on resistance of both output transistors PCH and NCH are about $10 \Omega$. |  |
| B1 | MLED_F | MLED filter capacitor connection pin. |  |
| B2 | MICTL | MLED external brightness control pin. <br> The main LED normal current value can be varied by applying a DC voltage to this pin. The set current value is obtained when $V_{D D^{2}}$ voltage is applied. The main LED normal current decreases as the voltage is lowered. The level of current change can be varied by the value of external resistor connected to the RT2 pin. |  |

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| Pin No. | Pin name | Pin Description | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| B3 | SCL | Serial clock signal input pin. |  |
| B4 | INT | Interrupt signal output pin. |  |
| B6 | $\mathrm{V}_{\mathrm{DD}}{ }^{2}$ | Reference power for MLED external sync circuit. |  |
| B7 | PGND | DC/DC pulse output driver GND pin. |  |
| C1 | SGND | Analog circuit GND pin. |  |
| $\begin{aligned} & \text { B5 } \\ & \text { C3 } \\ & \text { D3 } \end{aligned}$ | $\begin{aligned} & \text { GPO0 } \\ & \text { GPO1 } \\ & \text { GPO2 } \end{aligned}$ | General-purpose output pins. |  |
| C4 | SCTL | RBGLED external sync signal input pin. <br> When the serial R1SW, G1SW, and B1SW, G2SW, and B2SW are set to ON, setting the application voltage H causes tricolor LED to go ON . When the application voltage set to L, tricolor LED goes OFF. Note that if the serial settings SCSW1 and SCSW2 are set to "ignore SCTL," tricolor LED goes ON regardless of the state of SCTL. |  |
| C5 | PTEN | Brightness sensor ON/OF control pin. |  |
| C6 | RT | Reference current setting resistor connection pin. <br> By connecting the external resistor between this pin and GND, the reference current is generated. The pin voltage is about 0.25 V . Change of this current value enables change of the oscillation frequency and LED driver current value. |  |

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| Pin No. | Pin name | Pin Description | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { D6 } \\ & \text { C7 } \end{aligned}$ | KLED1 <br> KLED2 | Key LED driver output pins. |  |
| C2 <br> D1 <br> F1 <br> F2 <br> E2 <br> D2 | MLED1 <br> MLED2 <br> MLED3 <br> MLED4 <br> MLED5 <br> MLED6 | Main LCD backlight LED driver pin. <br> Feedback is applied so that the current flow through the output transistor becomes equal to the set current value. The driver current value can be adjusted in 0.6 mA steps from about 0.6 mA to 18.6 mA through serial setting. These pins are also used to switch from through to switching regulator mode and to sense the feedback of the output voltage to the LED pins. |  |
| D4 | PTD | Brightness sensor output connection pin. <br> Used to determine the brightness according to the DC input voltage. Must be connected to GND when not to be used. |  |
| D5 | $V_{\text {DD }}$ | Power pin for IF. |  |
| D7 | LEDGND3 | LED driver dedicated GND pin 3 |  |
| E1 | LEDGND1 | LED driver dedicated GND pin 1 |  |
| E3 | RT2 | Reference current setting resistor connection pin used when MLED is controlled externally. <br> The resistance value of the external resistor connected to the $\mathrm{V}_{\mathrm{DD}}{ }^{2}$ pin can set a variable value of the main LED normal mode current that is varied with the MICTL pin. |  |
| E4 | SDA | Serial data signal input pin. |  |
| E5 | RESET | Reset signal input pin. <br> Reset state when low. |  |
| $\begin{aligned} & \text { E7 } \\ & \text { F7 } \\ & \text { E6 } \end{aligned}$ | FLED1 <br> FLED2 <br> FLED3 | Flash LED driver pins. <br> Feedback is applied so that the current flow through the output transistor becomes equal to the set current value. Each driver output current value can be adjusted independently with the 0.6 step from about 0.8 mA to 18.6 mA through serial setting. |  |

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| Pin No. | Pin name | Pin Description | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { F3 } \\ & \text { F4 } \\ & \text { G5 } \\ & \text { F5 } \\ & \text { F6 } \\ & \text { G6 } \end{aligned}$ | RLED1 <br> RLED2 <br> GLED1 <br> GLED2 <br> BLED1 <br> BLED2 | Tricolor LED driver pins. <br> Feedback is applied so that the current flow through the output transistor becomes equal to the set current value. Each driver output current value can be adkusted independently with the 0.6 step from about 0.8 mA to 18.6 mA through serial setting. <br> These pins are turned ON only when the SCTL pin is set high or the serial SCTEN and SCSW2 pins are set to ignore SCTL. |  |
| $\begin{aligned} & \text { G3 } \\ & \text { G2 } \end{aligned}$ | $\begin{aligned} & \text { SLED1 } \\ & \text { SLED2 } \end{aligned}$ | Sub-LED backlight LED driver pins. <br> Feedback is applied so that the current flow through the output transistor becomes equal to the set current value. The driver output current value can be adjusted independently with the 0.6 step from about 0.8 mA to 18.6 mA through serial setting. |  |
| G4 | LEDGND2 | LED driver dedicated GND pin 2. |  |
| $\begin{aligned} & \text { G7 } \\ & \text { A7 } \\ & \text { G1 } \end{aligned}$ | $\begin{aligned} & \text { TEST1 } \\ & \text { TEST2 } \\ & \text { TEST3 } \end{aligned}$ | Test signal input pin. <br> Be sure to connect the pin to GND. |  |

## Serial Bus Communication Specifications

$I^{2} \mathrm{C}$ serial transfer timing conditions


Standard mode

| Parameter | symbol | Conditions | min | typ | max | unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SCL clock frequency | fscl | SCL clock frequency | 0 |  | 100 | kHz |
| Data set up time | ts1 | SCL setup time relative to the fall of SDA | 4.7 |  |  | $\mu \mathrm{s}$ |
|  | ts2 | SDA setup time relative to the rise of SCL | 250 |  |  | ns |
|  | ts3 | SCL setup time relative to the rise of SDA | 4.0 |  |  | $\mu \mathrm{s}$ |
| Data hold time | th1 | SCL data hold time relative to the rise of SDA | 4.0 |  |  | $\mu \mathrm{s}$ |
|  | th2 | SDA hold time relative to the fall of SCL | 0 |  |  | $\mu \mathrm{s}$ |
| Pulse width | twL | SCL pulse width for the L period | 4.7 |  |  | $\mu \mathrm{s}$ |
|  | tw H | SCL pulse width for the H period | 4.0 |  |  | $\mu \mathrm{s}$ |
| Input waveform conditions | ton | SCL and SDA (input) rise time |  |  | 1000 | ns |
|  | tof | SCL and SDA (input) fall time |  |  | 300 | ns |
| Bus free time | tbuf | Time between STOP and START conditions | 4.7 |  |  | $\mu \mathrm{s}$ |

High-speed mode

| Parameter | Symbol | Conditions | min | typ | max | unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SCL clock frequency | fscl | SCL clock frequency | 0 |  | 400 | kHz |
| Data setup time | ts1 | SCL setup time relative to the fall of SDA | 0.6 |  |  | $\mu \mathrm{s}$ |
|  | ts2 | SDA setup time relative to the rise of SCL | 100 |  |  | ns |
|  | ts3 | SCL setup time relative to the rise of SDA | 0.6 |  |  | $\mu \mathrm{s}$ |
| Data hold time | th1 | SCL data hold time relative to the rise of SDA | 0.6 |  |  | $\mu \mathrm{S}$ |
|  | th2 | SDA hold time relative to the fall of SCL | 0 |  |  | $\mu \mathrm{s}$ |
| Pulse width | twL | SCL pulse width for the L period | 1.3 |  |  | $\mu \mathrm{s}$ |
|  | tw H | SCL pulse width for the H period | 0.6 |  |  | $\mu \mathrm{s}$ |
| Input waveform conditions | ton | SCL and SDA (input) rise time |  |  | 300 | ns |
|  | tof | SCL and SDA (input) fall time |  |  | 300 | ns |
| Bus free time | tbuf | Time between STOP and START conditions | 1.3 |  |  | $\mu \mathrm{s}$ |

## $I^{2} \mathrm{C}$ bus transmission method

Start and stop conditions
In the $I^{2} \mathrm{C}$ bus, SDA must basically be kept in the constant state while SCL is " H " as shown below during data transfer.


When data transfer is not made, both SCL and SDA are in the " H " state.
When SCL = SDA = "H", change of SDA from "H" to "L" enables the start conditions to start access.
When SCL is "H", change of SDA from "L" to "H" enables the stop conditions to stop access.


## Data transfer and acknowledgement response

After establishment of start conditions, data transfer is made by one byte (8 bits).
Data transfer enables continuous transfer of any number of bytes.
Each time the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side.
The ACK signal is issued when SDA on the send side is released and SDA on the receive side is set "L" immediately after fall of the clock pulse at the SCL eighth bit of data transfer to "L".
When the next 1-byte transfer is left in the receive state after transmission of the ACK signal from the receive side, the receive side releases SDA at fall of the SCL ninth clock.
In the $\mathrm{I}^{2} \mathrm{C}$ bus, there is no CE signal. Instead, 7-bit slave address is assigned to each device and the first byte of transfer is assigned to the command ( $\mathrm{R} / \mathrm{W}$ ) representing the 7 -bit slave address and subsequent transfer direction. The 7-bit address is transferred sequentially from MSB and the second byte is WRITE when the eighth bit is "L" and READ when the eighth bit is " H ".

In LV5219LG, the slave address is specified as (1110100).


## Data transfer write format

The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.
For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.
Thus, continuous data transfer starting at the designated address is made possible.
After the register address reaches 7Fh, the transfer address for the next byte is set to 00 h .

Data write example



Master side transmission $\qquad$ Slave side transmission


## Serial modes setting

address : 00h (LEDCTL) LED Setting 1 Register Write

| 00h (LEDCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MLED6 | MLED5 | MLED4 | MSW2 | MSW1 | FXSW | RGSW | STBY |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : STBY (Standby setting)
0 : Standby state *Default
1 : Active state

D1: RGSW (Switching regulator operation setting)
0 : Switching regulator forced to OFF *Default
1 : Switching regulator waiting for step-up

D2 : FXSW (Fixed output voltage mode setting)
0 : Auto step-up mode *Default
1 : Fixed voltage step-up mode (fixed at voltage set through serial VD)
D3: MSW1 (Main LED output setting (dim mode))
0 : Dim mode OFF *Default
1 : Dim mode ON
D4 : MSW2 (Main LED output setting (normal mode))
0 : Normal mode OFF *Default
1 : Normal mode ON

D5 : MLED4 (MLED4 output setting)
0 : OFF *Default
1 : ON

D6 : MLED5 (MLED5 output setting)
0 : OFF *Default
1: ON

D7 : MLE6 (MLED6 output setting)
0 : OFF *Default
1: ON
address : 01h (LEDCTL2) LED Setting 2 Register Write

| 01h (LEDCTL2) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | SPM6 | SPM5 | SPM4 | SPS2 | S2SW | S1SW | MISW | VOCSW |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : VOCSW (Step-up setting)
0 : Manual setting *Default
1 : Automatic setting
*Sets, when FXSW is set to OFF, whether automatic step-up is to be carried out or not when LEDs other than the main LEDs are turned on.
In automatic setting mode, stepping-up is carried out when LEDs other than the MLEDs are turned on.

| D1: MISW | (MICTL setting = Enable brightness adjustment for LEDs other than main LEDs) <br> 0 : MICTL disabled *Default <br> 1 : MICTL enabled |
| :---: | :---: |
| D2 : S1SW | $\begin{aligned} & \text { (SLED1 output setting) } \\ & 0: \text { OFF *Default } \\ & 1: \text { ON } \end{aligned}$ |
| D3: S2SW | $\begin{aligned} & \text { (SLED2 output setting) } \\ & 0: \text { OFF *Default } \\ & 1: \text { ON } \end{aligned}$ |
| D4: SPS2 | (SLED2 independent control setting) $0:$ OFF $\quad \cdots$ Same operation as SLED1 when set to OFF. *Default $1:$ ON $\quad \cdots$ When set to ON, operate as SLED2 set current, independently of S |

D5 : SPM4 (MLED4 independent control setting)
0 : OFF $\quad \cdots$ Same operation as MLED1, 2, and 3 when set to OFF. *Default
1 : ON $\quad \cdots$ When set to ON, operate as MLED4 set current, irrespective of main LEDs.

D6 : SPM5 (MLED5 independent control setting)
0 : OFF $\quad \cdots$ Same operation as MLED1, 2, and 3 when set to OFF. *Default
$1:$ ON $\quad \cdots$ When set to ON, operate as MLED5 set current, irrespective of main LEDs.
D7 : SPM6 (MLED6 independent control setting)
0 : OFF $\quad$...Same operation as MLED1, 2, and 3 when set to OFF. *Default
1 : ON $\quad \cdots$ When set to ON, operate as MLED6 set current, irrespective of main LEDs.
address : 02h (LEDCTL3) LED Setting 3 Register Write

| 02h (LEDCTL3) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | SCSW2 | B2SW | G2SW | R2SW | SCSW1 | B1SW | G1SW | R1SW |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


| D0 : R1SW | (RLED1 output setting) <br> $0:$ OFF *Default <br> $1:$ ON |
| :--- | :--- |
|  |  |
| D1 : G1SW | (GLED1 output setting) <br>  <br>  <br>  <br>  <br>  <br> D2 : OFF *Default <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br> (BLED1 output setting) <br> $0:$ OFF *Default <br> $1:$ ON |

D3 : SCSW1 (SCTL signal enable 1 RLED1, GLED1, BLED1 setting)
0 : SCTL enabled *Default
1 : SCTL disabled

D4: R2SW (RLED2 output setting)
0 : OFF *Default
1: ON

D5 : G2SW (GLED2 output setting)
0 : OFF *Default
1: ON

D6 : B2SW (BLED2 output setting)
0 : OFF *Default
1: ON

D7 : SCSW2 (SCTL signal enable 2 RLED2, GLED2, BLED2 setting)
0 : SCTL enabled *Default
1 : SCTL disabled
*SCTL is the external sync pin input used for the synchronization with the sound signal from the sound source IC. It turns on and off the tricolor LEDs.
*The SCTL signal can be enabled or disabled with the SCT signal enable setting.
The relationships among SCSW, SCTL, and RLED, GLED, and BLED are shown below.

| SCSW1 | SCTL pin | RLED1, GLED1, BLED1 State |
| :---: | :---: | :---: |
| 0 | L | Turn off |
| 0 | $H$ | Turn-on enable |
| 1 | L | Turn-on enable |
| 1 | H | Turn-on enable |

Forced off regardless of the serial command when set to turn off.
When set to "turn-on enable," the LEDs can be turned on with the serial command R1SW, G1SW, or B1SW, or can be automatically turned on and off in the gradation/pulse mode.

| SCSW2 | SCTL pin | RLED2, GLED2, BLED2 State | Forced off regardless of the serial command when <br> set to turn off. |
| :---: | :---: | :---: | :---: |
| 0 | L | Turn off |  |
| turned on with the serial command R2SW, G2SW, or |  |  |  |
| 0 | H | Turn-on enable | Turn-on enable |
| 1 | L | Turn-on enable | B2SW, or B1SW, or can be automatically turned on <br> and off in the gradation/pulse mode. |
| 1 | H |  |  |

address : 03h (LEDCTL4) LED Setting 4 Register Write

| 03h (LEDCTL4) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MFSW | KESW4 | KESW3 | KESW2 | KESW1 | F3SW | F2SW | F1SW |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


| D0 : F1SW | (FLED1 output setting) <br> $0:$ OFF *Default <br> $1:$ ON |
| :--- | :--- |
|  |  |
| D1 : F2SW | (FLED2 output setting) <br>  <br>  <br>  <br>  <br>  <br> D2 : F3SF *Default <br>  <br>  <br>  <br>  <br>  <br>  <br> (FLED3 output setting) <br> $0:$ OFF *Default <br> $1:$ ON |

D3: KESW1 (KLED1 output setting 1)
0 : Forced *Default
1 : Automatic

D4: KESW2 (KLED1 output setting 2)
0 : OFF *Default
1: ON

* Controllable only when KESW1 is set to "Forced."

D5 : KESW3 (KLED2 output setting 1)
0 : Forced *Default
1 : Automatic

D6 : KESW4 (KLED2 output setting 2)
0 : OFF *Default
1: ON

* Controllable only when KESW3 is set to "Forced."

D7 : MFSW (Main LED filter ON/OFF setting)
0 : OFF *Default
1: ON
*Operate for main LED current other that dim mode.

LV5219LG
address : 04h (MLEDDACTL) MLED Current Setting Register Write

| 04h (MLEDDACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MAINL [2] | MAINL [1] | MAINL [0] | MAINH [4] | MAINH [3] | MAINH [2] | MAINH [1] | MAINH [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : MAINH [0] to MAINH [4] (MLED1, 2, and 3 current settings (normal mode))

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LED is turned off when these bits are set to 11111. Fade out operation using this setting is prohibited.

D5 to D7 : MAINL [0] to MAINL [2] (MLED current settings (dim mode))

| D7 | D6 | D5 | Current value (mA) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0.2 |
| 0 | 0 | 1 | 0.4 |
| 0 | 1 | 0 | 0.6 |
| 0 | 1 | 1 | 0.8 |
| 1 | 0 | 0 | 1.0 |
| 1 | 0 | 1 | 1.2 |
| 1 | 1 | 0 | 1.4 |
| 1 | 1 | 1 | 0.0 |

*Default

LED is turned off when these bits are set to 111. Fade out operation using this setting is prohibited.
Use of fade out operation is inhibited.

LV5219LG
address : 05h (M4DACTL) MLED4 Current Setting Register Write

| 05h (M4DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | M4C $[4]$ | M4C $[3]$ | M4C $[2]$ | M4C $[1]$ | M4C $[0]$ |
| R/W | W | W | $W$ | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : M4C [0] to M4C [4] (MLED4 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 06h (M5DACTL) MLED5 Current Setting Register Write

| 06h (M5DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | M5C $[4]$ | M5C $[3]$ | M5C $[2]$ | M5C $[1]$ | M5C $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : M5C [0] to M5C [4] (MLED5 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

address : 07h (M6_VD_DACTL) MLED6 Current Setting/Output Setting Register Write

| 07h (M6_VD_DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | VD [2] | VD [1] | VD [0] | M6C [4] | M6C [3] | M6C [2] | M6C [1] | M6C [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : M6C [0] to M6C [4] (MLED6 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

D5 to D7: VD [0] to VD [2] (Output DC settings)

| D7 | D6 | D5 | Output Voltage (V) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 5.0 |
| 0 | 0 | 1 | 4.3 |
| 0 | 1 | 0 | 4.5 |
| 0 | 1 | 1 | 4.7 |
| 1 | 0 | 0 | 4.9 |
| 1 | 0 | 1 | 5.1 |
| 1 | 1 | 0 | 5.3 |
| 1 | 1 | 1 | 5.5 |

LV5219LG
address : 08h (S1DACTL) SLED1 Current Setting Register Write

| 08h (S1DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | S1C $[4]$ | S1C $[3]$ | S1C $[2]$ | S1C $[1]$ | S1C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : S1C [0] to S1C [4] (SLED1 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

*Default

LED is turned off when these bits are set to 11111. Fade out operation using this setting is prohibited.

LV5219LG
address : 09h (S2DACTL) SLED2 Current Setting Register Write

| 09h (S2DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | S2C $[4]$ | S2C $[3]$ | S2C $[2]$ | S2C $[1]$ | S2C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : S2C [0] to S2C [4] (SLED2 current settings)

| D4 | D3 | D2 | D1 | DO | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 0Ah (R1DACTL) RLED1 Current Setting Register Write

| OAh (R1DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MAXC1 [2] | MAXC1 [1] | MAXC1 [0] | R1C $[4]$ | R1C $[3]$ | R1C $[2]$ | R1C $[1]$ | R1C $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : R1C [0] to R1C [4] (RLED1 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

*Default

LED is turned off when these bits are set to 11111. Fade out operation using this setting is prohibited.

D5 to D7 : MAXC1 [0] to MAXC1 [2] (Group 1 (RLED1, GLED1, BLED1) maximum current value settings)

| D7 | D6 | D5 | Max. Current value (mA) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $18.6(100 \%)$ |
| 0 | 0 | 1 | $16.275(87 \%)$ |
| 0 | 1 | 0 | $13.95(75 \%)$ |
| 0 | 1 | 1 | $11.625(62.5 \%)$ |
| 1 | 0 | 0 | $9.3(50 \%)$ |
| 1 | 0 | 1 | $6.975(37.5 \%)$ |
| 1 | 1 | 0 | $4.65(25 \%)$ |
| 1 | 1 | 1 | $2.325(12.5 \%)$ |

LV5219LG
address : 0Bh (G1DACTL) GLED1 Current Setting Register Write

| OBh (G1DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | G1C $[4]$ | G1C [3] | G1C [2] | G1C [1] | G1C [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : G1C [0] to G1C [4] (GLED1 current settings)

| D4 | D3 | D2 | D1 | DO | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 0Ch (B1DACTL) BLED1 Current Setting Register Write

| OCh (B1DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | B1C $[4]$ | B1C $[3]$ | B1C $[2]$ | B1C $[1]$ | B1C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : B1C [0] to B1C [4] (BLED1 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

*Default

LED is turned off when these bits are set to 11111. Fade out operation using this setting is prohibited.

LV5219LG
address : 0Dh (R2DACTL) RLED2 Current Setting Register Write

| ODh (R2DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MAXC2 [2] | MAXC2 [1] | MAXC2 [0] | R2C $[4]$ | R2C $[3]$ | R2C $[2]$ | R2C $[1]$ | R2C $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : R2C [0] to R2C [4] (RLED2 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

*Default

LED is turned off when these bits are set to 11111. Fade out operation using this setting is prohibited.

D5 to D7 : MAXC2 [0] to MAXC2 [2] (Group 2 (RLED2, GLED2, BLED2) maximum current value settings)

| D7 | D6 | D5 | Max. Current value (mA) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $18.6(100 \%)$ |
| 0 | 0 | 1 | $16.275(87 \%)$ |
| 0 | 1 | 0 | $13.95(75 \%)$ |
| 0 | 1 | 1 | $11.625(62.5 \%)$ |
| 1 | 0 | 0 | $9.3(50 \%)$ |
| 1 | 0 | 1 | $6.975(37.5 \%)$ |
| 1 | 1 | 0 | $4.65(25 \%)$ |
| 1 | 1 | 1 | $2.325(12.5 \%)$ |

LV5219LG
address : 0Eh (G2DACTL) GLED2 Current Setting Register Write

| OEh (G2DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | G2C $[4]$ | G2C $[3]$ | G2C $[2]$ | G2C $[1]$ | G2C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : G2C [0] to G2C [4] (GLED2 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 0Fh (B2DACTL) BLED2 Current Setting Register Write

| OFh (B2DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | B2C $[4]$ | B2C $[3]$ | B2C $[2]$ | B2C $[1]$ | B2C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : B2C [0] to B2C [4] (BLED2 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 10h (F1DACTL) FLED1 Current Setting Register Write

| 10h (F1DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MAXCF [2] | MAXCF [1] | MAXCF [0] | F1C [4] | F1C [3] | F1C [2] | F1C [1] | F1C [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : F1C [0] to F1C [4] (FLED1 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

D5 to D7 : MAXCF [0] to MAXCF [2] (Flash LED (FLED1, FLED2, FLED3) maximum current value settings)

| D7 | D6 | D5 | Max. Current value (mA) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $18.6(100 \%)$ |
| 0 | 0 | 1 | $16.275(87 \%)$ |
| 0 | 1 | 0 | $13.95(75 \%)$ |
| 0 | 1 | 1 | $11.625(62.5 \%)$ |
| 1 | 0 | 0 | $9.3(50 \%)$ |
| 1 | 0 | 1 | $6.975(37.5 \%)$ |
| 1 | 1 | 0 | $4.65(25 \%)$ |
| 1 | 1 | 1 | $2.325(12.5 \%)$ |

LV5219LG
address : 11h (F2DACTL) FLED2 Current Setting Register Write

| 11h (F2DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | F2C $[4]$ | F2C $[3]$ | F2C $[2]$ | F2C $[1]$ | F2C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : F2C [0] to F2C [4] (FLED2 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

address : 12h (F3DACTL) FLED3 Current Setting Register Write

| 12h (F3DACTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | - | F3C [4] | F3C $[3]$ | F3C $[2]$ | F3C $[1]$ | F3C $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D4 : F3C [0] to F3C [4] (FLED3 current settings)

| D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 1.2 |
| 0 | 0 | 0 | 1 | 0 | 1.8 |
| 0 | 0 | 0 | 1 | 1 | 2.4 |
| 0 | 0 | 1 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 0 | 1 | 3.6 |
| 0 | 0 | 1 | 1 | 0 | 4.2 |
| 0 | 0 | 1 | 1 | 1 | 4.8 |
| 0 | 1 | 0 | 0 | 0 | 5.4 |
| 0 | 1 | 0 | 0 | 1 | 6.0 |
| 0 | 1 | 0 | 1 | 0 | 6.6 |
| 0 | 1 | 0 | 1 | 1 | 7.2 |
| 0 | 1 | 1 | 0 | 0 | 7.8 |
| 0 | 1 | 1 | 0 | 1 | 8.4 |
| 0 | 1 | 1 | 1 | 0 | 9.0 |
| 0 | 1 | 1 | 1 | 1 | 9.6 |
| 1 | 0 | 0 | 0 | 0 | 10.2 |
| 1 | 0 | 0 | 0 | 1 | 10.8 |
| 1 | 0 | 0 | 1 | 0 | 11.4 |
| 1 | 0 | 0 | 1 | 1 | 12.0 |
| 1 | 0 | 1 | 0 | 0 | 12.6 |
| 1 | 0 | 1 | 0 | 1 | 13.2 |
| 1 | 0 | 1 | 1 | 0 | 13.8 |
| 1 | 0 | 1 | 1 | 1 | 14.4 |
| 1 | 1 | 0 | 0 | 0 | 15.0 |
| 1 | 1 | 0 | 0 | 1 | 15.6 |
| 1 | 1 | 0 | 1 | 0 | 16.2 |
| 1 | 1 | 0 | 1 | 1 | 16.8 |
| 1 | 1 | 1 | 0 | 0 | 17.4 |
| 1 | 1 | 1 | 0 | 1 | 18.0 |
| 1 | 1 | 1 | 1 | 0 | 18.6 |
| 1 | 1 | 1 | 1 | 1 | 0.0 |

LV5219LG
address : 13h (MFCTL) MLED Fade Time Setting Register Write

| 13h (MFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | MFOUT [2] | MFOUT [1] | MFOUT [0] | MFIN [2] | MFIN [1] | MFIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : MFIN [0] to MFIN [2] (Fin slope settings (MLED))

| D2 | D1 | D0 | MFIN (Normal Mode) | MFIN (Dim Mode) |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope | No slope |
| 0 | 0 | 1 | 0.050 s | 0.012 s |
| 0 | 1 | 0 | 0.1 s | 0.025 s |
| 0 | 1 | 1 | 0.15 s | 0.04 s |
| 1 | 0 | 0 | 0.2 s | 0.05 s |
| 1 | 0 | 1 | 0.25 s | 0.065 s |
| 1 | 1 | 0 | 0.3 s | 0.08 s |
| 1 | 1 | 1 | 0.5 s | 0.125 s |

D3 to D5 : MFOUT [0] to MFOUT [2] (Fout slope settings (MLED))

| D5 | D4 | D3 | MFOUT (Normal Mode) | MFOUT (Dim Mode) |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope | No slope |
| 0 | 0 | 1 | 0.1 s | 0.025 s |
| 0 | 1 | 0 | 0.15 s | 0.04 s |
| 0 | 1 | 1 | 0.2 s | 0.05 s |
| 1 | 0 | 0 | 0.25 s | 0.065 s |
| 1 | 0 | 1 | 0.3 s | 0.08 s |
| 1 | 1 | 0 | 0.5 s | 0.125 s |
| 1 | 1 | 1 | 1.0 s | 0.25 s |

address : 14h (SFCTL) MLED Fade Time Setting Register Write

| 14h (SFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | SFOUT [2] | SFOUT [1] | SFOUT [0] | SFIN [2] | SFIN [1] | SFIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : SFIN [0] to SFIN [2] (Fin slope settings (SLED1, SLED2))

| D2 | D1 | D0 | SFIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | 0.050 s |
| 0 | 1 | 0 | 0.1 s |
| 0 | 1 | 1 | 0.15 s |
| 1 | 0 | 0 | 0.2 s |
| 1 | 0 | 1 | 0.25 s |
| 1 | 1 | 0 | 0.3 s |
| 1 | 1 | 1 | 0.5 s |

D3 to D5 : SFOUT [0] to SFOUT [2] (Fout slope settings (SLED1, SLED2))

| D5 | D4 | D3 | SFOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | 0.1 s |
| 0 | 1 | 0 | 0.15 s |
| 0 | 1 | 1 | 0.2 s |
| 1 | 0 | 0 | 0.25 s |
| 1 | 0 | 1 | 0.3 s |
| 1 | 1 | 0 | 0.5 s |
| 1 | 1 | 1 | 1.0 s |

LV5219LG
address : 15h (R1FCTL) RLED1 Fade Time Setting Register Write

| 15h (R1FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R1FOUT [2] | R1FOUT [1] | R1FOUT [0] | R1FIN [2] | R1FIN [1] | R1FIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : R1FIN [0] to R1FIN [2] (Fin slope settings (RLED1))

| D2 | D1 | D0 | R1FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT1 time setting.

D3 to D5 : R1FOUT [0] to R1FOUT [2] (Fout slope settings (RLED1))

| D5 | D4 | D3 | R1FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT1 time setting.
address : 16h (G1FCTL) GLED1 Fade Time Setting Register Write

| 16h (G1FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G1FOUT [2] | G1FOUT [1] | G1FOUT [0] | G1FIN [2] | G1FIN [1] | G1FIN [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : G1FIN [0] to G1FIN [2] (Fin slope settings (GLED1))

| D2 | D1 | D0 | G1FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT1 time setting.

D3 to D5 : G1FOUT [0] to G1FOUT [2] (Fout slope settings (GLED1))

| D5 | D4 | D3 | G1FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

LV5219LG
address : 17h (B1FCTL) BLED1 Fade Time Setting Register Write

| 17h (B1FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B1FOUT [2] | B1FOUT [1] | B1FOUT [0] | B1FIN [2] | B1FIN [1] | B1FIN [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : B1FIN [0] to B1FIN [2] (Fin slope settings (BLED1))

| D2 | D1 | D0 | B1FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT1 time setting.

D3 to D5 : B1FOUT [0] to B1FOUT [2] (Fout slope settings (BLED1))

| D5 | D4 | D3 | B1FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT1 time setting

LV5219LG
address : 18h (RGB1GRCTL) RGB1 Gradation Setting Register Write

| 18h (RGB1GRCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | GHB1 | GHG1 | GHR1 | GR1M1 | GRON1 | AT1 $[2]$ | AT1 $[1]$ | AT1 $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : AT1 [0] to AT1 [2] (Automatic ON/OFF period settings (RED1, GLED1, BLED1))

| D2 | D1 | D0 | AT1 |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0.0625 s |
| 0 | 0 | 1 | 0.125 s |
| 0 | 1 | 0 | 0.25 s |
| 0 | 1 | 1 | 0.5 s |
| 1 | 0 | 0 | 1 s |
| 1 | 0 | 1 | 2 s |
| 1 | 1 | 0 | 4 s |
| 1 | 1 | 1 | 8 s |

*Default

D3 : GRON1 (Automatic ON/OFF function setting (RLED1, GLED1, BLED1))
0 : OFF *Default
1: ON
D4 : GR1M1 (Execute gradation once (RLED1, GLED1, BLED1))
0 : OFF *Default
1: ON
D5: GHR1 (Period mode setting (RLED1))
0 : Standard period *Default
1:1/2 period
D6 : GHG1 (Period mode setting (GLED1))
0 : Standard period *Default
1:1/2 period
D7: GHB1 (Period mode setting (BLED1))
0 : Standard period *Default
1:1/2 period
address : 19h (RGB1PUCTL) RGB1 Pulse Mode Setting Register Write

| 19h (RGB1PUCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | PRON1 | PT1 [2] | PT1 $[1]$ | PT1 $[0]$ | HO1 $[2]$ | HO1 $[1]$ | HO1 $[0]$ |
| R/W | $W$ | $W$ | $W$ | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : HO1 [0] to HO1 [2] (Hold time settings (RLED1, GRLD1, BLED1))

| D2 | D1 | D0 | HOLD TIME |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | None |
| 0 | 0 | 1 | ON/OFF period $\times 1$ |
| 0 | 1 | 0 | ON/OFF period $\times 2$ |
| 0 | 1 | 1 | ON/OFF period $\times 3$ |
| 1 | 0 | 0 | ON/OFF period $\times 4$ |
| 1 | 0 | 1 | ON/OFF period $\times 5$ |
| 1 | 1 | 0 | ON/OFF period $\times 6$ |
| 1 | 1 | 1 | ON/OFF period $\times 7$ |

D3 to D5 : PT1 [0] to PT1 [2] (Flashing count settings (RLED1, GRLD1, BLED1))

| D5 | D4 | D3 | Pulse Count |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | ON/OFF period $\times 1$ |
| 0 | 0 | 1 | ON/OFF period $\times 2$ |
| 0 | 1 | 0 | ON/OFF period $\times 3$ |
| 0 | 1 | 1 | ON/OFF period $\times 4$ |
| 1 | 0 | 0 | ON/OFF period $\times 5$ |
| 1 | 0 | 1 | ON/OFF period $\times 6$ |
| 1 | 1 | 0 | ON/OFF period $\times 7$ |
| 1 | 1 | 1 | ON/OFF period $\times 8$ |

[^0]LV5219LG
address : 1Ah (R1AOFFCTL) RLED1 OFF Position Setting Register Write

| 1Ah (R1AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R1Aoff [5] | R1Aoff [4] | R1Aoff [3] | R1Aoff [2] | R1Aoff [1] | R1Aoff [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : R1Aoff [0] to R1Aoff [5] (RLED1 automatic OFF position settings)
address : 1Bh (R1AONCTL) RLED1 ON Position Setting Register Write

| 1Bh (R1AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R1Aon [5] | R1Aon [4] | R1Aon [3] | R1Aon [2] | R1Aon [1] | R1Aon [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : R1Aon [0] to R1Aon [5] (RLED1 automatic ON position settings)
*R1Aoff = R1Aon = FF specifies "ON throughout the entire period."
R1Aoff $=$ R1Aon $\neq$ FF specifies "Off throughout the entire period."
LED control output waveform (RLED1), same for GLED1 and BLED1.
Rise position of clock 0 when D5 - D0 are set to all 0 .
Rise position of clock 63 when D5 - D0 are set to all 1.

address : 1Ch (G1AOFFCTL) GLED1 OFF Position Setting Register Write

| 1Ch (G1AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G1Aoff $[5]$ | G1Aoff $[4]$ | G1Aoff $[3]$ | G1Aoff $[2]$ | G1Aoff $[1]$ | G1Aoff $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : G1Aoff [0] to G1Aoff [5] (GLED1 automatic OFF position settings)

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address : 1Dh (G1AONCTL) GLED1 ON Position Setting Register Write

| 1Dh (G1AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G1Aon [5] | G1Aon [4] | G1Aon [3] | G1Aon [2] | G1Aon [1] | G1Aon [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : G1Aon [0] to G1Aon [5] (GLED1 automatic ON position settings)
*G1Aoff = G1Aon = FF specifies "ON throughout the entire period."
G1Aoff $=$ G1Aon $\neq$ FF specifies "OFF throughout the entire period."
address : 1Eh (B1AOFFCTL) BLED1 OFF Position Setting Register Write

| 1Eh (B1AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B1Aoff $[5]$ | B1Aoff $[4]$ | B1Aoff $[3]$ | B1Aoff $[2]$ | B1Aoff $[1]$ | B1Aoff $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : B1Aoff [0] to B1Aoff [5] (BLED1 automatic OFF position settings)
address : 1Fh (B1AONCTL) BLED1 ON Position Setting Register Write

| 1Fh (B1AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B1Aon [5] | B1Aon [4] | B1Aon [3] | B1Aon [2] | B1Aon [1] | B1Aon [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : B1Aon [0] to B1Aon [5] (BLED1 automatic ON position settings)
*B1Aoff = B1Aon = FF specifies "ON throughout the entire period."
B1Aoff $=$ B1Aon $\neq$ FF specifies "OFF throughout the entire period."
address : 20h (R2FCTL) RLED2 Fade Time Setting Register Write

| 20h (R2FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R2FOUT [2] | R2FOUT [1] | R2FOUT [0] | R2FIN [2] | R2FIN [1] | R2FIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : R2FIN [0] to R2FIN [2] (Fin slope settings (RLED2))

| D2 | D1 | D0 | R2FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT2 time setting.

D3 to D5 : R2FOUT [0] to R2FOUT [2] (Fout slope settings (RLED2))

| D5 | D4 | D3 | R2FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT2 time setting.
address : 21h (G2FCTL) GLED2 Fade Time Setting Register Write

| 21h (G2FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G2FOUT [2] | G2FOUT [1] | G2FOUT [0] | G2FIN [2] | G2FIN [1] | G2FIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : G2FIN [0] to G2FIN [2] (Fin slope settings (GLED2))

| D2 | D1 | D0 | G2FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT2 time setting.

D3 to D5 : G2FOUT [0] to G2FOUT [2] (Fout slope settings (GLED2))

| D5 | D4 | D3 | G2FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

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address : 22h (B2FCTL) BLED2 Fade Time Setting Register Write

| 22h (B2FCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B2FOUT [2] | B2FOUT [1] | B2FOUT [0] | B2FIN [2] | B2FIN [1] | B2FIN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : B2FIN [0] to B2FIN [2] (Fin slope settings (BLED2))

| D2 | D1 | D0 | B2FIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

The slope time MAX is $1 / 2$ of the AT2 time setting.

D3 to D5 : B2FOUT [0] to B2FOUT [2] (Fout slope settings (BLED2))

| D5 | D4 | D3 | R2FOUT |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No slope |
| 0 | 0 | 1 | $1 / 16$ |
| 0 | 1 | 0 | $1 / 8$ |
| 0 | 1 | 1 | $1 / 4$ |
| 1 | 0 | 0 | $3 / 8$ |
| 1 | 0 | 1 | $1 / 2$ |
| 1 | 1 | 0 | $3 / 4$ |
| 1 | 1 | 1 | Slope MAX |

*Default

LV5219LG
address : 23h (RGB2GRCTL) RGB2 Gradation Setting Register Write

| 23h (RGB2GRCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | GHB2 | GHG2 | GHR2 | GR1M2 | GRON2 | AT2 $[2]$ | AT2 $[1]$ | AT2 $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : AT2 [0] to AT2 [2] (Automatic ON/OFF period settings (RED2, GLED2, BLED2))

| D2 | D1 | D0 | AT2 |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0.0625 s |
| 0 | 0 | 1 | 0.125 s |
| 0 | 1 | 0 | 0.25 s |
| 0 | 1 | 1 | 0.5 s |
| 1 | 0 | 0 | 1 s |
| 1 | 0 | 1 | 2 s |
| 1 | 1 | 0 | 4 s |
| 1 | 1 | 1 | 8 s |

*Default

D3 : GRON2 (Automatic ON/OFF function setting (RLED2, GLED2, BLED2))
0 : OFF *Default
1: ON
D4 : GR1M2 (Execute gradation once (RLED2, GLED2, BLED2))
0 : OFF *Default
1: ON
D5: GHR2 (Period mode setting (RLED2))
0 : Standard period *Default
1:1/2 period
D6 : GHG2 (Period mode setting (GLED2))
0 : Standard period *Default
1:1/2 period
D7: GHB2 (Period mode setting (BLED2))
0 : Standard period *Default
1:1/2 period
address : 24h (RGB2PUCTL) RGB2 Pulse Mode Setting Register Write

| 24h (RGB2PUCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | PRON2 | PT2 [2] | PT2 $[1]$ | PT2 $[0]$ | HO2 $[2]$ | HO2 $[1]$ | HO2 $[0]$ |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : HO2 [0] to HO2 [2] (Hold time settings (RLED2, GRLD2, BLED2))

| D2 | D1 | D0 | HOLD TIME |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | None |
| 0 | 0 | 1 | ON/OFF period $\times 1$ |
| 0 | 1 | 0 | ON/OFF period $\times 2$ |
| 0 | 1 | 1 | ON/OFF period $\times 3$ |
| 1 | 0 | 0 | ON/OFF period $\times 4$ |
| 1 | 0 | 1 | ON/OFF period $\times 5$ |
| 1 | 1 | 0 | ON/OFF period $\times 6$ |
| 1 | 1 | 1 | ON/OFF period $\times 7$ |

D3 to D5 : PT2 [0] to PT2 [2] (Flashing count settings (RLED2, GRLD2, BLED2))

| D5 | D4 | D3 | PULSE |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | ON/OFF period $\times 1$ |
| 0 | 0 | 1 | ON/OFF period $\times 2$ |
| 0 | 1 | 0 | ON/OFF period $\times 3$ |
| 0 | 1 | 1 | ON/OFF period $\times 4$ |
| 1 | 0 | 0 | ON/OFF period $\times 5$ |
| 1 | 0 | 1 | ON/OFF period $\times 6$ |
| 1 | 1 | 0 | ON/OFF period $\times 7$ |
| 1 | 1 | 1 | ON/OFF period $\times 8$ |

D6 : PRON2 (Pulse mode setting (RLED2, GRLD2, BLED2))
0 : OFF *Default
1 : Pulse mode

LV5219LG
address : 25h (R2AOFFCTL) RLED2 OFF Position Setting Register Write

| 25h (R2AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R2Aoff [5] | R2Aoff $[4]$ | R2Aoff $[3]$ | R2Aoff $[2]$ | R2Aoff $[1]$ | R2Aoff $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : R2Aoff [0] to R2Aoff [5] (RLED2 automatic OFF position settings)
address : 26h (R2AONCTL) RLED2 ON Position Setting Register Write

| 26h (R2AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | R2Aon [5] | R2Aon [4] | R2Aon $[3]$ | R2Aon [2] | R2Aon [1] | R2Aon [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : R2Aon [0] to R2Aon [5] (RLED2 automatic ON position settings)
*R2Aoff = R2Aon = FF specifies "ON throughout the entire period."
R2Aoff $=$ R2Aon $\neq$ FF specifies "OFF throughout the entire period."
LED control output waveform (RLED2), same for GLED2 and BLED2.
Rise position of clock 0 when D5 - D0 are set to all 0 .
Rise position of clock 63 when D5 - D0 are set to all 1.

address : 27h (G2AOFFCTL) GLED2 OFF Position Setting Register Write

| 27h (G2AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G2Aoff $[5]$ | G2Aoff $[4]$ | G2Aoff $[3]$ | G2Aoff $[2]$ | G2Aoff $[1]$ | G2Aoff [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : G2Aoff [0] to G2Aoff [5] (GLED2 automatic OFF position settings)
address : 28h (G2AONCTL) GLED2 ON Position Setting Register Write

| 28h (G2AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | G2Aon [5] | G2Aon $[4]$ | G2Aon $[3]$ | G2Aon [2] | G2Aon [1] | G2Aon [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : G2Aon [0] to G2Aon [5] (GLED2 automatic ON position settings)
*G2Aoff = G2Aon = FF specifies "ON throughout the entire period."
G2Aoff $=$ G2Aon $\neq$ FF specifies "OFF throughout the entire period."
address : 29h (B2AOFFCTL) BLED2 OFF Position Setting Register Write

| 29h (B2AOFFCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B2Aoff [5] | B2Aoff [4] | B2Aoff [3] | B2Aoff [2] | B2Aoff [1] | B2Aoff [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : B2Aoff [0] to B2Aoff [5] (BLED2 automatic OFF position settings)
address : 2Ah (B2AONCTL) BLED2 ON Position Setting Register Write

| 2Ah (B2AONCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | B2Aon [5] | B2Aon $[4]$ | B2Aon $[3]$ | B2Aon [2] | B2Aon $[1]$ | B2Aon [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ | $W$ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D5 : B2Aon [0] to B2Aon [5] (BLED2 automatic ON position settings)
*B2Aoff = B2Aon = FF specifies "ON throughout the entire period."
B2Aoff $=$ B2Aon $=$ FF specifies "OFF throughout the entire period."
address : 2Bh (KEYCTL) KLED1, KLED2 Changeover Voltage Setting Register Write

| 2Bh (KEYCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | KEY2C [3] | KEY2C [2] | KEY2C [1] | KEY2C [0] | KEY1C [3] | KEY1C [2] | KEY1C [1] | KEY1C [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D3 : KEY1C [0] to KEY1C [3] (KEYLED control changeover voltage)

| D3 | D2 | D1 | D0 | KEY1C |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Brightness 1 |
| 0 | 0 | 0 | 1 | Brightness 2 |
| 0 | 0 | 1 | 0 | Brightness 3 |
| 0 | 0 | 1 | 1 | Brightness 4 |
| 0 | 1 | 0 | 0 | Brightness 5 |
| 0 | 1 | 0 | 1 | Brightness 6 |
| 0 | 1 | 1 | 0 | Brightness 7 |
| 0 | 1 | 1 | 1 | Brightness 8 |
| 1 | 0 | 0 | 0 | Brightness 9 |
| 1 | 0 | 0 | 1 | Brightness 10 |
| 1 | 0 | 1 | 0 | Brightness 11 |
| 1 | 0 | 1 | 1 | Brightness 12 |
| 1 | 1 | 0 | 0 | Brightness 13 |
| 1 | 1 | 0 | 1 | Brightness 14 |
| 1 | 1 | 1 | 0 | Brightness 15 |
| 1 | 1 | 1 | 1 | Inhibited |

*Default
*Lit (KLED : ON) when dark if KLED automatic ON is set.
*The setting brightness 2 means that KLED turns on when a changeover from brightness 3 to brightness 2 occurs if KLED automatic ON is set.

D4 to D7 : KEY2C [0] to KEY2C [3] (KEYLED control changeover voltage)

| D7 | D6 | D5 | D4 | KEY2C |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Brightness 1 |
| 0 | 0 | 0 | 1 | Brightness 2 |
| 0 | 0 | 1 | 0 | Brightness 3 |
| *Default |  |  |  |  |
| 0 | 0 | 1 | 1 | Brightness 4 |
| 0 | 1 | 0 | 0 | Brightness 5 |
| 0 | 1 | 0 | 1 | Brightness 6 |
| 0 | 1 | 1 | 0 | Brightness 7 |
| 0 | 1 | 1 | 1 | Brightness 8 |
| 1 | 0 | 0 | 0 | Brightness 9 |
| 1 | 0 | 0 | 1 | Brightness 10 |
| 1 | 0 | 1 | 0 | Brightness 11 |
| 1 | 0 | 1 | 1 | Brightness 12 |
| 1 | 1 | 0 | 0 | Brightness 13 |
| 1 | 1 | 0 | 1 | Brightness 14 |
| 1 | 1 | 1 | 0 | Brightness 15 |
| 1 | 1 | 1 | 1 | Inhibited |

*Lit (KLED : ON) when dark if KLED automatic ON is set.
*The setting brightness 2 means that KLED turns on when a changeover from brightness 3 to brightness 2 occurs if KLED automatic ON is set.

Brightness Levels

| Brightness <br> (Lx) | Threshold Current <br> ( $\mu \mathrm{A})$ | Threshold Voltage <br> (V) | Brightness Level | The resistance value of the external reresistor is $22 \mathrm{~K} \Omega$ Compatible with LOG type brightness sensor. |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Brightness 1 |  |
| 25 | 11 | 0.25 |  | Adjustment of sensor variations sensitivity variance <br> When TDA 0.42 V is set <br> When TAU 0.84 V is set |
|  |  |  | Brightness 2 |  |
| 40 | 12.8 | 0.29 |  |  |
|  |  |  | Brightness 3 |  |
| 60 | 14.6 | 0.33 |  |  |
|  |  |  | Brightness 4 |  |
| 90 | 16.3 | 0.38 |  |  |
|  |  |  | Brightness 5 |  |
| 140 | 18 | 0.42 |  |  |
|  |  |  | Brightness 6 |  |
| 220 | 19.7 | 0.46 |  |  |
|  |  |  | Brightness 7 |  |
| 350 | 21.4 | 0.50 |  |  |
|  |  |  | Brightness 8 |  |
| 550 | 23.1 | 0.55 |  |  |
|  |  |  | Brightness 9 |  |
| 850 | 24.8 | 0.59 |  |  |
|  |  |  | Brightness 10 |  |
| 1300 | 26.5 | 0.63 |  |  |
|  |  |  | Brightness 11 |  |
| 1900 | 28.2 | 0.67 |  |  |
|  |  |  | Brightness 12 |  |
| 3000 | 30.5 | 0.72 |  |  |
|  |  |  | Brightness 13 |  |
| 5000 | 33 | 0.76 |  |  |
|  |  |  | Brightness 14 |  |
| 7000 | 35.5 | 0.80 |  |  |
|  |  |  | Brightness 15 |  |
| 10000 | 38 | 0.84 |  |  |
|  |  |  | Brightness 16 |  |

Relationship between Brightness and Threshold Current


LV5219LG
address : 2Ch (PTCTL) Automatic Brightness Control Mode Setting 1 Register Write

| 2Ch (PTCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | SWCTL | PTSW | KISW | SMPN [1] | SMPN [0] | SMPF [2] | SMPF [1] | SMPF [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : SMPF [0] to SMPF [2] (Brightness sensor sampling period settings)

| D2 | D1 | D0 | SMPF |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 131.072 ms |
| 0 | 0 | 1 | 262.144 ms |
| 0 | 1 | 0 | 524.288 ms |
| 0 | 1 | 1 | 1.049 s |
| 1 | 0 | 0 | 2.098 s |
| 1 | 0 | 1 | 4.196 s |
| 1 | 1 | 0 | 8.392 s |
| 1 | 1 | 1 | 20 ms |

*Default


* Continuous operation when SMPF is set to 20 ms and intermittent operation otherwise.

D3 to D4 : SMPN [0] to SMPN [1] (Brightness sensor sampling count settings)

| D4 | D3 | SMPN |
| :---: | :---: | :---: |
| 0 | 0 | 1 time |
| 0 | 1 | 2 times |
| 1 | 0 | 3 times |
| 1 | 1 | 4 times |

D5 : KISW (MLED fixed/automatic current settings)
0 : Fixed *Default
1 : Automatic (brightness control)
D6 : PTSW (Sensor ON/OFF)
0 : OFF *Default
1: ON

D7 : SWCTL (Sensor ON/OFF SW polarity)
0 : Standard *Default
1 : Inverted
address : 2Dh (INTMASK) INT Mask Setting Register Write

| 2Dh (INTMASK) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | INTCR | - | INTM6 | INTM5 | INTM4 | INTM3 | INTM2 | INTM1 |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


| D0 : INTM1 | (INT1 mask setting - interrupt source 1 mask) <br> 0 : OFF *Default <br> 1: ON |
| :---: | :---: |
| D1: INTM2 | ```(INT2 mask setting - interrupt source 2 mask) 0: OFF *Default 1:ON``` |
| D2 : INTM3 | ```(INT3 mask setting - interrupt source 3 mask) 0 : OFF *Default 1 : ON``` |
| D3: INTM4 | ```(INT4 mask setting - interrupt source 4 mask) 0 : OFF *Default 1 : ON``` |
| D4 : INTM5 | ```(INT5 mask setting - interrupt source 5 mask) 0 : OFF *Default 1: ON``` |
| D5 : INTM6 | (INT6 mask setting - interrupt source 6 mask) <br> 0 : OFF *Default <br> 1: ON |
| D7 : INTCR | (INT clear) <br> 0 : INT accepted *Default <br> 1 : INT cleared <br> *This bit is set to 0 to enable interrupt |

LV5219LG
address : 2Eh (INTDET) INT Detection Register - Read only

| 2Eh (INTDET) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | - | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 |
| R/W | R | R | R | R | R | R | R | R |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


| D0 : INT1 | (interrupt source 1) |
| :--- | :--- |
|  | $0:$ OFF *Default |
|  | $1:$ ON |
|  | *Brightness detection for KEY-LED (read only) |


| D1 : INT2 | (interrupt source 2) |
| :--- | :--- |
|  | $0:$ OFF *Default |
|  | $1:$ ON |
|  | *End of white LED fade IN/OUT (read only) |

D2 : INT3 (interrupt source 3)
0 : OFF *Default
1: ON
*End of group 1 (RLED1, GLED1, BLED1) fade IN/OU (read only)

D3 : INT4 (interrupt source 4)
0 : OFF *Default
1: ON
*End of group 2(RLED2, GLED2, BLED2) fade IN/OU (read only)
D4 : INT5 (interrupt source 5)
0 : OFF *Default
1: ON
*End of group 1 (RLED1, GLED1, BLED1) gradation (read only)

```
D5 : INT6 (interrupt source 6)
0: OFF *Default
1:ON
    *End of group 2(RLED2, GLED2, BLED2) gradation (read only)
```

Interrupts associated with the 1 bits of the INT Detection Register occur.

LV5219LG
address : 2Fh (STATUS) Status Detect Register - Read only

| 2Fh (STATUS) | D 7 | D 6 | D 5 | D 4 | D 3 | D 2 | D 1 | D 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | $\mathrm{XM}[3]$ | $\mathrm{XM}[2]$ | $\mathrm{XM}[1]$ | $\mathrm{XM}[0]$ | - | - | KEYON | DCDC |
| R/W | R | R | R | R | R | R | R | R |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : DCDC (DC/DC step-up state (read only))
0 : Through $\cdots$ DC/DC is not stepped-up. *Default
1 : Step-up $\quad \cdots$ DC/DC stepped-up.
D1: KEYON (KEY ON/OFF(read only))
0 : OFF $\quad \cdots$ Brightness is above or equal to the KEYLED changeover voltage. *Default
$1:$ ON $\quad \cdots$ Brightness is less than the KEYLED changeover voltage.
D4 to D7 : XM [0] to XM [3] (Brightness information (read only))

| D7 | D6 | D5 | D4 | XM |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Brightness 1 |
| 0 | 0 | 0 | 1 | Brightness 2 |
| 0 | 0 | 1 | 0 | Brightness 3 |
| 0 | 0 | 1 | 1 | Brightness 4 |
| 0 | 1 | 0 | 0 | Brightness 5 |
| 0 | 1 | 0 | 1 | Brightness 6 |
| 0 | 1 | 1 | 0 | Brightness 7 |
| 0 | 1 | 1 | 1 | Brightness 8 |
| 1 | 0 | 0 | 0 | Brightness 9 |
| 1 | 0 | 0 | 1 | Brightness 10 |
| 1 | 0 | 1 | 0 | Brightness 11 |
| 1 | 0 | 1 | 1 | Brightness 12 |
| 1 | 1 | 0 | 0 | Brightness 13 |
| 1 | 1 | 0 | 1 | Brightness 14 |
| 1 | 1 | 1 | 0 | Brightness 15 |
| 1 | 1 | 1 | 1 | Brightness 16 |

LV5219LG
address : 30h (PTMDACTL0) Automatic Brightness Control Mode Current Settings 0 Register Write

| 30h (PTMDACTLO) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINO [6] | YMAIN0 [5] | YMAIN0 [4] | YMAIN0 [3] | YMAINO [2] | YMAIN0 [1] | YMAIN0 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN0 [0] to YMIAN0 [6] (MLED current settings (normal mode) * MLED current settings for brightness 1

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.15 inhibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.3 inhibited |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.45 inhibited |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.75 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.90 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.05 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.20 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.35 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.50 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.65 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.80 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.95 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 2.10 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 2.25 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 2.40 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 2.55 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 2.70 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 2.85 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 3.00 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 3.15 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 3.30 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 3.45 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 3.60 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 3.75 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 3.90 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 4.05 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 4.20 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 4.35 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 4.50 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4.65 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 4.80 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 4.95 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 5.10 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 5.25 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 5.40 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 5.55 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 5.70 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 5.85 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 6.00 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 6.15 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 6.30 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 6.45 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 6.60 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 6.75 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 6.90 |

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Continued from preceding page.

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 7.05 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 7.20 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 7.35 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 7.50 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 7.65 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 7.80 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 7.95 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 8.10 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 8.25 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 8.40 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8.55 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 8.70 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 8.85 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 9.00 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 9.15 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 9.30 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 9.45 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 9.60 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 9.75 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 9.90 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 10.05 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 10.20 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 10.35 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 10.50 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 10.65 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 10.80 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 10.95 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 11.10 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 11.25 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 11.40 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 11.55 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 11.70 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 11.85 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 12.00 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 12.15 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 12.30 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 12.45 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 12.60 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 12.75 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 12.90 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 13.05 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 13.20 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 13.35 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 13.50 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 13.65 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 13.80 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 13.95 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 14.10 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 14.25 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 14.40 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 14.55 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 14.70 |

Continued from preceding page.

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Current value (mA) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 14.85 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 15.00 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 15.15 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 15.30 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 15.45 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 15.60 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 15.75 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 15.90 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 16.05 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 16.20 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 16.35 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 16.50 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 16.65 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 16.80 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 16.95 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 17.10 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 17.25 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 17.40 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 17.55 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 17.70 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 17.85 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 18.00 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 18.15 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 18.30 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 18.45 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 18.60 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.00 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.00 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.00 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.00 |

address : 31h (PTMDACTL1) Automatic Brightness Control Mode Current Setting 1 Register Write

| 31h (PTMDACTL1) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN1 [6] | YMAIN1 [5] | YMAIN1 [4] | YMAIN1 [3] | YMAIN1 [2] | YMAIN1 [1] | YMAIN1 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN1 [0] to YMIAN1 [6] (MLED current settings for brightness 2)
*The current values are the same as those for the MLED current settings.
address : 32h (PTMDACTL2) Automatic Brightness Control Mode Current Setting 2 Register Write

| 32h (PTMDACTL2) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN2 [6] | YMAIN2 [5] | YMAIN2 [4] | YMAIN2 [3] | YMAIN2 [2] | YMAIN2 [1] | YMAIN2 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN2 [0] to YMIAN2 [6] (MLED current settings for brightness 3)
*The current values are the same as those for the MLED current settings.
address : 33h (PTMDACTL3) Automatic Brightness Control Mode Current Setting 3 Register Write

| 33h (PTMDACTL3) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN3 [6] | YMAIN3 [5] | YMAIN3 [4] | YMAIN3 [3] | YMAIN3 [2] | YMAIN3 [1] | YMAIN3 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN3 [0] to YMIAN3 [6] (MLED current settings for brightness 4)
*The current values are the same as those for the MLED current settings.
address : 34h (PTMDACTL4) Automatic Brightness Control Mode Current Setting 4 Register Write

| 34h (PTMDACTL4) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN4 [6] | YMAIN4 [5] | YMAIN4 [4] | YMAIN4 [3] | YMAIN4 [2] | YMAIN4 [1] | YMAIN4 [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN4 [0] to YMIAN4 [6] (MLED current settings for brightness 5)
*The current values are the same as those for the MLED current settings.
address : 35h (PTMDACTL5) Automatic Brightness Control Mode Current Setting 5 Register Write

| 35h (PTMDACTL5) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN5 [6] | YMAIN5 [5] | YMAIN5 [4] | YMAIN5 [3] | YMAIN5 [2] | YMAIN5 [1] | YMAIN5 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN5 [0] to YMIAN5 [6] (MLED current settings for brightness 6)
*The current values are the same as those for the MLED current settings.
address : 36h (PTMDACTL6) Automatic Brightness Control Mode Current Setting 6 Register Write

| 36h (PTMDACTL6) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN6 [6] | YMAIN6 [5] | YMAIN6 [4] | YMAIN6 [3] | YMAIN6 [2] | YMAIN6 [1] | YMAIN6 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN6 [0] to YMIAN6 [6] (MLED current settings for brightness 7)
*The current values are the same as those for the MLED current settings.
address: 37h (PTMDACTL7) Automatic Brightness Control Mode Current Setting 7 Register Write

| 37h (PTMDACTL7) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN7 [6] | YMAIN7 [5] | YMAIN7 [4] | YMAIN7 [3] | YMAIN7 [2] | YMAIN7 [1] | YMAIN7 [0] |
| R/W | $W$ | $W$ | $W$ | $W$ | $W$ | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN7 [0] to YMIAN7 [6] (MLED current settings for brightness 8)
*The current values are the same as those for the MLED current settings.
address: 38h (PTMDACTL8) Automatic Brightness Control Mode Current Setting 8 Register Write

| 38h (PTMDACTL8) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN8 [6] | YMAIN8 [5] | YMAIN8 [4] | YMAIN8 [3] | YMAIN8 [2] | YMAIN8 [1] | YMAIN8 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN8 [0] to YMIAN8 [6] (MLED current settings for brightness 9)
*The current values are the same as those for the MLED current settings.
address : 39h (PTMDACTL9) Automatic Brightness Control Mode Current Setting 9 Register Write

| 39h (PTMDACTL9) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIN9 [6] | YMAIN9 [5] | YMAIN9 [4] | YMAIN9 [3] | YMAIN9 [2] | YMAIN9 [1] | YMAIN9 [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAN9 [0] to YMIAN9 [6] (MLED current settings for brightness 10)
*The current values are the same as those for the MLED current settings.
address : 3Ah (PTMDACTLA) Automatic Brightness Control Mode Current Setting A Register Write

| 3Ah (PTMDACTLA) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINA [6] | YMAINA [5] | YMAINA [4] | YMAINA [3] | YMAINA [2] | YMAINA [1] | YMAINA [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIANA [0] to YMIANA [6] (MLED current settings for brightness 11)
*The current values are the same as those for the MLED current settings.
address : 3Bh (PTMDACTLB) Automatic Brightness Control Mode Current Setting B Register Write

| 3Bh (PTMDACTLB) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINB [6] | YMAINB [5] | YMAINB [4] | YMAINB [3] | YMAINB [2] | YMAINB [1] | YMAINB [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIANB [0] to YMIANB [6] (MLED current settings for brightness 12)
*The current values are the same as those for the MLED current settings.
address : 3Ch (PTMDACTLC) Automatic Brightness Control Mode Current Setting C Register Write

| 3Ch (PTMDACTLC) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINC [6] | YMAINC [5] | YMAINC [4] | YMAINC [3] | YMAINC [2] | YMAINC [1] | YMAINC [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIANC [0] to YMIANC [6] (MLED current settings for brightness 13)
*The current values are the same as those for the MLED current settings.
address : 3Dh (PTMDACTLD) Automatic Brightness Control Mode Current Setting D Register Write

| 3Dh (PTMDACTLD) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAIND [6] | YMAIND [5] | YMAIND [4] | YMAIND [3] | YMAIND [2] | YMAIND [1] | YMAIND [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIAND [0] to YMIAND [6] (MLED current settings for brightness 14)
*The current values are the same as those for the MLED current settings.
address : 3Eh (PTMDACTLE) Automatic Brightness Control Mode Current Setting E Register Write

| 3Eh (PTMDACTLE) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINE [6] | YMAINE [5] | YMAINE [4] | YMAINE [3] | YMAINE [2] | YMAINE [1] | YMAINE [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIANE [0] to YMIANE [6] (MLED current settings for brightness 15)
*The current values are the same as those for the MLED current settings.

LV5219LG
address : 3Fh (PTMDACTLF) Automatic Brightness Control Mode Current Setting F Register Write

| 3Fh (PTMDACTLF) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | YMAINF [6] | YMAINF [5] | YMAINF [4] | YMAINF [3] | YMAINF [2] | YMAINF [1] | YMAINF [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D6 : YMIANF [0] to YMIANF [6] (MLED current settings for brightness 16)
*The current values are the same as those for the MLED current settings.
address : 40h (PTCTL2) Automatic Brightness Control Mode Setting 2 Register Write

| 40h (PTCTL2) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | TUP [3] | TUP [2] | TUP [1] | TUP [0] | TDWN [3] | TDWN [2] | TDWN [1] | TDWN [0] |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D3 : TDWNE [0] to TDWN [3] (MLED current, brightness control change time (when decreasing)

| D3 | D2 | D1 | D0 | TDWN |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0.256 ms |
| 0 | 0 | 0 | 1 | 0.512 ms |
| 0 | 0 | 1 | 0 | 1.024 ms |
| 0 | 0 | 1 | 1 | 2.048 ms |
| 0 | 1 | 0 | 0 | 4.096 ms |
| 0 | 1 | 0 | 1 | 8.192 ms |
| 0 | 1 | 1 | 0 | 16.384 ms |
| 0 | 1 | 1 | 1 | 32.768 ms |
| 1 | 0 | 0 | 0 | 65.536 ms |
| 1 | 0 | 0 | 1 | 131.072 ms |
| 1 | 0 | 1 | 0 | 262.144 ms |
| 1 | 0 | 1 | 1 | 524.288 ms |
| 1 | 1 | 0 | 0 | 1.049 s |
| 1 | 1 | 0 | 1 | 2.097 s |
| 1 | 1 | 1 | 0 | 4.194 s |
| 1 | 1 | 1 | 1 | 8.389 s |

D4 to D7 : TUP [0] to TUP [3] (MLED current, brightness control change time (when increasing)

| D7 | D6 | D5 | D4 | TUP |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0.256 ms |
| 0 | 0 | 0 | 1 | 0.512 ms |
| 0 | 0 | 1 | 0 | 1.024 ms |
| 0 | 0 | 1 | 1 | 2.048 ms |
| 0 | 1 | 0 | 0 | 4.096 ms |
| 0 | 1 | 0 | 1 | 8.192 ms |
| 0 | 1 | 1 | 0 | 16.384 ms |
| 0 | 1 | 1 | 1 | 32.768 ms |
| 1 | 0 | 0 | 0 | 65.536 ms |
| 1 | 0 | 0 | 1 | 131.072 ms |
| 1 | 0 | 1 | 0 | 262.144 ms |
| 1 | 0 | 1 | 1 | 524.288 ms |
| 1 | 1 | 0 | 0 | 1.049 s |
| 1 | 1 | 0 | 1 | 2.097 s |
| 1 | 1 | 1 | 0 | 4.194 s |
| 1 | 1 | 1 | 1 | 8.389 s |

LV5219LG
address : 41h (PTCTL3) Automatic Brightness Control Mode Setting 3 Register Write

| 41h (PTCTL3) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | - | TAU [2] | TAU $[1]$ | TAU $[0]$ | - | TAD $[2]$ | TAD $[1]$ | TAD $[0]$ |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 to D2 : TAD [0] to TAD [2] (For sensor variation adjustment 1) *MIN setting : Value established when sensor variation adjustment 2 is set to 0.84 V
140 lux

| D2 | D1 | D0 | threshold voltage $(V)$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0.32 |
| 0 | 0 | 1 | 0.34 |
| 0 | 1 | 0 | 0.37 |
| 0 | 1 | 1 | 0.39 |
| 1 | 0 | 0 | 0.42 |
| 1 | 0 | 1 | 0.44 |
| 1 | 1 | 0 | 0.47 |
| 1 | 1 | 1 | 0.49 |

D4 to D6 : TAU [0] to TAU [2] (For sensor variation adjustment 2) * MAX setting 10000 lux

| D6 | D5 | D4 | threshold voltage $(\mathrm{V})$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0.65 |
| 0 | 0 | 1 | 0.71 |
| 0 | 1 | 0 | 0.78 |
| 0 | 1 | 1 | 0.84 |
| 1 | 0 | 0 | 0.90 |
| 1 | 0 | 1 | 0.97 |
| 1 | 1 | 0 | 1.03 |
| 1 | 1 | 1 | 1.10 |

*Default
address : 42h (GPOCTL) GPO Setting Register Write

| 42h (GPOCTL) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Register name | MFXSW | - | GPO22 | GPO12 | GPO02 | GPO21 | GPO11 | GPO01 |
| R/W | W | W | W | W | W | W | W | W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : GPO01 (GPO0 output setting 1)
0 : Low output *Default
1 : High output
D1: GPO11 (GPO1 output setting 1)
0 : Low output *Default
1 : High output
D2 : GPO21 (GPO2 output setting 1)
0 : Low output *Default
1 : High output
D3: GPO02 (GPO0 output setting 2)
0 : OPEN *Default
1 : Buffer output

D4: GPO12 (GPO1 output setting 2)
0 : OPEN *Default
1 : Buffer output

D5: GPO22 (GPO2 output setting 2)
0 : OPEN *Default
1 : Buffer output
D7 : MFXSW (Step-up mode settings in which LED pins are set to the same level)
0 : Turns on the step-up mode in which the LED pins are set to the predetermined voltage level when the voltage at the MLED pins goes down and a mode change from through to step-up occurs.
*Default
1 : Turns on the fixed voltage output mode when the voltage at the MLED pins goes down and a mode change from through to step-up occurs.

## Precautions for serial transmission and use

* When the switching regulator is to be started, the LED driver must be turned off.
* When the MLED4, 5 and 6 settings are to be turned on as the main LED drivers, either MLED4, MLED5, and MLED6 must be turned off after fade out, or they must be set to "always ON."
* When the SLED2 setting is to be turned on as the SLED driver, either SLED2 must be turned off after fade out, or it must be set to "always ON."
* When LED pins are not to be used

When no LED is to be connected to the LED pin, the LED driver pin must be connected to VBAT.

* Thermal shutdown operation

At a high temperature, the thermal shutdown is activated. In this case, all of the LEDs are turned off, and the voltage stepping-up operation is stopped.
The serial registers are held in the HOLD state. When the temperature goes down to the normal level, the IC self restores.
However, the IC will not self-restore if the short-circuit prevention circuit (SCP) is activated when DC/DC circuit is turned off.

* IN pin H limit operation

When the IN pin becomes approximately 0.6 V higher than the $\mathrm{DC} / \mathrm{DC}$ set voltage, the H limit operation is triggered.
H limit operation causes DC/DC circuit to stop the voltage stepping-up operation, but when the voltage falls to the normal level, the the IC self-restores.
The H limit voltage becomes approximately 0.6 V higher than the fixed mode set voltage and varies when the set voltage changes. When the set voltage is 4.3 V , the H limit voltage will be approximately 4.9 V , and when the set voltage is approximately 5.0 V , the H limit voltage will be approximately 5.6 V .
H limit operation is also effective in a mode in which the LED pin voltage is made constant, so in this mode as well a fixed mode output voltage must be set in consideration of the H limit voltage.

* RESET serial communication

The RESET pin must be cleared $(\mathrm{L} \rightarrow \mathrm{H})$ after VBAT is started.
$\mathrm{V}_{\mathrm{DD}}$ and $\mathrm{V}_{\mathrm{DD}} \mathrm{D} 2$ are unrelated to the RESET function.
Serial communication does not take place until VDD is started after RESET is released, When voltage VDD does not exist, no communication can be carried out and RESET is not triggered, either.
The registers hold their state.

* Regarding the switching regulator short-circuit protection circuit (SCP)

When the switching regulator output falls, it is assumed that a short circuit has occurred, and the SCP is activated to prevent an excessively large current from flowing. When the IN pin voltage falls by about 30 mV from the noload output value, an internal timer operates. If the reduced voltage condition continues for 10 msec , the LV5219LG will judge that a short circuit has occurred, and stop the switching regulator control circuit. After the switching regulator control circuit has stopped, it does not self-restore. However, it can be reset by either applying a RESET, or sending a command to set the serial control RGSW to 0 .

In a mode in which the LED pin voltage is made constant, the same operation takes place when the MLED pin voltage falls by 60 mV , and the SCP is activated. As in the case of the constant voltage mode, a self-restore does not take place, and the resetting method is also the same.

Serial map

| Address | Register name | Description | R/W | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00h | LEDCTL1 | LED Settings 1 Register | W | MLED6 | MLED5 | MLED4 | MSW2 | MSW1 | FXSW | RGSW | STBY |
|  |  |  |  | W | W | w | W | w | w | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | LEDCTL2 | LED Settings 2 Register | W | SPM6 | SPM5 | SPM4 | SPS2 | S2SW | S1SW | MISW | VOCSW |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | LEDCTL3 | LED Settings 3 Register | W | SCSW2 | B2SW | G2SW | R2SW | SCSW1 | B1SW | G1SW | R1SW |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | LEDCTL4 | LED Settings 4 Register | W | MFSW | KESW4 | KESW3 | KESW2 | KESW1 | F3SW | F2SW | F1SW |
|  |  |  |  | W | W | W | W | W | W | W | w |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | MLEDDACCTL | MLED Current Setting Register | W | MAINL [2: 0] |  |  | MAINH [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | M4DACTL | MLED4 Current Setting Register | W | - | - | - | M4C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | M5DACTL | MLED5 Current Setting Register | W | - | - | - | M5C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | M6_VD_DACTL | MLED6 Current Output Setting Register | W | VD [2: 0] |  |  | MC6 [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08h | S1DACTL | SLED1 Current <br> Setting Register | W | - | - | - | S1C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09h | S2DACTL | SLED2 Current <br> Setting Register | W | - | - | - | S2C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OAh | R1DACTL | RLED1 Current <br> Setting Register | W | MAXC1 [2:0] |  |  | R1C [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OBh | G1DACTL | GLED1 Current Setting Register | W | - | - | - | G1C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | B1DACTL | BLED1 Current Setting Register | W | - | - | - | B1C [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | R2DACTL | RLED2 Current Setting Register | W | MAXC2 [2:0] |  |  | R2C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OEh | G2DACTL | GLED2 Current Setting Register | W | - | - | - | G2C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OFh | B2DACTL | BLED2 Current Setting Register | W | - | - | - | B2C [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Upper column : Register name, Middle column : Read/Write, Lower column : Default value

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| Address | Register name | Description | R/W | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 10h | F1DACTL | FLED1 Current Setting Register | W | MAXCF [2:0] |  |  | F1C [4:0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | F2DACTL | FLED2 Current Setting Register | W | - | - | - | F2C [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12h | F3DACTL | FLED3 Current Setting Register | W | - | - | - | F3C [4: 0] |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13h | MFCTL | MLED Fade Time Setting Register | W | - | - | MFOUT [2:0] |  |  | MFIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14h | SFCTL | SLED Fade <br> Time <br> Setting Register | W | - | - | SFOUT [2:0] |  |  | SFIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15h | R1FCTL | RLED1 Fade Time Setting Register | W | - | - | R1FOUT [2:0] |  |  | R1FIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16h | G1FCTL | GLED1 Fade Time Setting Register | W | - | - | G1FOUT [2:0] |  |  | G1FIN [2: 0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | B1FCTL | BLED1 Fade Time Setting Register | W | - | - | B1FOUT [2:0] |  |  | B1FIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18h | RGB1GRCTL | RGB1 Gradation Setting Register | W | GHB1 | GHG1 | GHR1 | GR1M1 | GRON1 | AT1 [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19h | RGB1PUCTL | RGB1 Pulse Mode Setting Register | W | - | PRON1 | PT1 [2:0] |  |  | HO1 [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ah | R1AOFFCTL | RLED1 OFF Position Setting Register | W | - | - | R1Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Bh | R1AONCTL | RLED1 ON Position Setting Register | W | - | - | R1Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ch | G1AOFFCTL | GLED1 OFF <br> Position <br> Setting Register | W | - | - | G1Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Dh | G1AONCTL | GLED1 ON <br> Position <br> Setting Register | W | - | - | G1Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Eh | B1AOFFCTL | BLED1 OFF <br> Position <br> Setting Register | W | - | - | B1Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Fh | B1AONCTL | BLED1 ON Position Setting Register | W | - | - | B1Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Upper column : Register name, Middle column : Read/Write, Lower column : Default value

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| Address | Register name | Description | R/W | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 20h | R2FCTL | RLED2 Fade Time Setting Register | W | - | - | R2FOUT [2: 0] |  |  | R2FIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | w | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21h | G2FCTL | GLED2 Fade Time Setting Register | W | - | - | G2FOUT [2: 0] |  |  | G2FIN [2: 0] |  |  |
|  |  |  |  | W | w | W | w | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22h | B2FCTL | BLED2 Fade Time Setting Register | W | - | - | B2FOUT [2: 0] |  |  | B2FIN [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23h | RGB2GRCTL | RGB2 Gradation Setting Register | W | GHB2 | GHG2 | GHR2 | GR1M2 | GRON2 | AT2 [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24h | RGB2PUCTL | RGB2 Pulse Mode Setting Register | W | - | PRON2 | PT2[2:0] |  |  | HO2[2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 25h | R2AOFFCTL | RLED2 OFF <br> Position <br> Setting Register | W | - | - | R2Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | w | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26h | R2AONCTL | RLED2 ON <br> Position Setting Register | W | - | - | R2Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 27h | G2AOFFCTL | GLED2 OFF <br> Position <br> Setting Register | W | - | - | G2Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | w | W | w | w | w |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28h | G2AONCTL | GLED2 ON <br> Position <br> Setting Register | W | - | - | G2Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29h | B2AOFFCTL | BLED2 OFF <br> Position <br> Setting Register | W | - | - | B2Aoff [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Ah | B2AONCTL | BLED2 ON Position Setting Register | W | - | - | B2Aon [5:0] |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Bh | KEYCTL | KLED1, KLED2 <br> Changeover Voltage <br> Setting Register | W | KEY2C [3:0] |  |  |  | KEY1C [3: 0] |  |  |  |
|  |  |  |  | W | W | W | W | W | W | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Ch | PTCLT1 | Automatic <br> Brightness Control Mode Settings 1 Register | W | SWCTL | PTSW | KISW | SMPN [1:0] |  | SMPF [2:0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Dh | INTMASK | INT Mask Setting Register | W | INTCR | - | INTM6 | INTM5 | INTM4 | INTM3 | INTM2 | INTM1 |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Eh | INTDET | INT Detection Register | R | - | - | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 |
|  |  |  |  | R | R | R | R | R | R | R | R |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Fh | STATUS | Status <br> Detection Register | R | XM [3: 0] |  |  |  | - | - | KEYON | DCDC |
|  |  |  |  | R | R | R | R | R | R | R | R |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Upper column : Register name, Middle column : Read/Write, Lower column : Default value

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| Address | Register name | Description | R/W | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 30h | PTMDACTLO | Automatic <br> Brightness Control Mode Settings Current Settings 0 | W | - | YMAINO [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31h | PTMDACTL1 | Automatic Brightness Control Mode Settings Current Settings 1 | W | - | YMAIN1 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32h | PTMDACTL2 | Automatic <br> Brightness Control Mode Settings Current Settings 2 | W | - | YMAIN2 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 33h | PTMDACTL3 | Automatic <br> Brightness Control Mode Settings Current Settings 3 | W | - | YMAIN3 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34h | PTMDACTL4 | Automatic <br> Brightness Control <br> Mode Settings Current Settings 4 | W | - | YMAIN4 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 35h | PTMDACTL5 | Automatic <br> Brightness Control <br> Mode Settings Current Settings 5 | W | - | YMAIN5 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36h | PTMDACTL6 | Automatic <br> Brightness Control <br> Mode Settings Current Settings 6 | W | - | YMAIN6 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37h | PTMDACTL7 | Automatic <br> Brightness Control Mode Settings Current Settings 7 | W | - | YMAIN7 [6: 0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | w | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 38h | PTMDACTL8 | Automatic <br> Brightness Control Mode Settings Current Settings 8 | W | - | YMAIN8 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 39h | PTMDACTL9 | Automatic <br> Brightness Control Mode Settings Current Settings 9 | W | - | YMAIN9 [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Ah | PTMDACTLA | Automatic <br> Brightness Control Mode Settings Current Settings A | W | - | YMAINA [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | w | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Bh | PTMDACTLB | Automatic <br> Brightness Control Mode Settings Current Settings B | W | - | YMAINB [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Ch | PTMDACTLC | Automatic <br> Brightness Control Mode Settings Current Settings C | W | - | YMAINC [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Dh | PTMDACTLD | Automatic <br> Brightness Control Mode Settings Current Settings D | W | - | YMAIND [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Eh | PTMDACTLE | Automatic <br> Brightness Control Mode Settings Current Settings E | W | - | YMAINE [6:0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Fh | PTMDACTLF | Automatic <br> Brightness Control Mode Settings Current Settings F | W | - | YMAINE [6: 0] |  |  |  |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Upper column : Register name, Middle column : Read/Write, Lower column : Default value

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| Address | Register name | Contents | R/W | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 40h | PTCLT2 | Automatic <br> Brightness Control Mode Settings 2 Register | W | TUP [3: 0] |  |  |  | TDWN [3: 0] |  |  |  |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 41h | PTCLT3 | Automatic <br> Brightness Control Mode Settings 3 Register | W | - | TAU [2 : 0] |  |  | - | TAD [2 : 0] |  |  |
|  |  |  |  | W | W | W | W | W | W | W | w |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 42h | GPOCTL | GPO Register | W | MFXSW | - | GPO22 | GPO12 | GPO02 | GPO21 | GPO11 | GPO01 |
|  |  |  |  | W | W | W | W | W | W | W | W |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 43h | TEST | For Testing Inhibited |  | - | - | - | - | - | - | - | - |
|  |  |  |  | w | W | W | W | W | W | W | w |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Upper column : Register name, Middle column : Read/Write, Lower column : Default value

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[^0]:    D6 : PRON1 (Pulse mode setting (RLED1, GRLD1, BLED1))
    0 : OFF *Default
    1 : Pulse mode

