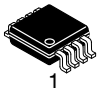
CAT5127, CAT5129

32-tap Digital Potentiometers (POTs)

ON Semiconductor®

http://onsemi.com

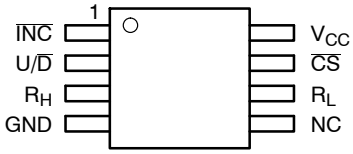


MSOP−8
Z SUFFIX
CASE 846AD

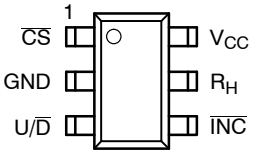
TSOT−23
TD SUFFIX
CASE 419AF

PIN CONFIGURATIONS

CAT5127
MSOP (Z)



CAT5129
TSOT−23 (TD)



(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Description

The CAT5127/CAT5129 are single digital POTs designed as an electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5127 contains a 32-tap series resistor array connected between two terminals R_H and R_L. The CAT5129 contains a 32-tap series resistor array connected between two terminals R_H and GND. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5127/CAT5129 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The devices are used as two-terminal variable resistors. Digital POTs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 32-position Linear Taper Potentiometer
- Non-volatile EEPROM Wiper Storage
- Low Standby Current
- Single Supply Operation: 2.5 V – 5.5 V
- Increment Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ and 100 kΩ
- CAT5127 in MSOP Packages
- CAT5129 in the 6-lead TSOT23 Package
- This Device is Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions

© Semiconductor Components Industries, LLC, 2013

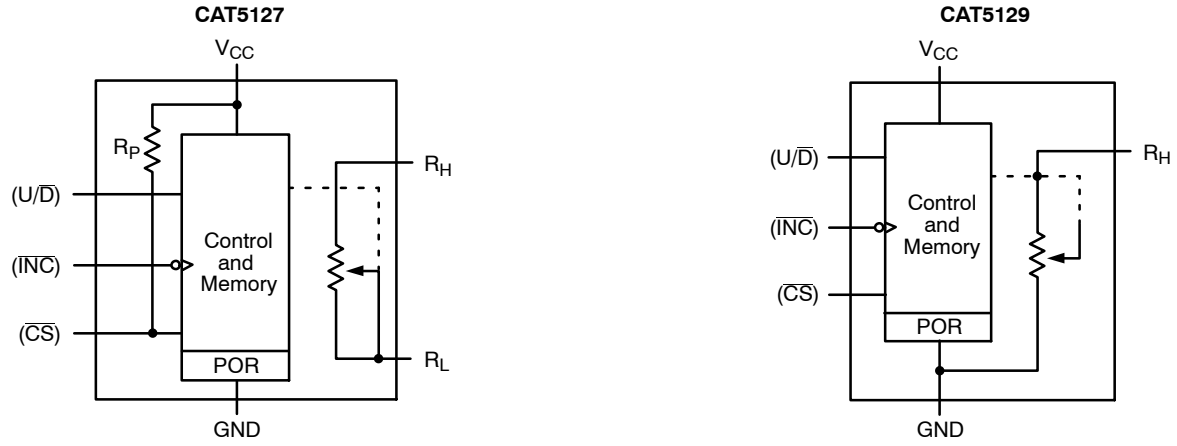


Figure 1. Functional Diagrams

Table 1. PIN DESCRIPTIONS

Name	Function	CAT5127 MSOP/TDFN	CAT5129 SOT23
$\overline{INC}$	Increment Control	1	4
U/$\overline{D}$	Up/Down Control	2	3
R_H	Potentiometer High Terminal	3	5
GND	Ground	4	2
NC	No Connect	5	–
R_L	Potentiometer Low Terminal	6	–
$\overline{CS}$	Chip Select	7	1
V_{CC}	Supply Voltage	8	6

DEVICE DESCRIPTION

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal (CAT5127 only)

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the device and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper. CAT5127 has an internal pull-up resistor on the $\overline{CS}$ input pin.

V_{CC}: Supply Input for the device.

DEVICE OPERATION

The CAT5127 operates like a digitally controlled variable resistor with R_H and R_L equivalent to the high and low terminals. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals.

The CAT5129 operates like a digitally controlled variable resistor with R_H equivalent to the high terminal. There are 32 available tap positions including the resistor end points, R_H and GND. There are 31 resistor elements connected in series between the R_H and GND terminals.

Operation is controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW, the device is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and five-bit counter). The wiper, when at either end terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the device is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the device may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

Table 2. OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L/GND
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

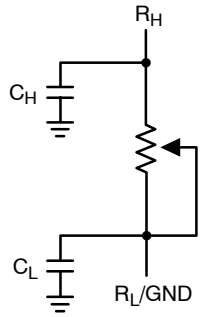


Figure 2. Variable Resistor Equivalent Circuit

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	 −0.5 to +7	V
Inputs $\overline{CS}$ to GND $\overline{INC}$ to GND U/$\overline{D}$ to GND H to GND L to GND W to GND	 −0.5 to V_{CC} +0.5 −0.5 to V_{CC} +0.5 −0.5 to V_{CC} +0.5 −0.5 to V_{CC} +0.5 −0.5 to V_{CC} +0.5 −0.5 to V_{CC} +0.5	V
Operating Ambient Temperature Commercial ('C' or Blank suffix) Industrial ('I' suffix)	 0 to 70 −40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	−65 to 150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP} (Note 1)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000			V
I_{LTH} (Notes 1, 2)	Latch-up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL−STD−883, Test Method 1008	100			Years
N_{END}	Endurance	MIL−STD−883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V
3. These parameters are periodically sampled and are not 100% tested.

Table 5. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5		5.5	V
I_{CC1}	CAT5127 Supply Current (Increment)	V_{CC} = 5.5 V, f = 1 MHz, I_W = 0			260	μA
		V_{CC} = 3.3 V, f = 1 MHz, I_W = 0			150	μA
	CAT5129 Supply Current (Increment)	V_{CC} = 5.5 V, f = 1 MHz, I_W = 0			160	μA
		V_{CC} = 3.3 V, f = 1 MHz, I_W = 0			50	μA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 5.5 V		300	600	μA
		Programming, V_{CC} = 3.3 V		150	400	μA
I_{SB1} (Note 4)	Supply Current (Standby)	$\overline{CS}$ = V_{CC} − 0.3 V U/$\overline{D}$, $\overline{INC}$ = V_{CC} or GND		0.35	1	μA
LOGIC INPUTS						
I_{IH}	CAT5127 Input Leakage Current	U/$\overline{D}$, $\overline{INC}$ = V_{CC}			1	μA
		$\overline{CS}$ = V_{CC} − 0.3 V			1	μA
	CAT5129 Input Leakage Current	V_{IN} = V_{CC}			1	μA
I_{IL}	CAT5127 Input Leakage Current	U/$\overline{D}$, $\overline{INC}$ = 0			−1	μA
		$\overline{CS}$ = 0			−120	μA
	CAT5129 Input Leakage Current	V_{IN} = 0 V			−1	μA
V_{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	V_{CC} x 0.7		V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		−0.3		V_{CC} x 0.2	V
V_{IH1}	CAT5129 TTL High Level Input Voltage	3.6 V ≤ V_{CC} ≤ 5.5 V	2		V_{CC}	V
V_{IL1}	CAT5129 TTL Low Level Input Voltage		0		0.8	V

Table 6. POTENTIOMETER CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	−10 Device		10		kΩ
		−50 Device		50		
		−00 Device		100		
R_{TOL}	Pot Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
RES	Resolution			3.2		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{Wi}	Wiper Resistance	V_{CC} = 5 V		70	100	Ω
		V_{CC} = 2.5 V		150	200	Ω
TC_{RPOT} (Note 6)	TC of Pot Resistance			±30	±300	ppm/°C
TC_{RATIO} (Note 6)	Ratiometric TC			±3	20	ppm/°C
V_N (Note 6)	Noise	100 kHz / 1 kHz		8/24		nV/√Hz
$C_H/C_L/C_W$ (Note 6)	Potentiometer Capacitances			8/8/25		pF
Fc (Note 6)	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz

4. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V
5. I_W = source or sink
6. These parameters are periodically sampled and are not 100% tested.

Table 7. AC TEST CONDITIONS

V_{CC} Range	2.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Levels	0.2 x V_{CC} to 0.7 x V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 x V_{CC}

Table 8. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50			ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100			ns
t_{IL}	$\overline{INC}$ LOW Period	250			ns
t_{IH}	$\overline{INC}$ HIGH Period	250			ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100			ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10			ms
t_{IR}	$\overline{INC}$ to R_H Change		1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1			µs
t_R, t_F (Note 8)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU} (Note 8)	Power-up to Wiper Stable			1	ms
t_{WR}	Store Cycle		2	5	ms

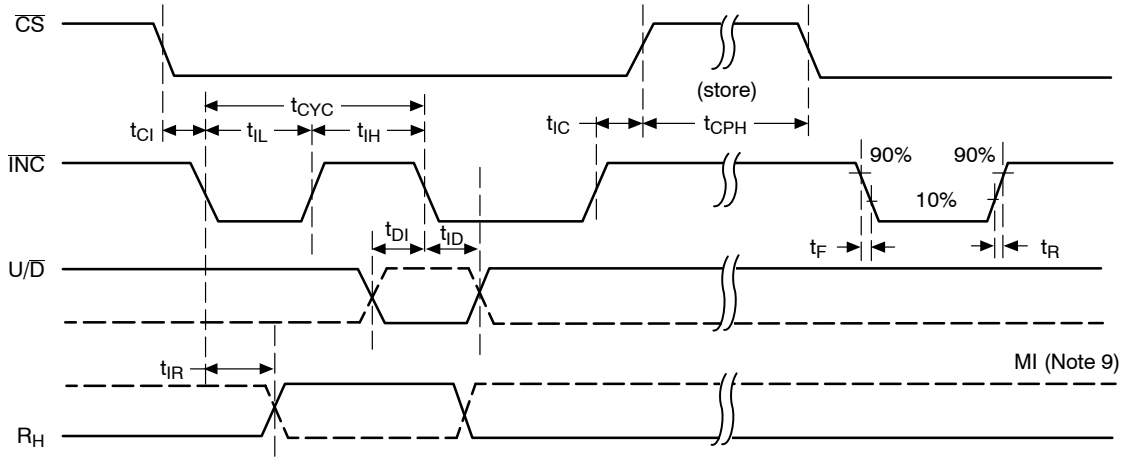


Figure 3. A.C. Timing

7. Typical values are for T_A = 25°C and nominal supply voltage.
8. This parameter is periodically sampled and not 100% tested.
9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

APPLICATION INFORMATION

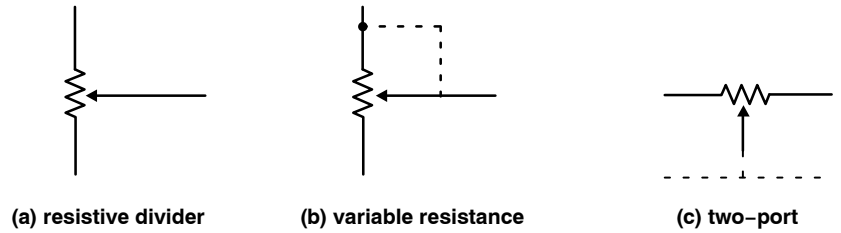


Figure 4. Potentiometer Configurations

Applications

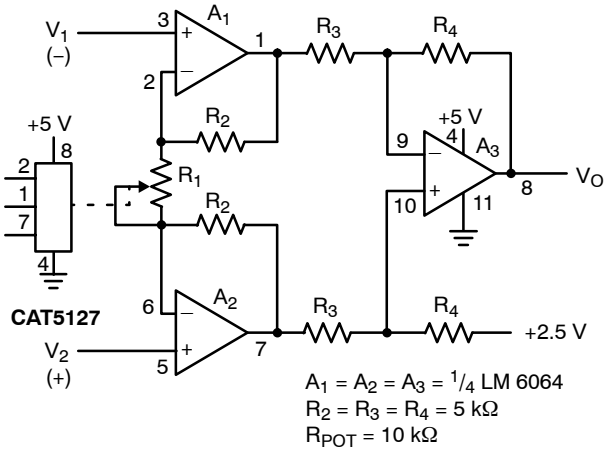


Figure 5. Programmable Instrumentation Amplifier

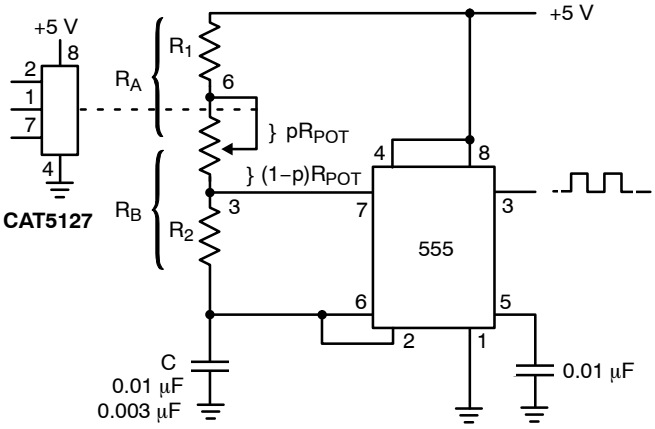


Figure 6. Programmable Sq. Wave Oscillator (555)

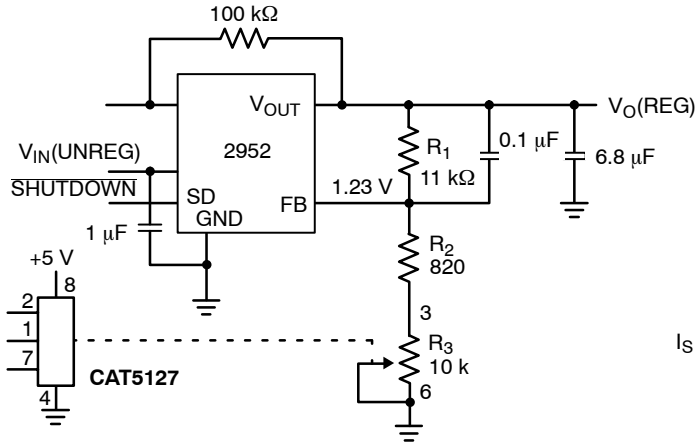


Figure 7. Programmable Voltage Regulator

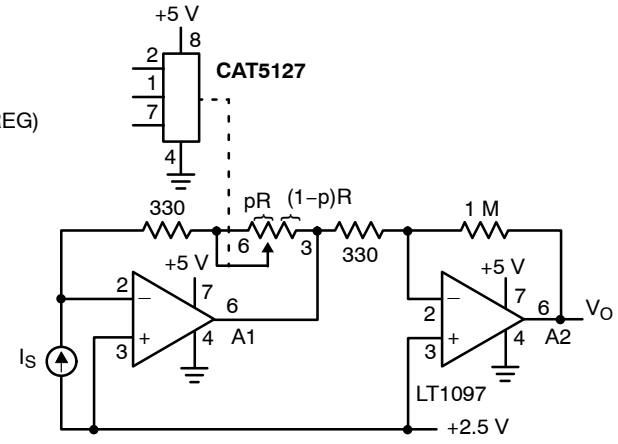


Figure 8. Programmable I to V Convertor

Table 9. ORDERING INFORMATION (Notes 10, 11)

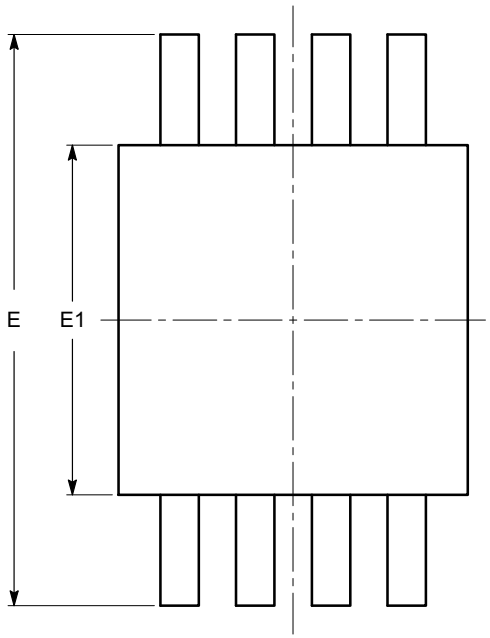
Device	Orderable Part Number	Resistor [kΩ]	Top Marking	Package/Pins	Shipping†
CAT5127	CAT5127ZI−10−GT3	10	ABNA	MSOP−8	3000 / Tape & Reel
	CAT5127ZI−50−GT3 (Note 13)	50	ABNB	MSOP−8	3000 / Tape & Reel
CAT5129	CAT5129TDI−10GT3	10	SJym (Note 14)	TSOT23−6	3000 / Tape & Reel
	CAT5129TDI−00GT3	100	SVym (Note 14)	TSOT23−6	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. All packages are RoHS-compliant (Lead-free, Halogen-free).
11. The standard lead finish is NiPdAu.
12. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
13. Contact factory for availability.
14. y = Production year (digit), m = Production month (digit).
15. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

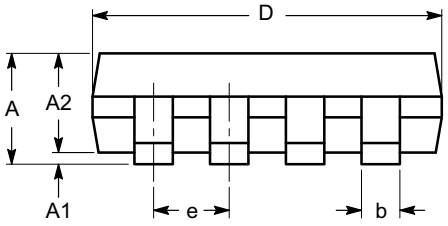
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD
ISSUE O

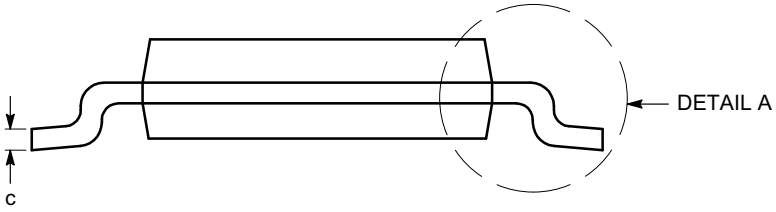


TOP VIEW

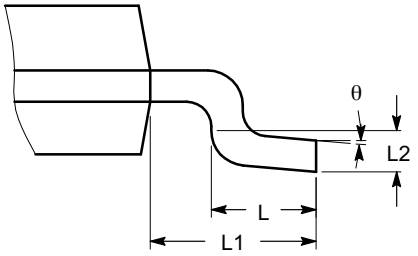
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW

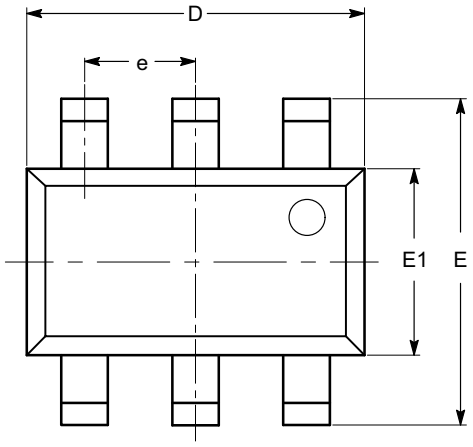


DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

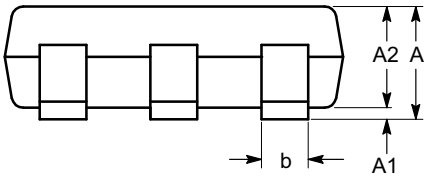
PACKAGE DIMENSIONS

TSOT−23, 6 LEAD
CASE 419AF
ISSUE O

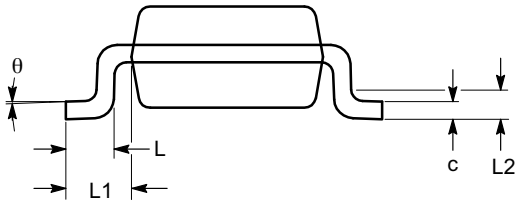


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative