

NLU1GT50

Single Buffer, Non-Inverting, TTL Level

TTL-Compatible Inputs

The NLU1GT50 MiniGate™ is an advanced CMOS high-speed non-inverting buffer in ultra-small footprint.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing.

The NLU1GT50 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- High Speed: $t_{PD} = 3.5$ ns (Typ) @ $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Input: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V, $V_{CC} = 5.0$ V
- CMOS-Compatible Output:
 $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @ Load
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Ultra-Small Packages
- These are Pb-Free Devices

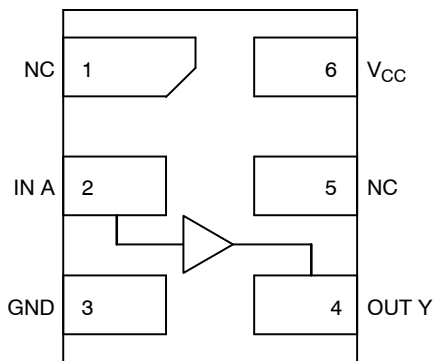


Figure 1. Pinout (Top View)

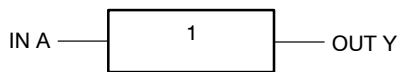


Figure 2. Logic Symbol

FUNCTION TABLE

A	Y
L	L
H	H

PIN ASSIGNMENT

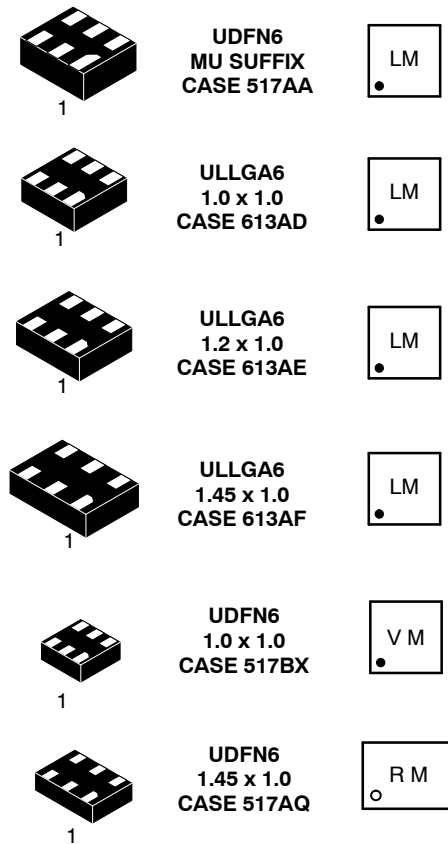
1	NC
2	IN A
3	GND
4	OUT Y
5	NC
6	V_{CC}



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



L = Device Marking
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NLU1GT50

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	±20	mA
I _O	DC Output Source/Sink Current	±12.5	mA
I _{CC}	DC Supply Current Per Supply Pin	±25	mA
I _{GND}	DC Ground Current per Ground Pin	±25	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{LATCHUP1}	Latchup Performance Above V _{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

NLU1GT50

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65 to 2.29	0.50 x V _{CC}			0.50 x V _{CC}				V
			2.3 to 2.99	0.45 x V _{CC}			0.45 x V _{CC}				
			3.0	1.4			1.4				
			4.5 to 5.5	2.0			2.0				
V _{IL}	Low-Level Input Voltage		1.65 to 2.29				0.10 x V _{CC}			0.10 x V _{CC}	V
			2.3 to 2.99				0.15 x V _{CC}			0.15 x V _{CC}	
			3.0				0.53			0.53	
			4.5 to 5.5				0.8			0.8	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	1.65 to 2.99	V _{CC} - 0.1			V _{CC} - 0.1			V _{CC} - 0.1	V
		I _{OH} = -50 μA	3.0	2.9	3.0	2.9			2.9		
			4.5	4.4	4.5	4.4			4.4		
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80			2.34 3.66	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	1.65 to 2.99		0	0.1		0.1		0.1	V
			3.0		0	0.1		0.1		0.1	
			4.5		0	0.1		0.1		0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	0 = V _{IN} = 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5			1.0		20		40	μA
I _{CC} T	Quiescent Supply Current	V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

NLU1GT50

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ n)

Symbol	Parameter	V_{CC} (V)	Test Condition	$T_A = 25^\circ\text{C}$			$T_A = +85^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} , t_{PHL}	Propagation Delay, Input A to Output Y	1.65 to 1.95	$C_L = 15$ pF			16.6		18.0		22.0	ns	
		2.3 to 2.7				13.3		14.5		17.5		
						19.5		22.0		25.5		
		3.0 to 3.6		$C_L = 15$ pF		4.5	10.0		11.0			13.0
				$C_L = 50$ pF		6.3	13.5		15.0			17.5
		4.5 to 5.5		$C_L = 15$ pF		3.5	6.7		7.5			8.5
$C_L = 50$ pF			4.3	7.7		8.5		9.5				
C_{IN}	Input Capacitance			5	10		10		10.0	pF		
C_{PD}	Power Dissipation Capacitance (Note 6)	5.0			12					pF		

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

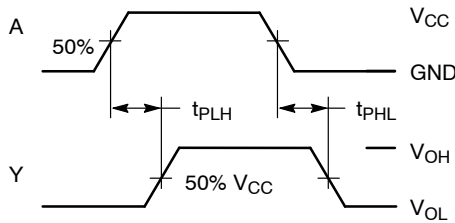
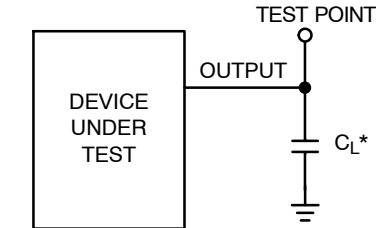


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

ORDERING INFORMATION

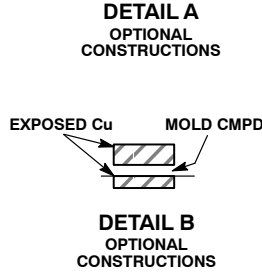
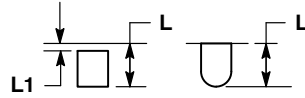
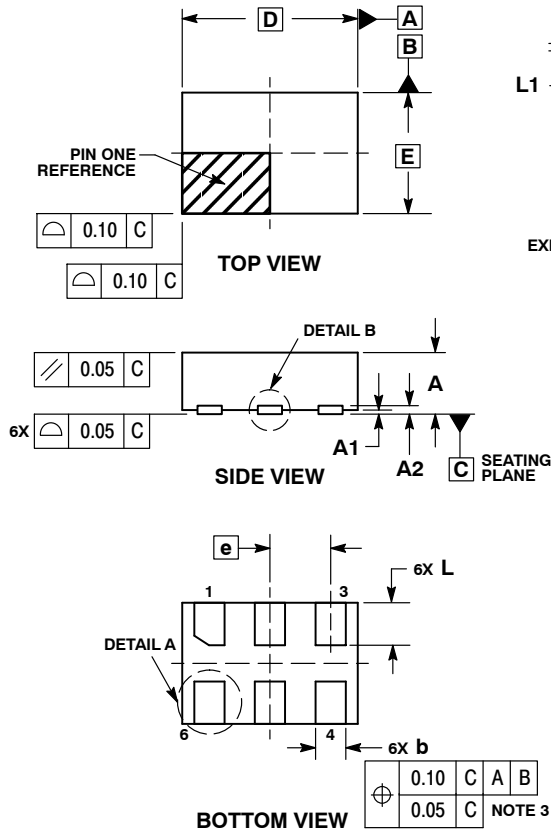
Device	Package	Shipping†
NLU1GT50MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLU1GT50AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLU1GT50BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLU1GT50CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel
NLU1GT50AMUTCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLU1GT50CMUTCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLU1GT50

PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

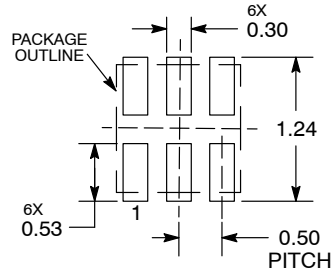


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



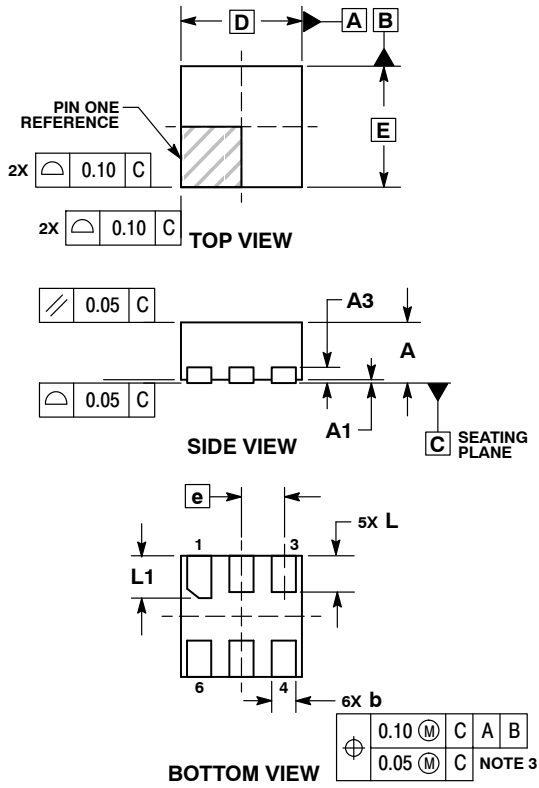
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLU1GT50

PACKAGE DIMENSIONS

UDFN6 1.0x1.0, 0.35P
CASE 517BX
ISSUE O

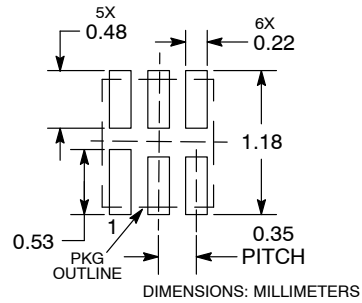


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

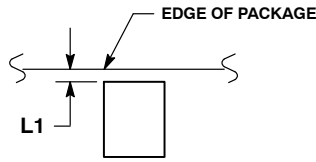
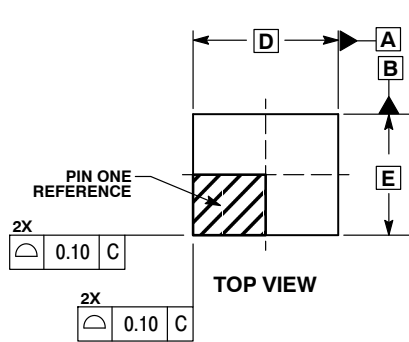


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLU1GT50

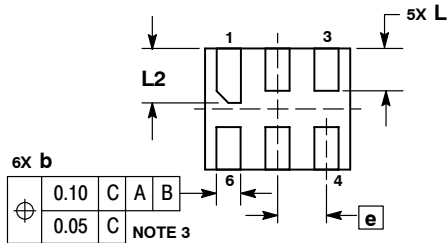
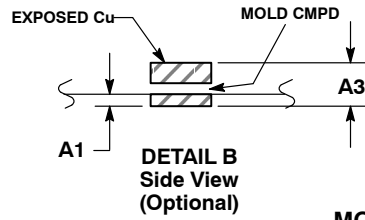
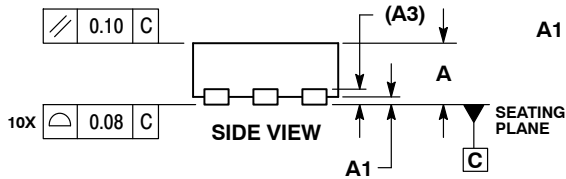
PACKAGE DIMENSIONS

UDFN6, 1.2x1.0, 0.4P
CASE 517AA
ISSUE C

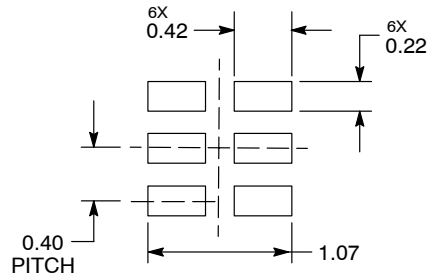


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	1.20	BSC
E	1.00	BSC
e	0.40	BSC
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50



MOUNTING FOOTPRINT*



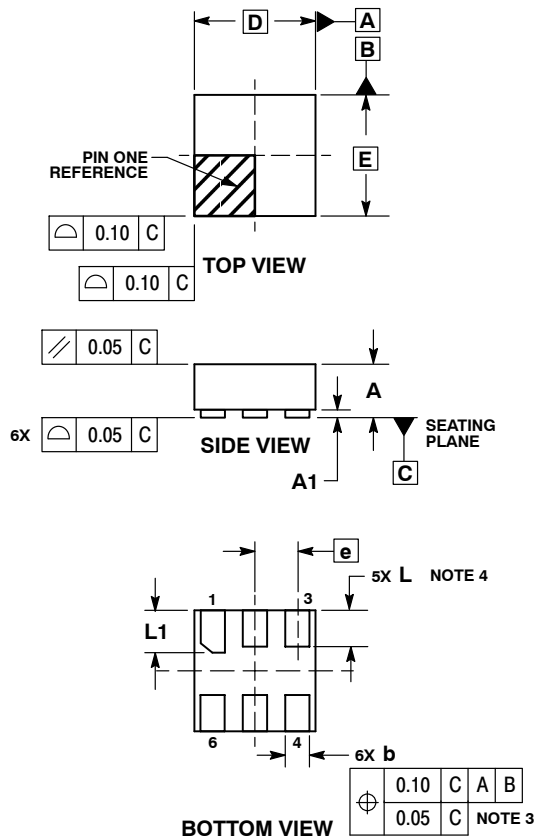
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLU1GT50

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P
CASE 613AD
ISSUE A

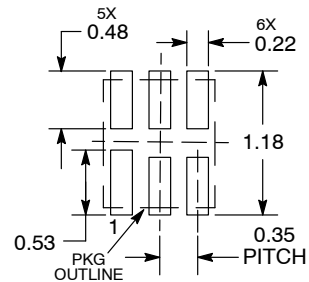


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



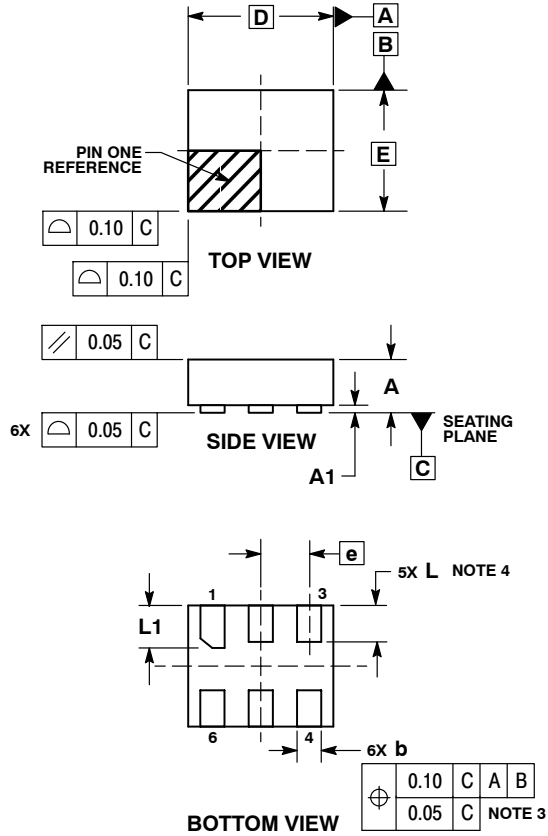
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLU1GT50

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P
CASE 613AE
ISSUE A

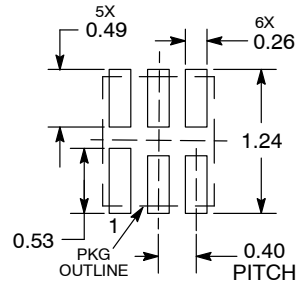


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

MOUNTING FOOTPRINT SOLDEMASK DEFINED*



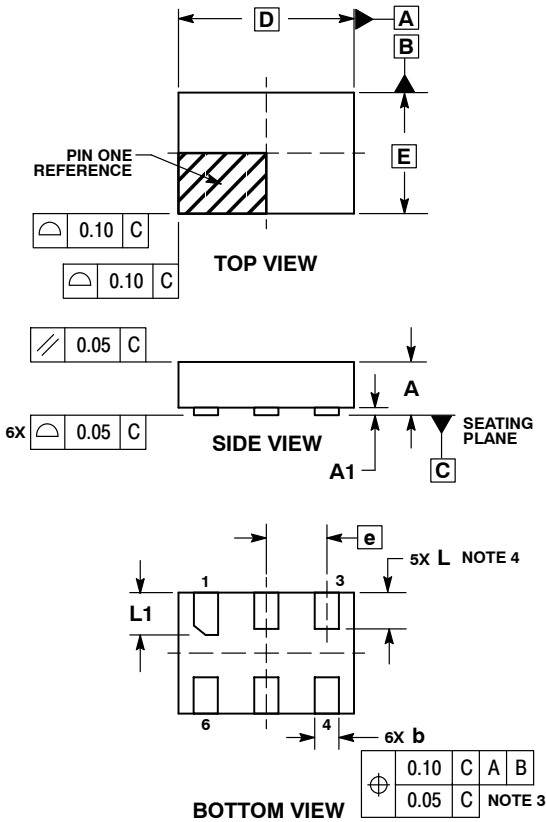
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLU1GT50

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P
CASE 613AF
ISSUE A

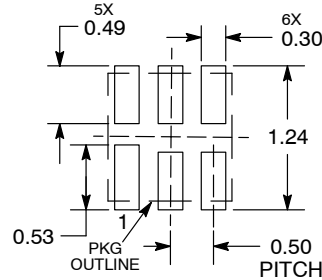


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative